ATA663211

LIN Transceiver

Features

- ISO 26262 Functional Safety Ready
- Supply Voltage up to 40V
- Operating Voltage V_{VS} = 5V to 28V
- Very Low Supply Current
  - Sleep mode: Typically 9 µA
  - Fail-Safe mode: Typically 80 µA
  - Normal mode: Typically 250 µA
- Fully Compatible with 3.3V and 5V Devices
- LIN Physical Layer according to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Wake-Up Capability through LIN bus (100 µs Dominant)
- External Wake Up through WKin pin (100 µs Low Level)
- INH Output to Control an External Voltage Regulator or to Switch the Commander Pull-Up
- Wake-Up Source Recognition
- TXD Time-Out Timer
- Bus Pin is Overtemperature and Short-Circuit Protected vs. GND and Battery
- Advanced EMC and ESD Performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.3”
- Interference and Damage Protection according to ISO7637
- Qualified according to AEC-Q100 and AEC-Q006
- Package: 8-Lead VDFN, 8-Lead SOIC, with Wettable Flanks (Moisture Sensitivity Level 1)

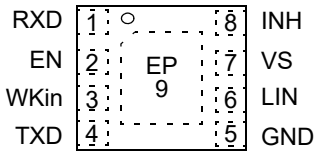
Description

The ATA663211 device is a fully integrated LIN transceiver designed in compliance with the LIN specification 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in convenience electronics, for example, in vehicles. Improved slope control at the LIN bus ensures data communication up to 20 Kbaud. Sleep mode guarantees minimal current consumption even in the case of a floating bus line or a short circuit on the LIN bus to GND.

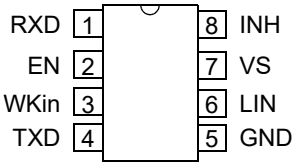
Note: The current LIN standards use the terminology "Master" and "Slave”. The LIN standard groups have decided that the terms "Commander" and "Responder" will be used in future.

Package Types

ATA663211
8-Lead VDFN



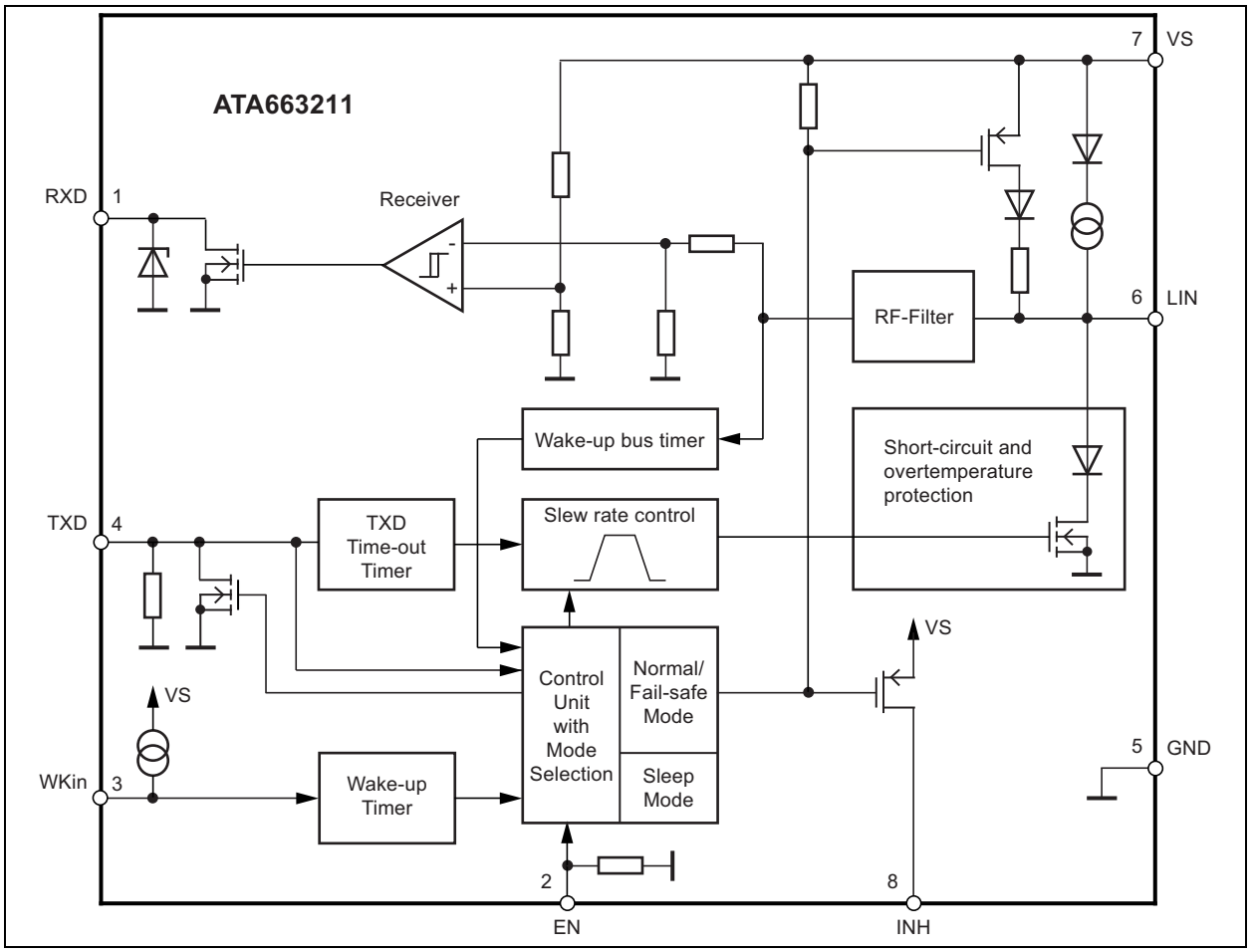
ATA663211
8-Lead SOIC



*Includes Exposed Thermal Pad (EP); see Table 1-4.

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ATA663211 Block Diagram



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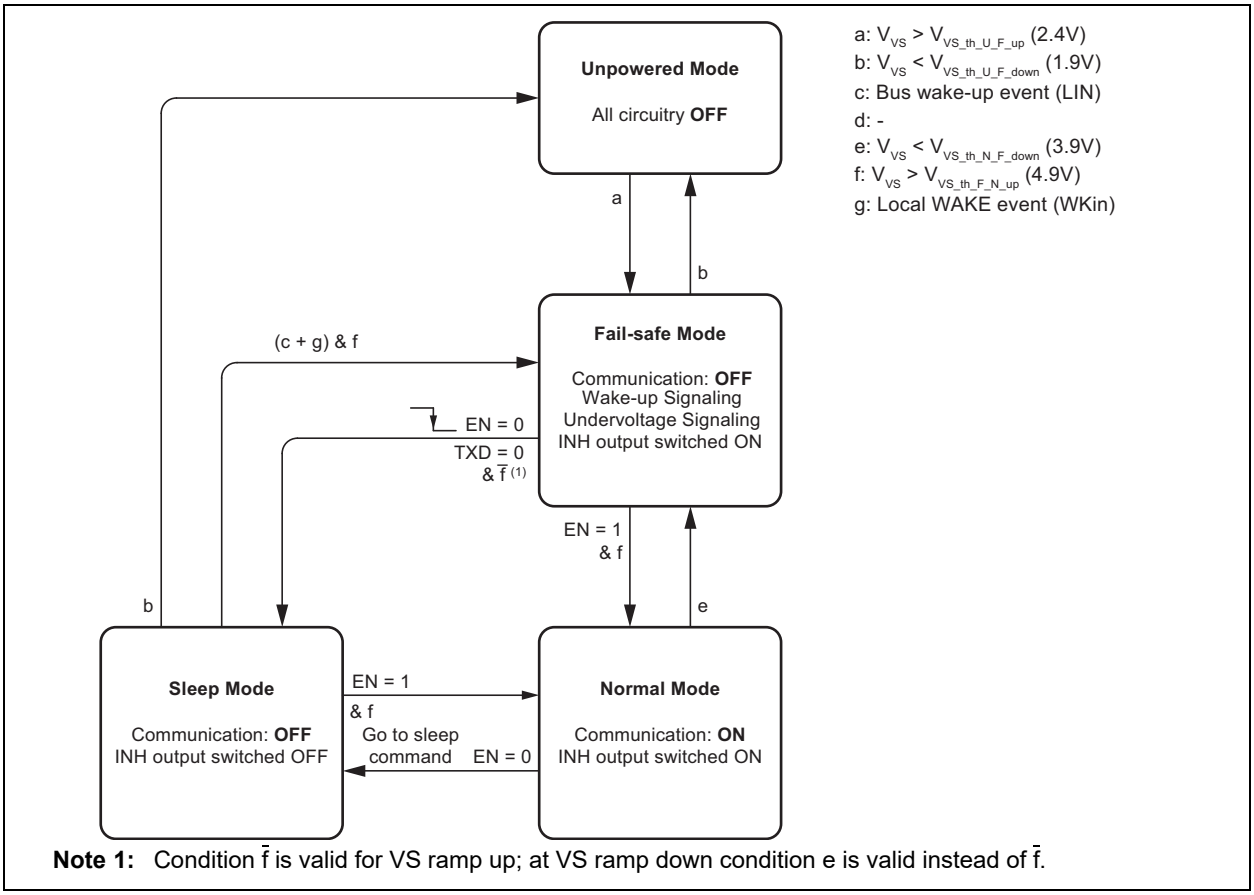
1.0 FUNCTIONAL DESCRIPTION

1.1 Physical Layer Compatibility

Since the LIN physical layer is independent of higher LIN layers (for example, LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes based on earlier versions (for instance, LIN 1.0, LIN 1.1,LIN 1.2, LIN 1.3) without any restrictions.

1.2 Operating Modes

FIGURE 1-1: ATA663211 OPERATING MODES



Note 1: Condition $\bar{f}$ is valid for VS ramp up; at VS ramp down condition e is valid instead of $\bar{f}$.

TABLE 1-1: ATA663211 OPERATING MODES

Operating Mode	Transceiver	INH	LIN	TXD	RXD
Fail-Safe	OFF	ON	Recessive	Signaling fail-safe sources (see Table 1-2)	
Normal	ON	ON	TXD-dependent	Follows data transmission	
Sleep/Unpowered	OFF	OFF	Recessive	Low	High Ohmic

1.2.1 NORMAL MODE

This is the normal transmitting and receiving mode of the LIN Interface, in accordance with LIN specification 2.x.

1.2.2 SLEEP MODE

A falling edge at EN switches the IC into Sleep mode. While in Sleep mode, the transmission path is disabled and the device is in Low-Power mode. Supply current from V_{BAT} is typically 9 µA. In Sleep mode the INH pin is switched off. The internal termination resistor between the LIN pin and VS pin is disabled. Only a weak pull-up current (typical 10 µA) between the LIN pin and VS pin is present. Sleep mode can be activated independently from the actual level on the LIN or WKin pin.

If the TXD pin is short-circuited to GND, it is possible to switch to Sleep mode though EN after $t > t_{dom}$.

1.2.3 FAIL-SAFE MODE

The device automatically switches to Fail-Safe mode at system power-up or after a wake-up event. The INH output is switched on and the LIN transceiver is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to Normal mode. During Fail-Safe mode the TXD pin is an output, and, together with the RXD output pin, signals the fail-safe source.

If the device enters Fail-Safe mode coming from the Normal mode (EN = 1) due to a VS undervoltage condition ($V_{VS} < V_{VS_th_N_F_down}$), it is possible to switch into Sleep mode by a falling edge at the EN input. With this feature, the current consumption is further reduced.

A wake-up event from Sleep mode is signaled to the microcontroller using the RXD pin and the TXD pin. A VS undervoltage condition is also signaled at these two pins. The coding is shown in Table 1-2.

TABLE 1-2: SIGNALING IN FAIL-SAFE MODE

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
VS_{th} (battery) undervoltage detection $V_{VS} < 3.9V$	High	Low

Note 1: Assuming an external pull-up resistor (typical 5 kΩ) has been added on pin TXD to the power supply of the microcontroller.

1.3 Wake-Up Scenarios from Sleep Mode

1.3.1 REMOTE WAKE UP THROUGH LIN BUS

1.3.1.1 Remote Wake-up from Sleep Mode

A voltage lower than the LIN pre-wake detection VLINL at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin, followed by a dominant bus level maintained for a certain period of time ($>t_{bus}$) and following a rising edge at the LIN pin result in a remote wake-up request and the device switches to Fail-Safe mode. The INH pin is activated (switches to VS) and the internal LIN termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD and interrupts the microcontroller.

1.3.2 LOCAL WAKE UP THROUGH WKIN PIN

A falling edge at the WKin pin followed by a low level maintained for a certain period of time ($>t_{WKin}$) result in a local wake-up request and the device switches to Fail-Safe mode. The INH pin is activated (switches to VS) and the internal LIN termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin and a high level at the RXD pin, generating an interrupt for the microcontroller. Even when the WKin pin is low, it is possible to switch to Sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high >10 µs before the negative edge at WKin starts a new local wake-up request.

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FIGURE 1-2: LIN WAKE-UP FROM SLEEP MODE

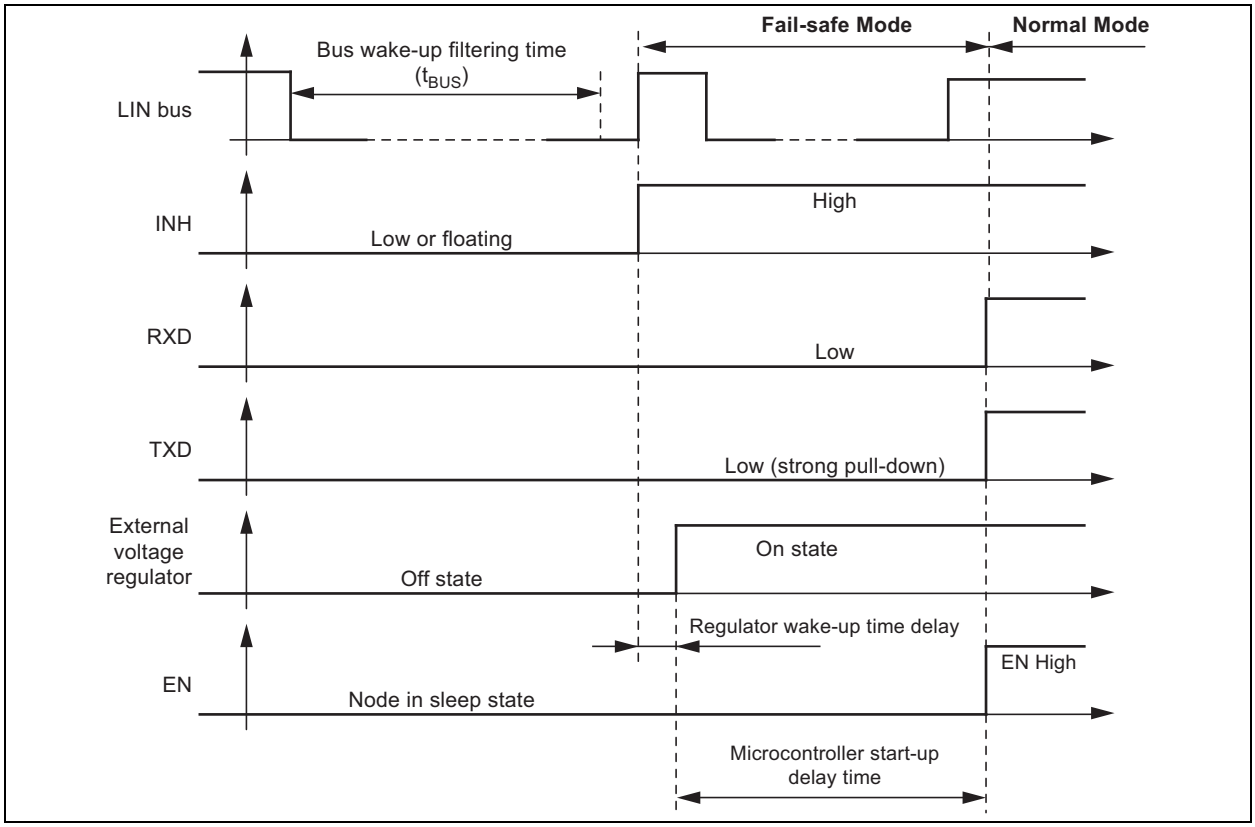
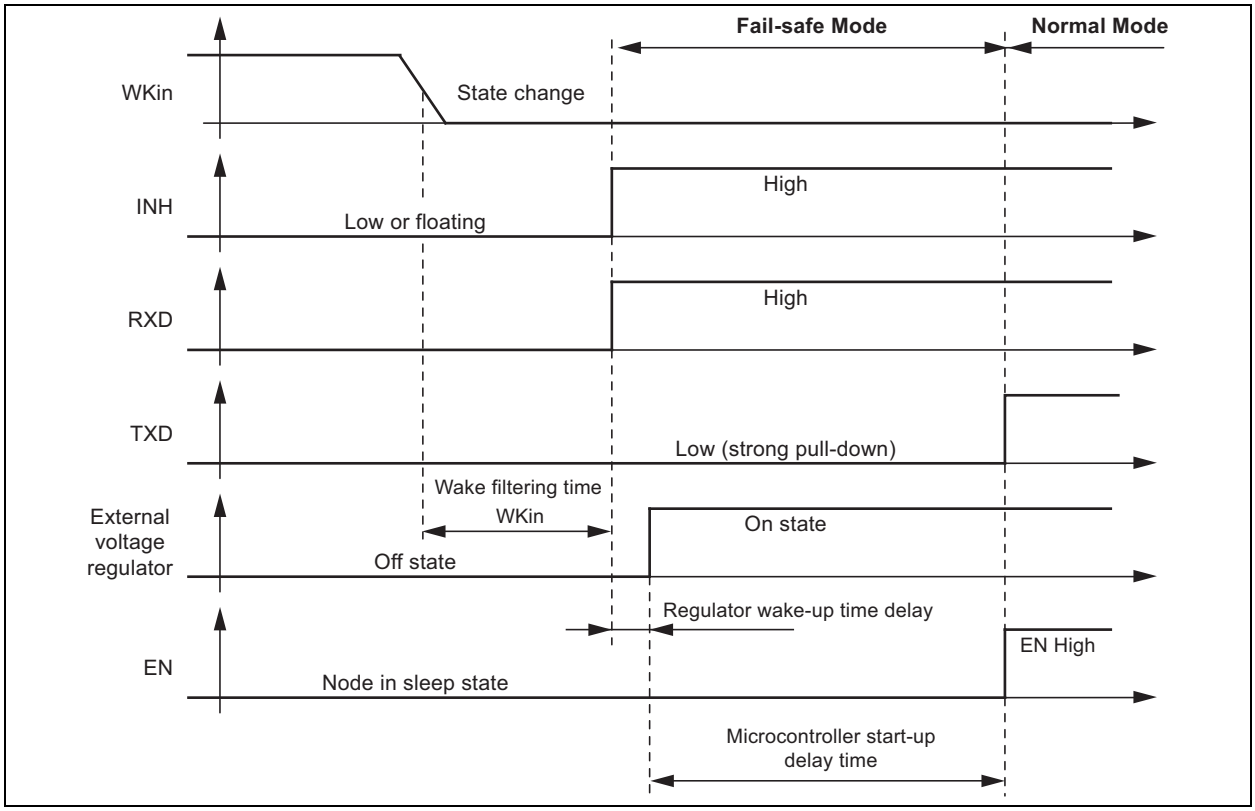


FIGURE 1-3: LOCAL WAKE-UP FROM WAKE-UP SWITCH



1.3.3 WAKE-UP SOURCE RECOGNITION

The device can distinguish between different wake-up sources. The wake-up source can be read on the TXD and RXD pin in Fail-Safe mode according to Table 1-3, if an external pull-up resistor (typically 5 kΩ) has been added on pin TXD to the power supply of the microcontroller. These flags are reset immediately if the microcontroller sets pin EN to high and the IC is in Normal mode.

TABLE 1-3: SIGNALING IN FAIL-SAFE MODE

Fail-Safe Sources	TXD	RXD
LIN wake up (LIN pin)	Low	Low
Local wake up (WKin pin)	Low	High
VS_{th} (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

Note 1: Assuming an external pull-up resistor (typical 5 kΩ) has been added on pin TXD to the power supply of the microcontroller.

1.4 Behavior under Low Supply Voltage Condition

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor used in the application (see **Figure "ATA663211 Block Diagram"**). If V_{VS} is higher than the minimum VS operation threshold $V_{VS_th_U_F_up}$, the IC mode changes from Unpowered mode to Fail-Safe mode, the INH output is switched on and the LIN transceiver can be activated.

If, during Sleep mode, the voltage level of V_{VS} drops below the under-voltage detection threshold $V_{VS_th_N_F_down}$ (typically 4.3V), the operation mode is not changed and no wake up is possible. Only if the supply voltage on the VS pin drops below the VS operation threshold $V_{VS_th_U_F_down}$ (typically 2.05V), does the IC switch to Unpowered mode.

If, during Normal mode, the voltage level on the VS pin drops below the VS undervoltage detection threshold $V_{VS_th_N_F_down}$ (typically 4.3V), the IC switches to Fail-Safe mode. This means that the LIN transceiver is disabled in order to avoid malfunctions or false bus messages. If the supply voltage V_{VS} drops further below the VS operation threshold $V_{VS_th_U_F_down}$ (typically 2.05V), the IC switches to Unpowered mode and the INH output switches off.

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1.5 Pin Descriptions

The descriptions of the pins are listed in Table 1-4.

TABLE 1-4: PIN FUNCTIONING TABLE

Pin	Symbol	Function
1	RXD	Receive data output
2	EN	Enables Normal mode if the input is high
3	WKin	High-voltage input for local wake-up request. If not needed, connect directly to VS
4	TXD	Transmit data input
5	GND	Ground, heat slug
6	LIN	LIN bus line input/output
7	VS	Supply voltage
8	INH	Battery-related high-side switch output for controlling an external voltage regulator or to switch off the LIN Commander pull-up resistor; switched on after a wake-up request
Backside	EP	Heat slug, internally connected to the GND pin (only for the VDFN8 package)

1.5.1 OUTING PIN (RXD)

In Normal mode, this pin reports the state of the LIN bus to the microcontroller. LIN high (Recessive state) is indicated by a high level at RXD; LIN low (Dominant state) is indicated by a low level at RXD.

The output is an open drain; it is compatible with a 3.3V or 5V power supply. The AC characteristics are defined by an external pull-up resistor of 4.7 kΩ to 5V and a load capacitor of 20 pF.

In Unpowered mode, RXD is switched off.

1.5.2 ENABLE INPUT PIN (EN)

The enable input pin controls the operating mode of the device. If EN is high, the circuit is in Normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active.

If EN is switched to low while TXD is still high, the device is forced to Sleep mode. This means that no data transmission is possible and current consumption is reduced to $I_{VSsleep}$ typical 9 μA.

The EN pin provides a pull-down resistor to force the transceiver into Recessive mode if EN is disconnected.

1.5.3 WKIN PIN

This pin is a high-voltage input used for waking up the device from Sleep mode. It is usually connected to an external switch in the application to generate a local wake up. A pull-up current source with typically 10 μA is implemented. The voltage threshold for a wake-up signal is typically 2V below the V_{VS} voltage.

If a local wake up is not needed in the application, the WKin pin can be connected directly to the VS pin.

1.5.4 INPUT/OUTPUT (TXD)

In Normal mode, the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high, the LIN output transistor is turned off and the bus is in the Recessive state. If the TXD pin stays at GND level while switching into Normal mode, it must be pulled to high level longer than 10 μs before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to Dominant state after Normal mode has been activated (also in case of a short circuit at TXD to GND). During Fail-Safe mode, this pin is used as output and signals the fail-safe source.

The TXD pin provides a pull-down resistor in order to have a defined level if TXD is disconnected.

An internal timer prevents the bus line from being driven permanently in the Dominant state. If TXD is forced to low longer than t_{dom} > 20 ms, the LIN bus driver is switched to the Recessive state. Nevertheless, when switching to Sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (>10 μs).

1.5.5 GROUND PIN (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It is able to handle a ground shift of up to 11.5% of V_{VS}.

1.5.6 BUS PIN (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from -27V to +40V. This pin exhibits no reverse current from the LIN bus to VS, even in the event of a GND shift or V_{Bat} disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope-controlled.

During a short circuit at LIN to V_{Bat}, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{off} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high.

During a short circuit from LIN to GND, the IC can be switched into Sleep mode and even in this case the current consumption is lower than 100 µA. If the short circuit disappears, the IC starts with a remote wake up.

The reverse current is <2 µA at pin LIN during loss of V_{Bat}. This is optimal behavior for bus systems where some nodes are supplied from battery or ignition.

1.5.7 SUPPLY PIN (VS)

LIN operating voltage is VS = 5V to 28V. Undervoltage detection is implemented to disable transmission if VS falls below typical 4.5V, in order to avoid false bus messages. After switching on V_{VS}, the IC starts in Fail-Safe mode and the INH output is switched on.

The supply current in Sleep mode is typically 9 µA.

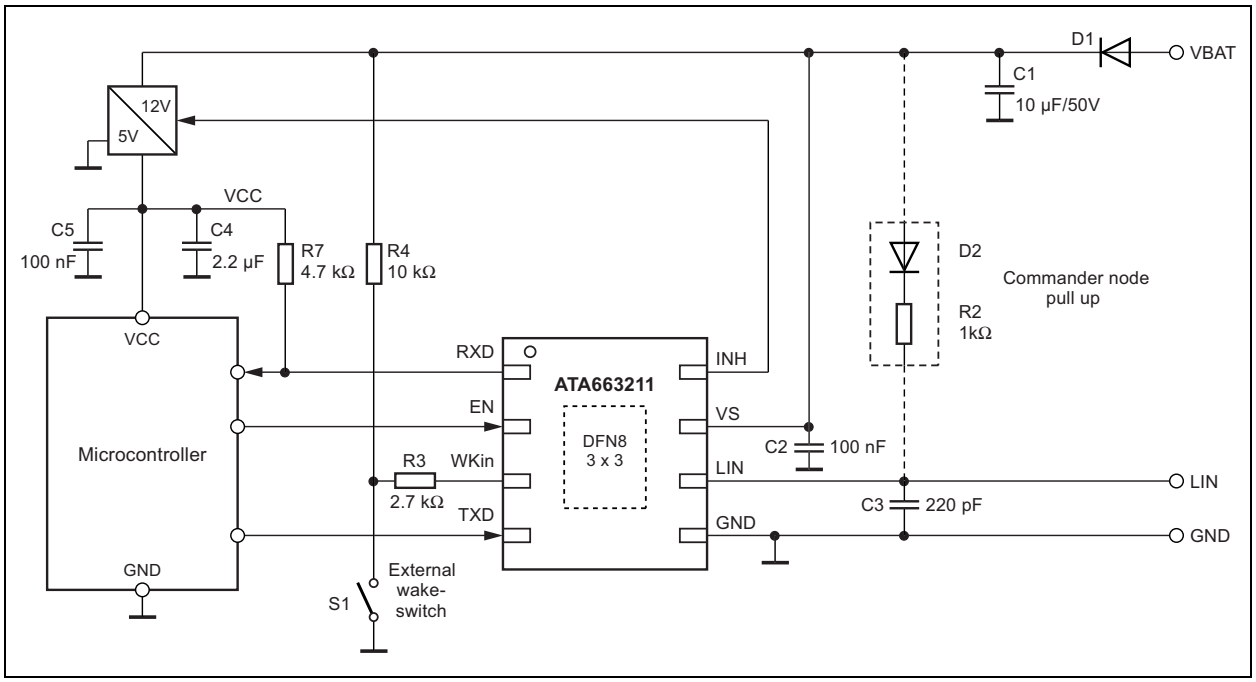
1.5.8 INHIBIT OUTPUT PIN (INH)

This pin is used to control an external voltage regulator or to switch the LIN Commander pull-up resistor ON/OFF in case the device is used in a Commander node. The inhibit pin provides an internal switch toward the VS pin which is protected by temperature monitoring. If the device is in normal or Fail-Safe mode, the inhibit high-side switch is turned on. When the device is in Sleep mode, the inhibit switch is turned off, thus disabling the voltage regulator or other connected external devices.

A wake-up event on the LIN bus or at the WKin pin switches the INH pin to the VS level. After a system power-up (V_{VS} rises from zero), the INH pin switches to the V_{VS} level automatically.

1.6 Typical Applications

FIGURE 1-4: ATA663211 TYPICAL APPLICATION CIRCUIT



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2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{VS}) ..... -0.3V to +40V

Logic Pins:

Voltage Levels (RXD, TXD, EN, NRES) (V_{Logic}) ..... -0.3V to +5.5V

Output DC currents (I_{Logic}) ..... -5 mA to +5 mA

LIN

DC Voltage ..... -27V to +40V

Pulse time <500 ms ..... -27V to +43V

INH

DC Voltage ..... -0.3V to (VS + 0.3V)

DC Voltage ..... -100 mA to +30 mA

WKin voltage levels

DC Voltage (V_{WKIN}) ..... -0.3V to +40V

Transient voltage according to ISO7637 (coupling 1 nF, with 2.7K serial resistor) ..... -150V to +100V

ESD according to IBEE LIN EMC; test specification 1.0 following IEC 61000-4-2

Pin VS, LIN to GND, WKin (with external circuitry according to applications diagram) ..... ±6 kV

ESD HBM following STM5.1 with 1.5 kΩ/100 pF

Pin VS, LIN, INH to GND ..... ±6 kV

Pin WKin to GND ..... ±5 kV

HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002) ..... ±3 kV

CDM ESD STM 5.3.1 ..... ±750V

Machine Model ESD AEC-Q100-RevF(003) ..... ±200V

Virtual Junction Temperature (T_{VJ}) ..... -40°C to +150°C

Storage Temperature (T_S) ..... -55°C to +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified all values refer to GND pins, 5V < V_{VS} < 28V, -40°C < T_{VJ} < 150°C.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
1	**VS Pin**						
1.1	Nominal DC Voltage Range	V_{VS}	5	13.5	28	V	
1.3	Supply Current in Sleep mode	$I_{VSsleep}$	3	9	15	µA	Sleep mode $V_{LIN} > V_{VS}$ - 0.5V V_{VS} < 14V, T = 27°C (**Note 1**)
		$I_{VSsleep}$	3	11	18	µA	Sleep mode $V_{LIN} > V_{VS}$ – 0.5V V_{VS} < 14V
		$I_{VSsleep_short}$	20	50	100	µA	Sleep mode, V_{LIN} = 0V bus shorted to GND VV_{VS} < 14V
1.4	Supply Current in Normal Mode	I_{VSrec}	150	250	320	µA	Bus recessive V_{VS} < 14V
1.5	Supply Current in Normal Mode	I_{VSdom}	200	700	950	µA	Bus dominant (internal LIN pull-up resistor active) V_{VS} < 14V
1.6	Supply Current in Fail-Safe mode	I_{VSfail}	40	80	110	µA	Bus recessive V_{VS} < 14V
1.7	VS Undervoltage Threshold (switching from Normal to Fail-Safe mode)	$V_{VS_th_N_F_down}$	3.9	4.3	4.7	V	Decreasing supply voltage
		$V_{VS_th_F_N_up}$	4.1	4.6	4.9	V	Increasing supply voltage
1.8	VS Undervoltage Hysteresis	$V_{VS_hys_F_N}$	0.1	0.25	0.4	V	
1.9	VS Operation Threshold (switching to Unpowered mode)	$V_{VS_th_U_F_down}$	1.9	2.05	2.3	V	Switch to Unpowered mode
		$V_{VS_th_U_F_up}$	2.0	2.25	2.4	V	Switch from Unpowered to Fail-Safe mode
1.10	VS Undervoltage Hysteresis	$V_{VS_hys_U}$	0.1	0.2	0.3	V	
2	**RXD Output Pin (Open Drain)**						
2.1	Low-Level Output Sink Capability	V_{RXDL}	—	0.2	0.4	V	Normal mode, V_{LIN} = 0V, I_{RXD} = 2 mA
2.3	High-Level Leakage Current	I_{RXDH}	-3	—	+3	µA	Normal mode $V_{LIN} = V_{VS}$, V_{RXD} = 5V
3	**TXD Input/Output Pin**						
3.1	Low-Level Voltage Input	V_{TXDL}	-0.3	—	+0.8	V	
3.2	High-Level Voltage Input	V_{TXDH}	2	—	5.5	V	
3.5	Pull-Down Resistor	R_{TXD}	150	200	300	kΩ	V_{TXD} = 5V
3.6	Low-level Leakage Current	I_{TXD}	-3	—	+3	µA	V_{TXD} = 0V

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values refer to GND pins, 5V < V_{VS} < 28V, -40°C < T_{VJ} < 150°C.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
3.7	Low-Level Output Sink Current at Wake-Up Request	I_{TXD}	2	2.5	8	mA	Fail-Safe mode V_{TXD} = 0.4V
4	**EN Input Pin**						
4.1	Low-Level Voltage Input	V_{ENL}	-0.3	—	+0.8	V	
4.2	High-Level Voltage Input	V_{ENH}	2	—	5.5	V	
4.3	Pull-Down Resistor	R_{EN}	50	125	200	kΩ	V_{EN} = 5V
4.4	Low-Level Input Current	I_{EN}	-3	—	+3	µA	V_{EN} = 0V
6	**WKin Input Pin**						
6.1	High-Level Input Voltage	VWKinH	V_{VS} – 1V	—	V_{VS} + 0.3V	V	
6.2	Low-Level Input Voltage	VWKinL	-1	—	V_{VS} – 3.3V	V	Initializes a wake-up signal
6.3	WKin Pull-Up Current	I_{WKIN}	-30	-10		µA	V_{VS} < 28V, V_{WKin} = 0V
6.4	High-Level Leakage Current	I_{WKINL}	-5	—	+5	µA	V_{VS} = 28V, V_{WKin} = 28V
6.5	Debounce Time of Low Pulse for Wake up via WKin	t_{WKin}	50	100	150	µs	V_{WKin} = 0V
7	**INH Output Pin**						
7.1	Switch on Resistance Between VS and INH	$R_{DSON,INH}$	—	12	25	Ω	Normal or Fail-Safe mode IINH = -15 mA
7.2	Leakage Current	$I_{LEAK,INH}$	-3	—	+3	µA	Transceiver in Sleep mode, VINH = 0V/28V, V_{VS} = 28V
7.3	High-Level Voltage	V_{INH}	V_{VS} – 0.375	—	V_{VS}	V	Normal or Fail-Safe mode IINH = -15 mA
10	**LIN Bus Driver: Bus Load Conditions: Load 1 (small): 1 nF, 1 kΩ; Load 2 (large): 10 nF, 500Ω; External Pull-up R_{RXD} = 4.7 kΩ ; C_{RXD} = 20 pF, Load 3 (medium): 6.8 nF, 660Ω characterized on samples, 12.7 and 12.8 specifies the timing parameters for proper operation at 20 kb/s and 12.9 and 12.10 at 10.4 kb/s**						
10.1	Driver Recessive Output Voltage	V_{BUSrec}	0.9 * V_{VS}	—	V_{VS}	V	Load1/Load2
10.2	Driver Dominant Voltage	$V_{_LoSUP}$	—	—	1.2	V	V_{VS} = 7V R_{load} = 500Ω
10.3	Driver Dominant Voltage	$V_{_HiSUP}$	—	—	2	V	V_{VS} = 18V R_{load} = 500Ω
10.4	Driver Dominant Voltage	$V_{_LoSUP_1k}$	0.6	—	—	V	V_{VS} = 7V R_{load} = 1000Ω
10.5	Driver Dominant Voltage	$V_{_HiSUP_1K}$	0.8	—	—	V	V_{VS} = 18V R_{load} = 1000Ω
10.6	Pull-Up Resistor to VS	R_{LIN}	20	30	47	kΩ	The serial diode is mandatory

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values refer to GND pins, 5V < V_{VS} < 28V, -40°C < T_{VJ} < 150°C.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
10.7	Voltage Drop at the Serial Diodes	$V_{SerDiode}$	0.4	—	1.0	V	In pull-up path with R_{LIN} $I_{SerDiode}$ = 10 mA (**Note 3**)
10.8	LIN Current Limitation V_{BUS} = V_{BAT_MAX}	I_{BUS_LIM}	40	120	200	mA	
10.9	Input leakage current at the receiver including pull-up resistor as specified	$I_{BUS_PAS_dom}$	-1	-0.35	—	mA	Input leakage current driver off V_{BUS}= 0V V_{BAT} = 12V
10.10	Leakage Current LIN Recessive	$I_{BUS_PAS_rec}$	—	10	20	µA	Driver off 8V < V_{BAT}< 18V 8V < V_{BUS} < 18V V_{BUS} ≥ V_{BAT}
10.11	Leakage current when control unit is disconnected from ground. Loss of local ground must not affect communication in the residual network	$I_{BUS_NO_gnd}$	-10	+0.5	+10	µA	GND_{Device} = V_{VS} V_{BAT}= 12V 0V < V_{BUS}< 18V
10.12	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	$I_{BUS_NO_bat}$	—	0.1	2	µA	V_{BAT} disconnected V_{SUP_device} = GND 0V < V_{BUS} < 18V
10.13	Capacitance on LIN pin to GND	C_{LIN}	—	—	20	pF	(**Note 3**)
11	**LIN Bus Receiver**						
11.1	Center of Receiver Threshold	V_{BUS_CNT}	0.475 * V_{VS}	0.5 * VS	0.525 * V_{VS}	V	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2
11.2	Receiver Dominant State	V_{BUSdom}	-27	—	0.4 * VS	V	V_{EN} = 5V
11.3	Receiver Recessive State	V_{BUSrec}	0.6 * V_{VS}	—	40	V	V_{EN} = 5V
11.4	Receiver Input Hysteresis	V_{BUShys}	0.028 * V_{VS}	0.1 * VS	0.175 * V_{VS}	V	V_{hys} = V_{th_rec} - V_{th_dom}
11.5	Pre-Wake Detection LIN High-Level Input Voltage	V_{LINH}	V_{VS} – 2V	—	V_{VS} + 0.3V	V	
11.6	Pre-Wake Detection LIN Low-Level Input Voltage	V_{LINL}	-27	—	V_{VS} – 3.3V	V	Activates the LIN receiver

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

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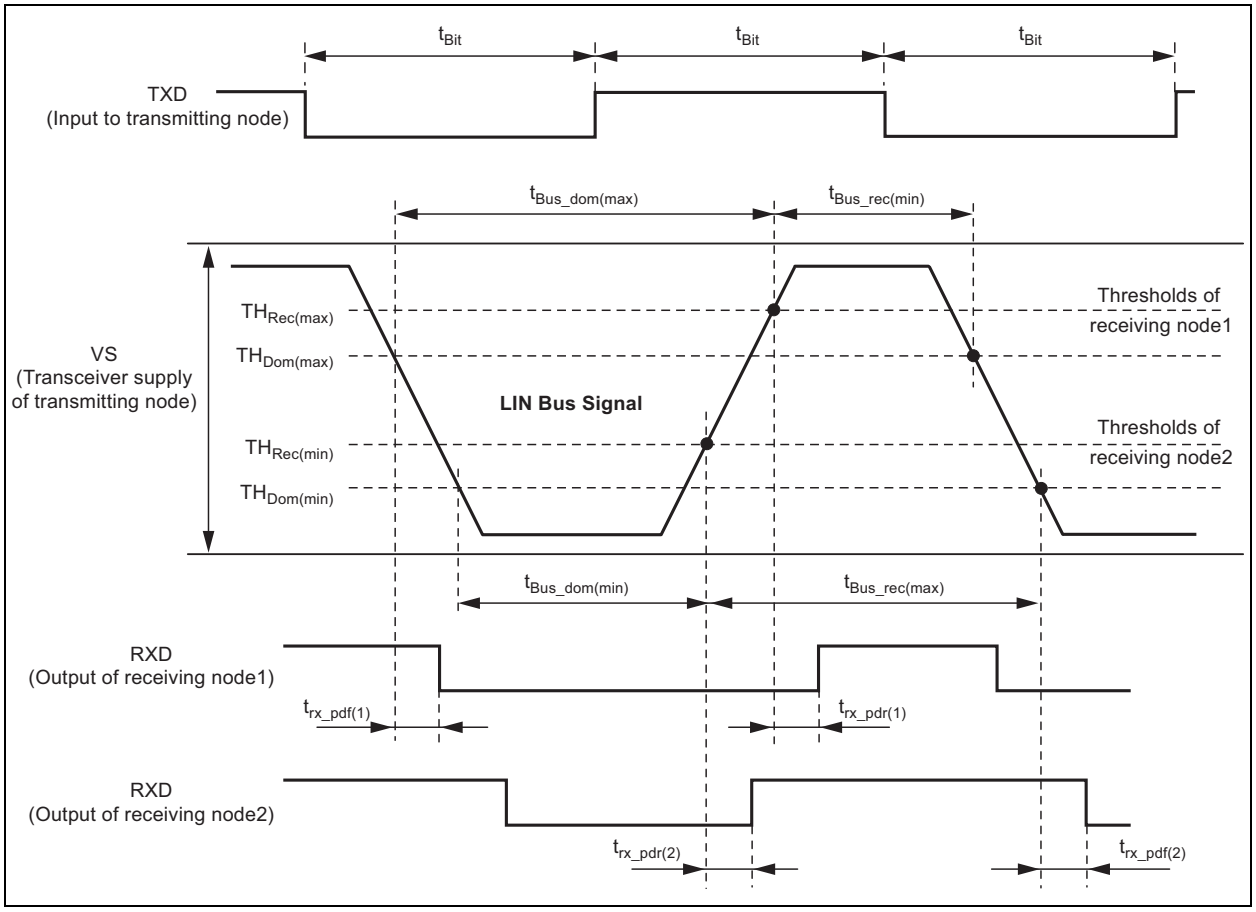
ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values refer to GND pins, 5V < V_{VS} < 28V, -40°C < T_{VJ} < 150°C.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
12	**Internal timers**						
12.1	Dominant time for wake up via LIN bus	t_{bus}	50	100	150	µs	V_{LIN} = 0V
12.2	Time delay for mode change from Fail-Safe into Normal mode via EN pin	t_{norm}	5	15	20	µs	V_{EN} = 5V
12.3	Time delay for mode change from Normal mode to Sleep mode via EN pin	t_{sleep}	5	15	20	µs	V_{EN} = 0V
12.4	Time delay for mode change from Sleep mode to Normal mode via EN pin	t_{s_n}	—	150	300	µs	V_{EN} = 5V
12.5	TXD dominant time-out time	t_{dom}	20	40	60	ms	V_{TXD} = 0V
12.7	Duty Cycle 1	D1	0.396	—	—	—	$TH_{Rec(max)}$ = 0.744 x V_{VS} $TH_{Dom(max)}$ = 0.581 x V_{VS} V_{VS} = 7.0V to 18V t_{Bit} = 50 µs D1 = $t_{bus_rec(min)}$/(2 x t_{Bit})
12.8	Duty Cycle 2	D2	—	—	0.581	—	$TH_{Rec(min)}$ = 0.422 x V_{VS} $TH_{Dom(min)}$ = 0.284 x V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 50 µs D2 = $t_{bus_rec(max)}$/(2 x t_{Bit})
12.9	Duty Cycle 3	D3	0.417	—	—	—	$TH_{Rec(max)}$ = 0.778 x V_{VS} $TH_{Dom(max)}$ = 0.616 x V_{VS} V_{VS} = 7.0V to 18V t_{Bit} = 96 µs D3 = $t_{bus_rec(min)}$/(2 x t_{Bit})
12.10	Duty Cycle 4	D4	—	—	0.590	—	$TH_{Rec(min)}$ = 0.389 x V_{VS} $TH_{Dom(min)}$ = 0.251 x V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 96 µs D4 = $t_{bus_rec(max)}$/(2 x t_{Bit})
12.11	Slope time falling and rising edge at LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5	—	22.5	µs	V_{VS} = 7.0V to 18V
13	**Receiver electrical AC parameters of the LIN physical layer** **LIN receiver, RXD load conditions: C_{RXD} = 20 pF, R_{RXD} = 4.7 kΩ**						
13.1	Propagation delay of receiver	t_{rx_pd}	—	—	5	µs	V_{VS} = 7.0V to 18V t_{rx_pd} = max(t_{rx_pdr}, t_{rx_pdf})
13.2	Symmetry of receiver propagation delay rising edge minus falling edge	t_{rx_sym}	-2	—	+2	µs	V_{VS} = 7.0V to 18V t_{rx_sym} = t_{rx_pdr} - t_{rx_pdf}

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

FIGURE 2-1: DEFINITION OF BUS TIMING CHARACTERISTICS



TEMPERATURE SPECIFICATIONS 8-LEAD VDFN

Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal resistance virtual junction to exposed thermal pad	R_{thvJC}	—	10	—	K/W
Thermal resistance virtual junction to ambient, where exposed thermal pad is soldered to the PCB, according to JEDEC	R_{thvJA}	—	50	—	K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	—	10	—	°C

TEMPERATURE SPECIFICATIONS 8-LEAD SOIC

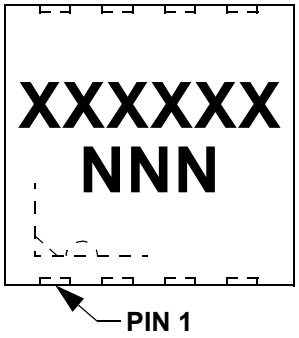
Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal resistance virtual junction to ambient, with a heat sink at GND (pin 5) on PCB (fused lead frame to pin 5)	R_{thvJA}	—	80	—	K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	5	10	20	°C

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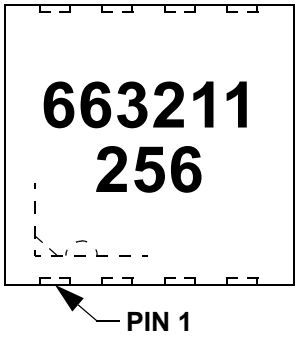
3.0 PACKAGING INFORMATION

Package Marking Information

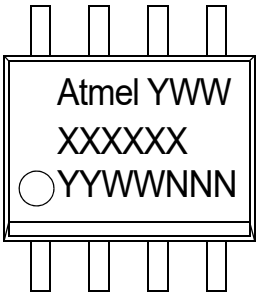
8-Lead VDFN (3x3 mm)



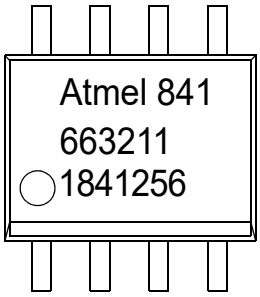
Example ATA663211



8-Lead SOIC (3.90 mm)



Example ATA663211



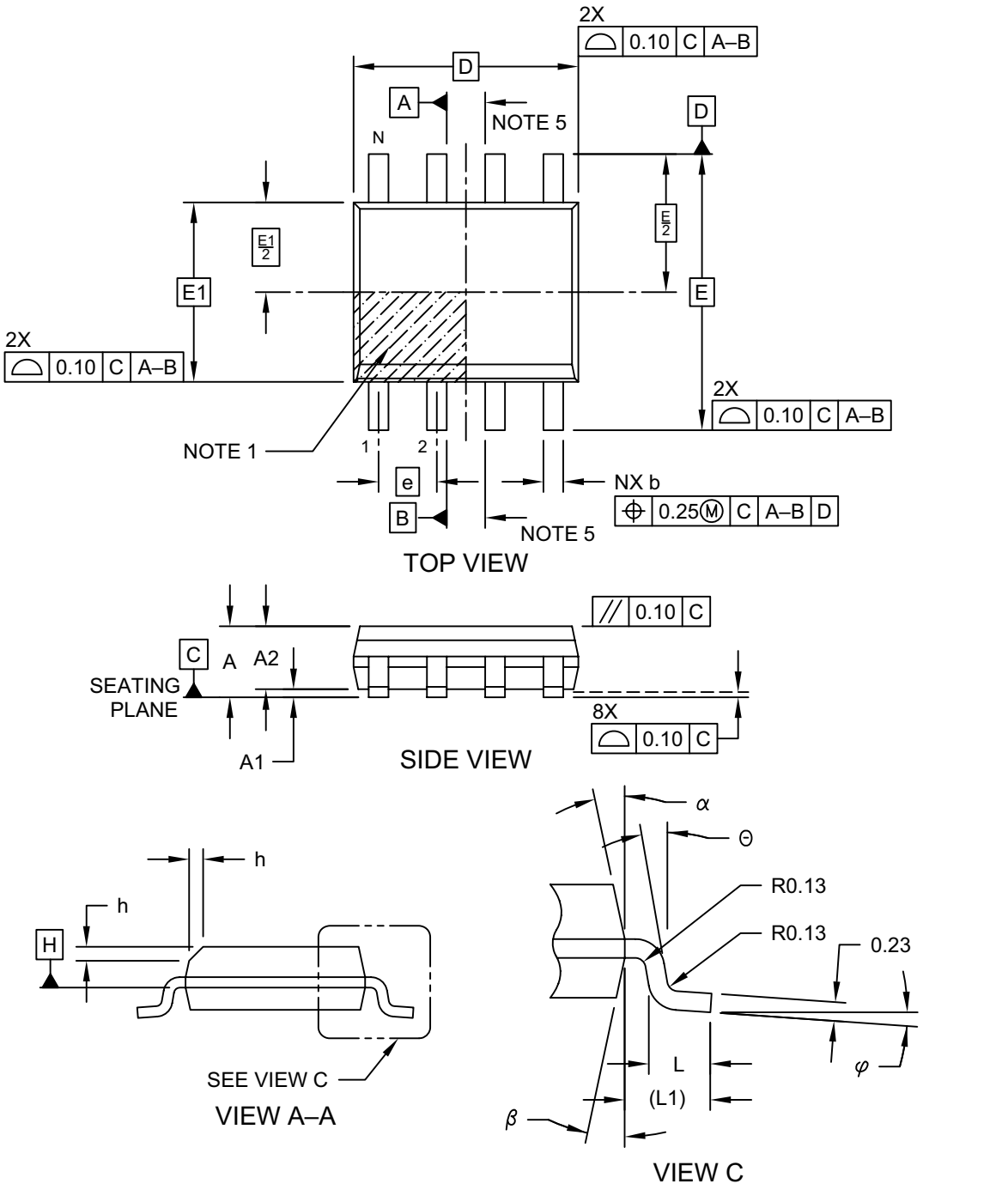
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) symbol may not be to scale.

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

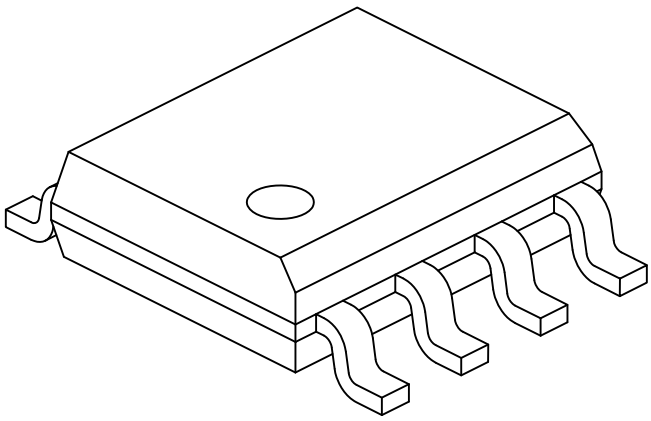


Microchip Technology Drawing No. C04-057-OA Rev F Sheet 1 of 2

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8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

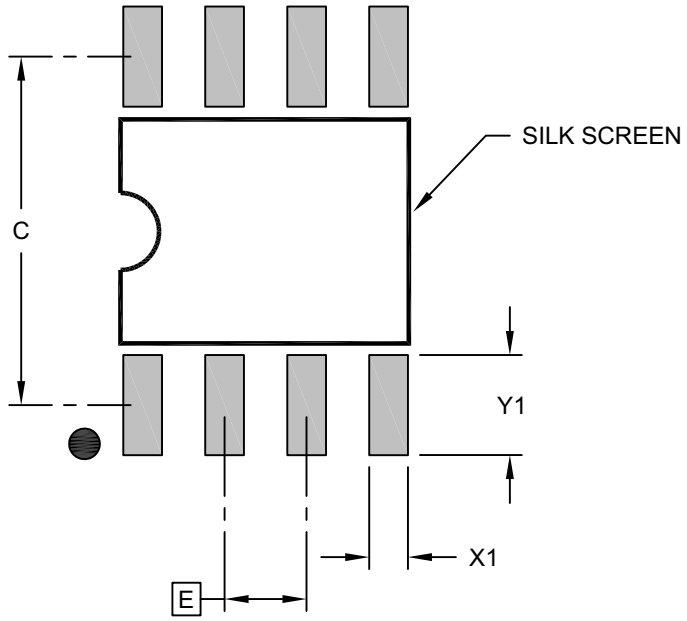
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-OA Rev F Sheet 2 of 2

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8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

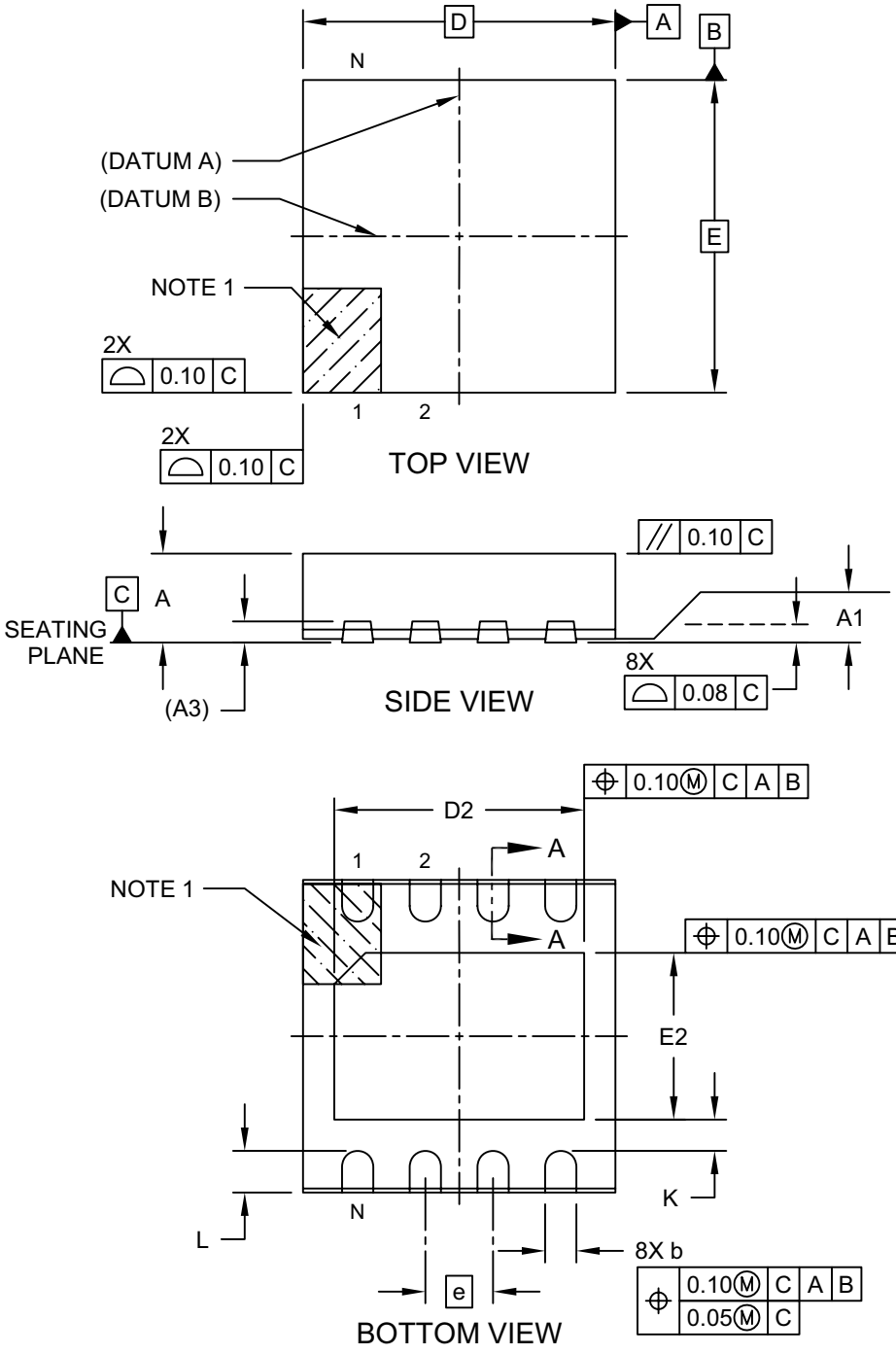
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-OA Rev F

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8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN]
With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

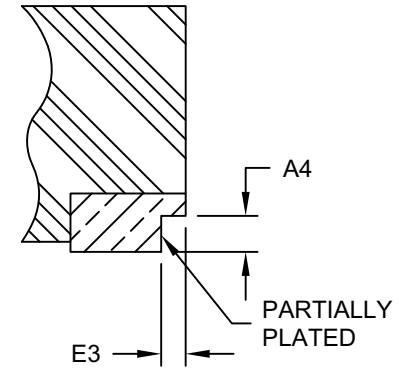
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



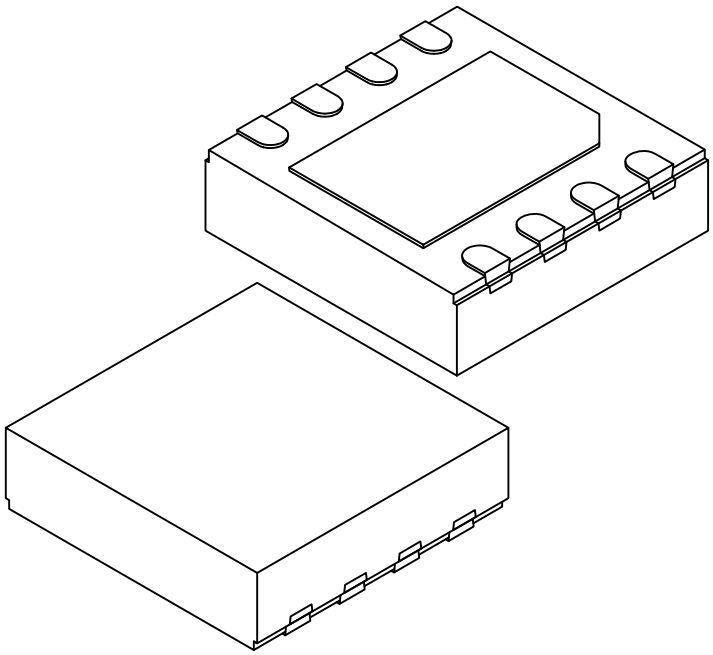
Microchip Technology Drawing C04-21358 Rev C Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy YCL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A–A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	-	0.19
Wettable Flank Step Cut Width	E3	-	-	0.085

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

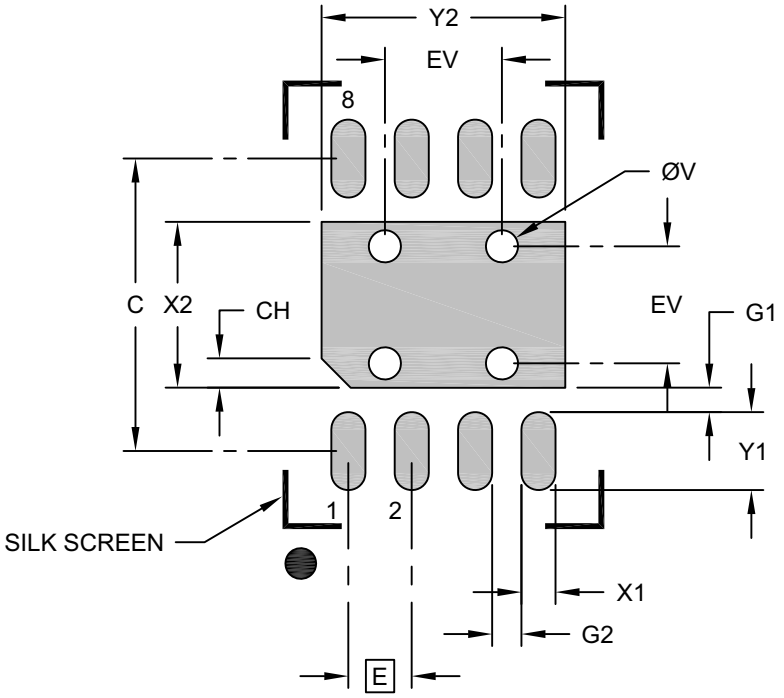
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev C Sheet 2 of 2

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8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev C

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision D (June 2021)

The following is the list of modifications:

- The current LIN standards use the terminology "Master" and "Slave". The LIN standard groups have decided that the terms "Commander" and "Responder" will be used in future.
- Updated the VDFN8 package drawing.
- Minor text updates.

Revision C (July 2020)

- Parameter 13.1 in chapter **2.0 "Electrical Characteristics"** updated
- Updated the marking information for the SOIC package in the **"Package Marking Information"** section

Revision B (April 2020)

- **"Package Marking Information"** updated
- Minor editorial changes

Revision A (April 2019)

- Original release of this document
- Minor text updates
- This document replaces Atmel – 9359D-AUTO-10/16

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. — XX [X](1) [X]
Device / Package / Tape and Reel Option / Package Directives Classification

Device:	ATA663211	
Package:	GA = 8-Lead SOIC GB = 8-Lead VDFN	
Tape and Reel Option:	Q	= 330 mm diameter Tape and Reel(1)
Package Directives Classification:	W	= Package according to RoHS(1)

Examples:

a) ATA663211-GAQW 8-Lead SOIC, Tape and Reel package according to RoHS

b) ATA663211-GBQW 8-Lead VDFN, Tape and Reel package according to RoHS

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: RoHS compliant; maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

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