Features

- Supported Frequency Ranges
  - Low-band 310MHz to 318MHz, 418MHz to 477MHz
  - High-band 836MHz to 928MHz
  - 315.00MHz/433.92MHz/868.30MHz and 915.00MHz with one 24.305MHz Crystal
- Low Current Consumption
  - 9.3mA for RXMode (Low-Band) 480µA for 50ms cycle 3 Channel Polling
  - 9.1mA/13.8mA for TXMode (Low-Band, Pout = 6dBm/10dBm)
- Typical OFFMode Current of 5nA (Max. 600nA at Vs = 3.6V and T = 85°C)
- Programmable Output Power –12dBm to +14.5dBm (0.4dB Step)
- Input 1dB Compression Point
  - –35dBm (Full Sensitivity Level)
  - –20dBm (15dB reduced Sensitivity)
- Programmable Channel Frequency with Fractional-N PLL
  - 93Hz Resolution for Low-Band
  - 185Hz Resolution for High-Band
- FSK Deviation ±0.375kHz to ±93kHz
- FSK Sensitivity (Manchester Coded) at 433.92MHz
  - –106dBm at 20Kbit/s, Δf = ±20kHz, BW_{IF} = 165kHz
  - –109dBm at 10Kbit/s, Δf = ±10kHz, BW_{IF} = 165kHz
  - –112dBm at 5Kbit/s, Δf = ±5kHz, BW_{IF} = 165kHz
  - –121dBm at 0.75Kbit/s, Δf = ±0.75kHz, BW_{IF} = 25kHz
- ASK Sensitivity (Manchester Coded) at 433.92MHz
  - –107dBm at 20Kbit/s, BW_{IF} = 366kHz
  - –117dBm at 1Kbit/s, BW_{IF} = 366kHz
- Programmable RX-IF Bandwidth 25kHz to 366kHz (approx. 10% Steps)
- Blocking (BW_{IF} = 165kHz): 64dBC at Freq. Offset = 1MHz and 48dBC at 225kHz
- High Image Rejection 55dB (315MHz/433.92MHz) 47dB (868.3MHz/915MHz) without Calibration
- Supported Buffered Data Rate 0.5Kbit/s to 20Kbit/s (Higher Data Rates up to 80Kbit/s Manchester Coded and 160Kbit/s NRZ with Transparent Data In/Output)
- Supports Pattern Based Wake-Up and Start of Frame Identification
- Digital RSSI with Very High Relative Accuracy of ±1dB due to Digitized IF Processing
- Programmable Clock Output Derived from Crystal Frequency
- 24KB ROM with Atmel Firmware and Integrated AVR® Microcontroller for Control
- 6KB In System Self Programmable Flash for an Additional Customer Application Software
- 512 byte EEPROM Data Memory for Transceiver Configuration and 768 byte SRAM
- SPI Interface for RX/TX Data Access and Transceiver Configuration
- Configurable EVENT Signal Indicates the Status of the IC
- Automatic Antenna Tuning at TX Center Frequency for Loop Antenna
- Automatic Low Power Channel Polling (3 RKE channels, TPMS, RS)
- ID Scanning up to 18 Different IDs with 1..4 byte
- Supply Voltage Ranges 1.9V to 3.6V and 4.5V to 5.5V
- Temperature Range –40°C to +105°C
- ESD Protection at all Pins (±4kV HBM, ±200V MM, ±750V FCDM)
- Small 5mm × 5mm QFN32 Package/Pitch 0.5mm
- Suitable for Applications Governed by EN 300 220 and FCC Part 15, Title 47

UHF ASK/FSK Transceiver

Atmel ATA5830 ATA5830N

Summary

NOTE: This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

9208DS–RKE–07/11

1. General Product Description

1.1 Overview

The Atmel® ATA5830 is a highly integrated, low power UHF ASK/FSK RF-transceiver. The Atmel ATA5830 is partitioned into several sections; an RF frontend, a digital baseband, and a low power 8 bit AVR microcontroller. The product is designed for the ISM frequency bands in the ranges of 310 to 318MHz, 418 to 477MHz and 836 to 928MHz. External part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. The receive path uses a low-IF architecture with an integrated double quadrature receiver and digitized IF processing. This results in high image rejection and excellent blocking performance. The transmit path uses a closed loop fractional-N modulator with gaussian shaping and preemphasis functionality for high data rates. In addition, the highly flexible and configurable baseband signal processing allows the transceiver to operate in several scanning, wake-up and automatic self polling scenarios. For example, during polling the IC can seek certain message content (IDs) and save valid telegram data in the FIFO buffer for later retrieval. The device possess two receive paths that enable parallel search for two telegrams with different modulations, data rates, wake-up conditions, etc. The highly configurable and autonomous scanning capability enables polling of up to five application channels such as 3-channel RKE, TPMS, PEG. The configuration of the transceiver is stored in a 512 byte EEPROM. The SPI allows for external control and reconfiguration of the device. The internal microcontroller and 6 KB Flash can be used to add customer extensions to the Atmel firmware. The debug wire and ISP interface are available for programming purposes.

1.2 Target Applications

The transceiver is designed to be used in the following application areas:

- Remote Keyless Entry System (RKE)
- Passive Entry Go System (PEG)
- Tire Pressure Monitoring System (TPM,TPMS)
- Remote Start System (RS)
- Remote Control System, e.g. garage door open
- Smart RF applications
- Telemetering Systems

Three applications with a total of 5 channels are supported by the Atmel firmware for autonomous self polling.

1.3 Main Extended Features of the Atmel ATA5830

1.3.1 RF Performance

The Atmel® ATA5830 provides high sensitivity and programmable transmit power up to 14dBm. The high image rejection and outstanding blocking performance enable a robust application against interferer with a low cost design. In addition, the programmable channel filter bandwidth provides flexibility to adapt to various system requirements.

1.3.2 Automatic Self Polling and Multi Channel Capability

The autonomous self polling supports the automatic scanning for three different applications such as Remote Keyless Entry (RKE), Tire Pressure Monitoring System (TPMS) and Remote Start (RS) using one IC. Additionally multi channel systems with up to three frequencies can be scanned. This means five frequencies can be scanned in the autonomous polling scheme; three for RKE, one for TPMS and one for RS. The configuration of each application is independent of the others. This is possible because of the flexibility in the digital baseband and two different baseband receiving paths. The IC can immediately scan all applications upon power-up without the need for any initial configuration by an external microcontroller.

1.3.3 Wake-up Scenario and ID Scanning

The powerful baseband signal processing is designed to offload these time consuming tasks from the host controller. This allows the transceiver to discard unwanted telegrams and limit external microcontroller wake up to valid telegrams only. Up to 7 criteria can be used to determine the telegram validity from carrier check on the lowest level to start of frame ID pattern match at the highest level.

1.3.4 Two Parallel Receiving Paths

The transceiver's baseband contains two data paths. The parameters of both paths can be set differently, e.g. the modulation type or data rate. Generally both paths are working simultaneously but only the first path detecting a valid telegram will be used for further data reception and filling of the 32 byte buffer. The 32 byte receive data buffer can be accessed using SPI commands from the external host microcontroller.

1.3.5 Channel Statistic

In order to accelerate the communication in multi channel applications the Atmel ATA5830 offers a feature defined as channel statistic. If this feature is selected, the IC will find the best channel within the three RKE channels (with regard to interference) and automatically select the best channel for the first transmission.

1.3.6 Antenna Tuning and SPDT

For applications using a loop antenna, the Atmel ATA5830 offers an automatic antenna tuning feature which improves the antenna performance by compensating for "hand effects" or matching component value variations. The integrated SPDT acts as RX/TX switch which eliminates the cost of an external RX/TX switch.

1.3.7 Customer Application Software

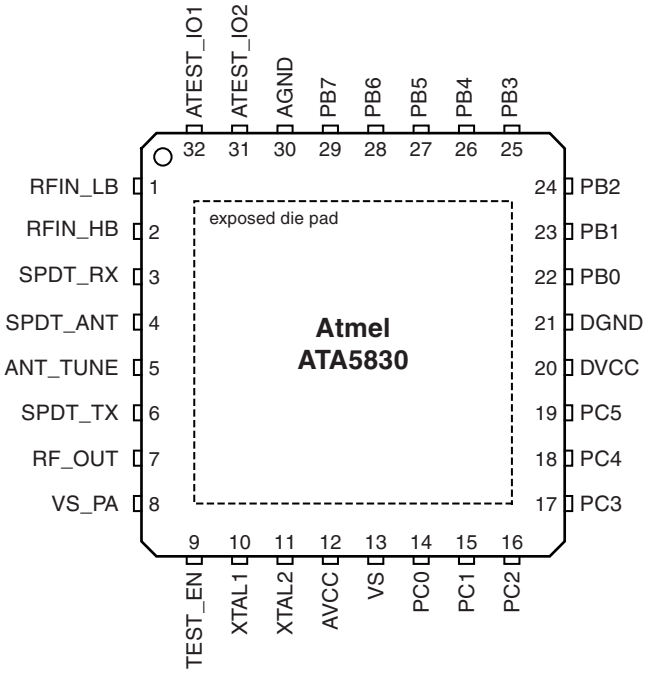
All the functionality is implemented in 24KB of ROM firmware and controlled by SPI commands. In addition, 6KB of Flash is available to enable customer specific software functionality. Examples for flash customization are a) extension of SPI commands, b) usage of a single wire interface instead of SPI, c) polling adaptations, d) protocol handling, etc. To achieve customer specific functionality, parts of the ROM code can be replaced with Flash code.

1.3.8 EEPROM Configuration

The configuration of the device e.g. RF-frequency, modulation type, data rate, etc. is stored in 512KB of EEPROM that is integrated within the Atmel® ATA5830. This improves the efficiency of the SPI control since most of the configuration comes from the EEPROM. In most applications, only the received or transmitted data and short SPI commands are required. The device is delivered with a standard configuration; only deviations from that need to be configured. Device configuration uses only a part of the 512KB of EEPROM leaving free space available for additional customer data storage.

1.4 Pin Diagram and Configuration of Atmel ATA5830

Figure 1-1. Pin Diagram



Note: The exposed die pad is connected to the internal die.

Table 1-2. Pin Configuration

Pin No.	Pin Name	Type	Description
1	RFIN_LB	Analog	RXMode, LNA input for Low-Band frequency range (< 500MHz)
2	RFIN_HB	Analog	RXMode, LNA input for High-Band frequency range (> 500MHz)
3	SPDT_RX	Analog	RXMode output of the SPDT switch (Damped signal output)
4	SPDT_ANT	Analog	Antenna input (RXMode) and output (TXMode) of the SPDT switch
5	ANT_TUNE	Analog	Antenna tuning input
6	SPDT_TX	Analog	TXMode Input of the SPDT switch
7	RFOUT	Analog	Power amplifier output
8	VS_PA	Analog	Power amplifier supply - 3V application supply voltage input - 5V application internal voltage regulator output
9	TEST_EN	-	Test enable, connected to GND in application
10	XTAL1	Analog	Crystal oscillator pin1 (Input)
11	XTAL2	Analog	Crystal oscillator pin2 (output)
12	AVCC	Analog	RF frontend supply regulator output
13	VS	Analog	Main supply voltage input
14	PC0	Digital	Main: AVR Port C0 Alternate: PCINT8/NRESET/Debug Wire
15	PC1	Digital	Main: AVR Port C1 Alternate: NPWRON1/PCINT9
16	PC2	Digital	Main: AVR Port C2 Alternate: NPWRON2/PCINT10/TRPA
17	PC3	Digital	Main: AVR Port C3 Alternate: NPWRON3/PCINT11/TMDO/TxD
18	PC4	Digital	Main: AVR Port C4 Alternate: NPWRON4/PCINT12/INT0/ TMDI/RxD
19	PC5	Digital	Main: AVR Port C5 Alternate: NPWRON5/PCINT13/TRPB/ TMDO_CLK
20	DVCC	-	Digital supply voltage regulater output
21	DGND	-	Digital ground
22	PB0	Digital	Main: AVR Port B0 Alternate: PCINT0/CLK_OUT
23	PB1	Digital	Main: AVR Port B1 Alternate: PCINT1 / SCK
24	PB2	Digital	Main: AVR Port B2 Alternate: PCINT2/MOSI (Master Out Slave In)
25	PB3	Digital	Main: AVR Port B3 Alternate: PCINT3/MISO (Master In Slave Out)
26	PB4	Digital	Main: AVR Port B4 Alternate: PWRON/PCINT4/LED1 (strong high side driver)
27	PB5	Digital	Main: AVR Port B5 Alternate: PCINT5/NSS
28	PB6	Digital	Main: AVR Port B6 Alternate: PCINT6/EVENT (firmware controlled external microcontroller event flag)

Table 1-2. Pin Configuration (Continued)

Pin No.	Pin Name	Type	Description
29	PB7	Digital	Main: AVR Port B7 Alternate: NPWRON6/PCINT7/ RX_ACTIVE (strong high side driver)/ LED0 (strong low side driver)
30	AGND	-	Analog ground
31	ATEST_IO2	-	RF frontend test input/output 2, connected to GND in application
32	ATEST_IO1	-	RF frontend test input/output 1, connected to GND in application
	GND	-	Ground/Backplane on exposed die pad

1.5 Typical Application Circuits

Figure 1-1. Typical 3V Application with External Microcontroller

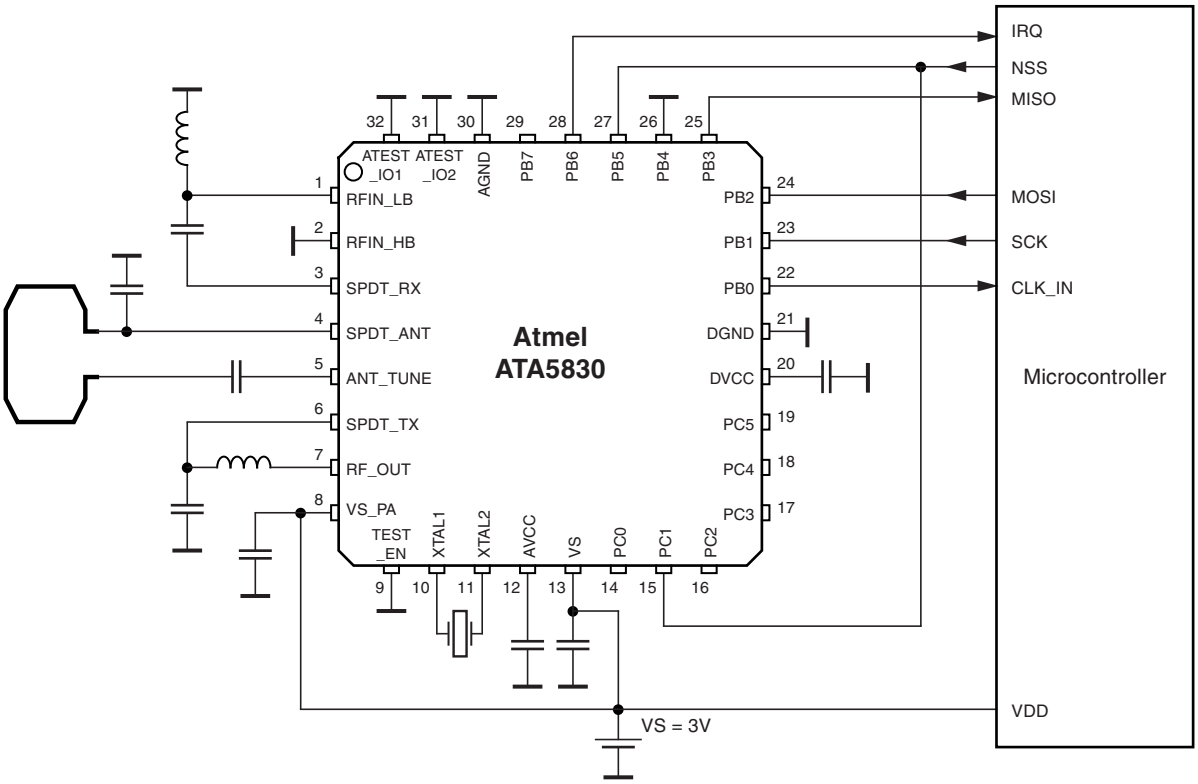


Figure 1-1 shows a key fob application circuit with an external host microcontroller for 315MHz or 433.92MHz running from a 3V lithium cell. The Atmel® ATA5830 stays in OFFMode until NSS(PB5) and NPWRON1(PC1) are used to wake it. In OFFMode the Atmel ATA5830 draws typically less than 5nA (600nA maximum at 3.6V/85°C).

In OFFMode all Atmel® ATA5830 AVR® Ports PB0..PB7 and PC0..PC5 are switched to Input. PC0..PC5 and PB7 have internal pull-up resistors ensuring that the voltage at these ports is VS. PB0..PB6 are tristate inputs and require additional consideration. PB1,PB2 and PB5 have defined voltages since they are connected to the output of the external microcontroller. PB4 is connected to ground to avoid unwanted power ups. PB0, PB3 and PB6 do not require external circuitry since the internal circuit avoids transverse currents in the OffMode. The external microcontroller has to tolerate the floating inputs. Otherwise additional pull down resistors are required on these floating lines.

Typically, the key fob buttons are connected to the external microcontroller and the Atmel ATA5830 wake-up is done by pulling NSS (pin 27) and NPWRON1 (pin 15) to ground. If there are not enough ports for button inputs on the microcontroller, it is possible to connect up to four additional buttons to the Ports PC2..PC5. In this case, the occurrence of a port event (button pressed) will generate an interrupt (pin 28). The port event that triggered the interrupt is available in the event register.

In this type of application a PCB trace loop antenna is typically used. An internal antenna tuning procedure tunes the resonant frequency of this loop antenna to the TX frequency. This is accomplished with an integrated variable capacitor on the ANT_TUNE pin. RF_OUT and RF_IN are optimally matched to the SPDT_TX and SPDT_RX pins of the integrated RX/TX switch. The SPDT_ANT pin has an impedance of 50Ω for both the RX and TX functions. The DC output voltage of the power amplifier is required at the SPDT_TX pin for proper operation. Also, the RFIN pin needs a DC path to ground, which is easily achieved with the matching shunt inductor. The impedance of the loop antenna is transformed to 50Ω with three capacitors, two of them external and one built into the Atmel ATA5830 on the ANT_TUNE pin.

An external crystal, together with the fractional-N PLL within the Atmel ATA5830 is used to fix the RX and TX frequency. Accurate load capacitors for this crystal are integrated, to reduce system part count and cost. Only four supply blocking capacitors are needed to decouple the different supply voltages AVCC, DVCC, VS and VS_PA of the Atmel ATA5830. The exposed die pad is the RF and analog ground of the Atmel ATA5830. It is directly connected to AGND via a fused lead. For applications operating in the 868.3MHz or 915MHz frequency bands, a high band RF input is supplied, RFIN_HB, and must be used instead of RFIN_LB.

The Atmel ATA5830 is controlled using specific SPI commands via the SPI interface and an internal EEPROM for application specific configuration.

Figure 1-3. Typical 3V Stand Alone Application

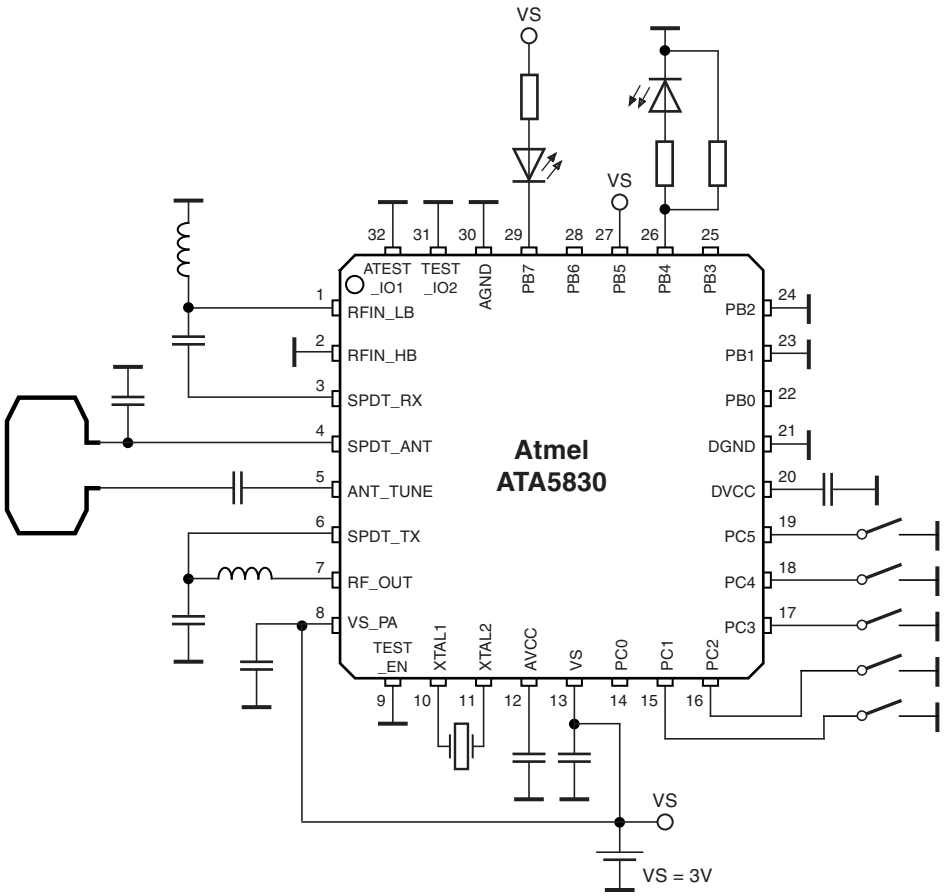


Figure 1-3 shows a stand alone key fob application circuit for 315MHz or 433.92MHz running from a 3V lithium cell. The Atmel® ATA5830 stays in OFFMode until one of the NPWRON Ports PC1..PC5 are pulled to ground level and therefore waking up the circuit. The NPWRON Ports PC1..PC5 have internal 50kΩ pull-up resistors and can be left open if not used.

Application software within the 6KB Flash is used to control the Atmel ATA5830 together with firmware in the 24KB ROM. The RF and decoupling circuitry is similar to Figure 1-1 on page 7.

In this application, an LED is connected to PB7 (alternatively, an additional wake-up button can be used on PB7 instead of an LED). An LED can also be connected to PB4. However, note the additional pull-down resistor connected in parallel that is needed to prevent transverse currents in OFFMode. This special case applies to PB4 because of its active input characteristics (PWRON).

Figure 1-4. Typical 5V Application Circuit with External Microcontroller

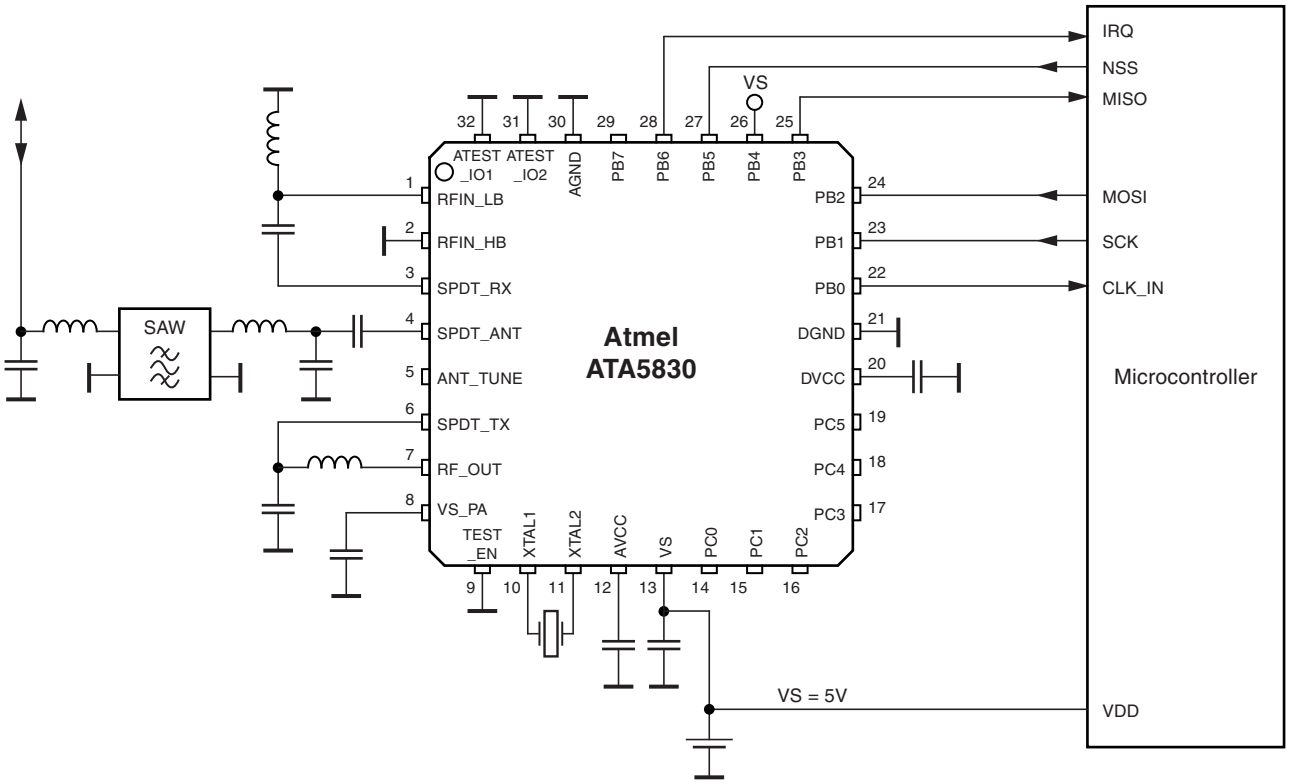


Figure 1-4 shows a typical vehicle side application circuit with an external host microcontroller running from a 5V voltage regulator. In contrast to the 3V application with external microcontroller, the pin PB4 (PWRON) is directly connected to VS and the Atmel® ATA5830 enters the IDLEMode after power on. In this configuration the Atmel ATA5830 can work autonomously while the microcontroller stays powered down to achieve low current consumption while being sensitive to RF telegrams.

To achieve low current in IDLEMode the Atmel ATA5830 can be configured in the EEPROM to work with the 125kHz RC oscillator (this mode is named IDLEMode(RC)). The Atmel ATA5830 can also be configured for autonomous multi channel and multi application PollingMode(RC). The external microcontroller is notified with IRQ if an appropriate RF message is received. Until that takes place, the Atmel ATA5830 periodically switches to RXMode, checks the different channels and applications configured in the EEPROM and returns to the IDLEMode(RC) all the while with the external host AVR® microcontroller in a deep sleep mode to achieve a low average current while being polling for valid RF messages. Once a valid RF message is detected, it can be buffered within the Atmel ATA5830 to allow the microcontroller time to wake-up and retrieve the buffered data.

In applications that use the 4.5 to 5.5V supply (VS), it is important to note that only Atmel ATA5830 Ports PB0..PB7, PC0..PC5 and the external host microcontroller use this supply. The power amplifier of the Atmel ATA5830 is limited to 3.6V therefore an internal LDO delivers 2.7V to 3.3V supply voltage in TXMode on pin VS_PA. The capacitor on pin VS_PA is needed to stabilize this regulator and decouple the power amplifier supply voltage. The ports PC0..PC5 have internal 50kΩ pull-up resistors and can be left open. The ANT_TUNE pin must be left open.

As in the 3V applications, RF_OUT and RF_IN are matched to SPDT_TX and SPDT_RX by absorbing the parasitics of the SPDT switch into the matching network, hence the SPDT_ANT is a 50Ω RX and TX port. The impedance of the SAW filter is transformed with LC matching circuits to the SPDT_ANT port and also to the antenna. Care has to be taken to insure the transmit power going through the SAW does not exceed its power handling capability. The series capacitor on pin SPDT_ANT is needed because the DC voltage on this pin is set to VS_PA/2 voltage in TXMode and SAW filters normally should not be subjected to a DC voltage. Alternatively, the SAW can also be inserted between SPDT_RX and RF_IN. In this case, special care for spurious and harmonics of the TX signal is required.

Figure 1-2. Typical 5V Application Circuit with One Wire Control

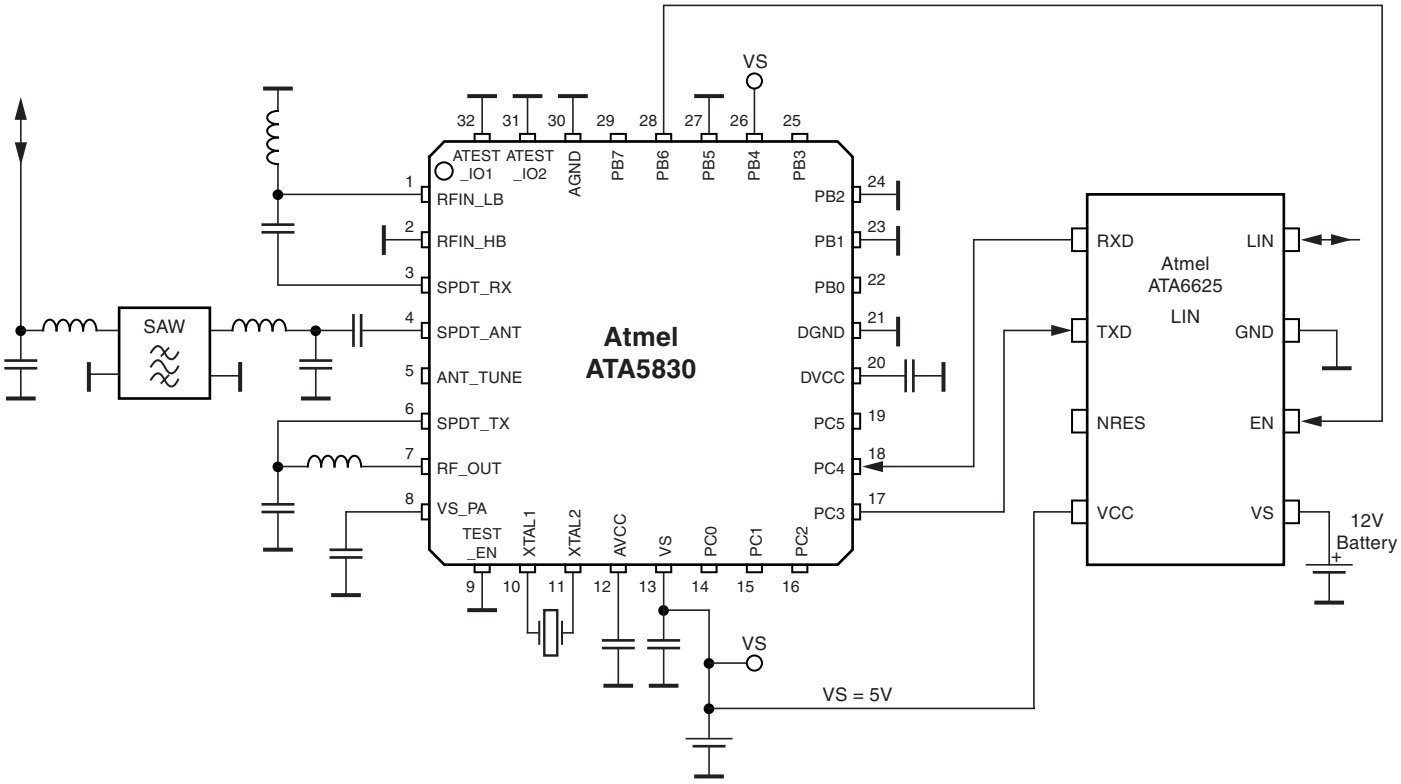


Figure 1-2 shows a typical vehicle side application circuit running from a 5V voltage regulator delivered from the LIN transceiver ATA6625 device. The application can be directly connected to vehicle's wiring harness. In this case, the pin PB4 (PWRON) is directly connected to VS and the Atmel® ATA5830 enters the IDLEMode upon power up of the ATA6625 and stays there after the software in the Flash asserts the EN pin on ATA6625 to HIGH. The system can be completely switched on or off with a command over the one wire bus. This application is used when the external host microcontroller must be separated over a distance from the Atmel ATA5830 such as systems having remote antennas integrated into window glass. In these situations, the Atmel ATA5830 can work autonomously and communicate to external host microcontroller on a 1 wire bus.

The Application software within the 6KB Flash, together with 24KB ROM firmware, is used for the control of the Atmel ATA5830 and Atmel ATA6625. A simplified LIN compliant physical layer can be used for one wire communication. The Atmel ATA5830 does not natively support one wire commands. However, through the use of application Flash software one wire communication can be achieved.

Please refer to the note in the previous example (Figure 1-4 on page 9) regarding the use of a 4.5 to 5.5V supply and its distribution within the Atmel® ATA5830. Ports PC0..PC2 have internal 50kΩ pull-up resistors and can be left open. But, ports PB1, PB2 and PB5 must be connected to ground. The ANT_Tune pin has to be left open. Notes about RF decoupling and supply circuitry are the same as application shown in Figure 1-4 on page 9.

1.6 System Overview

Figure 1-3. Circuit Overview

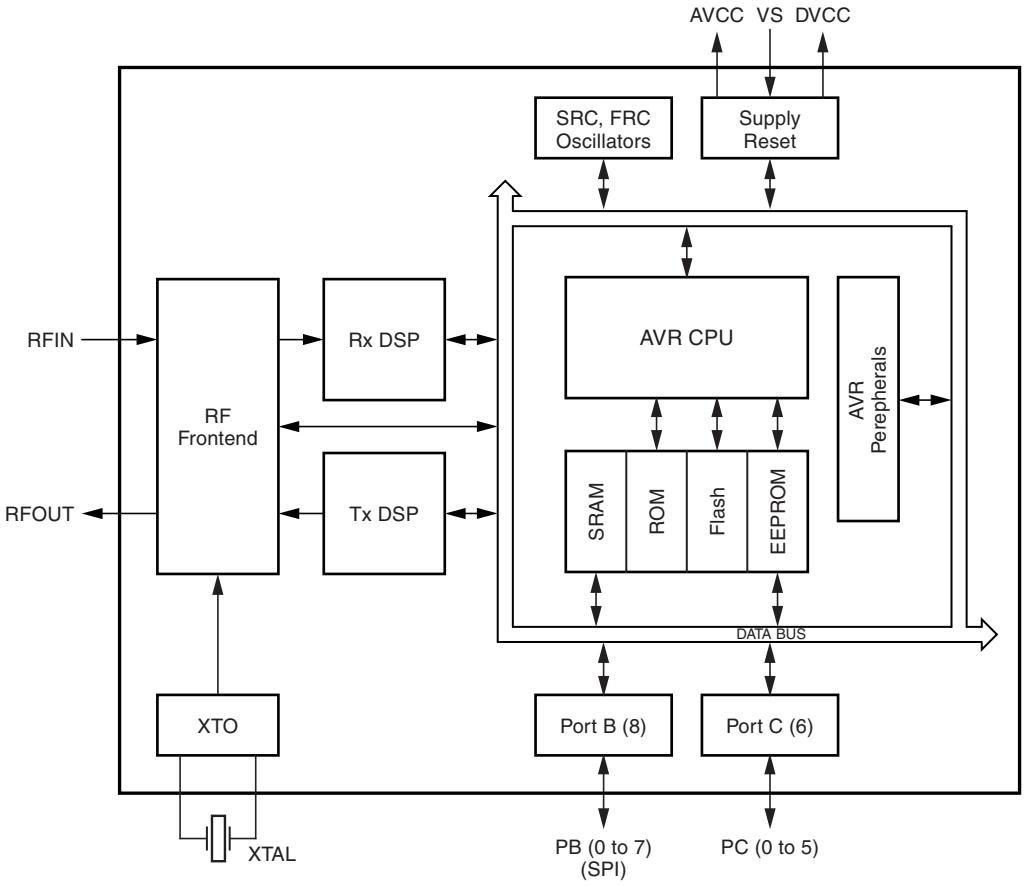


Figure 1-3 shows an overview of the main functional blocks of the Atmel ATA5830. The control of the Atmel ATA5830 is performed through the SPI pins SCK, MOSI, MISO and NSS found on port B. The configuration of the Atmel ATA5830 is stored in the EEPROM and a large part of the functionality is defined with the firmware located in the ROM and processed using the AVR®. e.g. a SPI command like “Start RXMode” uses the information located in the EEPROM configures all hardware registers of the different blocks according to this information, starts then the RXMode and directs the received data to the Rx Buffer located in the SRAM. An EVENT on port PB6 is signaled to the external microcontroller when the expected number of bytes are received.

Part of the EEPROM content is copied to the SRAM during start-up of the Atmel ATA5830 for faster access. Care should be taken to limit EEPROM R/W cycles so that the device's maximum rating is not exceeded. Alternatively, the user should consider modifying the parameters in the SRAM.

It is important to note that PWRON and NPWRON pins are active in OFFMode. This means that even if the Atmel® ATA5830 is in OFFMode and the DVCC voltage is switched off, power management circuitry within the Atmel ATA5830 will bias these pins with VS.

AVR® Ports can be used as button inputs, external LNA supply voltage (RX_ACTIVE), LED driver, Event Pins, switching control for additional SPDT switches, general purpose digital inputs, wake up inputs etc. Some functionality of these ports is already implemented in the firmware and can be activated with EEPROM configuration. Other functionality is possible only through custom software residing in the 6KB Flash program memory.

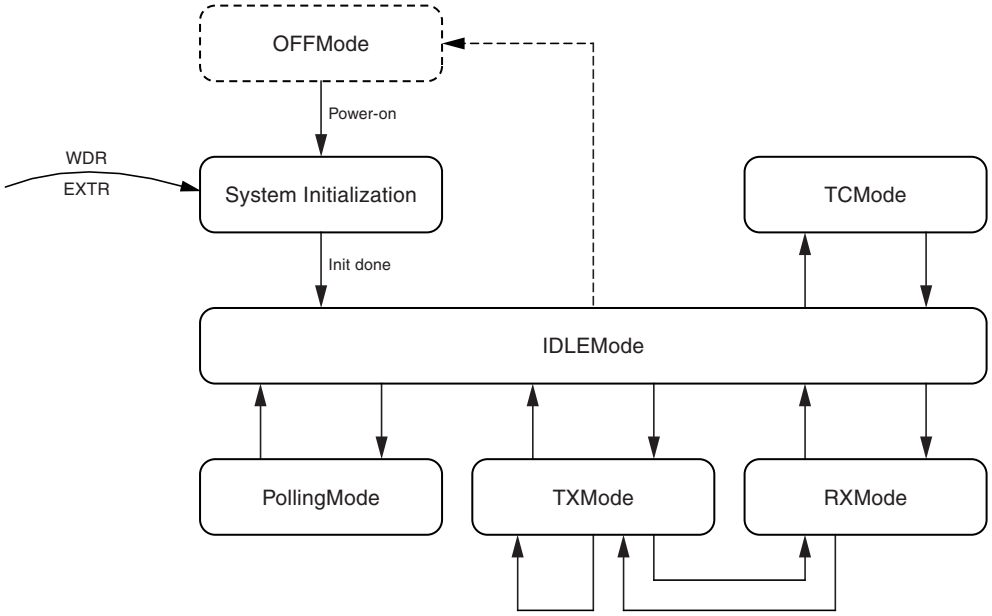
1.7 Compatibility to the Atmel UHF Receiver ATA5780

The transceiver Atmel ATA5830 is pin compatible to the receiver ATA5780. The receiver has the identical RX performance of the transceiver RX path. The difference exists in the digital block only. While extremely flexible, the receiver operates as a statemachine and its functionality is limited to user selectable EEPROM configuration options. As a result, the receiver is fully compatible with the transceiver but without the flexibility of 6KB Flash program space for custom applications.

2. System Operation Modes

The scope of this section is to give an overview of the Atmel® ATA5830 supported operation modes, shown in Figure 2-1.

Figure 2-1. Operation Modes Overview



After connecting the supply voltage to the VS pin, the Atmel ATA5830 always starts in OFF-Mode. All internal circuits are disconnected from the power supply. Therefore no SPI communication is supported. The Atmel ATA5830 can be woken up by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence. After firmware initialization the Atmel ATA5830 reaches the IDLEMode.

The IDLEMode is the basic system mode supporting SPI communication and transitions to all other operation modes. There are two options of the IDLEMode to be configured in the EEPROM settings:

- IDLEMode(RC) with low power consumption using the Fast RC (FRC) oscillator for processing
- IDLEMode(XTO) with active crystal oscillator for high accuracy clock output or timing measurements

The transmit mode (TXMode) allows for data transmission on one of the preconfigured channels for e.g. RKE, TPM, RS. It is usually enabled by SPI command, or directly after power-on, when selected in the EEPROM setting.

The receive mode (RXMode) provides data reception on one of the preconfigured channels. The precondition for data reception is a valid preamble. The receiver is continuously searching for a valid telegram and receives the data if all preconfigured checks are successfully passed. The RXMode is usually enabled by SPI command, or directly after power-on, when selected in the EEPROM setting.

In PollingMode the receiver is activated for a short period of time to check for a valid telegram on the selected channels. The receiver will be deactivated if no valid telegram is found and a sleep period with very low power consumption elapses. This process is repeated periodically according to the EEPROM configuration. Up to 5 channels and a wide range of sleep times are supported by the Atmel firmware. This mode is activated via an SPI command, or directly after power-on, when selected in the EEPROM setting.

The tune and check mode (TCMode) offers a calibration and self-checking functionality for the VCO and FRC oscillators as well as for the antenna tuning and polling cycle accuracy. This mode is activated via an SPI command. When selected in the EEPROM settings the TCMode is used during system initialization after power-on. Furthermore, the TCMode can be activated periodically during PollingMode.

Table 2-1 shows the relations between the operation modes and its corresponding power supplies, clock sources and sleep mode settings.

Table 2-1. Operation Modes versus Supplies and Oscillators

Operation Mode	AVR Sleep Mode	DVCC	AVCC	VS_PA	XTO	SRC	FRC
OFFMode	-	off	off	off	off	off	off
IDLEMode(RC)	Active mode	on	off	off	off	on	on
	Power-down(1)		off	off	off	on	off
IDLEMode(XTO)	Active mode		on	off	on	on	off
	Power-down(1)		on	off	on	on	off
TXMode	Active mode		on	on(2)	on	on	off
RXMode	Active mode		on	off	on	on	off
PollingMode(RC)							
- Active Period	Active mode		on	off	on	on	on
- Sleep Period	Power-down(1)		off	off	off	on	off
PollingMode(XTO)							
- Active Period	Active mode		on	off	on	on	off
- Sleep Period	Power-down(1)		on	off	on	on	off

Notes:
1. During IDLEMode(RC) and IDLEMode(XTO) the AVR microcontroller will enter a sleep mode to reduce the current consumption. The sleep mode of the microcontroller section can be defined in the EEPROM. To achieve the optimum current consumption the power-down mode is recommended.
2. Only activated at 5 V applications. This is selectable in the EEPROM setting.

3. Hardware Description

3.1 Overview

Figure 3-1. System Block Diagram

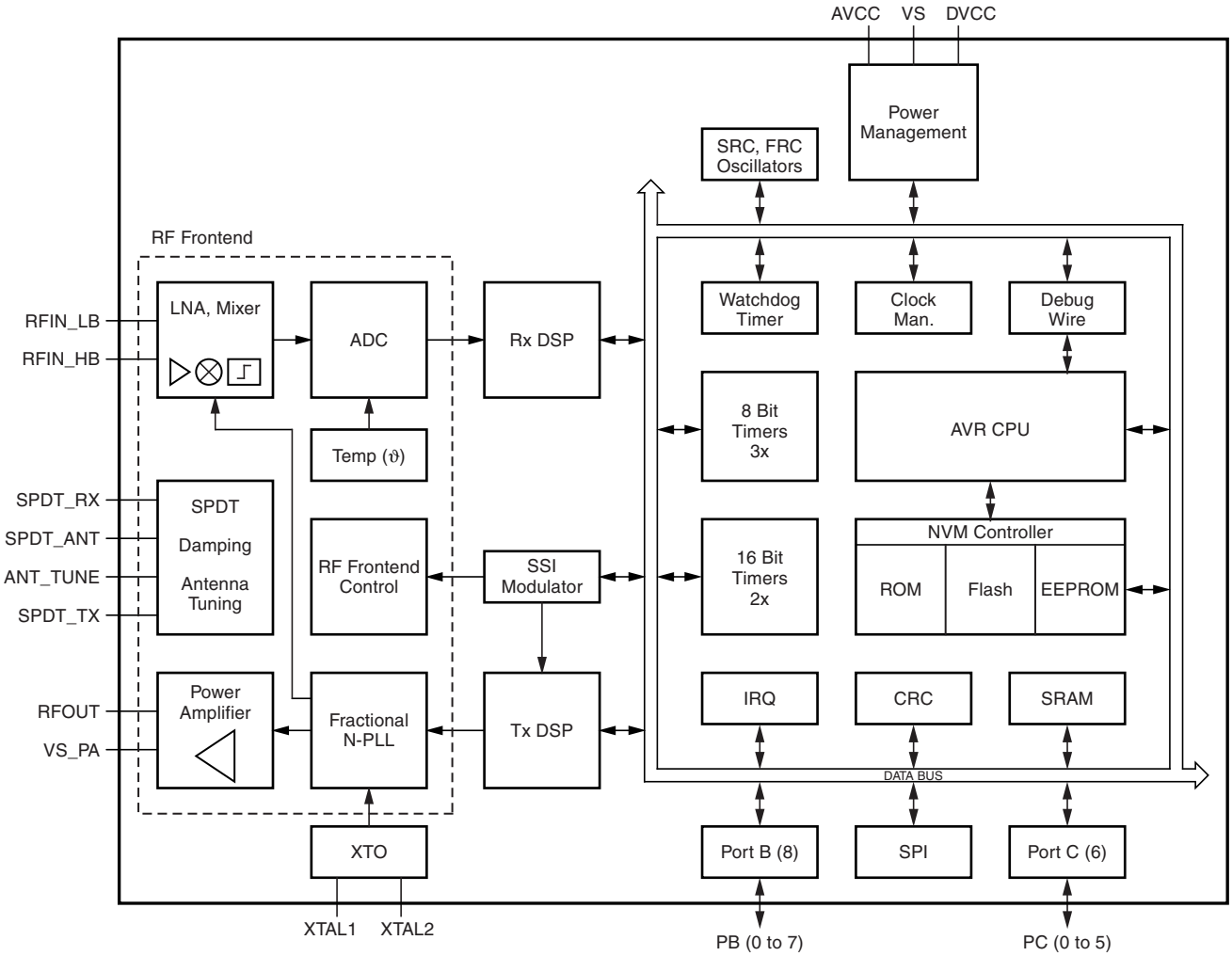


Figure 3-1 shows the system block diagram of Atmel® ATA5830.

In RXMode the crystal oscillator (XTO) together with the fractional-N PLL generates the local oscillator (LO) signal.The RF signal coming either from the lowband input (RFIN_LB) or high-band input (RFIN_HB) is amplified by the low noise amplifier (LNA) and downconverted by the mixer to the intermediate frequency (IF) using the LO signal. Afterwards the IF signal is sampled using a high resolution analog to digital converter (ADC). Within the RX digital signal processing (RxDSP) the received signal from the ADC is filtered by a digital channel filter and demodulated. Two data receive paths are included into the RxDSP after the digital channel filter. The receive path can also be configured to provide the digital output of an internal temperature sensor (Temp( )).

In TXMode the fractional-N PLL generates the TX frequency. The power amplifier generates a programmable RF output power of –10dBm to 14dBm on RFOUT. The FSK modulation is performed by changing the frequency setting of the fractional-N PLL dynamically with the TX digital signal processing (TxDSP). Digital preemphasis and digital gauss filtering can be activated in the TxDSP for higher data rates or low occupied bandwidth. The ASK modulation is performed by switching the power amplifier on and off.

With the single pole double throw (SPDT) switch the RF signal from the antenna is switched to RFIN in RXMode and from RFOUT to the antenna in TXMode. An adjustable capacitor and an RF leveldetector on ANT_TUNE is used to tune the center frequency of loop antennas to reduce tolerances and capacitive proximity effects.

The system is controlled by an AVR® CPU with 24KB ROM, 6KB Flash, 512byte EEPROM, 768 byte SRAM and other peripherals supporting the transceiver handling. Two ports PB[0..7] and PC[0..5] are available for external digital connections, e.g. the SPI interface is connected to port B. The Atmel® ATA5830 is controlled by EEPROM configuration and SPI commands. The functional behavior is mainly determined by the firmware in the ROM. It can be configured to a high degree by modifying the EEPROM settings. The firmware running on the AVR gives access to the hardware functionality of the Atmel ATA5830. Extensions to this firmware can be added in the 6 KB of Flash memory. The RXDSP and TXDSP registers are directly accessible from the AVR since these DSP's are directly connected to the AVR data Bus. The RF frontend registers are programmed with an on chip serial interface(SSI) accessing the RF frontend control.

The power management contains low-dropout (LDO) regulators and reset circuits for the supply voltages VS, AVCC, DVCC and VS_PA of the Atmel ATA5830. In OFFMode all the supply voltages AVCC, DVCC and VS_PA (VS_PA only for 4.5V to 5.5V operation) are switched off to achieve a very low current consumption. The Atmel ATA5830 can be powered up by activating the PWRON pin or one of the NPWRON1..6 pins since they are still active in OFFMode.

The RF frontend circuits and the XTO are connected to AVCC, the AVCC domain can be switched on and off independently from DVCC.

Atmel ATA5830 provides two idle modes. In IDLEMode(RC) only the DVCC voltage regulator, the FRC and SRC oscillators are active and the AVR uses a power down mode to achieve a low current consumption. The same power down mode can be used during the inactive phases of the PollingMode. In IDLEMode(XTO) the AVCC voltage domain as well as the XTO are activated additionally.

An integrated watchdog timer is available to restart the Atmel ATA5830.

3.2 Receive Path

3.2.1 Overview

The receive path consists of a low noise amplifier (LNA), mixer, analog-to-digital converter (ADC) and a Rx digital signal processor (DSP) as shown Figure 3-1 on page 16. The fractional-N phase locked loop (PLL) and the Quartz oscillator (XTO) described above delivers the local oscillator frequency f_{LO} in RXMode. The receive path is controlled wit the RF frontend registers.

Two separate LNA inputs, one for Low-Band and one for High-Band, are provided to obtain optimum performance matching for each frequency range and to allow multi band applications. A radio frequency (RF) level detector at the LNA output and a switchable damping included into single-pole double-trough (SPDT) switch is used in the presence of large blockers to achieve better system blocking performance.

The mixer converts the received RF signal to a low intermediate frequency (IF) of about 250kHz. A double quadrature architecture is used for the mixer to achieve high image rejection. Additionally, the 3rd order suppression of local oscillator (LO) harmonic receiving will make receiving without a frontend SAW filter, for example in a car keyfob application, less critical.

The ADC converts the IF signal into the digital domain. Due to the high effective resolution (14Bit) of the used ADC the channel filter and RSSI can be realized in the digital signal domain and no analog gain control (AGC) which can lead to critical timing issues or analog filtering is required in front of the ADC. This leads to a receiver frontend with good blocking performance up to the 1dB compression point of the LNA and mixer, and a steep digital channel filters can be used.

The Rx DSP performs channel filtering and converts the digital output signals of the ADC to the baseband for demodulation. Due to the digital realization of these functions the Rx DSP can be adapted to the needs of many different applications since channel bandwidth, data rate, modulation type, wake-up criteria, signal checks, clock recovery and many other properties are configurable. See Rx DSP description in Section 3.2.2 “RX Digital Signal Processing (Rx DSP)” on page 19.

A received signal strength indicator (RSSI) value is built within the Rx DSP completely in the digital signal domain allowing for a high relative RSSI accuracy and a good absolute accuracy, which is only deteriorated by the gain errors of LNA, mixer and ADC.

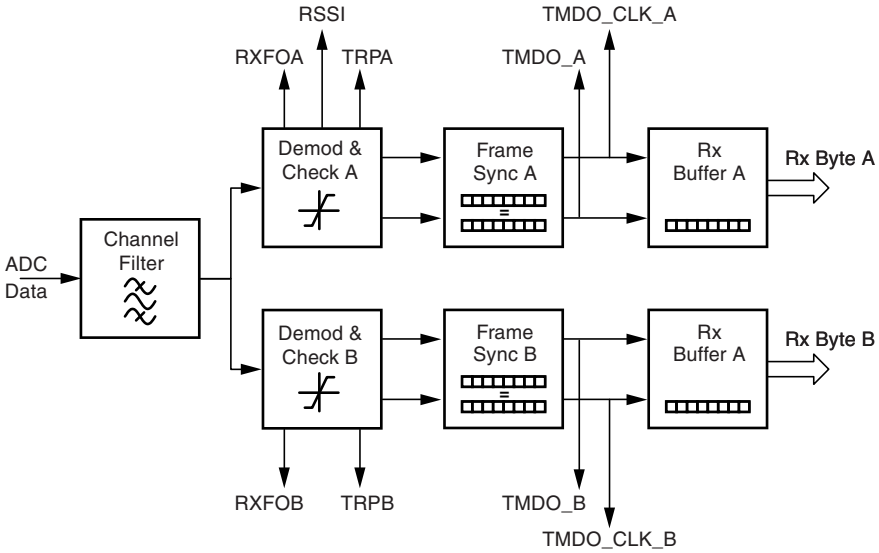
Two independent receive paths A and B are integrated in the Rx DSP after the channel filter see Section 3.2.2 “RX Digital Signal Processing (Rx DSP)” on page 19 and allow the use of different data rate, modulation type and protocol without the need to power up the receive path more than once to decide which signal should be received. This allows a much lower polling current in several applications.

The integration of remote keyless entry (RKE), passive entry and go (PEG) and tire pressure monitoring systems (TPM) into one module is simplified since completely different protocols can be supported and a low polling current is achieved. It is even possible using different receive RF bands for different applications by using the two LNA inputs. For example a TPM receiver can be realized at 433.92MHz while a PEG system uses the 868MHz ISM band with multi channel bidirectional communication.

3.2.2 RX Digital Signal Processing (Rx DSP)

The Rx DSP block performs the digital signal processing, decoding and checking of the Rx samples from the ADC. It delivers the raw data at the TRPA/B pins, the decoded data at the TMDO output and the buffered data bytes (Rx byte A/B) from the Rx buffer. It also provides auxiliary information about the signal like the received signal strength indication (RSSI) and the frequency offset of the received signal versus the selected center frequency (RXFOA/B).

Figure 3-2. Rx DSP Overview



The channel filter determines the receiver bandwidth. Its output is used for both receiving paths A and B. Therefore it has to be configured to be suitable for both. The receiving paths A and B are identical and consist of an ASK/FSK demodulator with attached signal checks, a frame synchronizer supporting pattern based search for the telegram start and a 1 byte hardware buffer for received data.

The receiver architecture with parallel receiving paths A and B allows for a simultaneous search for two different transmitters. The simultaneous search is supported only when the flexible telegram support is enabled (see EEPROM description).

E.g. Path A can be configured for an ASK telegram with high data rate and path B can be configured for an FSK telegram with low data rate. During PollingMode both settings are applied and the check occurs simultaneously. This results in a shorter active time during polling.

3.3 Transmit Path

3.3.1 Overview

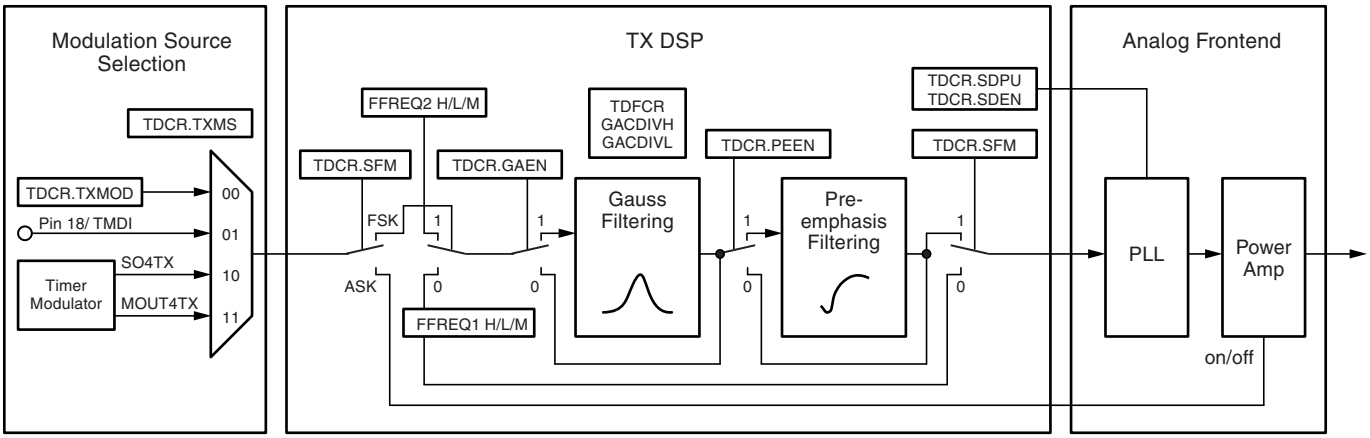
The Atmel® ATA5830 integrates a transmitter that is capable of sending data with various options:

- Frequency bands 310MHz – 318MHz, 418MHz – 477MHz, 836MHz – 928MHz
- Data rates up to 80Kbit/s Manchester or 160kSym/s NRZ in transparent mode
- ASK or FSK modulation
- Transparent or buffered mode
- Gauss-shaping digital filter

This section describes the hardware blocks that are integrated to perform the transmit functionality.

Figure 3-3 shows a block diagram of the transmit data path.

Figure 3-3. Transmit Data Path



The transmission data source can be selected from a register bit, a transparent input pin 18 (TMDI) and an internal 32 byte buffer.

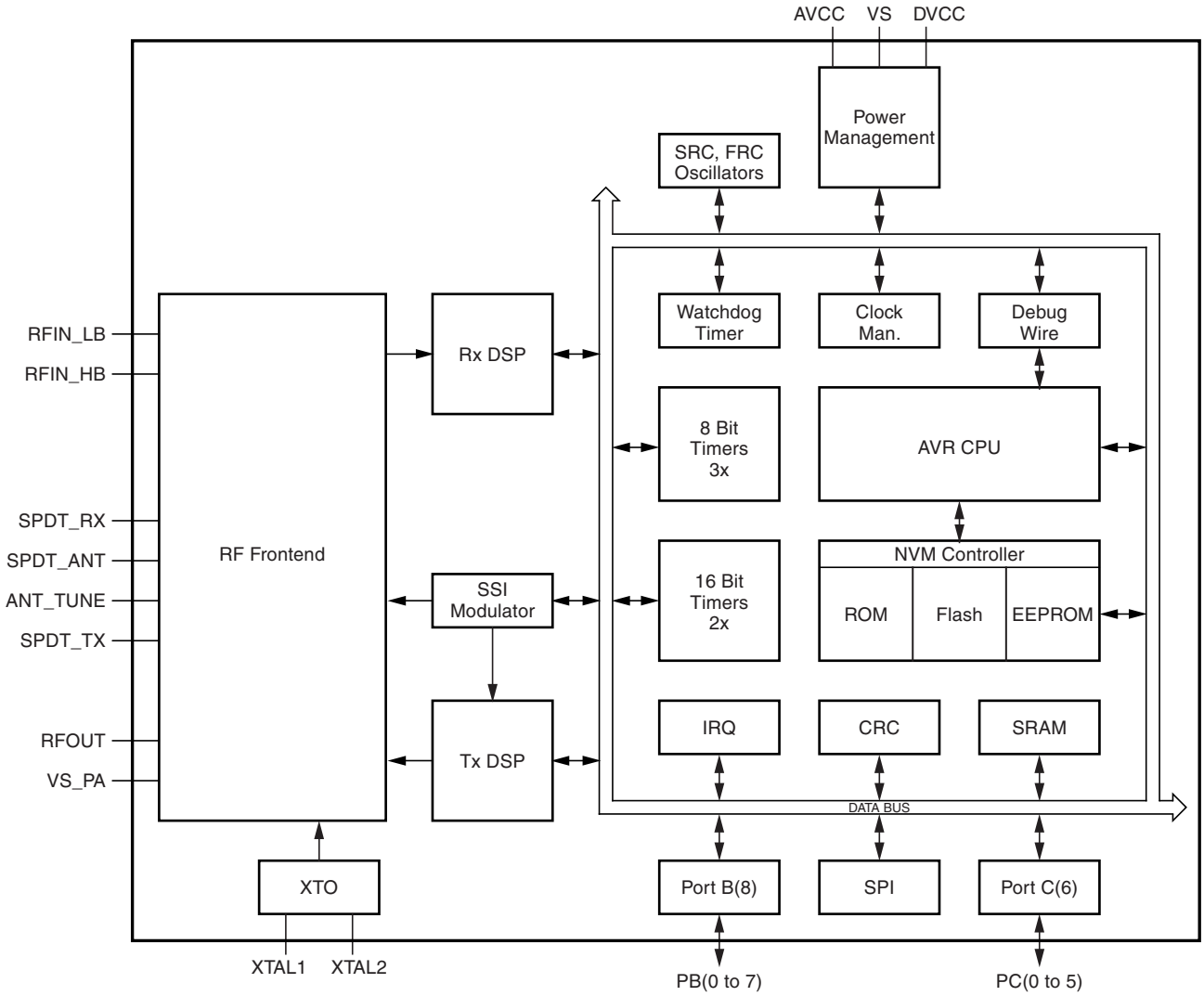
If ASK/OOK modulation is selected the data stream is used to directly switch on and off the power amplifier. The transmitted carrier frequency is set by the frequency synthesizer PLL.

If FSK modulation is selected the data stream is used to switch between two frequencies that are generated by the frequency synthesizer PLL. The power amplifier is constantly on. To reduce the occupied bandwidth a digital gauss filtering can be enabled. For data rates above 20kHz Manchester or 40kHz NRZ-coding a digital pre-emphasis filter has to be enabled to compensate for the PLL loop filter.

3.4 AVR Controller

3.4.1 CPU Core

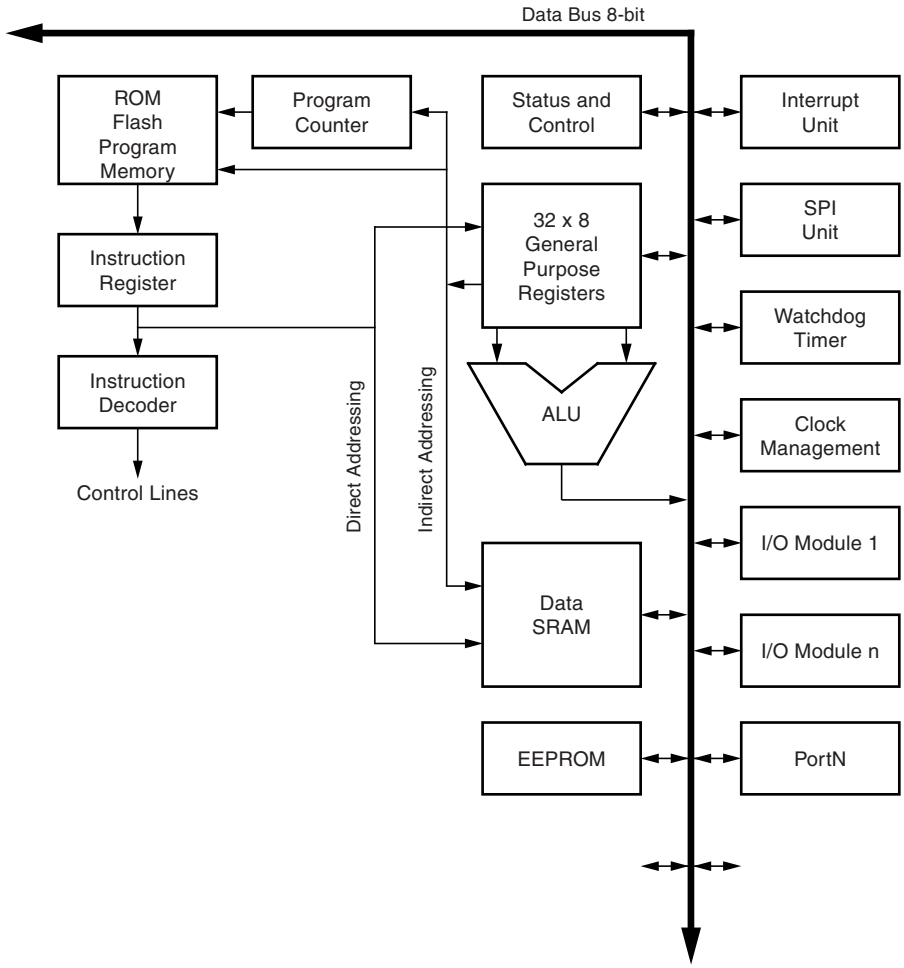
Figure 3-4. CPU Core Overview



3.4.1.1 *Architectural Overview*

This section discusses the AVR® core architecture in general. The main function of the CPU core is to ensure correct program execution. Therefore it must be able to access memories, perform calculations, control peripherals, and handle interrupts.

Figure 3-5. Architectural Overview



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In- System Reprogrammable Flash memory.

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR® instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

Program memory space is divided in two sections, the Boot Program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM (Store Program Memory) instruction that writes into the Application Flash memory section must reside in the Boot Program section.

During interrupts and subroutine calls, the return address of the Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the Stack Pointer (SP) in the Reset routine (before subroutines or interrupts are executed). The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional Global Interrupt Enable bit in the Status Register. All interrupts have a separate Interrupt Vector in the Interrupt Vector table. The interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register File, 0x20 - 0x5F. In addition, the circuit has Extended I/O space from 0x60 - 0xFF and SRAM where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

3.5 Power Management

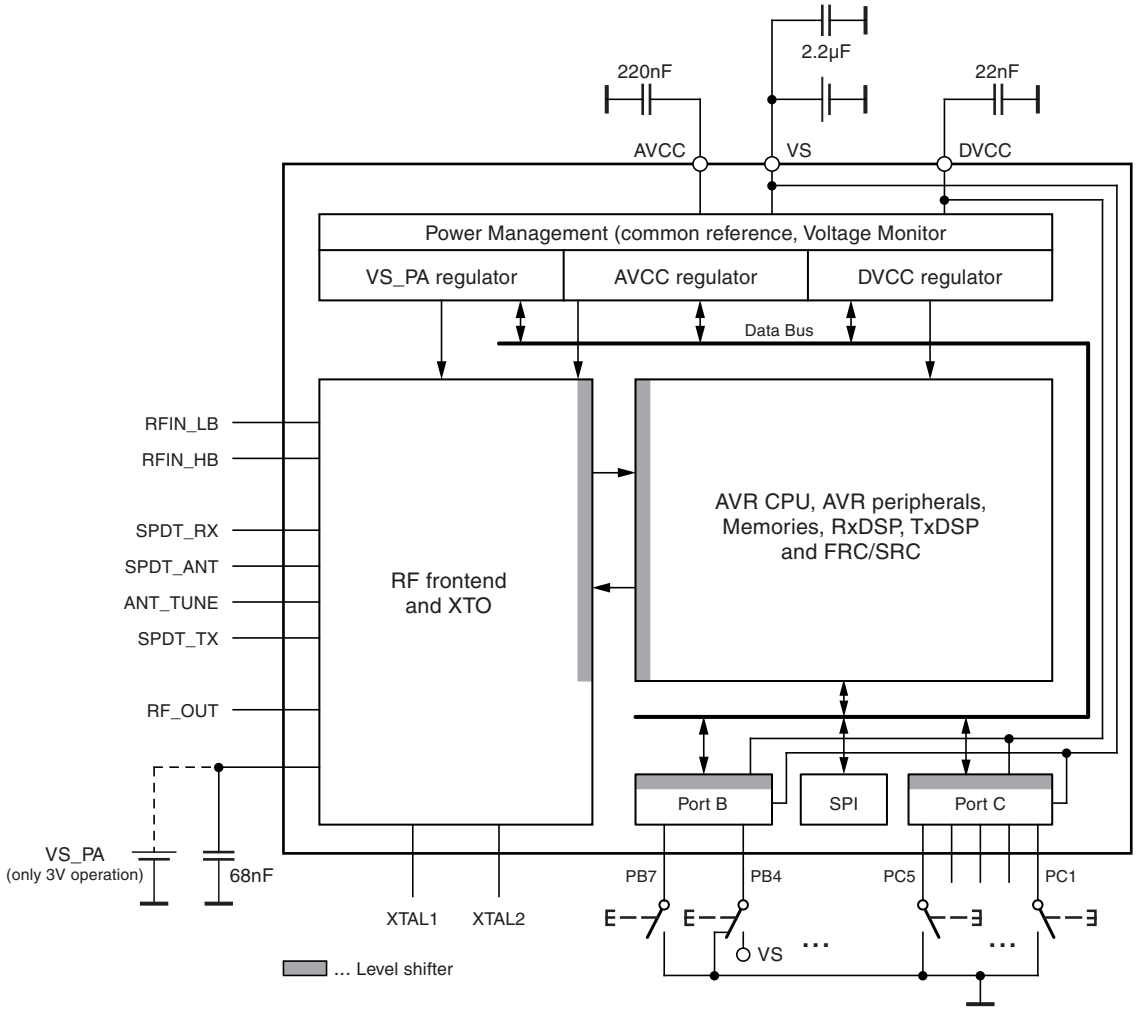
3.5.1 Overview

The IC has four power domains:

- VS – The unregulated battery voltage input.
- DVCC – The internally regulated digital supply voltage. Typical value is 1.35V.
- AVCC – The internally regulated RF frontend and XTO supply. Typical value is 1.85V.
- VS_PA – The power amplifier supply has two application modes depending on the battery voltage (VS) range:
  - Connected externally to the battery in 3V applications.
  - Generated by an internal regulator in 5V applications.

The AT5830 can be operated from V_S = 1.9V to 3.6V (3V application) and from V_S= 4.5V to 5.5V (5V application). For TX output powers above 10dBm applied in high band frequency ranges 836MHz to 928MHz, the minimum battery voltage is limited to 2.1V.

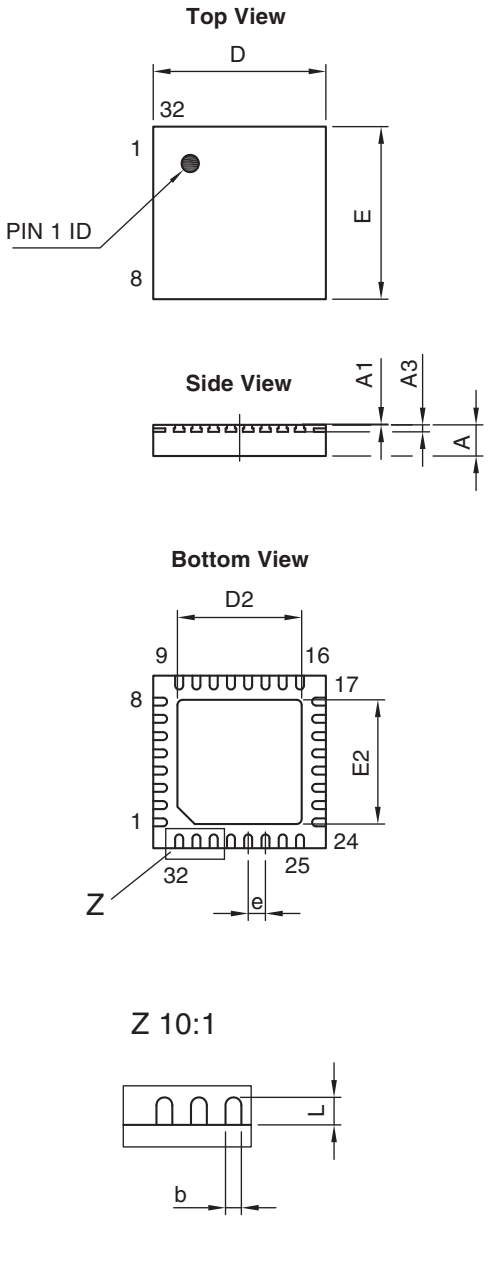
Figure 3-1. Power Supply Management



4 Ordering Information

Extended Type Number	Package	Remarks
ATA5830-PNQW	QFN32	5mm × 5mm PB free
ATA5830N-PNQW	QFN32	5mm × 5mm PB free

5 Package Information



technical drawings according to DIN specifications

Dimensions in mm

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	MIN	NOM	MAX	NOTE
A	0.8	0.9	1	
A1	0.0	0.02	0.05	
A3	0.15	0.2	0.25	
D	4.9	5	5.1	
D2	3.45	3.6	3.75	
E	4.9	5	5.1	
E2	3.45	3.6	3.75	
L	0.3	0.4	0.5	
b	0.16	0.23	0.3	
e		0.5 BSC		

10/12/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	Package: VQFN_5x5_32L Exposed pad 3.6x3.6	6.543-5124.01-4	2

6. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9208DS-RKE-07/11	• Set datasheet from Preliminary to standard
9208CS-RKE-07/11	• Document completely redesigned
9208BS-RKE-01/11	• Section 5 “Ordering Information” on page 29 changed

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