ATA5575M2

Read/Write LF RFID IDIC 100kHz to 150kHz

DATASHEET

Features

- Contactless power supply
- Contactless read/write data transmission
- Radio frequency f_{RF} from 100kHz to 150kHz
- 128-bit EEPROM user memory: 16 Bytes (8 Bits each)
- 8-bit configuration memory
- High Q-antenna tolerance due to built-in options
- Applications
  - Animal ID, waste management, industrial identification
    - ISO/IEC 11784/785 compatibility
    - FDX-A
    - FDX-B
- On-chip trimmed antenna capacitor
  - 330pF ±3%
  - 250pF ±3%
- Mega pads 200µm x 400µm
- Mega pads 200µm x 400µm with 25µm gold bumps for direct coil bonding
- Other options:
  - Direct access mode
- OTP functionality

1. Description

The Atmel® ATA5575M2 is a contactless read/write identification IC (IDIC®) for applications in the 100-kHz to 150-kHz frequency band. A single coil connected to the chip serves as the IC's power supply and bi-directional communication interface. This antenna coil together with the chip form a transponder or tag.

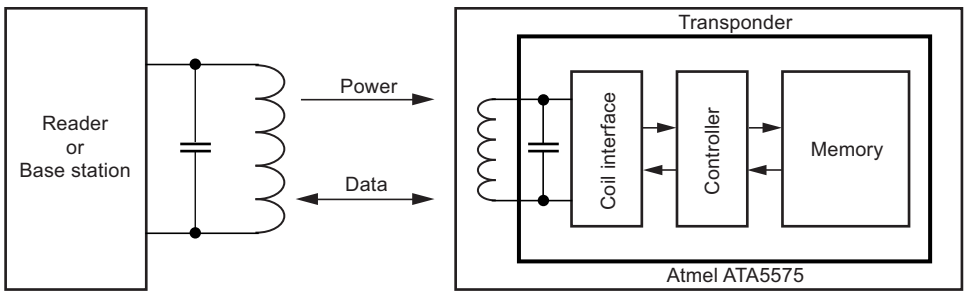
The on-chip 128-bit User EEPROM (16 bytes with 8 bits each) can be read and written byte-wise from a base station (reader). Data is transmitted from the IDIC (uplink) using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1 and Coil 2. The IC receives and decodes serial base station commands (downlink), which are encoded as 100% amplitude-modulated (OOK) pulse-interval-encoded bit streams.

The Atmel ATA5575M2 is an EEPROM-based circuit. It is optimized for maximum read range. Programming is also possible but the write range is limited.

The typical animal ID application conforming to ISO11784/85 is read-only and operates at 134.2kHz. The Atmel ATA5575M2 thus has to be locked after programming the animal-specific code.

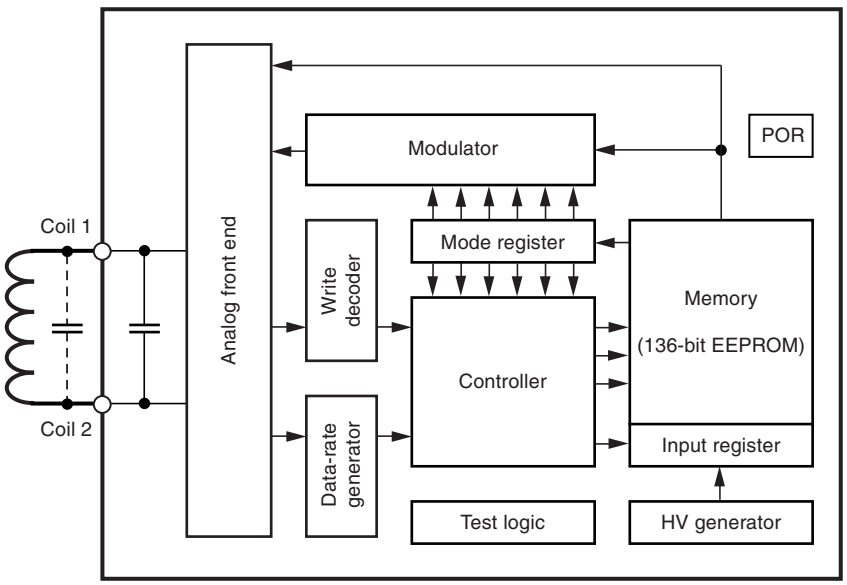
2. System Block Diagram

Figure 2-1. RFID System Using Atmel ATA5575M2 Tag



3. Atmel ATA5575M2 - Functional Blocks

Figure 3-1. Block Diagram



4. Analog Front End (AFE)

The AFE includes all circuits which are connected directly to the coil terminals. The AFE generates the IC power supply and handles bi-directional data communication with the reader. The AFE consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil 1 and Coil 2 for data transmission from tag to the reader
- Field-gap detector for data transmission from the base station to the tag
- ESD protection circuitry

4.1 Data Rate Generator

The data rate of the Atmel ATA5575M2 is programmable to operate at RF/50 (FDX-A mode) and RF/32 (FDX-B mode).

4.2 Write Decoder

The write decoder detects the write gaps and verifies the validity of the data stream according to the Atmel® downlink protocol (pulse-interval encoding).

4.3 HV Generator

This on-chip charge pump circuit generates the high voltage required for programming the EEPROM.

4.4 DC Supply

Power is supplied externally to the IDIC via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

4.5 Power-On Reset (POR)

The power-on reset circuit blocks the voltage supply to the IDIC until an acceptable voltage threshold has been reached. This, in turn, triggers the default initialization delay sequence. During this configuration period of 98 field clocks, the ATA5575M2 is initialized with the configuration data stored in EEPROM byte 16.

4.6 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

4.7 Controller

The control logic module executes the following functions:

- Load mode register with configuration data from EEPROM byte 16 after power-on and during reading
- Controls each EEPROM memory read/write access and handles data protection
- Handle downlink command decoding, detecting protocol violations and error conditions

4.8 Mode Register

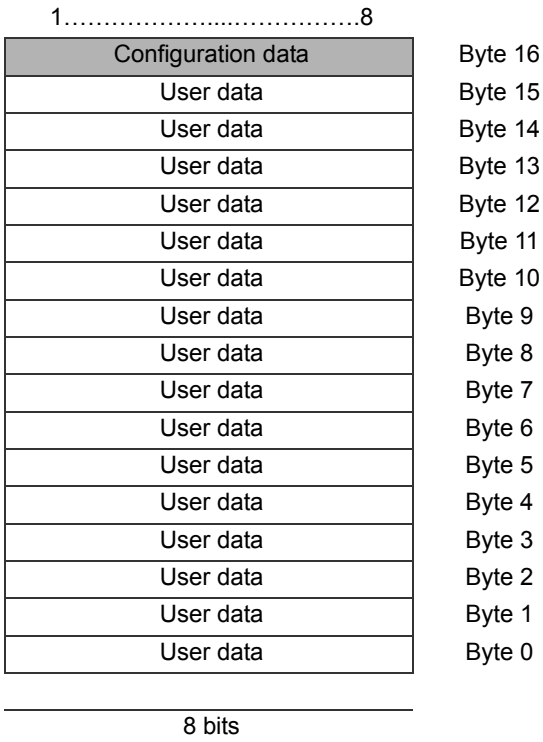
The mode register maintains a readable shadow copy of the configuration data held in byte 16 of the EEPROM. It is continually refreshed during read mode and (re-)loaded after every POR event or reset command. Depending on the version, upon leaving the Atmel® factory site, the configuration data is pre-programmed according to Table 10-1 on page 18 and Table 10-4 on page 20.

4.9 Modulator

The modulator encodes the serialized EEPROM data for transmission to a tag reader or base station. Two types of encoding are implemented: Differential Biphase and FSK.

4.10 Memory

Figure 4-1. Memory Map



The memory is a 136-bit EEPROM arranged in 17 bytes of 8 bits each. Programming takes place on a byte basis meaning a complete byte is programmed with a single command.

Byte 16 contains the mode/configuration data which is otherwise not transmitted during regular-read operations.

A special combination of bits in byte 16 (see Table 5-1 on page 5) locks the whole memory. Once locked, the memory (including byte 16 itself) is not reprogrammable through the RF field again.

5. Operating the Atmel ATA5575M2

5.1 Configuration

The Atmel® ATA5575M2 is mainly designed for ISO11784/11785 applications. It supports FDX-A and FDX-B mode (see also Figure 7-1 on page 14 for the structure of a FDX-B telegram typically used for animal ID applications). The configuration register, byte 16, enables the customer to configure the chip according to the individual application.

In delivery state the default configuration is memory reprogrammable, read user data in diff. biphase RF/32 and ID length 128 bit which leads to the byte value '00001001b'.

Table 5-1. Atmel ATA5575M2: Byte 16 Configuration Register Mapping

1	2	3	4	5	6	7	8
					0		

ID Length
- 0 64 bits (96 bits for FSK2 RF/50 coding [2])
- 1 128 bits [1]

Modulation
- 0 Differential bi-phase RF/32 [1]
- 1 FSK2 RF/50 [2]

Fixed '0'

Lock-bits

0	0	0	0	1	Memory reprogrammable
0	1	1	0	1	Memory locked
	- otherwise -				unassigned

Bit 6 must always be at '0', otherwise a malfunction will appear

Notes: 1. Setting for ISO 11785 FDX-B
2. Setting for ISO 11785 FDX-A

5.1.1 Lock-bits

The lock bits of the Configuration register are the bits 1 to 5 of the configuration byte and are able to prevent the whole memory of the Atmel ATA5575M2 from reprogramming.

As long as the lock bits are set to '00000b' the memory is alterable and the device can be programmed by the customer. In this case the Atmel ATA5575M2 sends out dummy data (all digits set to '0' in the programmed modulation scheme; see Section 5.3.3 “Dummy Data” on page 7) after Reset.

If the lock bits are set to '00001b' the memory is still alterable but in difference to the first option the Atmel ATA5575M2 sends out the programmed user data in the modulation scheme defined with bit 7.

By setting the lock bits to '01101b' the whole memory is locked and cannot be altered. After Reset the Atmel ATA5575M2 enters regular-read mode and sends out the programmed user data in the configured way.

All other combinations of bit 1 - bit 5 are not defined and may lead to malfunction of the IC.

5.1.2 Modulation

The modulator consists of data encoders for the following types of modulation.

Table 5-2. Atmel ATA5575M2: Types of Modulation

Symbol	Direct Data Output Encoding		
FSK2 RF/50	FSK/10 – FSK/8	0 = RF/10	1 = RF/8
Differential bi-phase	Transition at each bit start 0 creates an additional mid-bit change		

5.1.3 ID Length

The Atmel® ATA5575M2 offers settings for different ID lengths. If bit 8 of byte 16 is set to '1', the ID length is 128 bits. Depending on the modulation scheme, resetting bit 8 of byte 16 to '0' leads either to the ID length of 64 bit with differential bi-phase coding or to the ID length of 96 bit with FSK2 coding respectively.

5.2 Animal ID and Traceability

During Atmel's production process the Atmel ATA5575M2 will be pre-configuered in the ISO11784/11785 FDX-B mode and a unique ID (UID) will be stored in the user memory. The unique ID consists of Atmel's production information like lot number, wafer number, and die-on-wafer number. With these data each chip can be traced and concurrently each chip has its own unique ID for identification purposes(1).

For ISO11784/11785 FDX-B telegrams please refer to Section 7. "Examples for Programming the ATA5575M2" on page 14. Section 10.2 "ATA5575M2 Configuration on Delivery" on page 18 describes how the unique ID is formed based on Atmel production information.

Note: 1. Please note that this traceability data is only for production control and does not conform with any ISO, national or other regulations.

5.3 Tag-to-reader Communication (Uplink)

Immediately after entering the reader field, generating the internal supply voltage and the analog POR, in the delivery state the tag cycles its data stored in EEPROM by load modulation according to the configuration setting. This resistive load modulation can be detected at the reader device.

5.3.1 Regular-read Mode

In regular-read mode data from the memory is transmitted in series, starting with byte 0, bit 1, up to the last byte, bit 8. Last byte is defined in bit 8 of byte 16, ID Length. When the last bit of the last byte (defined by ID length) has been read, data transmission restarts with byte 0, bit 1.

The device enters regular-read mode in delivery state (lock bits set to '00001b' or set to '01101b'; please refer to Section 5.1.1 "Lock-bits" on page 5).

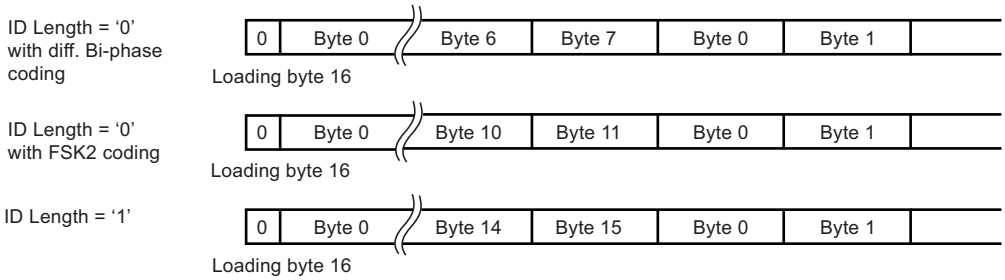
Last byte is 15, when ID Length = 1 (128 bit).

For differential bi-phase modulation, the last byte is 7 when ID Length = 0 (64 bits) is chosen.

For FSK2 RF/50 modulation, the last byte is 11 when ID length = 0 (96 bits) is chosen.

Every time the Atmel ATA5575M2 enters regular or byte read mode, the first bit transmitted is a logical '0'. The data stream starts with bit 1 of byte 0 or bit 1 of the addressed byte.

Figure 5-1. Examples of Different ID Length Settings



5.3.2 Byte-read Mode

With the direct access command, only the addressed byte is read repetitively. This mode is called byte-read mode. Direct access is entered by transmitting the opcode ('10'), a single 0 bit, and the requested 5-bit byte address.

5.3.3 Dummy Data

The dummy data are a predefined bit sequence of all bits set to value '0'. This sequence is read out instead of the data stored in the user memory if the lock bits are set to '00000b'.

5.4 Reader-to-tag Communication (Downlink)

Data is transmitted to the tag by interrupting the RF field with short field gaps (on-off keying) according to the Atmel® ATA5577 fixed-bit-length protocol (downlink mode). The duration of these field gaps is, for example, 100µs. The time between two gaps encodes the 0/1 information to be transmitted (pulse interval encoding). The time between two gaps is nominally 25 field clocks for a 0 and 58 field clocks for a 1. When there is no gap for more than 64 field clocks after a previous gap, the Atmel ATA5575M2 exits the downlink mode. The tag starts with the command execution if the correct number of bits were received. If an error condition occurs, the Atmel ATA5575M2 does not continue command execution and enters read mode depending on the setting of the lock bits.

The initial gap is referred to as the start gap. This triggers reader-to-tag communication. The start gap may need to be longer than subsequent gaps - so-called write gaps - in order to be detected reliably.

A start gap is accepted at any time after the mode register has been loaded (≥ 1ms).

Figure 5-2. Start of Reader-to-tag Communication (Downlink)

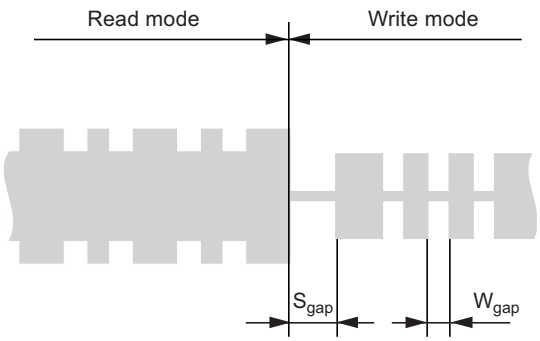


Table 5-3. Downlink Data Decoding Scheme

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Start gap		S_{gap}	8	15	50	T_C
Write gap		W_{gap}	8	10	20	T_C
Write data coding (gap separation)	0 data	d_0	18	25	33	T_C
	1 data	d_1	50	58	65	T_C

Note: All absolute times are given under the assumption $T_C = 1/f_C = 8\mu s$ ($f_C = 125kHz$)

All absolute times assume $T_C = 1/f_C = 8\mu s$ ($f_C = 125kHz$)

5.4.1 Downlink Data Protocol

The Atmel® ATA5575M2 expects to receive a dual bit opcode as a part of a reader command sequence. There are three valid opcodes and overall five different commands (please refer to Figure 5-4 on page 9):

- The RESET opcode '00' starts an initialization cycle
- A single '10' opcode (Read ID) leads to reading the ID out of the EEPROM memory. This is suitable to check the programmed user data if the memory is not locked already. The opcode '10' precedes all downlink operations for writing data into the EEPROM
- The opcode '11' reads the upper bytes when ID length (bit 8 of byte 16) is set to '0'
  If ID length is set to '1' opcode '11' is the same than opcode '10'
- The *Write Byte* requires the opcode '10', a '0' bit, 8 data bits and the 5-bit address (16 bits total)
- For *Direct access*, the opcode '10', a '0' bit and a 5-bit address (8 bits total), is required

Note: The data bits are read in the same order as written.

Figure 5-3. Complete Write Sequence

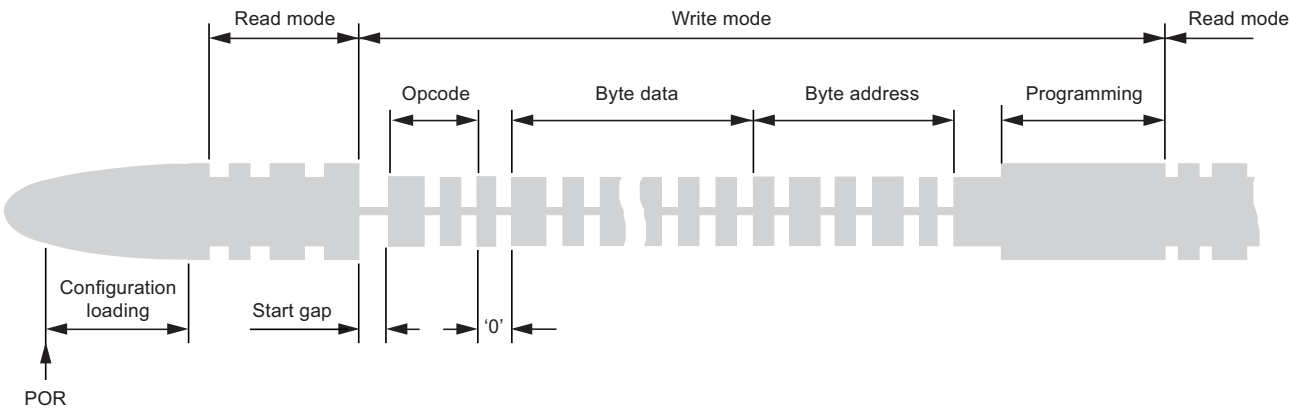
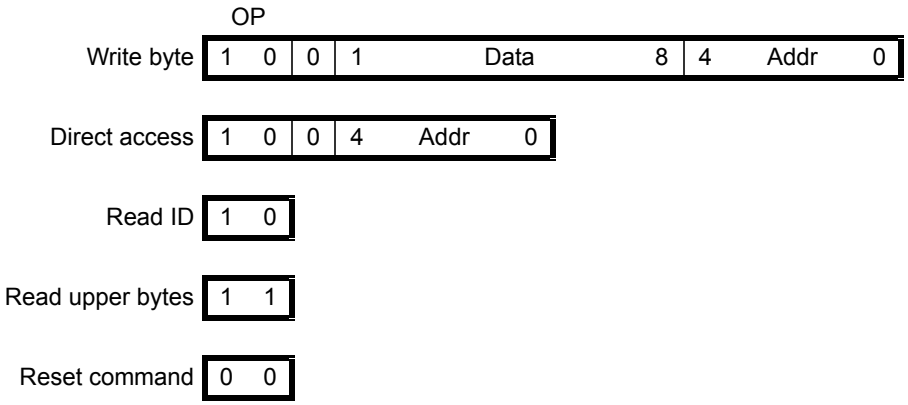


Figure 5-4. ATA5575M2 Command Formats



5.5 Programming

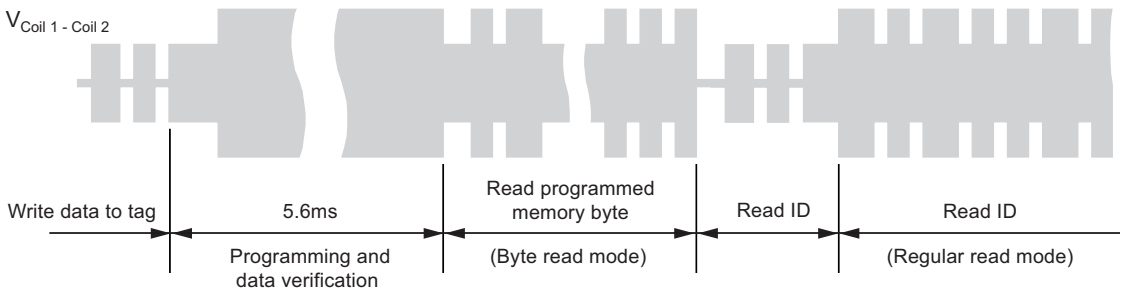
When all necessary information has been received by the ATA5575M2, programming may proceed. There is a clock delay between the end of the writing sequence and the start of programming.

Typical programming time is 5.6ms. This cycle includes a data verification read to grant secure and correct programming. After programming is successfully executed, the ATA5575M2 enters byte-read mode, transmitting the byte just programmed.

If the command sequence is validated, the new data is programmed into the EEPROM memory.

Each programming cycle consists of four consecutive steps: erase byte, erase verification (data = 0), programming, programming verification (corresponding data bits = 1).

Figure 5-5. Coil Voltage after Programming a Byte



6. Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types which result into two different actions.

6.1 Errors During Command Sequence

The following detectable errors could occur when sending a command sequence to the Atmel® ATA5575M2:

- The wrong number of field clocks between two gaps (i.e., not a valid 1 or 0 pulse stream)
- The number of bits received in the command sequence is incorrect

Table 6-1. Bit Counts of Command Sequences

Command	Number of Bits
Write byte	16
Direct access	8
Read ID	2
Read upper bytes	2
Reset command	2

6.2 Errors Before/During Programming of EEPROM

If the command sequence was received successfully, the following errors may still prevent programming:

- The lock bits of the memory are already set
- If the memory is locked, programming is not possible. The Atmel ATA5575M2 enters byte-read mode, continuously transmitting the currently addressed byte.
- If a data verification error is detected after programming of an executed data byte, the tag will stop modulation (modulation defeat) until a new command is transmitted.

Figure 6-1. Atmel ATA5575M2 Functional Diagram

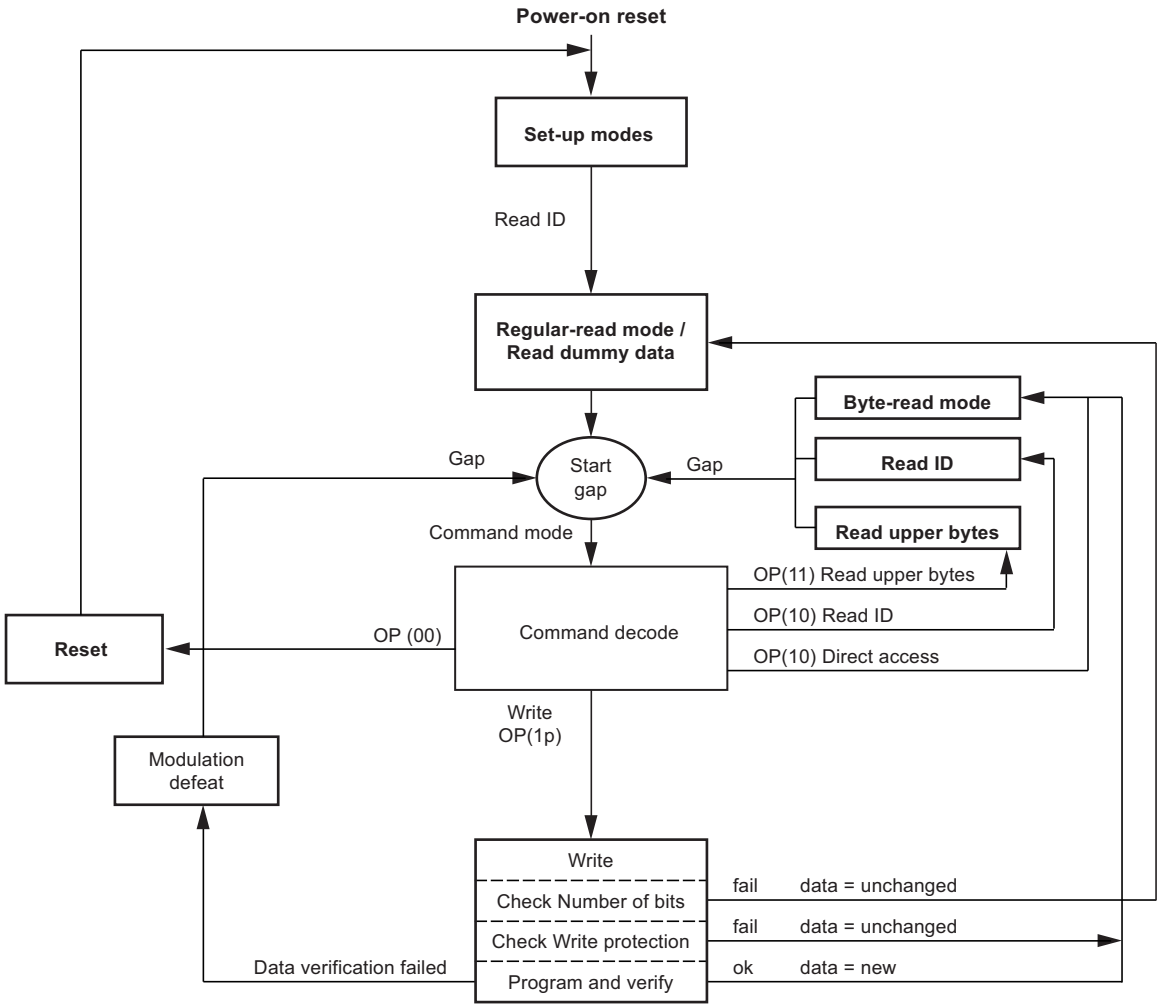


Figure 6-2. Example of Differential Bi-phase Coding with Data Rate RF/32

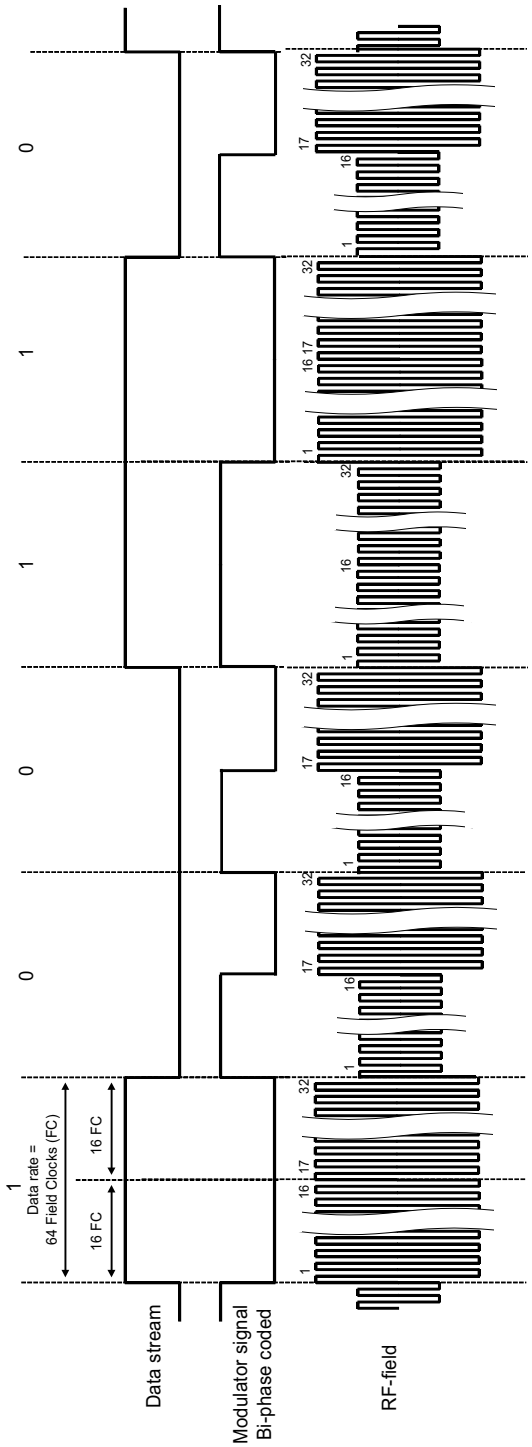
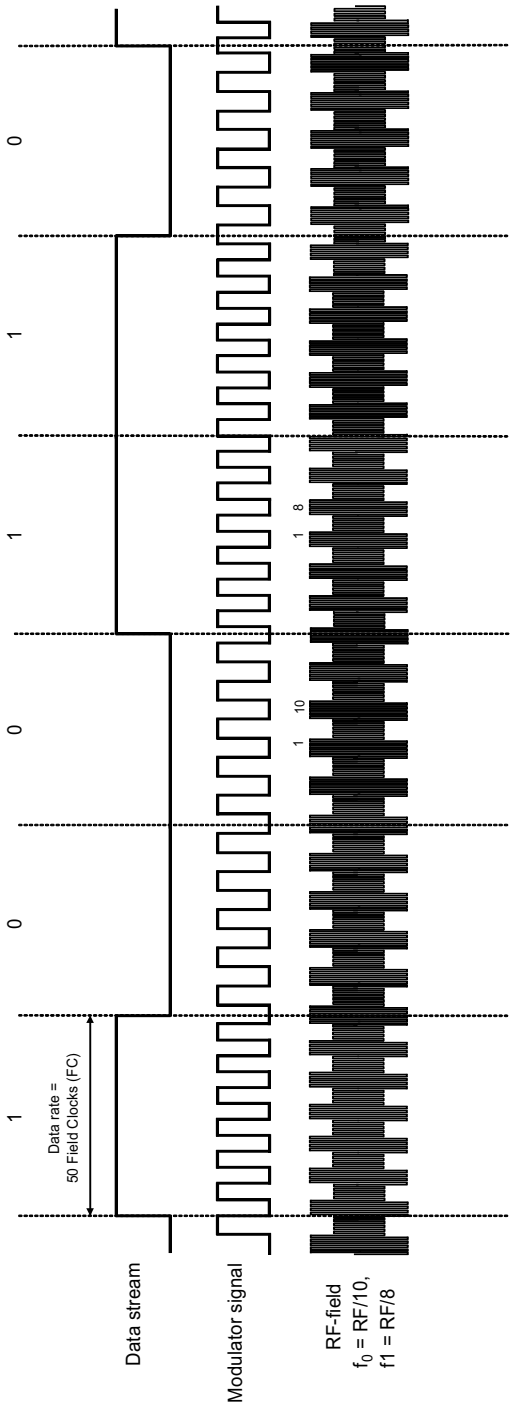


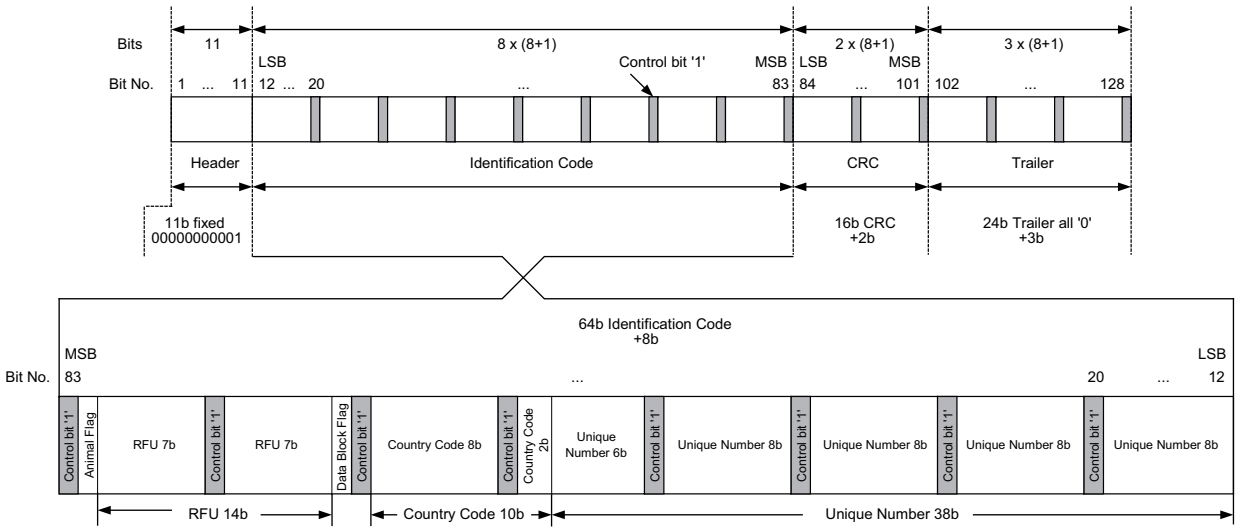
Figure 6-3. Example of FSK2 Coding with Data Rate RF/50, Subcarrier f_0 = RF/10, f_1 = RF/8



7. Examples for Programming the ATA5575M2

Animal ID is a typical application with ISO11784/11785. The following describes the data structure of an FDX-B telegram and a flow for programming ATA5575M2 using sample data.

Figure 7-1. ATA5575M2: Structure of the ISO 11785 FDX-B Telegram



Notes:

- Except for the header, every 8 bits are followed by one control bit (1), to prevent the header from recurring.
- All data is transmitted LSB first.
- Country codes are defined in ISO 3166
- The bits reserved for future use (RFU) are all set to 0.
- If the data block flag is not set, the trailer bits are all set to 0.
- CRC is performed on the 64-bit identification code without the control bits. The generator polynomial is $P(x) = x^{16} + x^{12} + x^5 + 1$. Reverse CRC-CCITT (0x 8 408) is used. The data stream is LSB first.

Example data for programming Atmel ATA5575M2 in FDX-B mode:

- Animal flag: 1
- RFU: 0
- Data block flag: 0
- Country code: 999
- Unique number: 123456789
- Trailer: 0

Table 7-1. Atmel ATA5575M2: Programming with FDX-B Example Data

Base Station	Atmel ATA5575M2
Field on for t = 5ms	POR and regular-read mode
Command 00	Reset
Command 10 0 0000 1001 10000	Programming byte 16 with ‘09h’ (FDX-B mode, memory reprogrammable)
Command 10 0 0000 0000 00000	Programming byte 0 with ‘00h’
Command 10 0 0011 0101 00001	Programming byte 1 with ‘35h’
Command 10 0 0001 1011 00010	Programming byte 2 with ‘1Bh’
Command 10 0 0011 1110 00011	Programming byte 3 with ‘3Eh’
Command 10 0 1101 0111 00100	Programming byte 4 with ‘D7h’
Command 10 0 1000 0010 00101	Programming byte 5 with ‘82h’
Command 10 0 0000 0111 00110	Programming byte 6 with ‘07h’
Command 10 0 1001 1111 00111	Programming byte 7 with ‘9Fh’
Command 10 0 1000 0000 01000	Programming byte 8 with ‘80h’
Command 10 0 0100 0000 01001	Programming byte 9 with ‘40h’
Command 10 0 0110 1110 01010	Programming byte 10 with ‘6Eh’
Command 10 0 1001 1000 01011	Programming byte 11 with ‘98h’
Command 10 0 1010 1000 01100	Programming byte 12 with ‘A8h’
Command 10 0 0000 0100 01101	Programming byte 13 with ‘04h’
Command 10 0 0000 0010 01110	Programming byte 14 with ‘02h’
Command 10 0 0000 0001 01111	Programming byte 15 with ‘01h’
Command 10	Read ID
Field on for t = 50ms Read and verify FDX-B data	Send FDX-B data
Command 10 0 0110 1001 10000	Programming byte 16 with ‘69h’ (FDX-B mode, memory locked)
Command 00	Reset
Field on for t = 50ms Read and verify FDX-B data	Send FDX-B data

8. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Maximum DC current into Coil1/Coil2	I_{coil}	20	mA
Maximum AC current into Coil1/Coil2 f = 125kHz	$I_{coil\ p}$	20	mA
Power dissipation (dice) (free-air condition, time of application: 1s)	P_{tot}	100	mW
Electrostatic discharge maximum to ANSI/ESD-STM5.1-2001 standard (HBM)	V_{max}	2000	V
Operating ambient temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +150	°C

Note: For data retention please refer to Section 9. “Electrical Characteristics” on page 16.

9. Electrical Characteristics

T_{amb} = +25°C; f_{coil} = 125kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF frequency range		f_{RF}	100	125	150	kHz	
2.1	Supply current (without current consumed by the external LC tank circuit)	T_{amb} = 25°C (1)	I_{DD}		1.5	3	µA	T
2.2		Read – full temperature range			2	5	µA	Q
2.3		Programming – full temperature range			25		µA	Q
3.1	Coil voltage (AC supply)	Read mode and write command 2)	$V_{coil\ pp}$	6		V_{clamp}	V	Q
3.2		Program EEPROM(2)		16		V_{clamp}	V	Q
4	Start-up time	$V_{coil\ pp}$ = 6V	$t_{startup}$		1.1		ms	Q
5.1	Clamp	3mA current into Coil1/2	V_{pp}	15	18	21	V	T
5.2		20mA current into Coil1/2	V_{pp}	17	20	24	V	T
6.1	Modulation parameters	3mA current into Coil1/2 and modulation ON	V_{pp}	2	3	4	V	T
6.2		20mA current into Coil1/2 and modulation ON	V_{pp}	4.5	5	8.5	V	T
6.3	Thermal stability of modulation parameter		V_p/T_{amb}		–1		mV/°C	Q

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil1/Coil2 is limited to 10mA.
3. Since the EEPROM performance is influenced by assembly processes, Atmel cannot confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. See Section 10. “Ordering Information” on page 18.

9. Electrical Characteristics (Continued)

T_{amb} = +25°C; f_{coil} = 125kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
7.1	Clock detection level	$V_{coil\ pp}$ = 8V	V_{clkdet}	400	550	750	mV	T
7.2	Gap detection level	$V_{coil\ pp}$ = 8V	$V_{gapdet\ med}$	400	550	750	mV	T
8	Programming time	From last command gap to re-enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
9	Endurance	Erase all/Write all(3)	n_{cycle}	100000			Cycles	Q
10.1	Data retention	Top = 55°C(3)	$t_{retention}$	10	20	50	Years	Q
10.2		Top = 150°C(3)	$t_{retention}$	96			hrs	T
10.3		Top = 250°C(3)	$t_{retention}$	24			hrs	Q
11.1	Resonance capacitor	Mask option(4) $V_{coil\ pp}$ = 1V	C_r	320	330	340	pF	T
11.2				242	250	258		

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil1/Coil2 is limited to 10mA.
3. Since the EEPROM performance is influenced by assembly processes, Atmel cannot confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. See Section 10. “Ordering Information” on page 18.

10. Ordering Information

ATA5575M2	ccc	-xxx	Package		Drawing
			DDB	6” sawn wafer on foil with ring, thickness 150µm (approx. 6mil)	Figure 11-1 on page 21
			DBB	6” sawn wafer on foil with ring and gold bumps 25µm, thickness 150µm (approx. 6mil)	Figure 11-2 on page 22
			DBQ	Die in blister tape with gold bumps 25µm, thickness 280µm	Figure 11-3 on page 23
		On-chip Capacity Value in pF			
		250	(planned)		
		330			

10.1 Available Order Codes

Atmel ATA5575M2330-DDB

Atmel ATA5575M2330-DBB

Atmel ATA5575M2330-DBQ

New order codes will be created by customer request if order quantities exceed 250k pieces.

10.2 ATA5575M2 Configuration on Delivery

On delivery Atmel’s production information is stored in EEPROM with the FDX-B data structure as described in Figure 7-1 on page 14.

Table 10-1. ATA5575M2: Configuration on Delivery

Byte	Address	Value	Comment
User data byte 0 to byte 15	0b 0 0000 to 0b 0 1111	Variable data	Unique ID within a FDX-B telegram
Configuration (byte 16)	0b 1 0000	0x 09	Send FDX-B telegram with user data byte 0 to byte 15

The user data contains Atmel’s lot and production information as described in Table 10-2. With 38 bits, 12 decimals in the range from 0 to 274 877 906 943 can be formed. The following Atmel production information is stored within these 12 decimal places.

Table 10-2. Atmel ATA5575M2: Meaning of the Digits of Unique Number in Delivery State

Decimal	11	10, 9	8	7	6	5, 4, 3, 2	1, 0
Denotation	Header	CID	ICR	Y	Q	NNNN	Wafer#
Range [dec]	1 (fixed)	1-99	0-9	0-9	1-4	0-9999	1-25
For example	1	04	0	9	1	0164	12

Notes:

- First decimal *Header* is always fixed at ‘1’
- CID denotes the chip ID and is set to ‘4’ for Atmel® ATA5575M2
- ICR stands for the revision and/or foundry version of the IC
- YQNNNN gives the Atmel lot information
  - Y: alphanumeric 0, …, 9
  - Q: Characters F, G, H and J - are transformed to 1, …, 4
  - NNNN: Alphanumeric consecutive number 0, …, 9999
- Wafer# describes a lot's wafer numbers; alphanumeric 1, …, 25

The *Unique Number* will then calculated to:
***Unique Number* = Header*10^{11} + CID*10^{9} + ICR*10^{8} + Y*10^{7} + Q*10^{6} + NNNN*10^{2} + Wafer#**
For the example given in Table 10-2 on page 18 the *Unique Number* is 104 091 016 412

With the 24 trailer bits 8 decimals in the range 0 to 16 777 216 can be established. The following Atmel production information is stored within these 8 decimal places.

Table 10-3. Atmel ATA5575M2: Meaning of the Digits of *Trailer* Bits in Delivery State

Decimal	7, 6, 5	4, 3, 2, 1, 0
Denotation	Header	Die-on-wafer no. (DW)
Range [dec]	111 (fixed)	0 to 99 999
For example	111	09 127

Notes:

- The first 3 decimals of the Header are always fixed: '111'
- Die on wafer (DW): Consecutive number of die on wafer: 1 to 99 999

The *Trailer* is then calculated to:
***Trailer* = Header*10^{5} + DW**
With the example given in Table 10-3 the *Trailer* is 11 109 127

10.2.1 ATA5575M2 Example for Memory Content on Delivery

The following describes an example of the memory content after Atmel®'s production.

- CID: 4
- ICR: '00b'
- Lot number: 9F0164
- Wafer number: 12
- Die on wafer: 9.127

$$\textit{Unique Number} = 1 \times 10^{11} + 4 \times 10^{9} + 0 \times 10^{8} + 9 \times 10^{7} + 1 \times 10^{6} + 0164 \times 10^{2} + 12 = 104\,091\,016\,412$$

$$\textit{Trailer} = 111 \times 10^{5} + 9{,}127 = 11\,109\,127$$

With the sample data above the FDX-B telegram fields are:

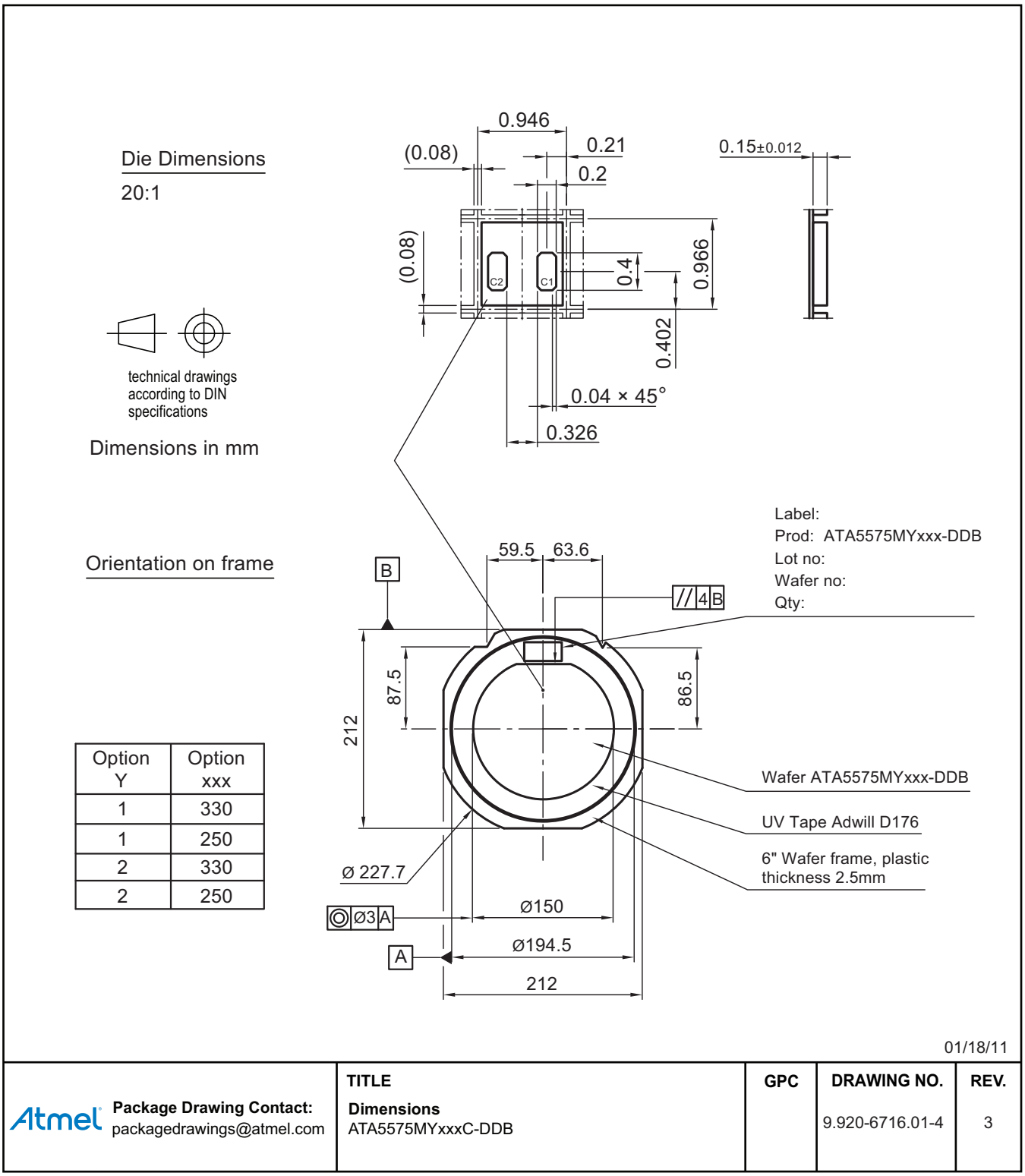
- Animal flag (1 bit) = ‘1b’ fixed
- RFU (14 bit) = ’00 0000 0000 0000b’ fixed
- Data block flag (1 bit) = ‘0b’ fixed
- Country code (10 bit) = 999 (= '11 1110 0111b') fixed
- Unique number (38 bit) = 104 091 016 412
- CRC (16 bit) = 39 505
- Trailer (24 bit) = 11 109 127

Table 10-4. ATA5575M2: Example of Memory Content on Delivery

Byte#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Meaning	Header	Header/ Unique Number	Unique number	Unique number	Unique number	Unique number	Unique number/ Country Code	Country code	Data Block Flag/ RFU	RFU	RFU/ Animal Flag/ CRC	CRC	CRC/ Trailer	Trailer	Trailer	Trailer	Confi-guration
Value [hex]	00	27	73	BB	94	F2	37	9F	80	40	71	55	9F	07	07	2B	09

11. Package Information

Figure 11-1. 6” Wafer on Foil with Ring



Option Y	Option xxx
1	330
1	250
2	330
2	250

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Dimensions** ATA5575MYxxxC-DDB		9.920-6716.01-4	3

Figure 11-2. 6” Wafer on Foil with Ring and Gold Bumps 25µm

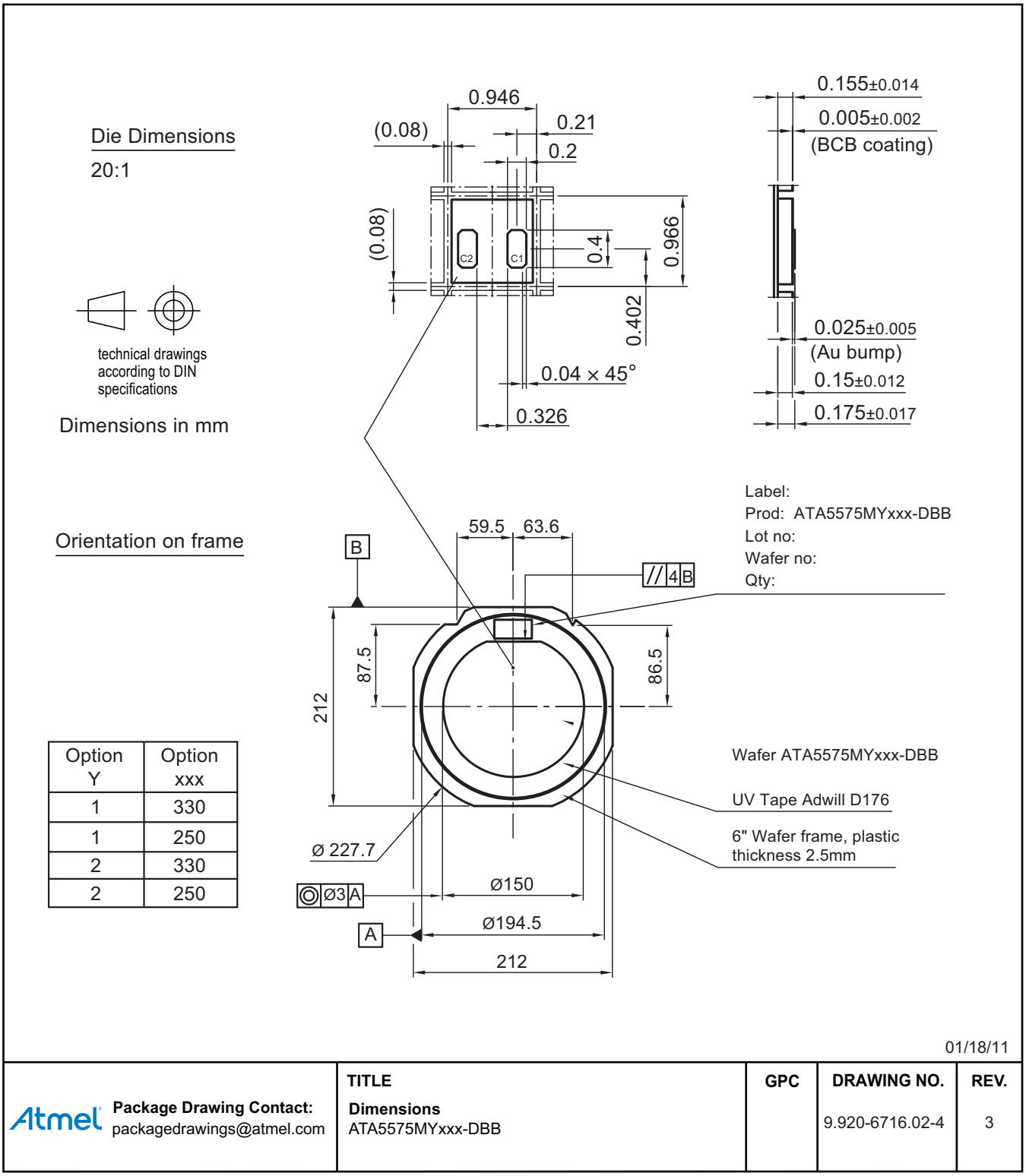
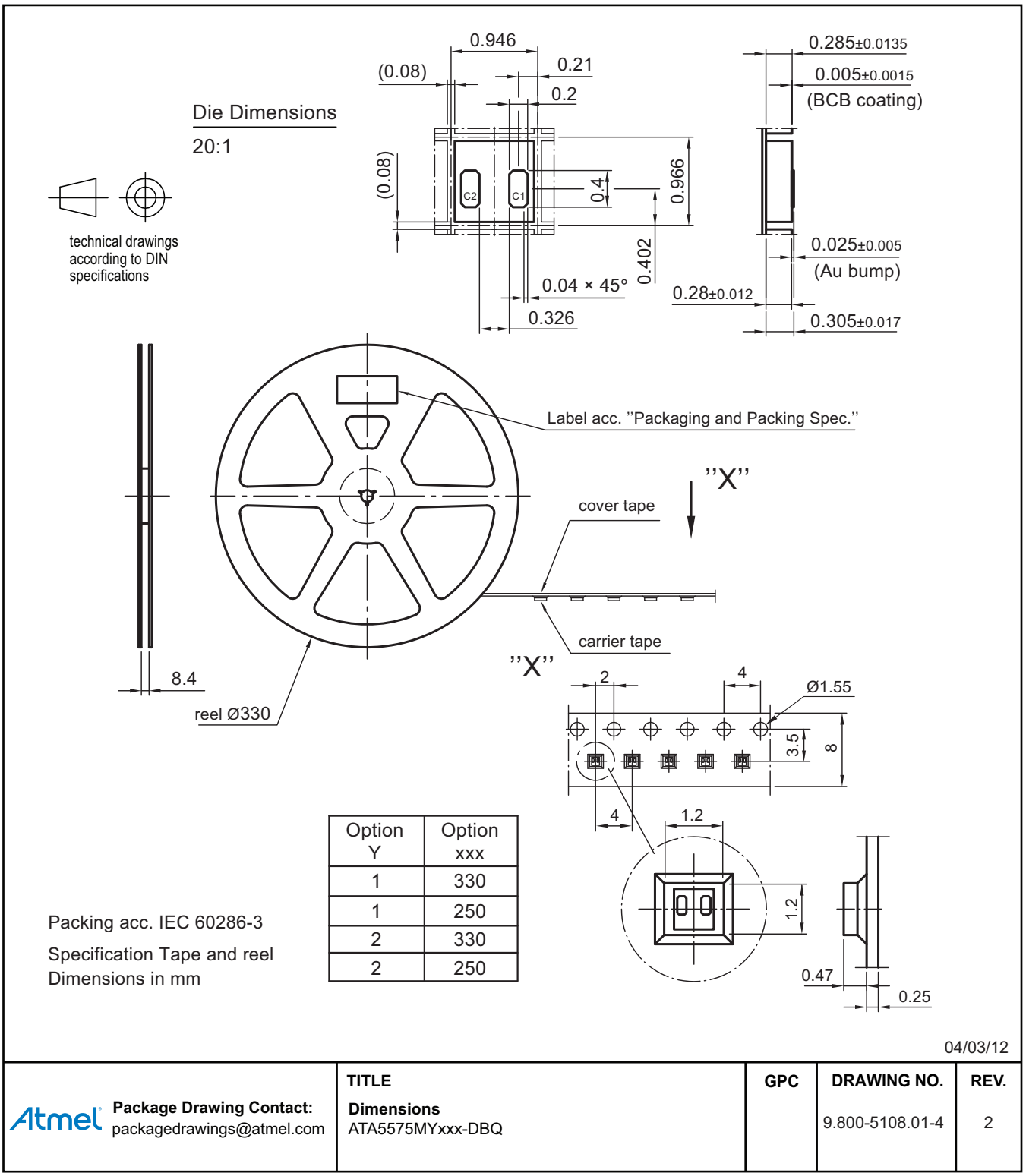


Figure 11-3. Die in Blister Tape with Gold Bumps 25µm



Option Y	Option xxx
1	330
1	250
2	330
2	250

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Dimensions** ATA5575MYxxx-DBQ		9.800-5108.01-4	2

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9217E-RFID-06/14	• Put datasheet in the latest template
9217D-RFID-04/13	• Section 10 “Ordering Information” on page 18 updated • Section 11 “Package Information” on page 23 updated
9217C-RFID-12/11	• Set datasheet from Preliminary to Standard
9217B-RFID-05/11	• Section 1 “Description” on page 1 changed • Section 4 “Analog Front End (AFE) on pages 3 to 4 changed • Section 5 “Operating the Atmel ATA5575M2” on pages 5 to 9 changed • Section 6.2 Errors Before/During Programming of EEPROM” on page 11 changed • Section 8 “Absolute Maximum Ratings” on page 16 changed • Section 9 “Electrical Characteristics” on page 16 changed • Section 10.2 “Atmel ATA5575M2 Configuration on Delivery” on pages 18 to 19 changed

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