Features

- Monolithic Field Programmable System Level Integrated Circuit (FPSLIC®)
  - AT40K SRAM-based FPGA with Embedded High-performance RISC AVR® Core, Extensive Data and Instruction SRAM and JTAG ICE
- 5,000 to 40,000 Gates of Patented SRAM-based AT40K FPGA with FreeRAM™
  - 2 - 18.4 Kbits of Distributed Single/Dual Port FPGA User SRAM
  - High-performance DSP Optimized FPGA Core Cell
  - Dynamically Reconfigurable In-System – FPGA Configuration Access Available On-chip from AVR Microcontroller Core to Support Cache Logic® Designs
  - Very Low Static and Dynamic Power Consumption – Ideal for Portable and Handheld Applications
- Patented AVR Enhanced RISC Architecture
  - 120+ Powerful Instructions – Most Single Clock Cycle Execution
  - High-performance Hardware Multiplier for DSP-based Systems
  - Approaching 1 MIPS per MHz Performance
  - C Code Optimized Architecture with 32 x 8 General-purpose Internal Registers
  - Low-power Idle, Power-save and Power-down Modes
  - 100 µA Standby and Typical 2-3 mA per MHz Active
- Up to 36 Kbytes of Dynamically Allocated Instruction and Data SRAM
  - Up to 16 Kbytes x 16 Internal 15 ns Instructions SRAM
  - Up to 16 Kbytes x 8 Internal 15 ns Data SRAM
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Extensive On-chip Debug Support
  - Limited Boundary-scan Capabilities According to the JTAG Standard (AVR Ports)
- AVR Fixed Peripherals
  - Industry-standard 2-wire Serial Interface
  - Two Programmable Serial UARTs
  - Two 8-bit Timer/Counters with Separate Prescaler and PWM
  - One 16-bit Timer/Counter with Separate Prescaler, Compare, Capture Modes and Dual 8-, 9- or 10-bit PWM
- Support for FPGA Custom Peripherals
  - AVR Peripheral Control – 16 Decoded AVR Address Lines Directly Accessible to FPGA
  - FPGA Macro Library of Custom Peripherals
- 16 FPGA Supplied Internal Interrupts to AVR
- Up to Four External Interrupts to AVR
- 8 Global FPGA Clocks
  - Two FPGA Clocks Driven from AVR Logic
  - FPGA Global Clock Access Available from FPGA Core
- Multiple Oscillator Circuits
  - Programmable Watchdog Timer with On-chip Oscillator
  - Oscillator to AVR Internal Clock Circuit
  - Software-selectable Clock Frequency
  - Oscillator to Timer/Counter for Real-time Clock
- V_{CC}: 3.0V - 3.6V
- 3.3V 33 MHz PCI-compliant FPGA I/O
  - 20 mA Sink/Source High-performance I/O Structures
  - All FPGA I/O Individually Programmable
- High-performance, Low-power 0.35µ CMOS Five-layer Metal Process
- State-of-the-art Integrated PC-based Software Suite including Co-verification
- 5V I/O Tolerant
- Green (Pb/Halide-free/ROHS compliant) Package Options Available

FPSLIC®

5K - 40K Gates of AT40K FPGA with 8-bit AVR® Microcontroller, up to 36K Bytes of SRAM and On-chip JTAG ICE

AT94KAL Series Field Programmable System Level Integrated Circuit

Summary

1138IS–FPSLI–1/08

Note: This is a summary document. A complete document is available on our web site at *www.atmel.com*.

1. Description

The AT94KAL Series FPSLIC family shown in Table 1-1 is a combination of the popular Atmel AT40K Series SRAM FPGAs and the high-performance Atmel AVR 8-bit RISC microcontroller with standard peripherals. Extensive data and instruction SRAM as well as device control and management logic are included on this monolithic device, fabricated on Atmel's 0.35µ five-layer metal CMOS process.

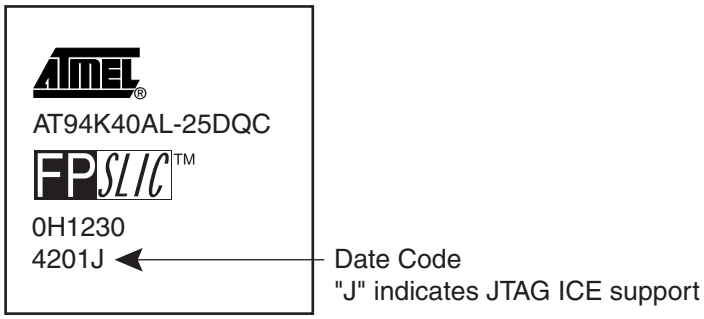
The AT40K FPGA core is a fully 3.3V PCI-compliant, SRAM-based FPGA with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data) and 5,000 to 40,000 usable gates.

Table 1-1. The AT94K Series Characteristics

Device		AT94K05AL	AT94K10AL	AT94K40AL
FPGA Gates		5K	10K	40K
FPGA Core Cells		256	576	2304
FPGA SRAM Bits		2048	4096	18432
FPGA Registers (Total)		436	846	2862
Maximum FPGA User I/O		96	116	120
AVR Programmable I/O Lines		8	16	16
Program SRAM		4 Kbytes - 16 Kbytes	20 Kbytes - 32 Kbytes	20 Kbytes - 32 Kbytes
Data SRAM		4 Kbytes - 16 Kbytes	4 Kbytes- 16 Kbytes	4 Kbytes - 16 Kbytes
Hardware Multiplier (8-bit)		Yes	Yes	Yes
2-wire Serial Interface		Yes	Yes	Yes
UARTs		2	2	2
Watchdog Timer		Yes	Yes	Yes
Timer/Counters		3	3	3
Real-time Clock		Yes	Yes	Yes
JTAG ICE		Yes[1]	Yes[1]	Yes[1]
Typical AVR throughput	@ 25 MHz	19 MIPS	19 MIPS	19 MIPS
Operating Voltage		3.0 - 3.6V	3.0 - 3.6V	3.0 - 3.6V

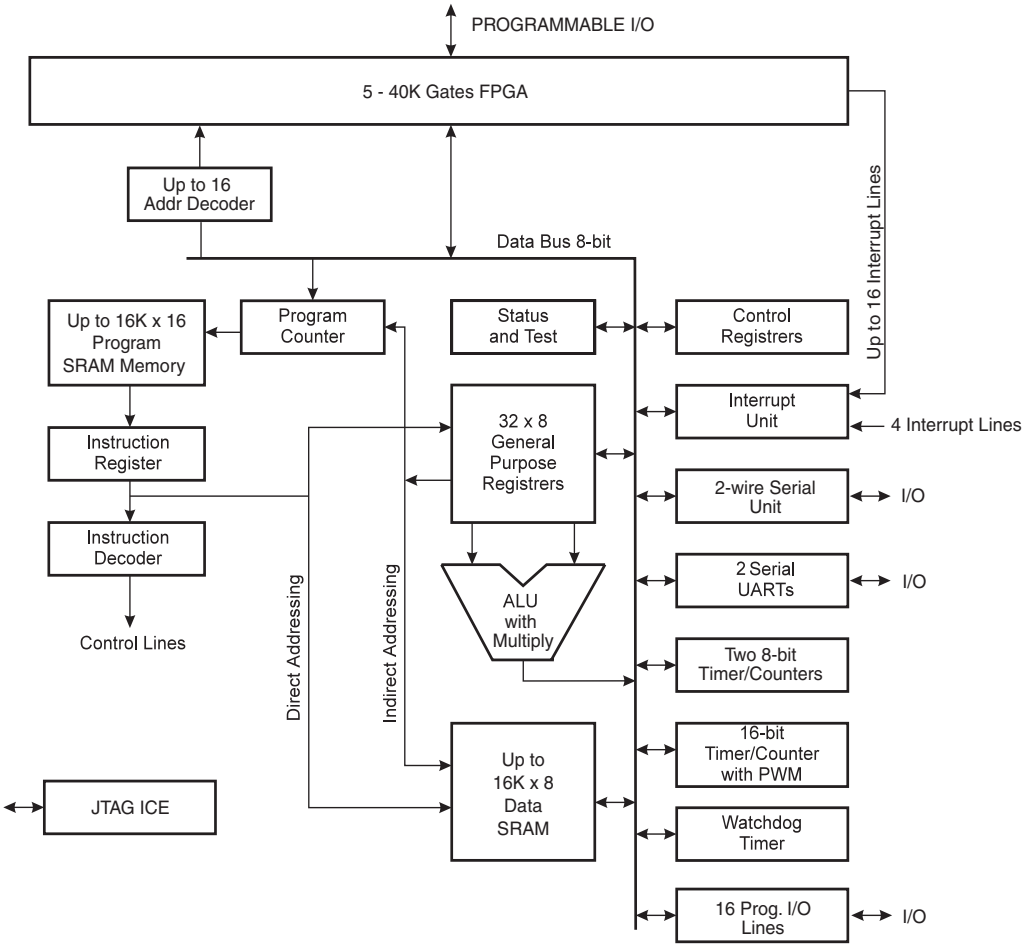
Notes: 1. FPSLIC parts with JTAG ICE support can be identified by the letter "J" after the device date code, e.g., 4201 (no ICE support) and 4201J (with ICE support), see Figure 1-1.

Figure 1-1. FPSLIC Device Date Code with JTAG ICE Support



The AT94K series architecture is shown in Figure 1-2.

Figure 1-2. AT94K Series Architecture



The embedded AVR core achieves throughputs approaching 1 MIPS per MHz by executing powerful instructions in a single-clock cycle, and allows system designers to optimize power consumption versus processing speed. The AVR core is based on an enhanced RISC architecture that combines a rich instruction set with 32 general-purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code-efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers at the same clock frequency. The AVR executes out of on-chip SRAM. Both the FPGA configuration SRAM and the AVR instruction code SRAM can be automatically loaded at system power-up using Atmel's In-System Programmable (ISP) AT17 Series EEPROM Configuration Memories.

State-of-the-art FPSLIC design tools, System Designer, were developed in conjunction with the FPSLIC architecture to help reduce overall time-to-market by integrating microcontroller development and debug, FPGA development and Place and Route, and complete system co-verification in one easy-to-use software tool.

Table 1-2. FPSLIC Configuration Devices

FPSLIC Device	FPSLIC Configuration Device	Configuration Data	Spare Memory
AT94K05	AT17LV256	226520 Bits	35624 Bits
AT94K10	AT17LV512	430488 Bits	93800 Bits
AT94K40	AT17LV010	815382 Bits	233194 Bits

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