AT91SAM9RL-EK Evaluation Board

User Guide



6325C–ATARM–22-Jul-10

Table of Contents

Section 1

Overview 1-1

1.1 Scope 1-1
1.2 Deliverables 1-1
1.3 AT91SAM9RL-EK Evaluation Board 1-1

Section 2

Setting Up the AT91SAM9RL-EK Board 2-1

2.1 Electrostatic Warning 2-1
2.2 Requirements 2-1
2.3 Layout 2-2
2.4 Powering Up the Board 2-4
2.5 Backup Power Supply 2-4
2.6 Getting Started 2-4
2.7 AT91SAM9RL-EK Block Diagram 2-5

Section 3

Board Description 3-1

3.1 AT91SAM9RL64 Microcontroller 3-1
3.2 AT91SAM9RL Block Diagram 3-4
3.3 Microcontroller 3-4
3.4 Memory 3-4
3.5 Clock Circuitry 3-4
3.6 Reset Circuitry 3-5
3.7 Shutdown Controller 3-5
3.8 Power Supply Circuitry 3-5
3.9 Remote Communication 3-5
3.10 Audio Stereo Interface 3-5
3.11 User Interface 3-5
3.12 Debug Interface 3-5
3.13 Expansion Slot 3-6
3.14 PIO Usage 3-7

Section 4

Jumpers 4-1

4.1 Jumpers 4-1
4.2 JTAG/ICE 4-1

4.3 Microcontroller Clock 4-2
4.4 Memory 4-2
4.5 Miscellaneous 4-2

Section 5

Schematics 5-1

5.1 Board Schematics 5-1

Section 6

Revision History 6-1

6.1 Revision History 6-1

Section 1

Overview

1.1 Scope

The AT91SAM9RL-EK evaluation kit enables the evaluation of and code development for applications running on an AT91SAM9RL device. It significantly reduces design cycle time, increasing confidence in a right-first-time system solution.

This guide focuses on the AT91SAM9RL-EK board as an evaluation platform.

The board supports the AT91SAM9RL in an LFBGA217 package.

1.2 Deliverables

The AT91SAM9RL-EK package contains the following items:

- an AT91SAM9RL-EK board
- universal input AC/DC power supply with US, UK and Europe plug adapter
- one 3V battery backup (CR1225 or equivalent)
- one A/B-type USB cable
- one serial RS232 cable
- one CD-ROM that allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 AT91SAM9RL-EK Evaluation Board

- The board is equipped with an AT91SAM9RL64 (217-ball LFBGA package) together with the following:
- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory
- one Atmel serial DataFlash®
- one Atmel TWI serial EEPROM (footprint only)
- one USB High Speed device port interface
- one DBGU serial communication port
- one additional serial communication port with RTS/CTS handshake control
- JTAG/ICE debug interface
- one AC97 Audio Codec
- one 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- one Power LED and two general-purpose LED

- two user input push buttons
- one Wakeup input push button
- one reset push button
- one MCI SD/MMC card slot
- four expansion connectors (PIOA, PIOB, PIOC, PIOD)
- one BGA-like EBI expansion footprint connector
- one Lithium Coin Cell Battery Retainer for 12 mm cell size

Section 2

Setting Up the AT91SAM9RL-EK Board

2.1 Electrostatic Warning

Upon delivery, the AT91SAM9RL-EK evaluation board is wrapped in a protective anti-static bag. The board must not be exposed to electrostatic discharges. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other on-board metallic element.

2.2 Requirements

In order to set up the AT91SAM9RL-EK evaluation board, the following items are needed:

- The AT91SAM9RL-EK evaluation board itself
- AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm

2.3 Layout

Figure 2-1. AT91SAM9RL-EK Layout - Top View

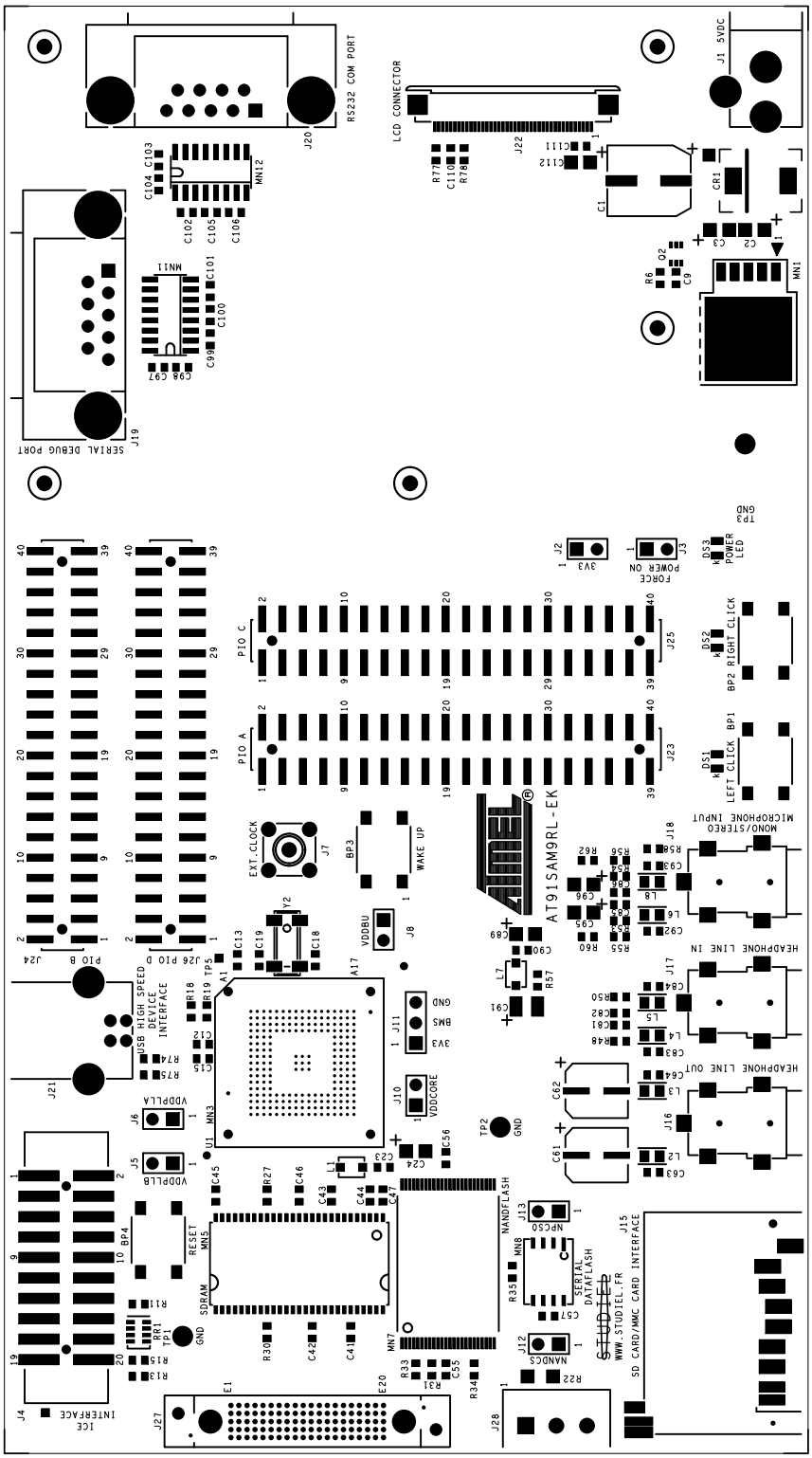
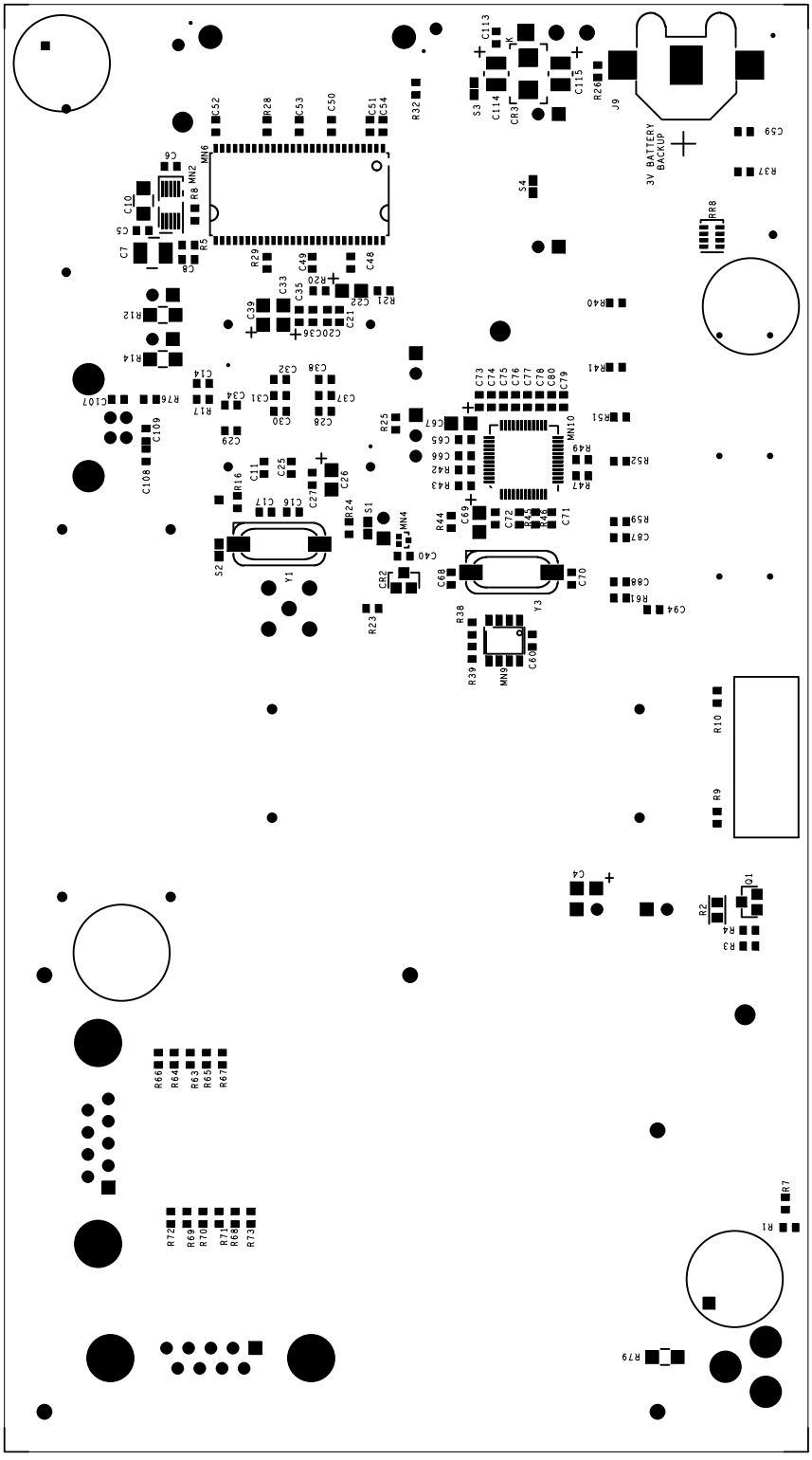


Figure 2-2. AT91SAM9RL-EK Layout - Bottom View



2.4 Powering Up the Board

The AT91SAM9RL-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket J1. Coaxial plug center positive standard.

2.5 Backup Power Supply

The user has the possibility to plug a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device.

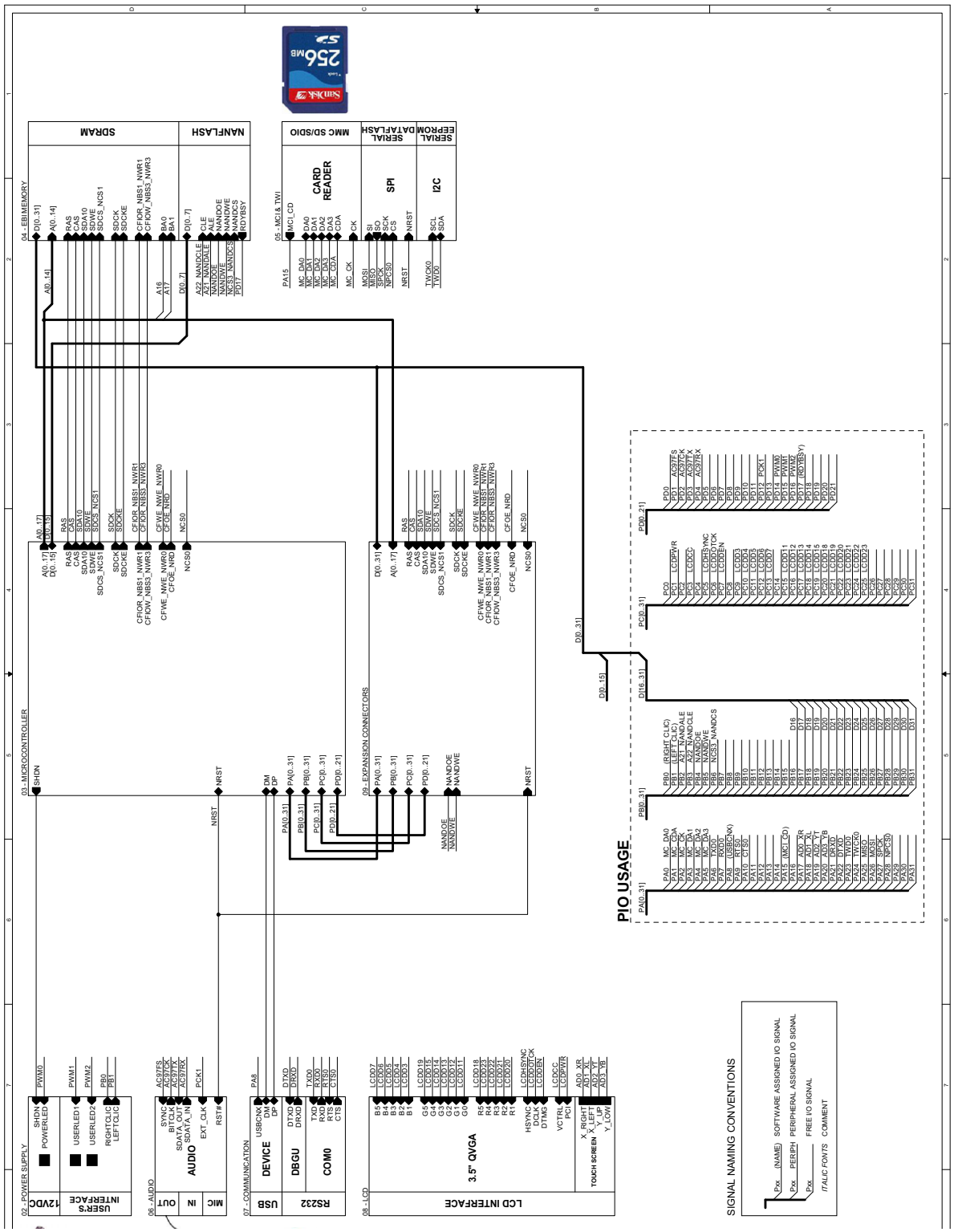
Refer to Section 4.

2.6 Getting Started

The AT91SAM9RL-EK evaluation board is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this CD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9RL-EK.

2.7 AT91SAM9RL-EK Block Diagram

Figure 2-3. AT91SAM9RL-EK Block Diagram



Section 3

Board Description

3.1 AT91SAM9RL64 Microcontroller

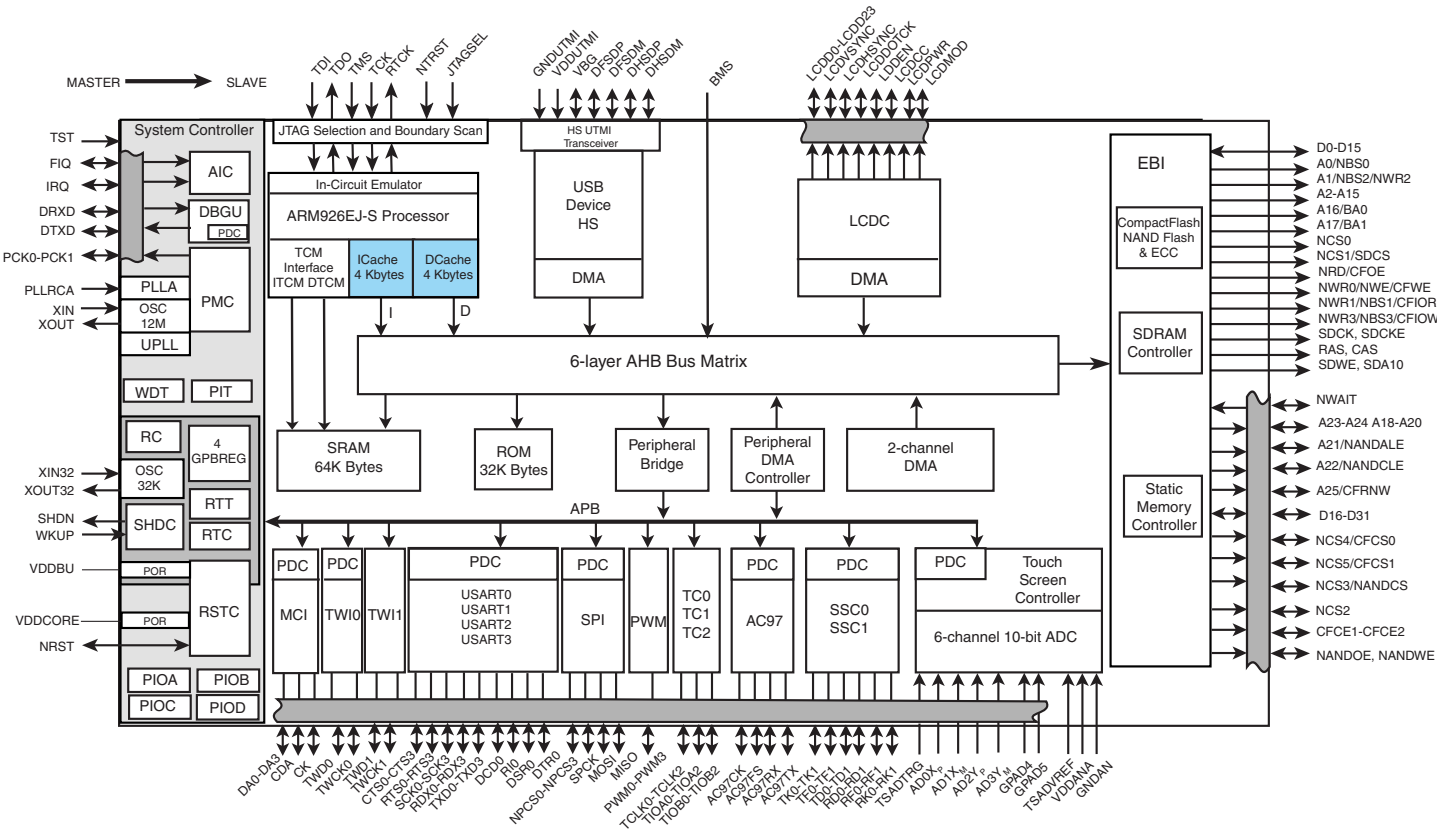
- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions
  - ARM Jazelle® Technology for Java® Acceleration
  - 4 Kbyte Data Cache, 4 Kbyte Instruction Cache, Write Buffer
  - 210 MIPS at 190 MHz
  - Memory Management Unit
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
  - Mid-level implementation Embedded Trace Macrocell™
- Multi-layer AHB Bus Matrix for Large Bandwidth Transfers
  - Six 32-bit-layer Matrix
  - Boot Mode Select Option, Remap Command
- One 32-KByte internal ROM, Single-cycle Access at Maximum Speed
- One 64-KByte internal SRAM, Single-cycle Access at Maximum Speed
  - 4 Blocks of 16 Kbytes Configurable in TCM or General-purpose SRAM on the AHB Bus Matrix
- Single-cycle Accessible on AHB Bus at Bus Speed
- Single-cycle Accessible on TCM Interface at Processor Speed
- 2-channel DMA
  - Memory to Memory Transfer
  - 16 Bytes FIFO
  - LInked List
- External Bus Interface (EBI)
  - EBI Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 Bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Virtual Screen Support
- High Speed (480 Mbit/s) USB 2.0 Device Controller
  - On-Chip High Speed Transceiver, UTMI+ Physical Interface
  - Integrated FIFOs and Dedicated DMA
  - 4 Kbyte Configurable Integrated DPRAM
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller

  - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer and Real-time Clock
- Reset Controller (RSTC)
  - Based on Two Power-on Reset Cells
  - Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - Selectable 32768 Hz Low-power oscillator or Internal Low-power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 12 MHz On-chip Oscillator for Main System Clock and USB Clock
  - One PLL up to 240 MHz
  - One PLL 480 MHz Optimized for USB HS
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - One External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and support for Debug Communication Channel
- Periodic Interval Timer (PIT)
  - 20-bit interval timer plus 12-bit interval counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- Real-time Clock (RTC)
  - Time, Date and Alarm 32-bit Parallel Load
  - Low Power Consumption
  - Programmable Periodic Interrupt
- One 6-channel 10-Bit Analog-to-Digital Converter
  - Touch Screen Interface Compatible with Industry Standard 4-wire Sensitive Touch Panels
- Four 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC and PIOD)
  - 118 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os for 217-ball BGA package
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- 24-channel Peripheral DMA Controller (PDC)
- One Multimedia Card Interface (MCI)
  - SDCard/SDIO 1.0 and MultiMedia Card 3.1 Compliant

  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- Two Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One AC97 Controller (AC97C)
  - 6-channel Single AC97 Analog Front End Interface, Slot Assigner
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- One Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - High-speed Synchronous Communications
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- Two Two-wire Interfaces (TWI)
  - Compatible with Standard Two-wire Serial Memories
  - One, Two or Three Bytes for Slave Address
  - Sequential Read/Write Operations
  - Master, Multi-master and Slave Mode Operation
  - Bit Rate: Up to 400 Kbits
  - General Call Supported in Slave mode
  - Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode Only (TWI0 only)
- SAM-BA Boot Assistant
  - Default Boot Program
  - Interface with SAM-BA Graphic User Interface
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.08 to 1.32V for VDDCORE, VDDPLLB and VDDBU
  - 3.0V to 3.6V for VDDPLLA, VDDANA, VDDUTMI and VDDIOP
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM
- Available in a 144-ball BGA (AT91SAM9R64) and a 217-ball LFBGA (AT91SAM9RL64) Package

3.2 AT91SAM9RL Block Diagram

Figure 3-1. AT91SAM9RL Block Diagram



3.3 Microcontroller

- One AT91SAM9RL64 217-ball LFBGA fitted on board

3.4 Memory

- 32 Kbytes of Internal ROM
- 64 Kbyte of Internal SRAM
- Atmel serial DataFlash
- 64 Mbytes of SDRAM memory (32-bit bus width)
- 256 Mbytes of NAND Flash memory (8-bit bus width)
- TWI serial EEPROM (footprint only)

3.5 Clock Circuitry

- 12 MHz standard crystal for the embedded oscillator

- Software selectable, 32768Hz Low-power external standard crystal Oscillator or Internal Low Power RC Oscillator

3.6 Reset Circuitry

- Internal reset controller with bi-directional reset pin
- External reset pushbutton

3.7 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.8 Power Supply Circuitry

- On-board 1.2V High Efficiency step-down charge pump regulator with shutdown control
- On-board 3.3V linear regulator with shutdown control

3.9 Remote Communication

- One serial interface (DBGU COM Port) via RS-232 DB9 male socket
- One additional serial interface (COM Port 1) with RTS/CTS handshake control via RS-232 DB9 male socket
- One High Speed USB 2.0 port 480 Mbits per second (UDP)

3.10 Audio Stereo Interface

- One AC97 audio CODEC with:
- One 32 Ohm Stereo Headset output (J16) with master volume and mute controls
- One line-in
- One Mono/Stereo Microphone input.

3.11 User Interface

- Two user input pushbuttons
- Two user green LED
- One yellow power LED (can be also software controlled)

3.12 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM port

3.13 Expansion Slot

- One DataFlash, SD/MMC card slot
- All I/Os of the AT91SAM9RL are routed to peripheral extension connectors (J23, J24, J25, J26).
- All EBI Signals of the AT91SAM9RL are routed to extension footprint connectors (J27). Refer to the Atmel application note Connecting EBI Memory Daughter Boards to AT91SAM Evaluation Boards, lit. no. 6309.
- This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

3.14 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Application Usage		Powered by
PA0	MC_DA0		SD/MMC CARD READER	MC_DA0	VDDIOP
PA1	MC_CDA		SD/MMC CARD READER	MC_CDA	VDDIOP
PA2	MC_CK		SD/MMC CARD READER	MC_CK	VDDIOP
PA3	MC_DA1	TCLK0	SD/MMC CARD READER	MC_DA1	VDDIOP
PA4	MC_DA2	TIOA0	SD/MMC CARD READER	MC_DA2	VDDIOP
PA5	MC_DA3	TIOB0	SD/MMC CARD READER	MC_DA3	VDDIOP
PA6	TXD0		RS232 COM PORT	TXD0	VDDIOP
PA7	RXD0		RS232 COM PORT	RXD0	VDDIOP
PA8	SCK0	RF1	USB DEVICE	PA8 as USB_CNX	VDDIOP
PA9	RTS0	RK1	RS232 COM PORT	RTS0	VDDIOP
PA10	CTS0	RK0	RS232 COM PORT	CTS0	VDDIOP
PA11	TXD1				VDDIOP
PA12	RXD1				VDDIOP
PA13	TXD2	TD1			VDDIOP
PA14	RXD2	RD1			VDDIOP
PA15	TD0		SD/MMC CARD READER	PA15 as MCI_CD	VDDIOP
PA16	RD0				VDDIOP
PA17	AD0		TOUCH SCREEN PANEL	AD0_XR	VDDIOP
PA18	AD1	RTS1	TOUCH SCREEN PANEL	AD1_XL	VDDIOP
PA19	AD2	CTS1	TOUCH SCREEN PANEL	AD2_YT	VDDIOP
PA20	AD3	SCK3	TOUCH SCREEN PANEL	AD3_YB	VDDIOP
PA21	DRXD		SERIAL DEBUG PORT	DRXD	VDDIOP
PA22	DTXD	RF0	SERIAL DEBUG PORT	DTXD	VDDIOP
PA23	TWD0		I2C MEMORY	TWD0	VDDIOP
PA24	TWCK0		I2C MEMORY	TWCK0	VDDIOP
PA25	MISO		DATAFLASH DEVICE	MISO	VDDIOP
PA26	MOSI		DATAFLASH DEVICE	MOSI	VDDIOP
PA27	SPCK		DATAFLASH DEVICE	SPCK	VDDIOP
PA28	NPCS0		DATAFLASH DEVICE	NPCS0	VDDIOP
PA29	RTS2	TF1			VDDIOP
PA30	CTS2	TK1			VDDIOP
PA31	NWAIT	IRQ			VDDIOP

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Application Usage		Powered by
PB0	TXD3		USER'S PUSH BUTTON 1	PB0 as LEFT CLICK	VDDIOP
PB1	RXD3		USER'S PUSH BUTTON 2	PB1 as RIGHT CLICK	VDDIOP
PB2	A21/NANDALE		NAND FLASH MEMORY	NANDALE	VDDIOM
PB3	A22/NANDCLE		NAND FLASH MEMORY	NANDCLE	VDDIOM
PB4	NANDOE		NAND FLASH MEMORY	NANDOE	VDDIOM
PB5	NANDWE		NAND FLASH MEMORY	NANDWE	VDDIOM
PB6	NCS3/NANDCS		NAND FLASH MEMORY	NCS3/NANDCS	VDDIOM
PB7	NCS4/CFCS0	NPCS1			VDDIOM
PB8	CFCE1	PWM0			VDDIOM
PB9	CFCE2	PWM1			VDDIOM
PB10	A25/CFRNW	FIQ			VDDIOM
PB11	A18				VDDIOM
PB12	A19				VDDIOM
PB13	A20				VDDIOM
PB14	A23	PCK0			VDDIOM
PB15	A24	ADTRG			VDDIOM
PB16	D16		SDRAM MEMORY	D16	VDDIOM
PB17	D17		SDRAM MEMORY	D17	VDDIOM
PB18	D18		SDRAM MEMORY	D18	VDDIOM
PB19	D19		SDRAM MEMORY	D19	VDDIOM
PB20	D20		SDRAM MEMORY	D20	VDDIOM
PB21	D21		SDRAM MEMORY	D21	VDDIOM
PB22	D22		SDRAM MEMORY	D22	VDDIOM
PB23	D23		SDRAM MEMORY	D23	VDDIOM
PB24	D24		SDRAM MEMORY	D24	VDDIOM
PB25	D25		SDRAM MEMORY	D25	VDDIOM
PB26	D26		SDRAM MEMORY	D26	VDDIOM
PB27	D27		SDRAM MEMORY	D27	VDDIOM
PB28	D28		SDRAM MEMORY	D28	VDDIOM
PB29	D29		SDRAM MEMORY	D29	VDDIOM
PB30	D30		SDRAM MEMORY	D30	VDDIOM
PB31	D31		SDRAM MEMORY	D31	VDDIOM

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Application Usage		Powered by
PC0	TF0				VDDIOP
PC1	TK0	LCDPWR	LCD PANEL	LCDPWR	VDDIOP
PC2	LCDMOD	PWM0			VDDIOP
PC3	LCDCC	PWM1	LCD PANEL	LCDCC	VDDIOP
PC4	LCDVSYNC				VDDIOP
PC5	LCDHSYNC		LCD PANEL	LCDHSYNC	VDDIOP
PC6	LCDDOTCK		LCD PANEL	LCDDOTCK	VDDIOP
PC7	LCDDEN		LCD PANEL	LCDDEN	VDDIOP
PC8	LCDD0	LCDD2	LCD PANEL	LCDD2	VDDIOP
PC9	LCDD1	LCDD3	LCD PANEL	LCDD3	VDDIOP
PC10	LCDD2	LCDD4	LCD PANEL	LCDD4	VDDIOP
PC11	LCDD3	LCDD5	LCD PANEL	LCDD5	VDDIOP
PC12	LCDD4	LCDD6	LCD PANEL	LCDD6	VDDIOP
PC13	LCDD5	LCDD7	LCD PANEL	LCDD7	VDDIOP
PC14	LCDD6	LCDD10	LCD PANEL	LCDD10	VDDIOP
PC15	LCDD7	LCDD11	LCD PANEL	LCDD11	VDDIOP
PC16	LCDD8	LCDD12	LCD PANEL	LCDD12	VDDIOP
PC17	LCDD9	LCDD13	LCD PANEL	LCDD13	VDDIOP
PC18	LCDD10	LCDD14	LCD PANEL	LCDD14	VDDIOP
PC19	LCDD11	LCDD15	LCD PANEL	LCDD15	VDDIOP
PC20	LCDD12	LCDD18	LCD PANEL	LCDD18	VDDIOP
PC21	LCDD13	LCDD19	LCD PANEL	LCDD19	VDDIOP
PC22	LCDD14	LCDD20	LCD PANEL	LCDD20	VDDIOP
PC23	LCDD15	LCDD21	LCD PANEL	LCDD21	VDDIOP
PC24	LCDD16	LCDD22	LCD PANEL	LCDD22	VDDIOP
PC25	LCDD17	LCDD23	LCD PANEL	LCDD23	VDDIOP
PC26	LCDD18				VDDIOP
PC27	LCDD19				VDDIOP
PC28	LCDD20				VDDIOP
PC29	LCDD21	TIOA1			VDDIOP
PC30	LCDD22	TIOB1			VDDIOP
PC31	LCDD23	TCLK1			VDDIOP

Table 3-4. PIO Controller D

I/O Line	Peripheral A	Peripheral B	Application Usage		Powered by
PD0	NCS2				VDDIOP
PD1	AC97_FS		AC97 CODEC	AC97_FS	VDDIOP
PD2	AC97_CK	SCK1	AC97 CODEC	AC97_CK	VDDIOP
PD3	AC97_TX	CTS3	AC97 CODEC	AC97_TX	VDDIOP
PD4	AC97_RX	RTS3	AC97 CODEC	AC97_RX	VDDIOP
PD5	DTXD	PWM2			VDDIOP
PD6	AD4				VDDIOP
PD7	AD5				VDDIOP
PD8	NPCS2	PWM3			VDDIOP
PD9	SCK2	NPCS3			VDDIOP
PD10	TWD1	TIOA2			VDDIOP
PD11	TWCK1	TIOB2			VDDIOP
PD12	PWM2	PCK1			VDDIOP
PD13	NCS5/CFCS1	NPCS3			VDDIOP
PD14	DSR0	PWM0	POWER LED	PD14 or PWM0	VDDIOP
PD15	DTR0	PWM1	USER LED 1	PD15 or PWM1	VDDIOP
PD16	DCD0	PWM2	USER LED 2	PD16 or PWM2	VDDIOP
PD17	RI0		NAND FLASH MEMORY	PD17 as RDYBSY	VDDIOP
PD18	PWM3				VDDIOP
PD19	PCK0				VDDIOP
PD20	PCK1				VDDIOP
PD21	TCLK2				VDDIOP

Section 4

Jumpers

4.1 Jumpers

Table 4-1. Jumpers Configuration

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper(1)
J3	Closed	Forces power on. To use the software shutdown control, J3 must be opened. 3V battery backup must be present.
J5	Closed	VDDPLLB Jumper(1)
J6	Closed	VDDPLLA Jumper(1)
J8	Closed	VDDBU Jumper(1)
J10	Closed	VDDCORE Jumper(1)
J11	1-2	BMS (Boot Mode Select) 1-2: Internal ROM 2-3: NCS0
J12	Closed	Enables the use of the embedded NAND FLASH device (MN7)
J13	Closed	Enables the use of the embedded SERIAL DATAFLASH device (MN8)

Note: 1. These jumpers are provided for power consumption measurement use. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.

4.2 JTAG/ICE

Table 4-2. JTAG/ICE Configuration

Designation	Default Setting	Feature
S1	Opened	Selects ICE mode or JTAG mode
R11	Soldered	Enables the ICE NTRST input
R13	Soldered	Enables the ICE NRST input

4.3 Microcontroller Clock

Table 4-3. Microcontroller Clock Configuration

Designation	Default Setting	Feature
S2	Opened	To use an external source clock, the user has to close S2 and populate J7. In this case, C16, C17 and J7 have to be unsoldered.

4.4 Memory

Table 4-4. Memory Configuration

Designation	Default Setting	Feature
SDRAM (MN5 & MN6)		
R29	Soldered	Enables MN5 Chip select access
R30	Soldered	Enables MN6 Chip select access
NANDFLASH (MN7)		
J12	Closed	Enables the use of the NANDFLASH device
R32	Soldered	Enables the use of the Ready/Busy signal
S3	Opened	Disables the write protect
SERIAL DATAFLASH (MN8)		
J13	Closed	Enables the use of the DATAFLASH device
S4	Opened	Disables the write protect.
TWI SERIAL EEPROM NOT POPULATED (MN9)		

4.5 Miscellaneous

Refer to the TOP level schematic for the PIO usage.

Table 4-5. Miscellaneous

Designation	Default Setting	Feature
USB HIGH SPEED DEVICE INTERFACE		
R75	Soldered	USB DEVICE: Enables the use of the USBCNX signal
DBGU COM PORT		
R64	Soldered	Enables the use of DTXD output signal
R66	Soldered	Enables the use of DRXD input
RS232 COM PORT: Enable the use of Input/output signals		

Table 4-5. Miscellaneous

Designation	Default Setting	Feature
R70 R71 R72 R73	Soldered Soldered Soldered Soldered	TXD RTS RXD CTS
TP1	N.A	GND Test point
TP2	N.A	GND Test point
TP3	N.A	GND Test point

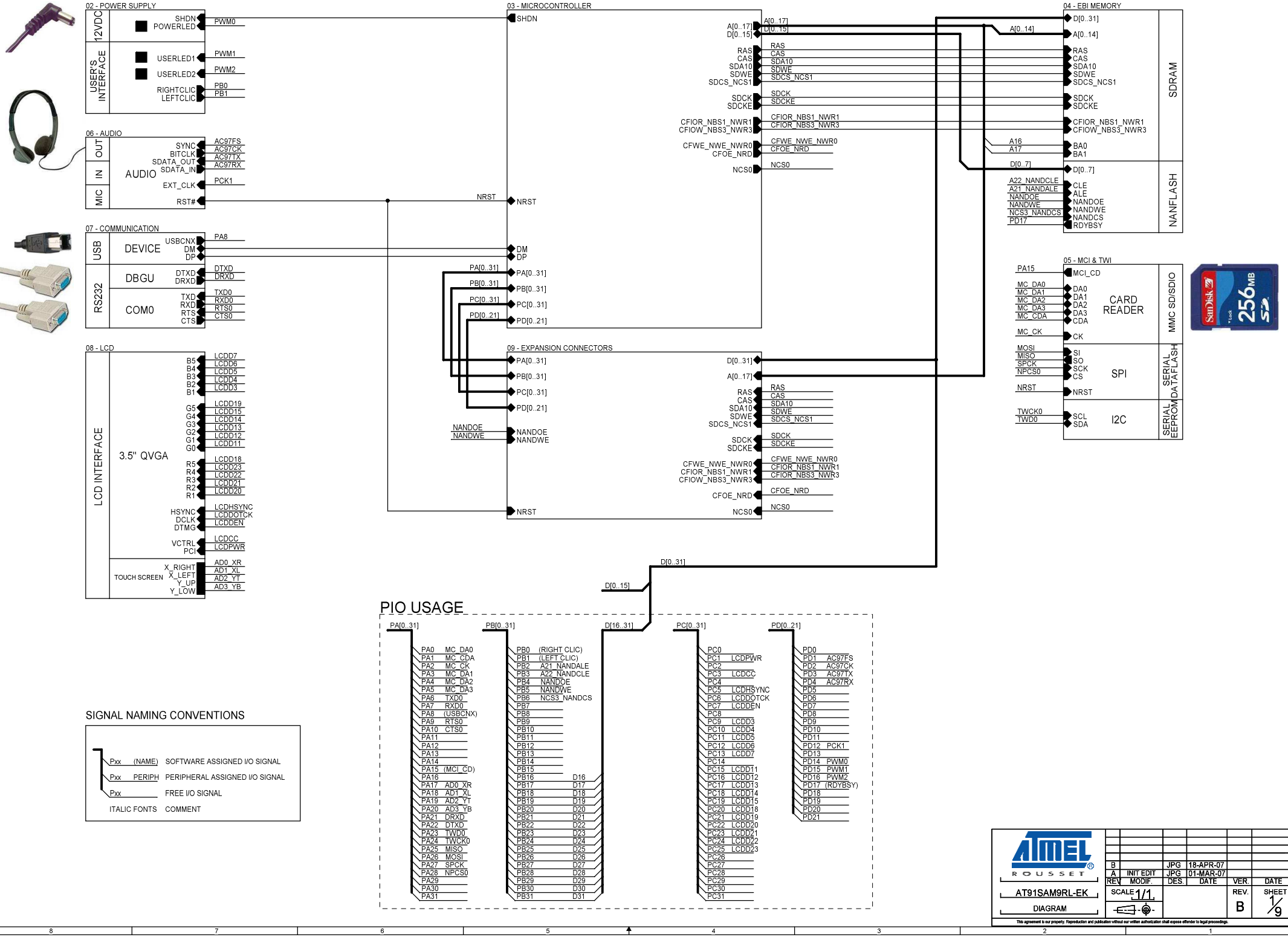
Section 5

Schematics

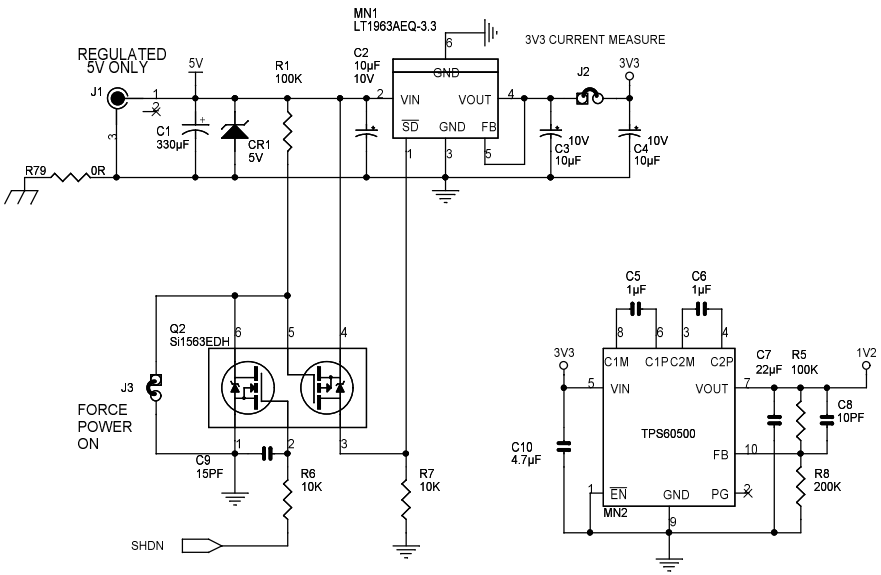
5.1 Board Schematics

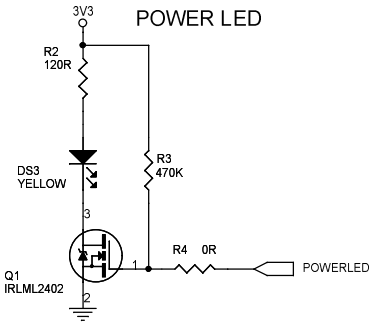
This section contains the following schematics:

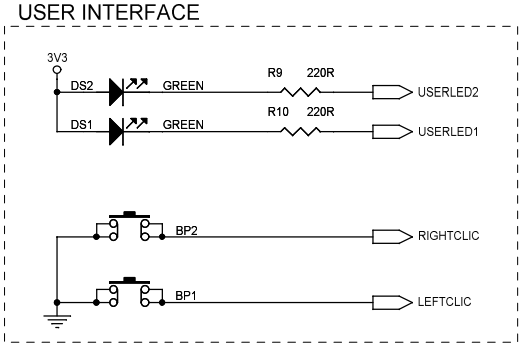
- Board Diagram - Schematic Top Level
- Power supply
- AT91SAM9RL Microcontroller
- EBI Memory
- Serial Memory
- Audio AC97
- Serial Interface
- TFT LCD display
- Expansion connectors

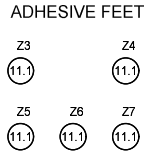

02 - POWER SUPPLY
12VDC
SHDN
POWERLED
PWM0
USER'S INTERFACE
USERLED1
USERLED2
RIGHTCLIC
LEFTCLIC
PWM1
PWM2
PB0
PB1
06 - AUDIO
OUT
IN
MIC
AUDIO
SYNC
BITCLK
SDATA_OUT
SDATA_IN
EXT_CLK
RST#
AC97FS
AC97CK
AC97TX
AC97RX
PCK1
07 - COMMUNICATION
USB
DEVICE
USBCNX
DM
DP
PA8
RS232
DBGU
DTXD
DRXD
COM0
TXD
RXD
RTS
CTS
TXD0
RXD0
RTS0
CTS0
08 - LCD
LCD INTERFACE
3.5" QVGA
B5 B4 B3 B2 B1
G5 G4 G3 G2 G1 G0
R5 R4 R3 R2 R1
LCDD7 LCDD6 LCDD5 LCDD4 LCDD3
LCDD19 LCDD15 LCDD14 LCDD13 LCDD12 LCDD11
LCDD18 LCDD23 LCDD22 LCDD21 LCDD20
HSYNC
DCLK
DTMG
VCTRL
PCI
LCDHSYNC
LCDDOTCK
LCDDEN
LCDCC
LCDPWR
TOUCH SCREEN
X_RIGHT
X_LEFT
Y_UP
Y_LOW
AD0_XR
AD1_XL
AD2_YT
AD3_YB
03 - MICROCONTROLLER
SHDN
NRST
DM
DP
PA[0..31]
PB[0..31]
PC[0..31]
PD[0..21]
A[0..17]
D[0..15]
RAS
CAS
SDA10
SDWE
SDCS_NCS1
SDCK
SDCKE
CFIOR_NBS1_NWR1
CFIOW_NBS3_NWR3
CFWE_NWE_NWR0
CFOE_NRD
NCS0
NANDOE
NANDWE
09 - EXPANSION CONNECTORS
D[0..31]
A[0..17]
04 - EBI MEMORY
A[0..14]
A16
A17
BA0
BA1
D[0..7]
A22_NANDCLE
A21_NANDALE
NANDOE
NANDWE
NCS3_NANDCS
PD17
CLE
ALE
NANDCS
RDYBSY
SDRAM
NANFLASH
05 - MCI & TWI
PA15
MCI_CD
MC_DA0
MC_DA1
MC_DA2
MC_DA3
MC_CDA
MC_CK
DA0
DA1
DA2
DA3
CDA
CK
CARD READER
MMC SD/SDIO
MOSI
MISO
SPCK
NPCS0
SI
SO
SCK
CS
SPI
SERIAL DATAFLASH
TWCK0
TWD0
SCL
SDA
I2C
SERIAL EEPROM
PIO USAGE
PA[0..31]
PB[0..31]
D[16..31]
PC[0..31]
PD[0..21]
PA0 MC_DA0
PA1 MC_CDA
PA2 MC_CK
PA3 MC_DA1
PA4 MC_DA2
PA5 MC_DA3
PA6 TXD0
PA7 RXD0
PA8 (USBCNX)
PA9 RTS0
PA10 CTS0
PA15 (MCI_CD)
PA17 AD0_XR
PA18 AD1_XL
PA19 AD2_YT
PA20 AD3_YB
PA21 DRXD
PA22 DTXD
PA23 TWD0
PA24 TWCK0
PA25 MISO
PA26 MOSI
PA27 SPCK
PA28 NPCS0
PB0 (RIGHT CLIC)
PB1 (LEFT CLIC)
PB2 A21_NANDALE
PB3 A22_NANDCLE
PB4 NANDOE
PB5 NANDWE
PB6 NCS3_NANDCS
PC0
PC1 LCDPWR
PC2
PC3 LCDCC
PC4
PC5 LCDHSYNC
PC6 LCDDOTCK
PC7 LCDDEN
PC8
PC9 LCDD3
PC10 LCDD4
PC11 LCDD5
PC12 LCDD6
PC13 LCDD7
PC14
PC15 LCDD11
PC16 LCDD12
PC17 LCDD13
PC18 LCDD14
PC19 LCDD15
PC20 LCDD18
PC21 LCDD19
PC22 LCDD20
PC23 LCDD21
PC24 LCDD22
PC25 LCDD23
PD0
PD1 AC97FS
PD2 AC97CK
PD3 AC97TX
PD4 AC97RX
PD12 PCK1
PD14 PWM0
PD15 PWM1
PD16 PWM2
PD17 (RDYBSY)
SIGNAL NAMING CONVENTIONS
Pxx (NAME) SOFTWARE ASSIGNED I/O SIGNAL
Pxx PERIPH PERIPHERAL ASSIGNED I/O SIGNAL
Pxx FREE I/O SIGNAL
ITALIC FONTS COMMENT
ATMEL ROUSSET
AT91SAM9RL-EK
DIAGRAM
SCALE 1/1
REV. B
SHEET 1/9
B JPG 18-APR-07
A INIT EDIT JPG 01-MAR-07
REV MODIF. DES. DATE VER. DATE

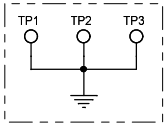
10 SQUARE CM COPPER AREA FOR HEAT SINKING
WITH NO SOLDER MASK







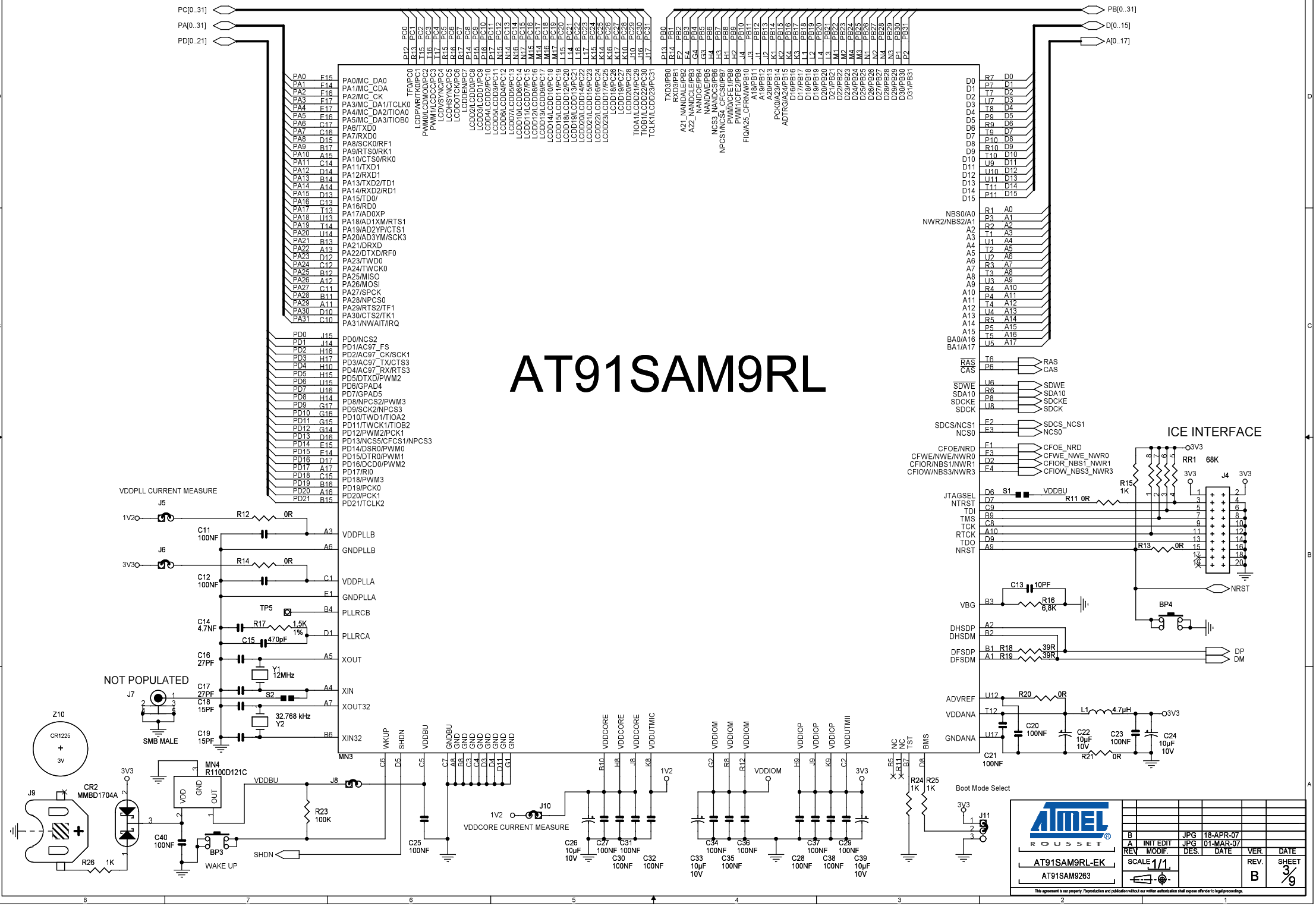


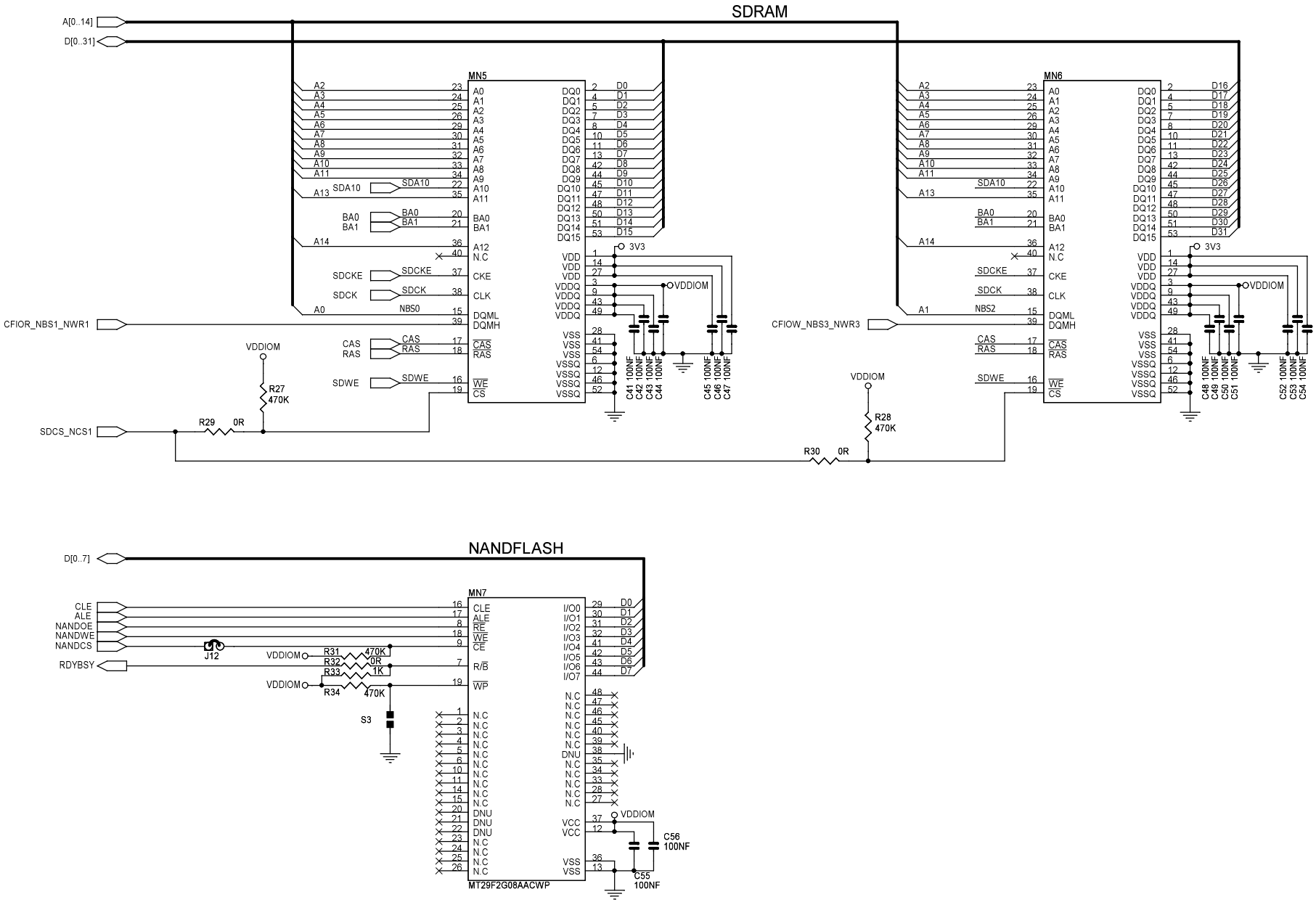


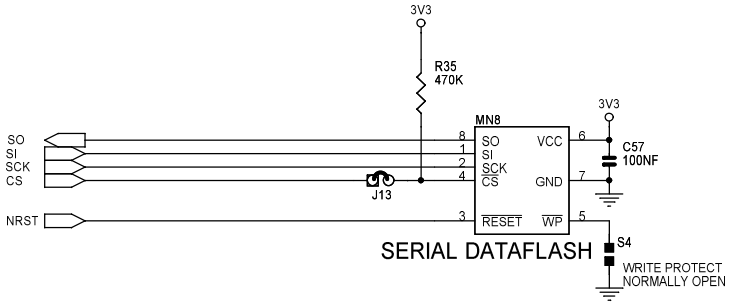
REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	18-APR-07		
A	INIT EDIT	JPG	01-MAR-07		

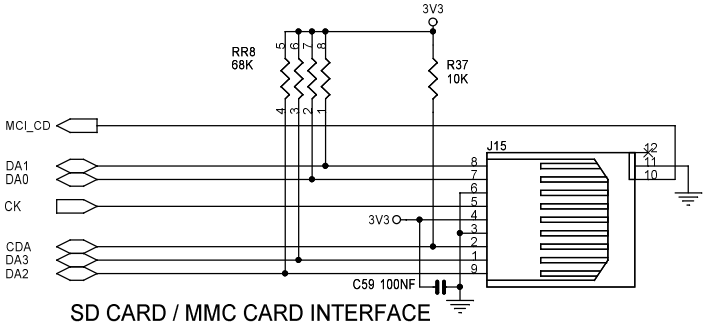
AT91SAM9RL-EK
POWER SUPPLY
SCALE 1/1
REV. B
SHEET 2/9

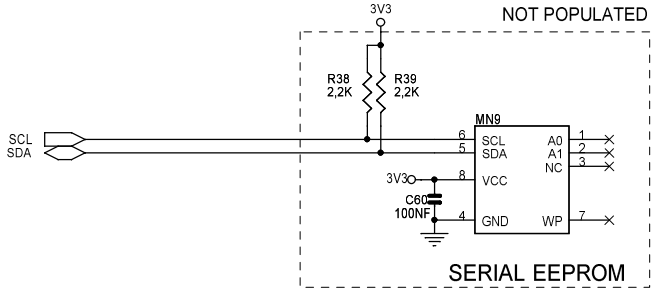
This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.


AT91SAM9RL
ICE INTERFACE
VDDPLL CURRENT MEASURE
NOT POPULATED
SMB MALE
VDDCORE CURRENT MEASURE
Boot Mode Select
WAKE UP
AT91SAM9RL-EK
AT91SAM9263
B JPG 18-APR-07
A INIT EDIT JPG 01-MAR-07
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. B
SHEET 3/9
This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.


SDRAM
A[0..14]
D[0..31]
MN5
MN6
CFIOR_NBS1_NWR1
CFIOW_NBS3_NWR3
SDCS_NCS1
VDDIOM
3V3
R27 470K
R28 470K
R29 0R
R30 0R
NANDFLASH
D[0..7]
CLE
ALE
NANDOE
NANDWE
NANDCS
RDYBSY
J12
R31 470K
R32 0R
R33 1K
R34 470K
S3
MN7
MT29F2G08AACWP
C56 100NF
C55 100NF
AT91SAM9RL-EK
EBI MEMORY
SCALE 1/1
REV. B
SHEET 4/9
B JPG 18-APR-07
A INIT EDIT JPG 01-MAR-07
This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.







REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	18-APR-07		
A	INIT EDIT	JPG	01-MAR-07		

AT91SAM9RL-EK

SERIAL MEMORY

SCALE 1/1

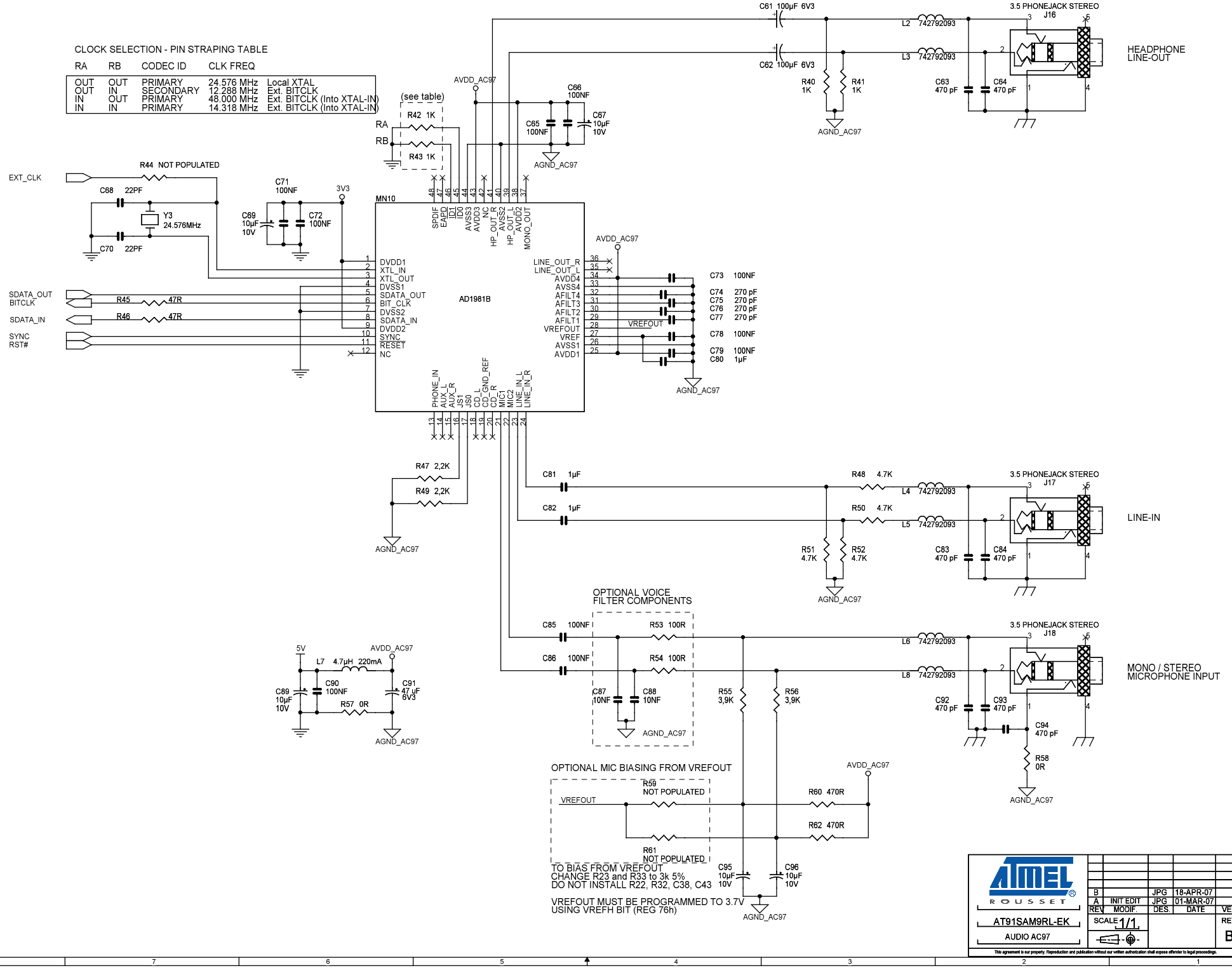
REV. B

SHEET 5/9

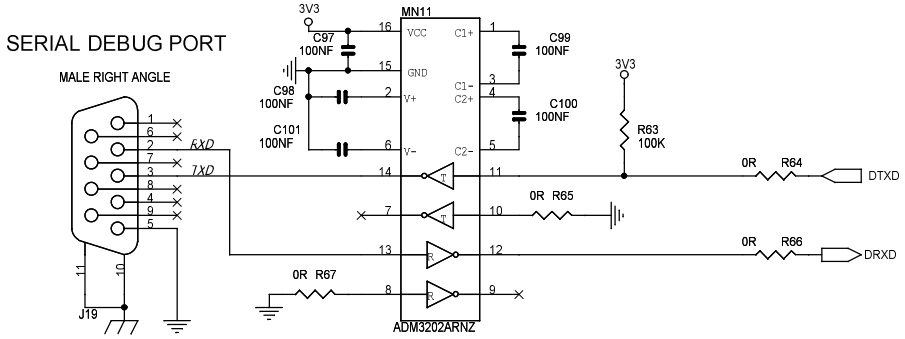
This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.

CLOCK SELECTION - PIN STRAPING TABLE

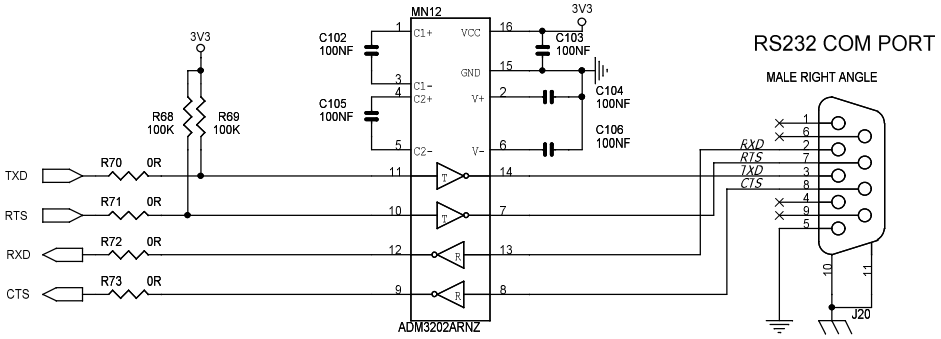
RA	RB	CODEC ID	CLK FREQ	
OUT	OUT	PRIMARY	24.576 MHz	Local XTAL
OUT	IN	SECONDARY	12.288 MHz	Ext. BITCLK
IN	OUT	PRIMARY	48.000 MHz	Ext. BITCLK (Into XTAL-IN)
IN	IN	PRIMARY	14.318 MHz	Ext. BITCLK (Into XTAL-IN)



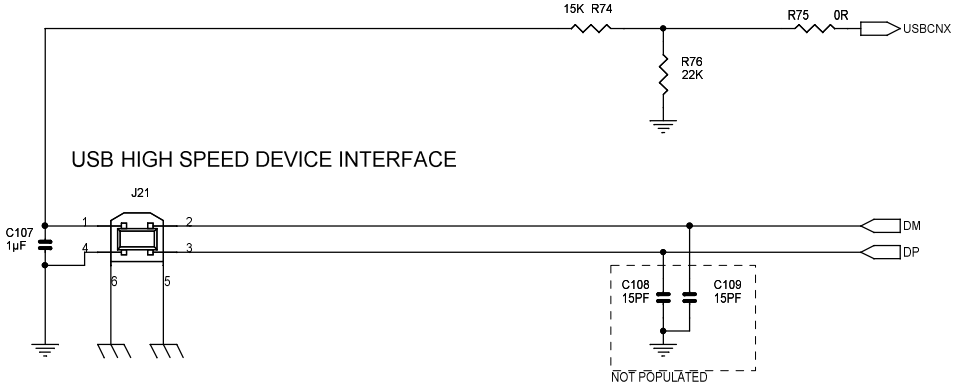
SERIAL DEBUG PORT



RS232 COM PORT



USB HIGH SPEED DEVICE INTERFACE



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	18-APR-07		
A	INIT EDIT	JPG	01-MAR-07		

AT91SAM9RL-EK

SERIAL INTERFACES

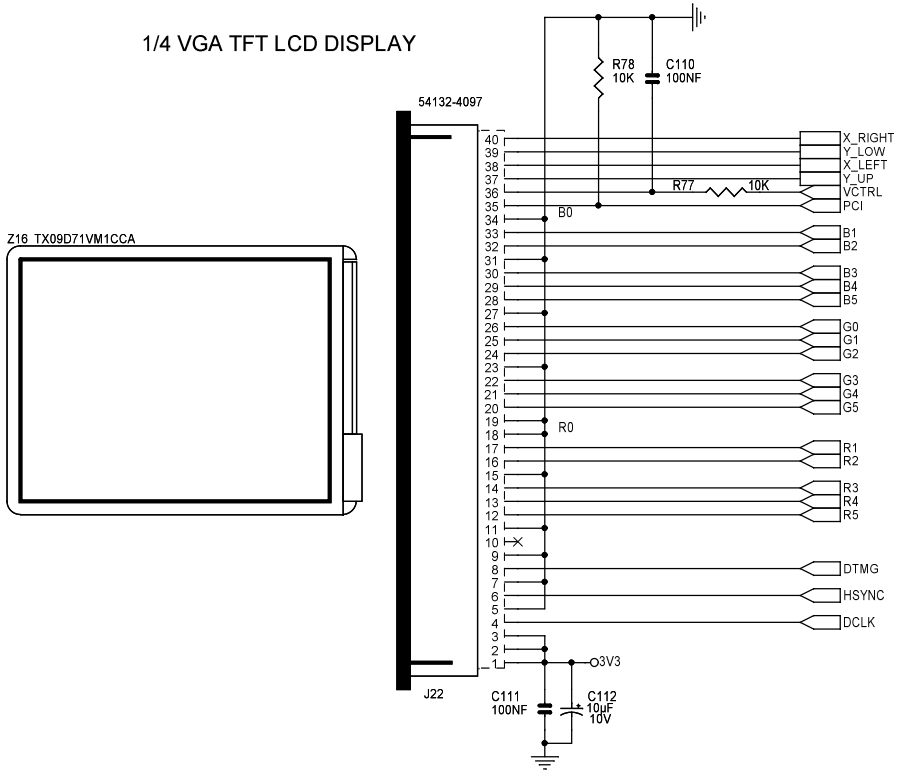
SCALE 1/1

REV. B

SHEET 7/9

This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.

1/4 VGA TFT LCD DISPLAY



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	18-APR-07		
A	INIT EDIT	JPG	01-MAR-07		

ATMEL ROUSSET

AT91SAM9RL-EK

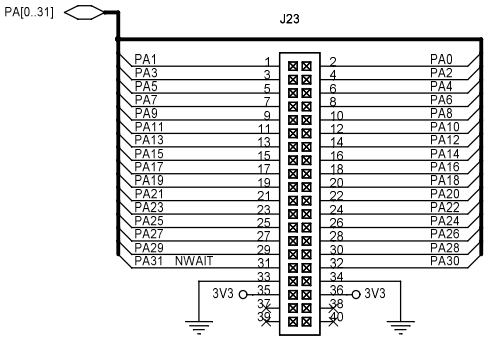
LCD

SCALE 1/1

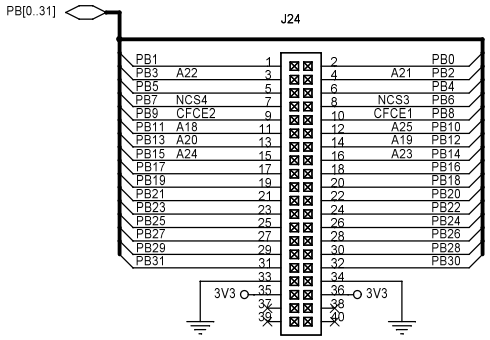
REV. B

SHEET 8/9

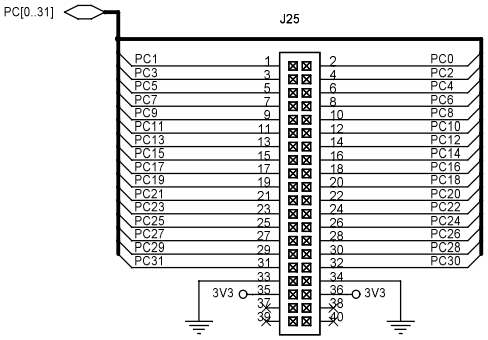
This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.



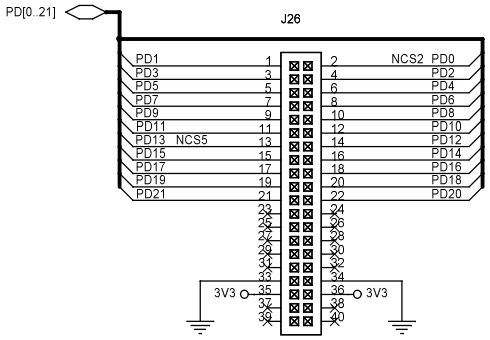
PIO A



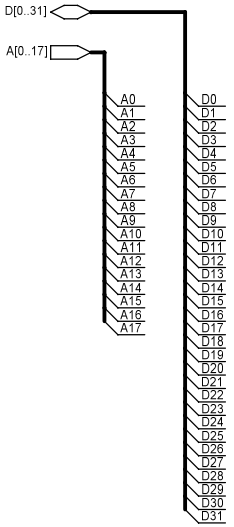
PIO B

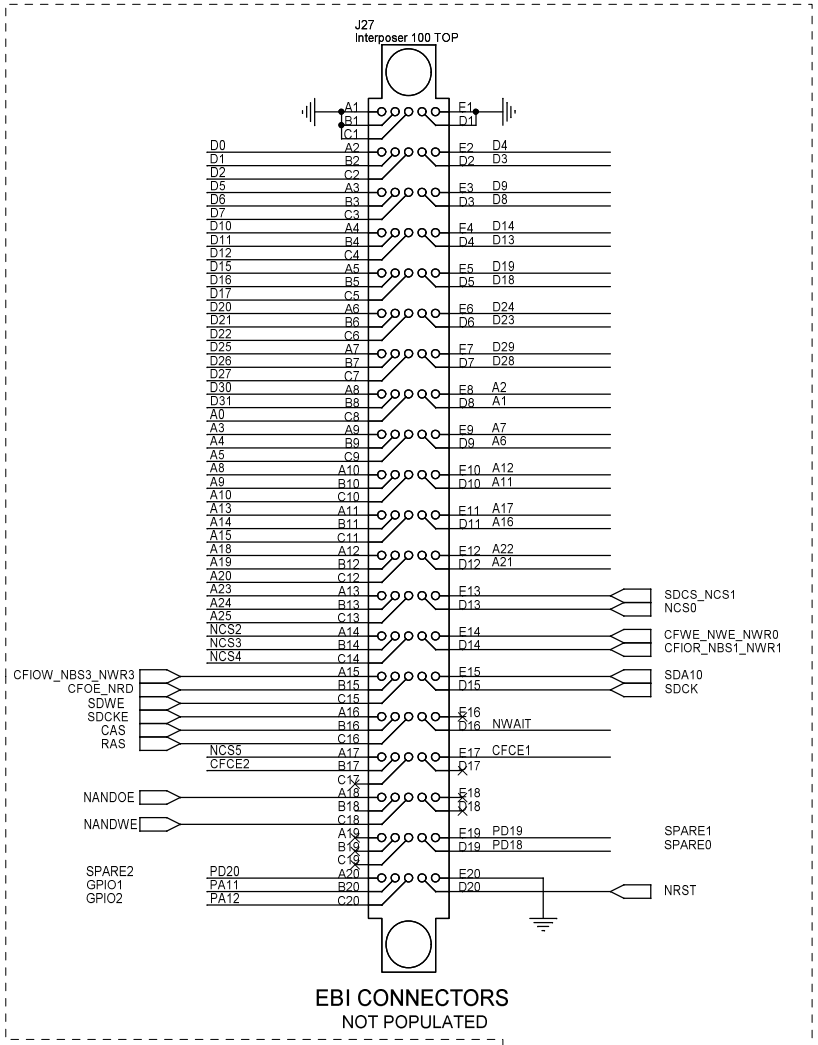


PIO C

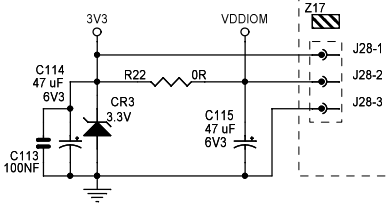


PIO D





EBI CONNECTORS
NOT POPULATED



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	18-APR-07		
A	INIT EDIT	JPG	01-MAR-07		

AT91SAM9RL-EK

EXPANSION

SCALE 1/1

REV. B

SHEET 9/9

This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.

Section 6

Errata

6.1 Pull-up Resistor on the Wrong Pin

The RTCK pin (connector J4, pin 11), which is an input, has a pull-up resistor whereas the TCK pin (connector J4, pin 9), which is an output, has not.

Problem Fix/Workaround

The user may observe a possible increase in the power consumption on VDDIO (a few micro-amps) but it does not prevent the JTAG-ICE interface to work correctly on this board.

Correct schematics would have a pull-up on the TCK pin to tie the CMOS input to a known level, in order to avoid a possible pad oscillation and a possible increase in power consumption.

6.2 VDDCORE Power Consumption Measurement Impossible

If the AT91SAM9RL64 device is an engineering sample (ES), VDDCORE power consumption measurement is impossible on J10 Jumper.

Problem Fix/Workaround

None.

Section 7

Revision History

7.1 Revision History

Table 7-1. Revision History

Document Ref.	Comments	Change Request Ref.
6325C	Section 6.2 ”VDDCORE Power Consumption Measurement Impossible” errata added	7188
6325B	CFE1 and CFE2 changed into CFCE1 and CFCE2 in Table 3-2 on page 3-8	5864
	Section 6.1 ”Pull-up Resistor on the Wrong Pin” errata added	5983
6325A	First issue.	

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

Technical Support
AT91SAM Support

Sales Contacts
www.atmel.com/contacts/

Literature Requests
www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2010 Atmel Corporation. All rights reserved. Atmel®, logo and combinations thereof, DataFlash® and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. ARM®, the ARMPowered® logo, Thumb® and others are the registered trademarks or trademarks of ARM Ltd. Other terms and product names may be trademarks of others.