AT91SAM9G10-EK Evaluation Board

User Guide



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Section 1

Overview 1-1

1.1 Scope 1-1
1.2 Deliverables 1-1
1.3 The AT91SAM9G10-EK Evaluation Board 1-1

Section 2

Setting Up the AT91SAM9G10-EK Evaluation Board 2-1

2.1 Electrostatic Warning 2-1
2.2 Requirements 2-1
2.3 Layout 2-2
2.4 Powering Up the Board 2-4
2.5 Backup Power Supply 2-4
2.6 Getting Started 2-4
2.7 AT91SAM9G10-EK Block Diagram 2-5

Section 3

Board Description 3-1

3.1 AT91SAM9G10 Microcontroller 3-1
3.2 AT91SAM9G10 Block Diagram 3-4
3.3 Memory 3-5
3.4 Clock Circuitry 3-5
3.5 Reset Circuitry 3-5
3.6 Shutdown Controller 3-5
3.7 Power Supply Circuitry 3-5
3.8 Remote Communication 3-5
3.9 Audio Stereo Interface 3-5
3.10 User Interface 3-6
3.11 Debug Interface 3-6
3.12 Expansion Slot 3-6
3.13 PIO Usage 3-7

Section 4

Configuration Straps 4-1

4.1 Configuration Straps 4-1

Section 5

Schematics 5-1

5.1 Schematics 5-1

Section 6

Errata 6-1

6.1 JTAGSEL S5 Footprint Selector 6-1

6.2 External Capacitor Values on XIN and XOUT 6-1

Section 7

Revision History 7-1

7.1 Revision History 7-1

Section 1

Overview

1.1 Scope

The AT91SAM9G10-EK evaluation kit is an effective platform for evaluating chip performance and developing code for applications based on the AT91SAM9G10.

This guide is a description of the hardware included in the AT91SAM9G10-EK evaluation kit. Software files are available embedded into the board's memory upon delivery.

1.2 Deliverables

The AT91SAM9G10-EK package contains the following items:

- an AT91SAM9G10-EK board
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- universal input AC/DC power supply with US and EU plug adapter

1.3 The AT91SAM9G10-EK Evaluation Board

The board is equipped with an AT91SAM9G10 (217-ball LFBGA package) together with the following:

- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory
- one Atmel® serial DataFlash®
- one USB device port interface
- two USB host port interfaces
- one DBGU serial communication port
- JTAG/ICE debug interface
- one Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- one Power LED and two general-purpose LEDs
- four user input pushbuttons
- one wakeup input pushbutton
- one reset pushbutton
- one DataFlash SD/MMC card slot

- two expansion footprint connectors (solder side)
- one Lithium Coin Cell Battery Retainer for 12 mm cell size
- dual pitch prototyping area

Section 2

Setting Up the AT91SAM9G10-EK Evaluation Board

2.1 Electrostatic Warning

The AT91SAM9G10-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. In risky ESD environments (e.g. offices with carpet) a grounding strap or similar protective device should be worn when handling the board. Also, generally avoid touching the component pins or any other metallic element of the board.

2.2 Requirements

In order to set up the AT91SAM9G10-EK evaluation board, the following items are required:

- the AT91SAM9G10-EK evaluation board itself
- AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm

2.3 Layout

Figure 2-1. AT91SAM9G10-EK Layout - Top View

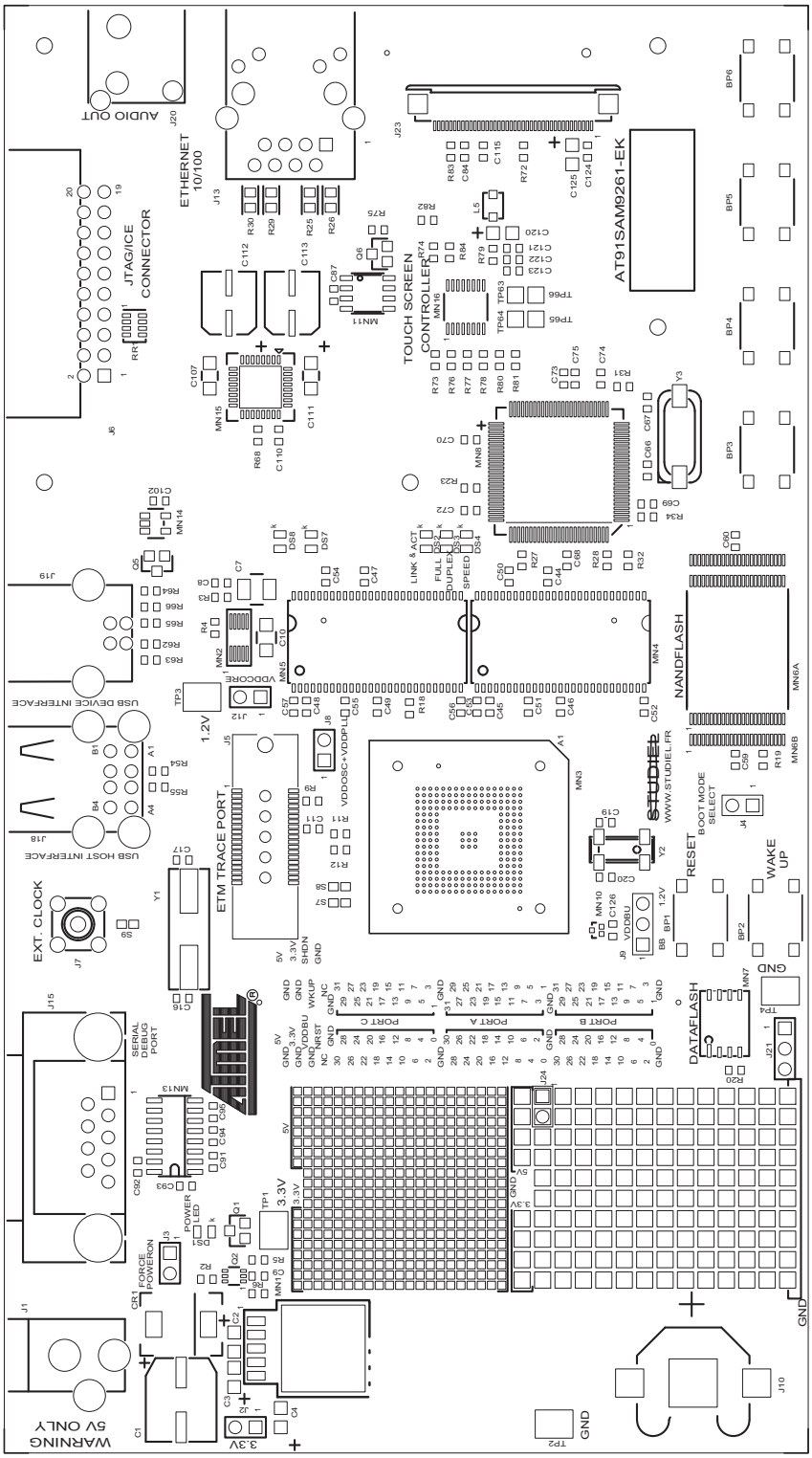
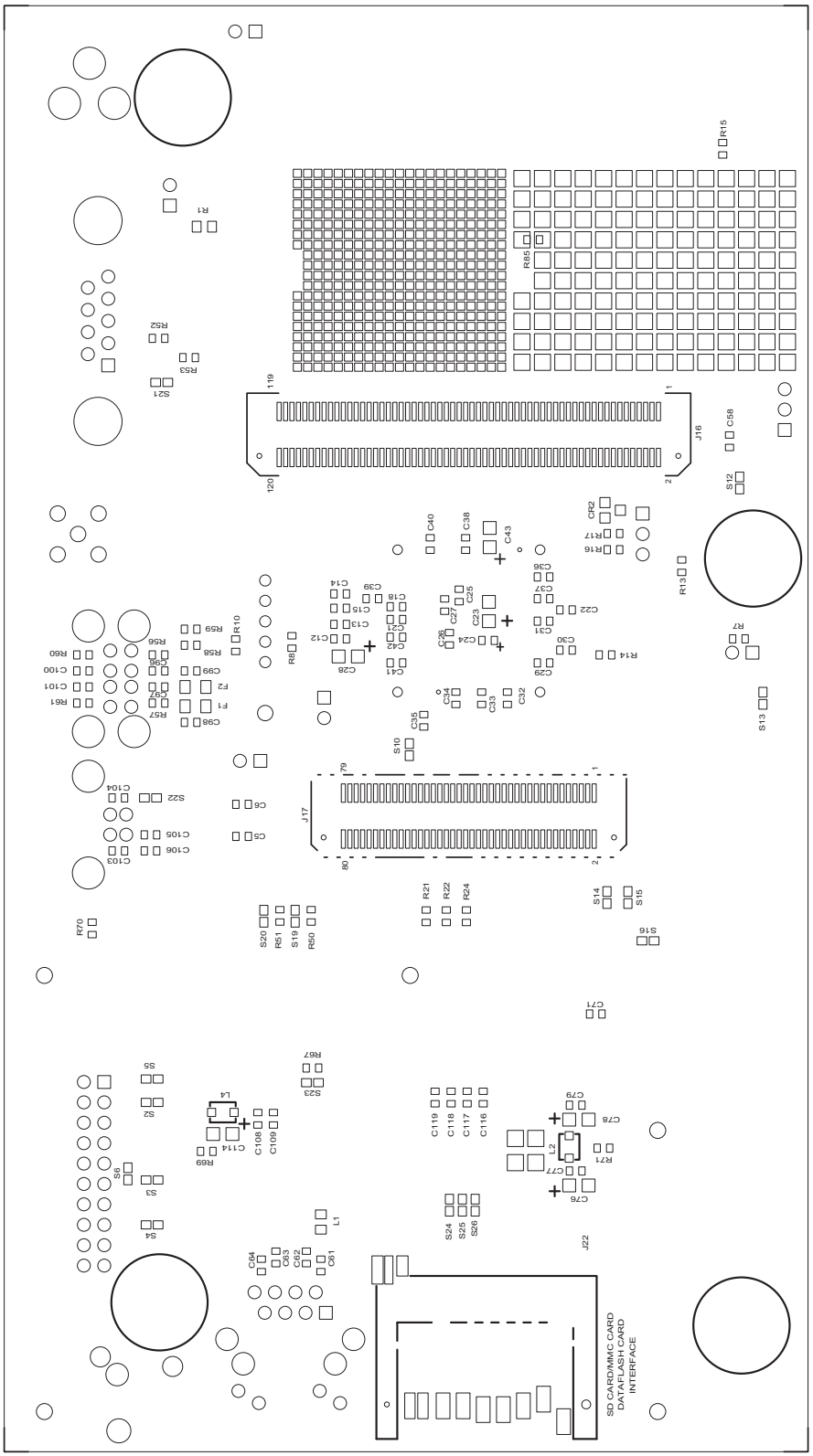


Figure 2-2. AT91SAM9G10-EK Layout - Bottom View



2.4 Powering Up the Board

AT91SAM9G10-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket (J1). The coaxial power plug center pin is positive polarity.

2.5 Backup Power Supply

The user has the possibility to add a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J9 configuration must to be set in position 1, 2.

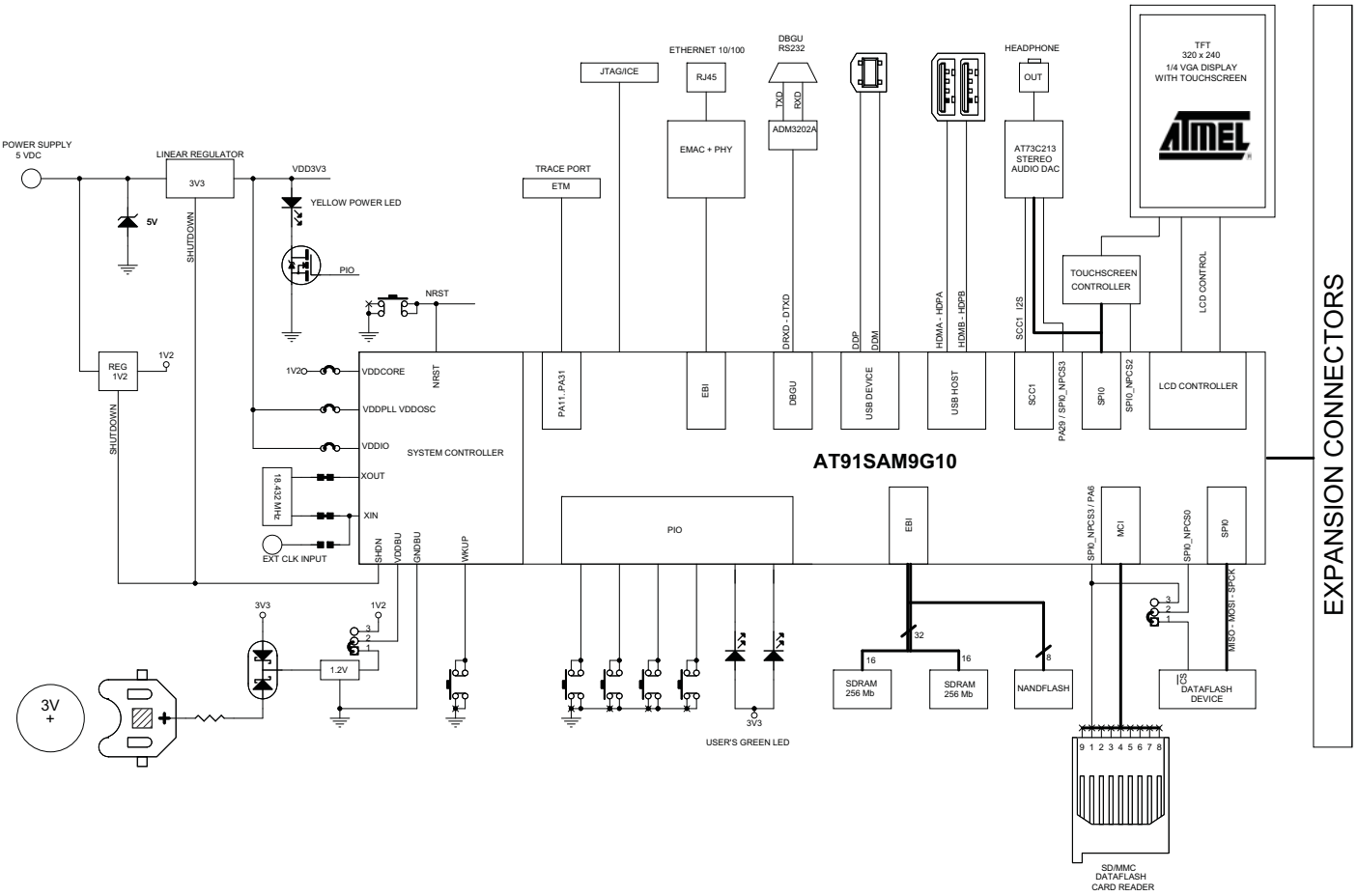
Refer to Table 4-1, “Configuration Jumpers and Straps”.

2.6 Getting Started

The AT91SAM9G10-EK evaluation board is delivered with an embedded demo and documentation files allowing the user to begin evaluating the AT91 ARM Thumb 32-bit microcontroller quickly. Simply power the board and connect it to the USB port of your PC to open it. Also, please refer to the AT91 web site, www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9G10-EK.

2.7 AT91SAM9G10-EK Block Diagram

Figure 2-3. Block Diagram



Section 3

Board Description

3.1 AT91SAM9G10 Microcontroller

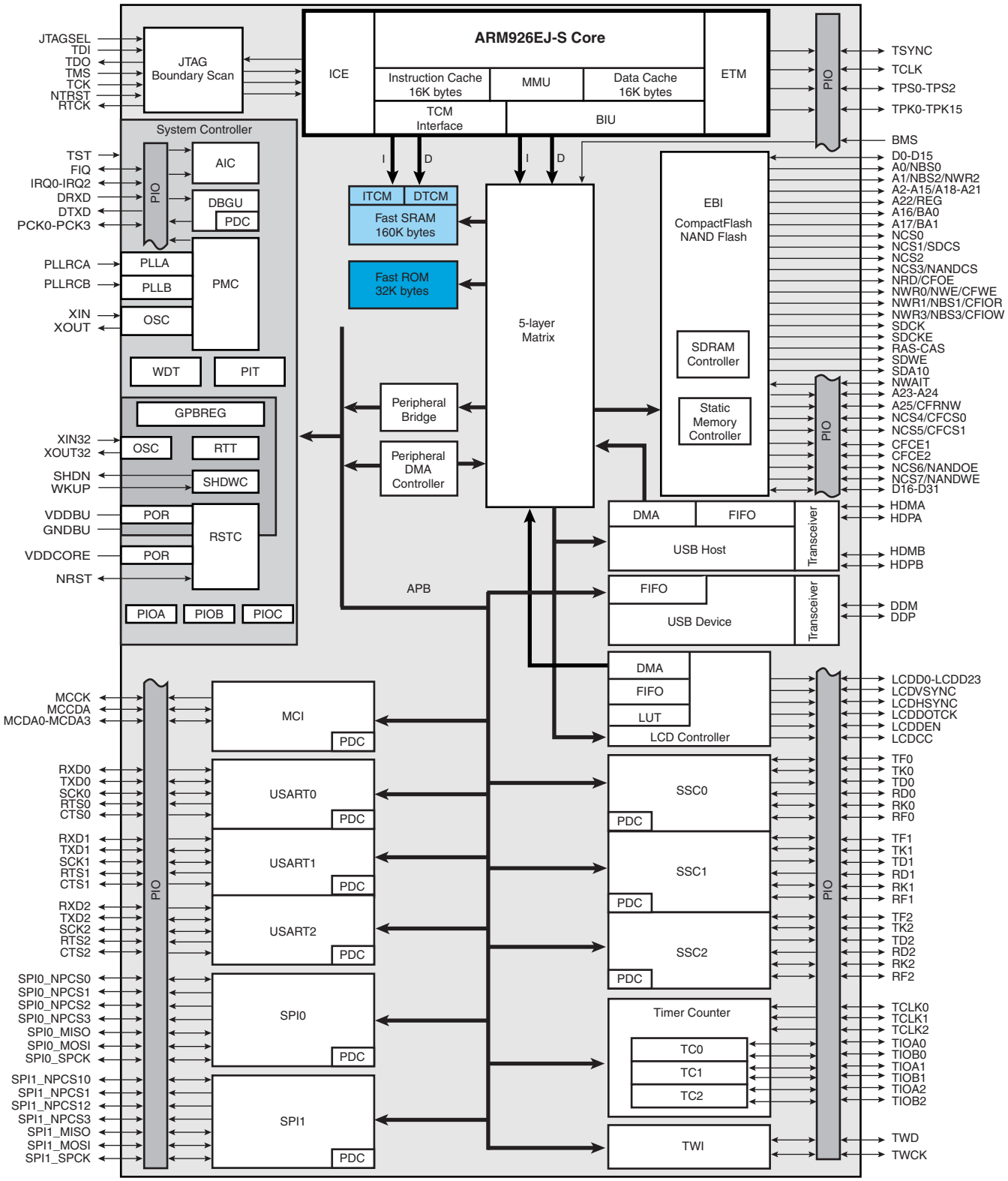
- Incorporates the ARM926EJ-S™ ARM Thumb Processor
  - DSP Instruction Extensions
  - ARM Jazelle® Technology for Java® Acceleration
  - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
  - 266 MHz core frequency
  - Memory Management Unit
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
  - Mid-level implementation Embedded Trace Macrocell™
- Additional Embedded Memories
  - 32K Bytes of Internal ROM, Single-cycle Access at Maximum Bus Speed
  - 160K Bytes of Internal SRAM, Single-cycle Access at Maximum Processor or Bus Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, NAND Flash and CompactFlash®
- LCD Controller
  - RGB Addressing
  - Supports Passive or Active Displays
  - Up to 16-bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode (24-bit per Pixel), Resolution up to 2048 x 2048
- USB
  - USB 2.0 Full Speed (12 Mbits per second) Host Double Port
    Dual On-chip Transceivers
    Integrated FIFOs and Dedicated DMA Channels
  - USB 2.0 Full Speed (12 Mbits per second) Device Port
    On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
- Bus Matrix
  - Handles Five Masters and Five Slaves
  - Boot Mode Select Option
  - Remap Command
- Fully Featured System Controller (SYSC) for Efficient System Management, including
  - Reset Controller, Shutdown Controller, Four 32-bit Battery Backup Registers for a Total of 16 Bytes

  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
  - Three 32-bit PIO Controllers
- Reset Controller (RSTC)
  - Based on Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32.768 kHz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator and two PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire USART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key Protected, Programmable Only Once, Windowed 12-bit Counter, Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock
- Three 32-bit Parallel Input/Output Controllers (PIO) PIOA, PIOB and PIOC
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Nineteen Peripheral DMA (PDC) Channels
- Multimedia Card Interface (MCI)
  - Compliant with Multimedia Cards and SDCards
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation

  - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC and for VDDPLL
  - 2.7V to 3.6V for VDDIOP (Peripheral I/Os)
  - 1.65V to 1.95V and 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 217-ball LFBGA RoHS-compliant Package

3.2 AT91SAM9G10 Block Diagram

Figure 3-1. Block Diagram



3.3 Memory

- 32 Kbytes of Internal ROM
- 160 Kbytes of Internal High-speed SRAM
- Atmel serial DataFlash
- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory

3.4 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- 32.768 kHz standard crystal for the slow clock oscillator

3.5 Reset Circuitry

- Internal reset controller with a bi-directional reset pin
- External reset push button

3.6 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.7 Power Supply Circuitry

- For dynamic power consumption, the AT91SAM9G10 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm
- On-board 1.2V high efficiency step-down charge pump regulator with shutdown control
- On-board 3.3V linear regulator with shutdown control

3.8 Remote Communication

- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
- USB V2.0 Full-speed Compliant, 12 Mbits per second (UDP)
- Two USB Host port V2.0 Full-speed Compliant, 12 Mbits per second (UHP)
- One Ethernet 100-base TX with three status LEDs

3.9 Audio Stereo Interface

- One Atmel stereo audio DAC AT73C213
- One 32 Ohm/20 mW Stereo Headset output (J20) with Master Volume and Mute Controls

3.10 User Interface

- Four user input pushbuttons
- Two user green LEDs
- One yellow power LED (can be also software controlled)
- One ¼ VGA display LCD with Touchscreen and white LED backlight

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM Port

3.12 Expansion Slot

- One DataFlash, SD/MMC card slot
- All I/Os of the AT91SAM9G10 are routed to peripheral extension footprint connectors (J16 and J17). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

3.13 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Comments	
PA0	SPI0_MISO	MCDA0	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_MISO or MCI0_DA0
PA1	SPI0_MOSI	MCCDA	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_MOSI or MCI0_CDA
PA2	SPI0_SPCK	MCCK	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_SPCK or MCCK
PA3	SPI0_NPCS0		DATAFLASH DEVICE or DATAFLASH SOCKET (J9)	SPI0_NPCS0
PA4	SPI0_NPCS1	MCDA1	SD/MMC/DATAFLASH SOCKET (J9)	MCDA1
PA5	SPI0_NPCS2	MCDA2	SD/MMC/DATAFLASH SOCKET (J9)	MCDA2
PA6	SPI0_NPCS3	MCDA3	SD/MMC/DATAFLASH SOCKET (J9)	SPI0_NPCS3 or MCDA3
PA7	TWD	PCK0		
PA8	TWCK	PCK1		
PA9	DRXD	PCK2	SERIAL DEBUG PORT (J15)	DRXD
PA10	DTXD	PCK3	SERIAL DEBUG PORT (J15)	DTXD
PA11	TSYNC	SCK1	TOUCH SCREEN CONTROLLER (MN16) BUSY	PA11
PA12	TCLK	RTS1	TFT PANEL CONTROL (J23) POWER CONTROL IN	PA12
PA13	TPS0	CTS1	GREEN USER'S LED 1 (DS8)	PA13
PA14	TPS1	SCK2	GREEN USER'S LED 2 (DS7)	PA14
PA15	TPS2	RTS2		
PA16	TPK0	CTS2		
PA17	TPK1	TF1	I2S AUDIO DAC AT73C213 (MN15) LRFS	TF1
PA18	TPK2	TK1	I2S AUDIO DAC AT73C213 (MN15) BCLK	TK1
PA19	TPK3	TD1	I2S AUDIO DAC AT73C213 (MN15) SDIN	TD1
PA20	TPK4	RD1		
PA21	TPK5	RK1		
PA22	TPK6	RF1		
PA23	TPK7	RTS0	YELLOW POWER LED CONTROL (DS1)	PA23
PA24	TPK8	SPI1_NPCS1	USER'S PUSH BUTTON INPUT (BP6)	PA24
PA25	TPK9	SPI1_NPCS2	USER'S PUSH BUTTON INPUT (BP5)	PA25
PA26	TPK10	SPI1_NPCS3	USER'S PUSH BUTTON INPUT (BP4)	PA26
PA27	TPK11	SPI0_NPCS1	USER'S PUSH BUTTON INPUT (BP3)	PA27
PA28	TPK12	SPI0_NPCS2	TOUCH SCREEN CONTROLLER (MN16)	SPI0_NPCS2
PA29	TPK13	SPI0_NPCS3	I2S AUDIO DAC AT73C213 (MN15)	SPI0_NPCS3
PA30	TPK14	A23		
PA31	TPK15	A24		

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Comments		
PB0	LCDVSYNC				
PB1	LCDHSYNC		TFT PANEL CONTROL (J23)	LCDHSYNC	
PB2	LCDDOTCK	PCK0	TFT PANEL CONTROL (J23)	LCDDOTCK	
PB3	LCDDEN		TFT PANEL CONTROL (J23)	LCDDEN	
PB4	LCDCC	LCDD2	TFT PANEL CONTROL (J23) BACKLIGHT	LCDCC	
PB5	LCDD0	LCDD3			
PB6	LCDD1	LCDD4			
PB7	LCDD2	LCDD5	TFT PANEL CONTROL (J23)	LCDD2	RED
PB8	LCDD3	LCDD6	TFT PANEL CONTROL (J23)	LCDD3	RED
PB9	LCDD4	LCDD7	TFT PANEL CONTROL (J23)	LCDD4	RED
PB10	LCDD5	LCDD10	TFT PANEL CONTROL (J23)	LCDD5	RED
PB11	LCDD6	LCDD11	TFT PANEL CONTROL (J23)	LCDD6	RED
PB12	LCDD7	LCDD12	TFT PANEL CONTROL (J23)	LCDD7	RED
PB13	LCDD8	LCDD13			
PB14	LCDD9	LCDD14			
PB15	LCDD10	LCDD15	TFT PANEL CONTROL (J23)	LCDD10	GREEN
PB16	LCDD11	LCDD19	TFT PANEL CONTROL (J23)	LCDD11	GREEN
PB17	LCDD12	LCDD20	TFT PANEL CONTROL (J23)	LCDD12	GREEN
PB18	LCDD13	LCDD21	TFT PANEL CONTROL (J23)	LCDD13	GREEN
PB19	LCDD14	LCDD22	TFT PANEL CONTROL (J23)	LCDD14	GREEN
PB20	LCDD15	LCDD23	TFT PANEL CONTROL (J23)	LCDD15	GREEN
PB21	TF0	LCDD16			
PB22	TK0	LCDD17			
PB23	TD0	LCDD18	TFT PANEL CONTROL (J23)	LCDD18	BLUE
PB24	RD0	LCDD19	TFT PANEL CONTROL (J23)	LCDD19	BLUE
PB25	RK0	LCDD20	TFT PANEL CONTROL (J23)	LCDD20	BLUE
PB26	RF0	LCDD21	TFT PANEL CONTROL (J23)	LCDD21	BLUE
PB27	SPI1_NPCS1	LCDD22	TFT PANEL CONTROL (J23)	LCDD22	BLUE
PB28	SPI1_NPCS0	LCDD23	TFT PANEL CONTROL (J23)	LCDD23	BLUE
PB29	SPI1_SPCK	IRQ2	USB DEVICE INTERFACE (J19) USB_CNX	PB29	
PB30	SPI1_MISO	IRQ1			
PB31	SPI1_MOSI	PCK2	I2S AUDIO DAC AT73C213 (MN15) MCLK	PCK2	

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Comments	
PC0	NANDOE	NCS6	NAND FLASH DEVICE (MN6x)	NANDOE
PC1	NANDWE	NCS7	NAND FLASH DEVICE (MN6x)	NANDWE
PC2	NWAIT	IRQ0	TOUCH SCREEN CONTROLLER (MN16) PENIRQ	IRQ0
PC3	A25/CFRNW			
PC4	NCS4/CFCS0			
PC5	NCS5/CFCS1			
PC6	CFCE1			
PC7	CFCE2			
PC8	TXD0	PCK2		
PC9	RXD0	PCK3		
PC10	RTS0	SCK0	ETHERNET CONTROLLER (MN8) RST	PC10
PC11	CTS0	FIQ	ETHERNET CONTROLLER (MN8) IRQ	PC11
PC12	TXD1	NCS6		
PC13	RXD1	NCS7		
PC14	TXD2	SPI1_NPCS2	NAND FLASH DEVICE (MN6x) CHIP ENABLE (CE)	PC14
PC15	RXD2	SPI1_NPCS3	NAND FLASH DEVICE (MN6x) READY/BUSY (R/B)	PC15
PC16	D16	TCLK0	EBI DATA BUS D16	D16
PC17	D17	TCLK1	EBI DATA BUS D17	D17
PC18	D18	TCLK2	EBI DATA BUS D18	D18
PC19	D19	TIOA0	EBI DATA BUS D19	D19
PC20	D20	TIOB0	EBI DATA BUS D20	D20
PC21	D21	TIOA1	EBI DATA BUS D21	D21
PC22	D22	TIOB1	EBI DATA BUS D22	D22
PC23	D23	TIOA2	EBI DATA BUS D23	D23
PC24	D24	TIOB2	EBI DATA BUS D24	D24
PC25	D25	TF2	EBI DATA BUS D25	D25
PC26	D26	TK2	EBI DATA BUS D26	D26
PC27	D27	TD2	EBI DATA BUS D27	D27
PC28	D28	RD2	EBI DATA BUS D28	D28
PC29	D29	RK2	EBI DATA BUS D29	D29
PC30	D30	RF2	EBI DATA BUS D30	D30
PC31	D31	PCK1	EBI DATA BUS D31	D31

Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1 gives details on configuration straps on the AT91SAM9G10-EK evaluation board and their default settings.

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper (1) This jumper footprint is provided for 3.3V power consumption measurement use. By default, it is closed. To use this feature, the user has to open the strap by cutting it before soldering a jumper.
J3	Closed	Forces power on. To use the software shutdown control, J3 must be opened.
J4	Open	Enables Boot on the internal ROM
	Closed	Enables Boot on the NCS0
J8	Closed	VDDPLL Jumper (1)
J9	2-3	VDDBU Jumper select (1) 1-2: Lithium 3V Battery 2-3: 1.2V from VDDCORE
J12	Closed	VDDCORE Jumper (1)
J21	1-2	NPCS0 select 1-2: DataFlash device (MN7) 2-3: DataFlash card interface (J22) **Warning: In this case NPCS03 must be configured as input.**
J24	Closed	Enables the selection of the on-board Nand-Flash device. Remove this jumper to prevent the system boot from that device and to be able to reprogram it.
S2	Open	Disables the ICE NTRST input
S3	Closed	Enables the ICE RTCK return. S6 must be opened
S4	Closed	Enables the ICE NRST input
S5	Open	Selects ICE mode or JTAG mode (See Section 6, Errata)
S6	Open	Disables TCK <-> RTCK local loop. If S6 is closed, S3 must be opened.
S7-S8	Closed	Enables the use of 18.432 MHz crystal. If external clock used, S7-S8 must be opened and S9 closed.
S9	Open	

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
S10	Closed	Enables the use of SDRAM (NCS1_SDCS)
S12	Open	Disables Serial DataFlash write protect.
S13	Closed	Disables NAND FLASH write protect.
S14	Closed	Enables the use of interrupt ETHERNET MAC (PC11_FIQ).
S15	Closed	Enables the use of ETHERNET MAC (NCS2).
S16	Open	Disables the use of NWAIT ETHERNET MAC signal (PC2_NWAIT)
S19	Closed	Enables the use of the User LED DS7 (PA14)
S20	Closed	Enables the use of the User LED DS8 (PA13)
S21	Closed	Enables the use of the DBGU RXD signal (PA9)
S22	Closed	Enables the use of the USB CNX detection (PB29)
S23	Closed	Enables the use of AUDIO DAC INTERFACE (NPCS03)
S24	Closed	Enables the use of TOUCH SCREEN CONTROLLER (NPCS02)
S25	Closed	Enables the use of TOUCH SCREEN CONTROLLER BUSY signal (PA11)
S26	Closed	Enables the use of TOUCH SCREEN CONTROLLER PENIRQ (PC2_IRQ0)
TP1	N.A	3.3V Test point.
TP2	N.A	GND Test point.
TP3	N.A	1.2V Test point.
TP4	N.A	GND Test point.
TP63	N.A	0 to 3.3V analog user's input
TP64	N.A	0 to 3.3V analog user's input
TP65	N.A	AGND of TP63
TP66	N.A	AGND of TP64

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Power Supply and Audio
- AT91SAM9G10 Device
- SDRAM and NAND Flash
- Ethernet
- LCD and User Interface
- Serial and I/O Expansion











5 V

AUDIO DAC INTERFACE

SHEET 2

POWER

PIO A,B,C

DEBUG PORT

HOST

DEVICE

USB INTERFACES

EXPANSION CONNECTORS

SHEET 7

PIO A,B,C

LCD

TOUCH SCREEN CONTROLLER

USER INTERFACE



SHEET 6

PIO A,B,C

ATMEL
ARM9 Processor
SAM9G10 (LFBGA217)

ICE INTERFACE

SHEET 3

EBI SDRAM INTERFACE

DATA BUS

ADRESSE BUS

PIO A,B,C

DATA BUS

EBI SDRAM

SDRAM

NAND FLASH

SERIAL DATA FLASH

CARD READER

MMC/SD DATAFASH CARD

SHEET 4

ETHERNET

SHEET 5







PIO MUXING									
PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE
PA0	SPI0_MISO /MCDA0	PA16	--	PB0	--	PB16	G1	PC0	NANDOE
PA1	SPI0_MOSI /MCCDA	PA17	TF1	PB1	LCDHSYNC	PB17	G2	PC1	NANDWE
PA2	SPI0_SPCK	PA18	TK1	PB2	LCDDDOTCK	PB18	G3	PC2	IRQ0 /NWAIT
PA3	SPI0_NPCS0	PA19	TD1	PB3	LCDDEN	PB19	G4	PC3	--
PA4	MCDA1	PA20	--	PB4	LCDCC	PB20	G5	PC4	--
PA5	MCDA2	PA21	--	PB5	--	PB21	--	PC5	--
PA6	SPI0_NPCS3 MCDA3	PA22	--	PB6	--	PB22	--	PC6	--
PA7	--	PA23	POWER LED	PB7	R0	PB23	B0	PC7	--
PA8	--	PA24	BP6	PB8	R1	PB24	B1	PC8	--
PA9	DBGU_RXD	PA25	BP5	PB9	R2	PB25	B2	PC9	--
PA10	DBGU_TXD	PA26	BP4	PB10	R3	PB26	B3	PC10	RST
PA11	BUSY	PA27	BP3	PB11	R4	PB27	B4	PC11	FIQ
PA12	POWER CONTROL IN	PA28	SPI0_NPCS2	PB12	R5	PB28	B5	PC12	--
PA13	USER LED	PA29	SPI0_NPCS3	PB13	--	PB29	USB_CNX	PC13	--
PA14	USER LED	PA30	--	PB14	--	PB30	USB_DP_PUP	PC14	#CE
PA15	--	PA31	--	PB15	G0	PB31	PCK2	PC15	R/#B

NOTE

"DNP" means the component is not populated by default

REV	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	PP	15MAY09	XXX	XX/XX/XX

AT91SAM9G10-EK

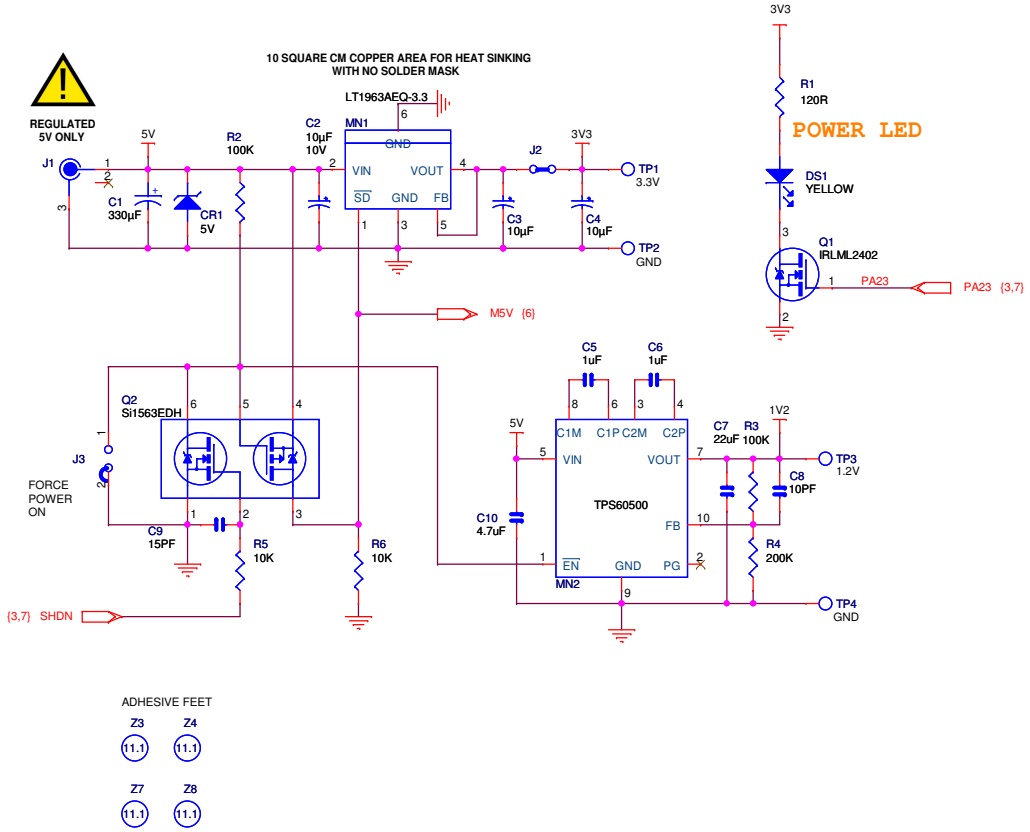
TOP LEVEL

SCALE 1/1

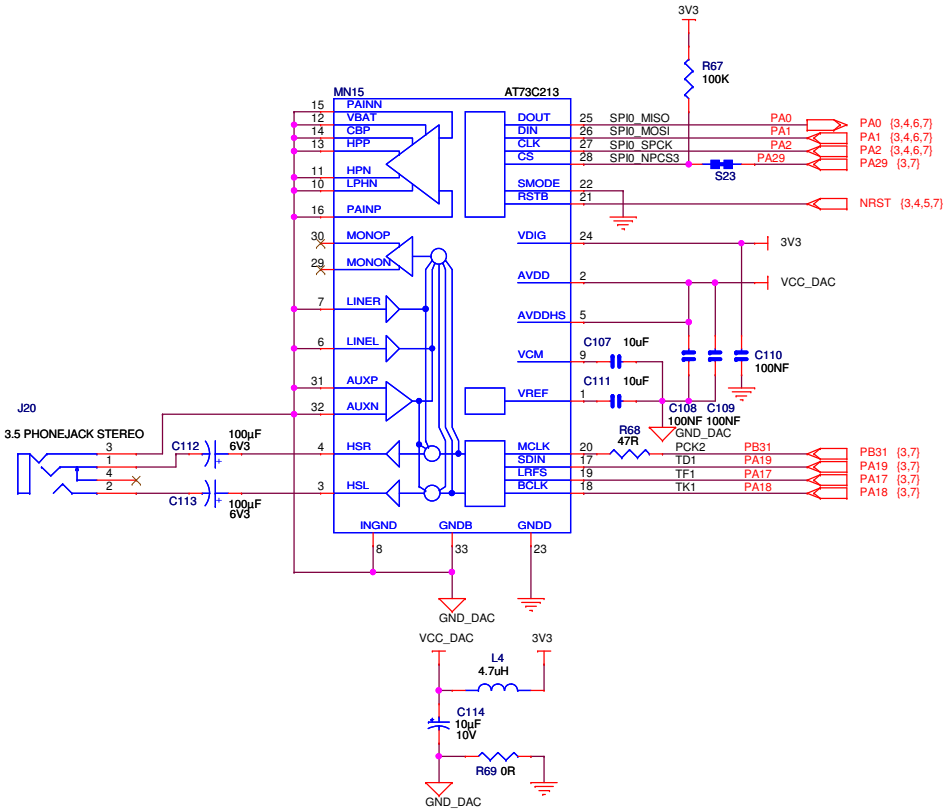
REV. A

SHEET 1/7

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AUDIO DAC INTERFACE



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REV	MODIF.	DES.	DATE	VER.	DATE

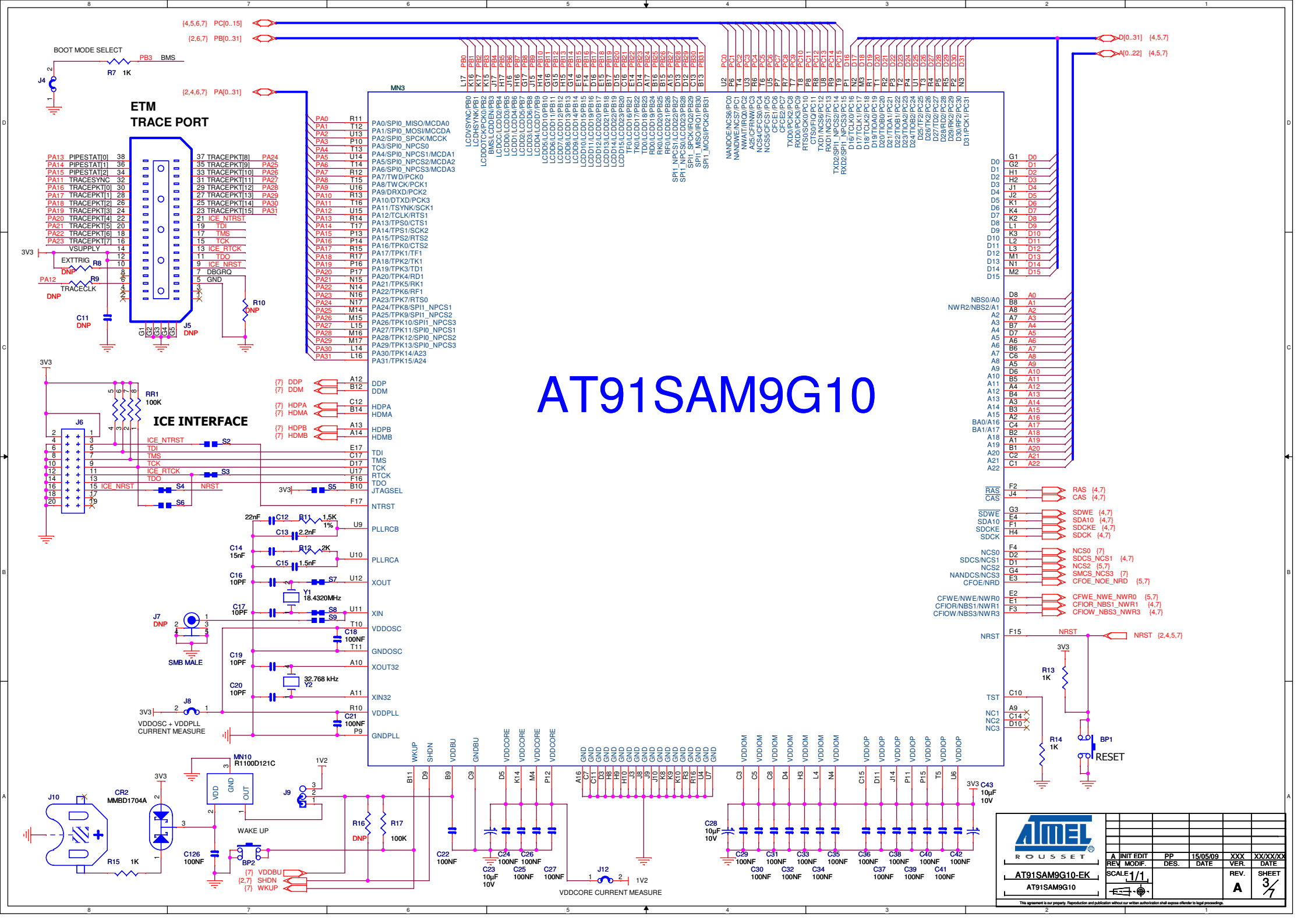
AT91SAM9G10-EK
POWER SUPPLY & AUDIO

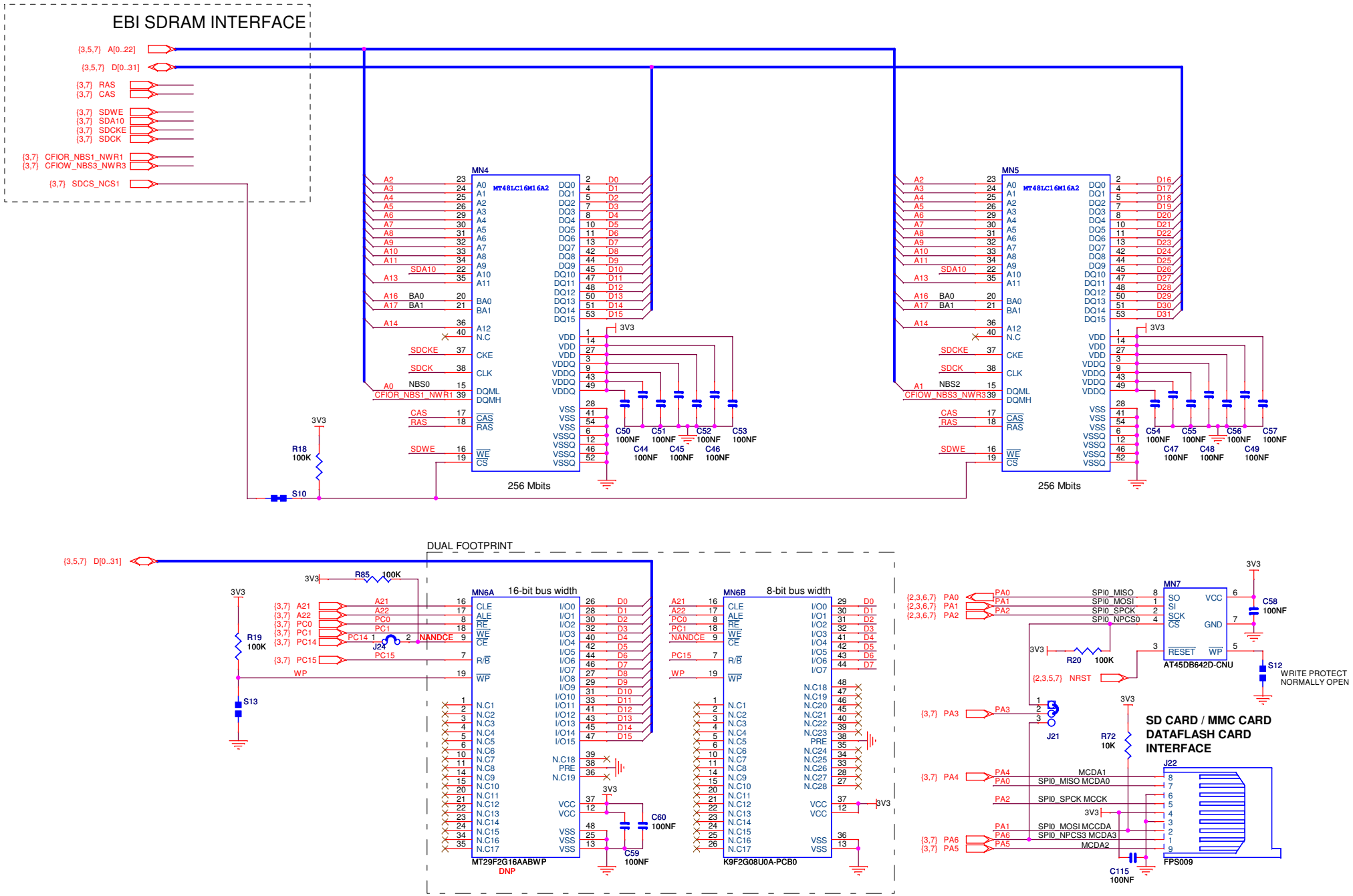
SCALE 1/1

REV. A

SHEET 2/7

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AT91SAM9G10
ETM
TRACE PORT
ICE INTERFACE
BOOT MODE SELECT
VDDOSC + VDDPLL
CURRENT MEASURE
VDDCORE CURRENT MEASURE
WAKE UP
SMB MALE
RESET
ATMEL
ROUSSET
AT91SAM9G10-EK
AT91SAM9G10
SCALE 1/1
REV. A
SHEET 3/7



A	INIT EDIT	PP	15MAY09	XXX	XX/XX/XX
REV	MODIF.	DES.	DATE	VER.	DATE

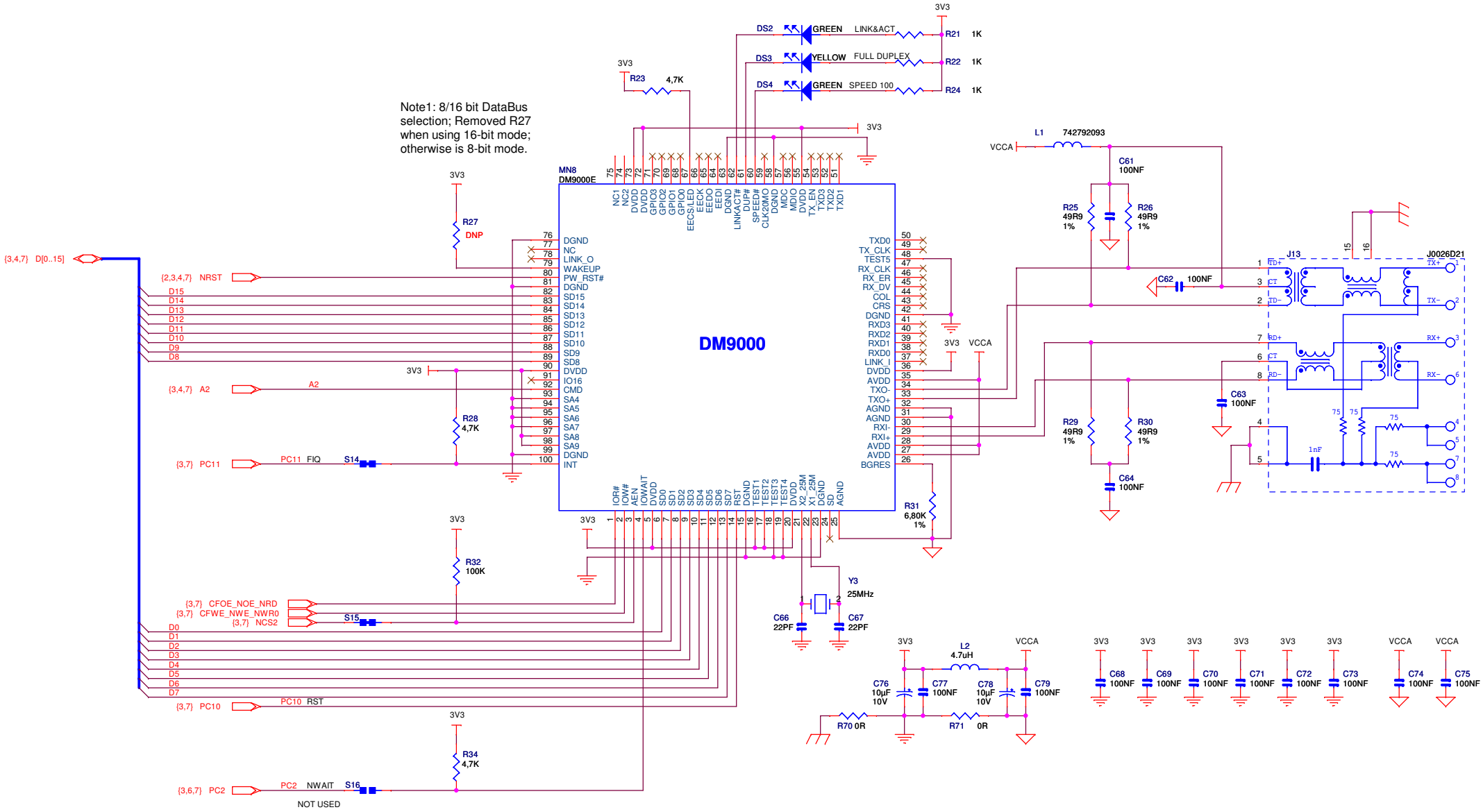
AT91SAM9G10-EK
SDRAM & NANDFLASH

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REV. A

SHEET 4/7

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A	INIT EDIT	PP	15MAY09	XXX	XX/XX/XX
REV.	MODIF.	DES.	DATE	VER.	DATE

AT91SAM9G10-EK

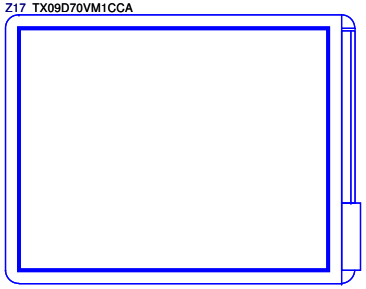
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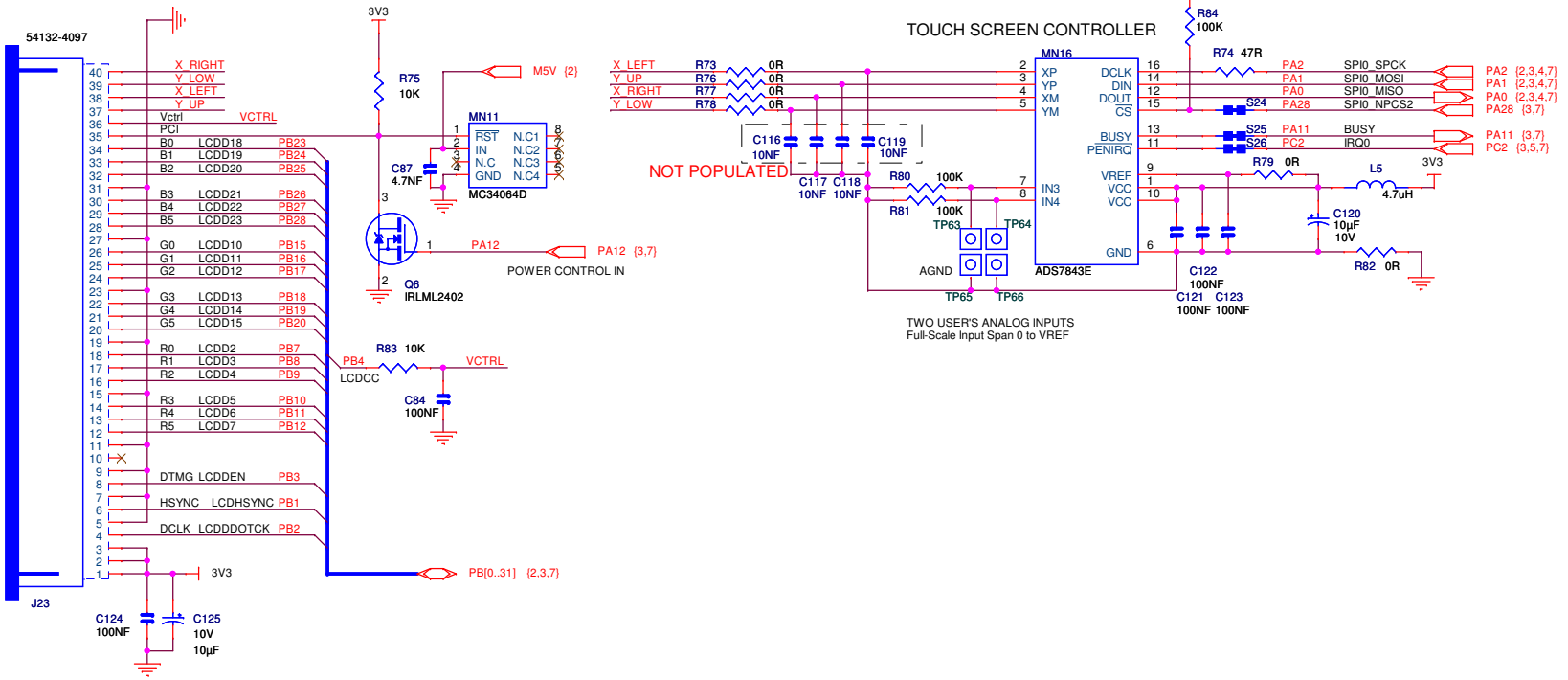
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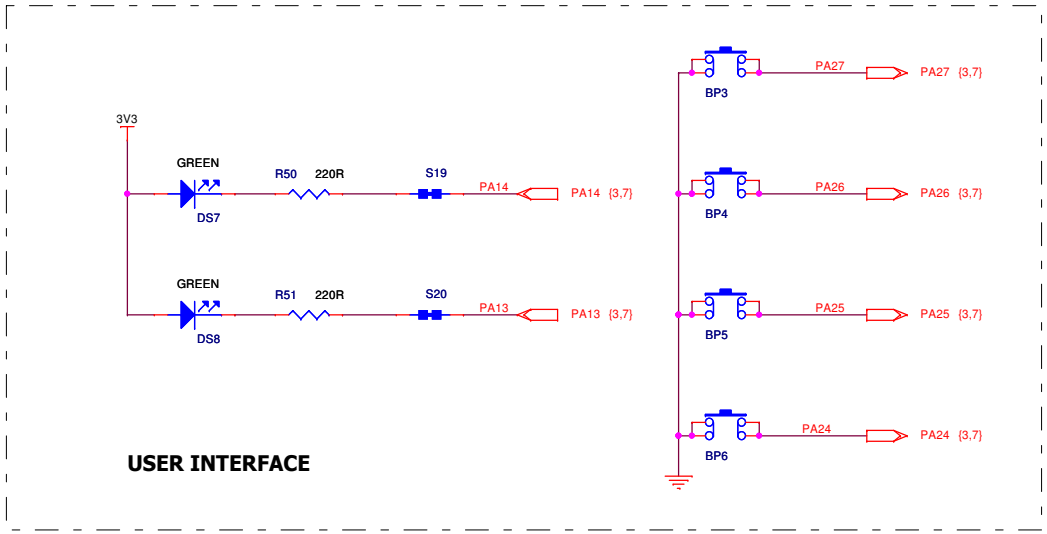
REV. A

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REV	MODIF.	DES.	DATE	VER.	DATE

AT91SAM9G10-EK

LCD_USER'S INTERFACE

SCALE 1/1

REV. A

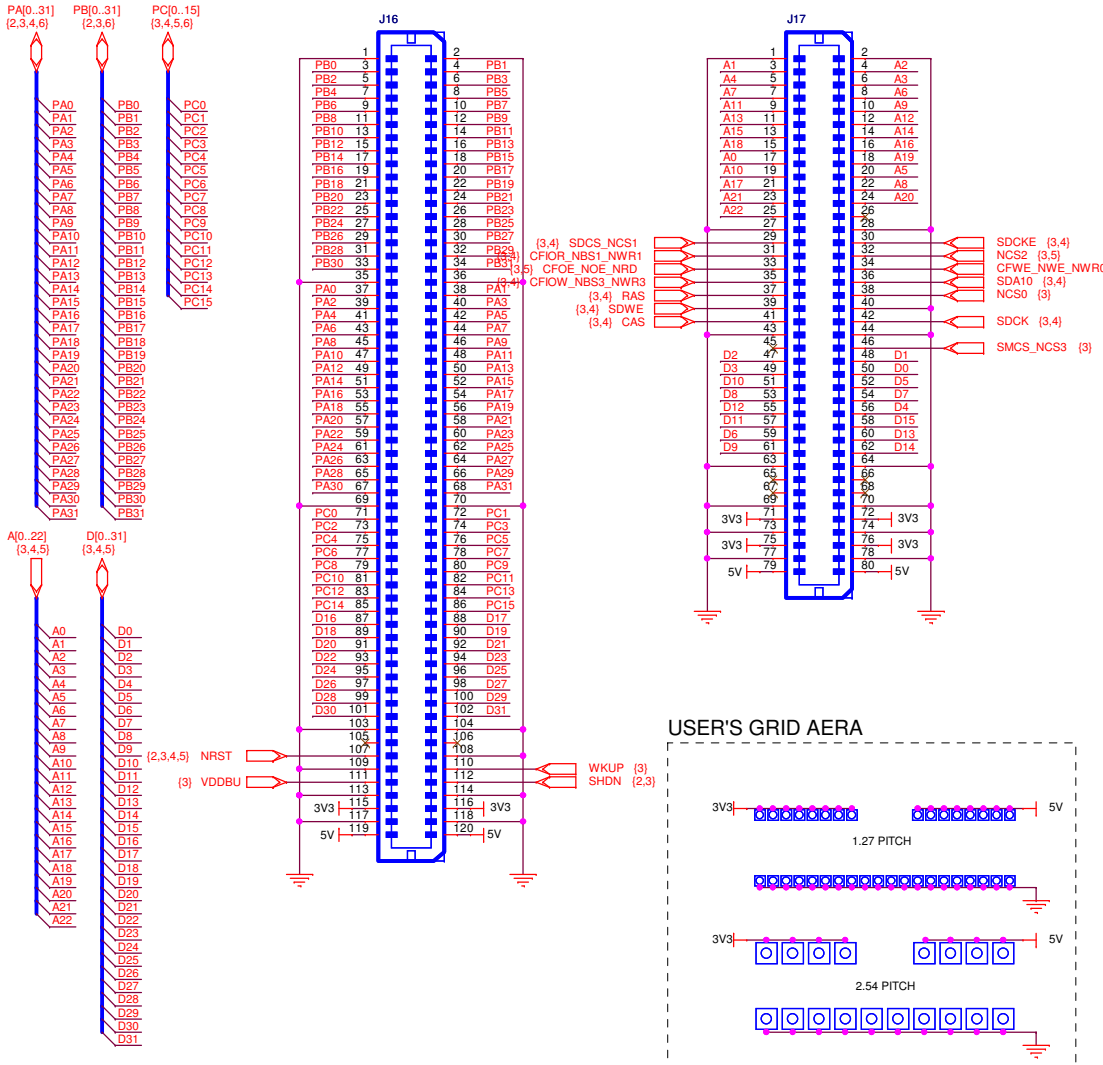
SHEET 6/7

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EXPANSION CONNECTORS

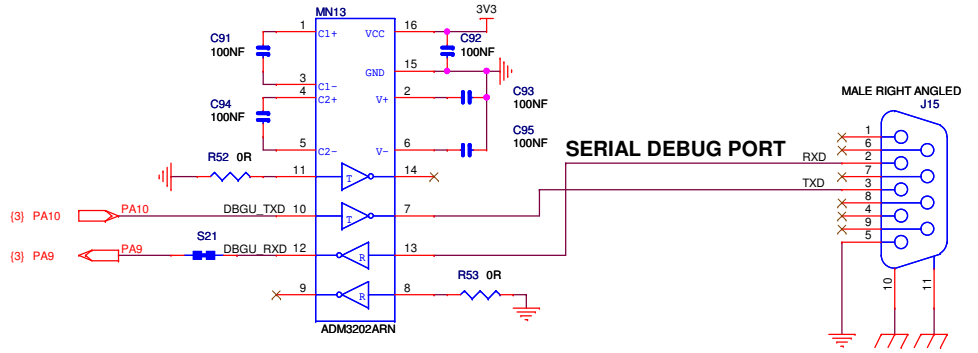
NOT POPULATED

NOT POPULATED

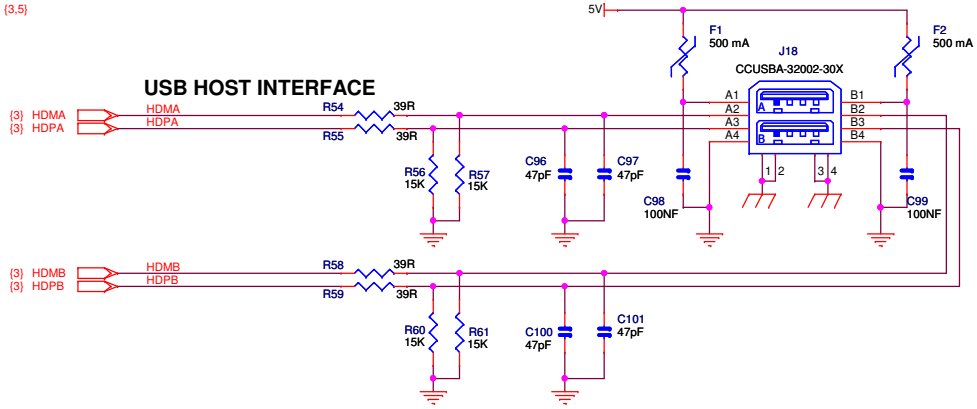


USER'S GRID AERA

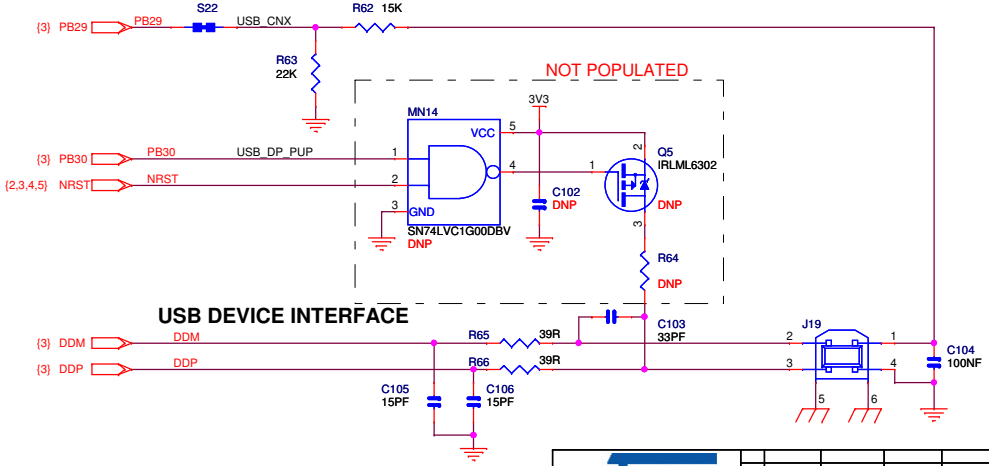
SERIAL DEBUG PORT



USB HOST INTERFACE



USB DEVICE INTERFACE



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Section 6

Errata

6.1 JTAGSEL S5 Footprint Selector

For JTAG selection, the S5 footprint must never be soldered, otherwise the chip can be damaged.

By default, the JTAGSEL input pin integrates a pull-down resistor (ICE mode).

To select JTAG mode, the designer should connect the JTAGSEL input pin to VDDBU power.

6.2 External Capacitor Values on XIN and XOUT

The external capacitor values on XIN and XOUT are not correct.

The 10 pF capacitors must be replaced by 22 pF capacitors.

Please refer to the electrical parameters section of the datasheet.

Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6479A	First issue.	

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

Technical Support
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