Features

- Incorporates the ARM7TDMI™ ARM Thumb Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-circuit Emulation)
- 136K Bytes On-chip SRAM
  - 32-bit Data Bus
  - Single-clock Cycle Access
- Fully-programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - Up to 8 Chip Selects
  - Software-programmable 8/16-bit External Databus
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 4 External Interrupts, Including a High-priority Low-latency Interrupt Request
- 32 Programmable I/O Lines
- 3-channel 16-bit Timer/Counter
  - 3 External Clock Inputs
  - 2 Multi-purpose I/O Pins per Channel
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Programmable Watchdog Timer
- Advanced Power-saving Features
  - CPU and Peripheral Can Be Deactivated Individually
- Fully Static Operation:
  - 0 Hz to 33 MHz Internal Frequency Range at 3.0V, 85°C
- 1.8V to 3.6V Operating Range
- -40°C to +85°C Temperature Range
- Available in a 100-lead TQFP Package

Description

The AT91R40807 microcontroller is a member of the Atmel AT91 16/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

The AT91R40807 microcontroller features a direct connection to off-chip memory, including Flash, through the fully-programmable External Bus Interface (EBI). An eight-level priority vectored interrupt controller, in conjunction with the Peripheral Data Controller, significantly improves the real-time performance of the device.

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with a large on-chip high-speed SRAM and a wide range of peripheral functions on a monolithic chip, the AT91R40807 is a powerful microcontroller that offers a flexible and high-performance solution to many compute-intensive embedded control applications.

AT91 ARM® Thumb® Microcontrollers

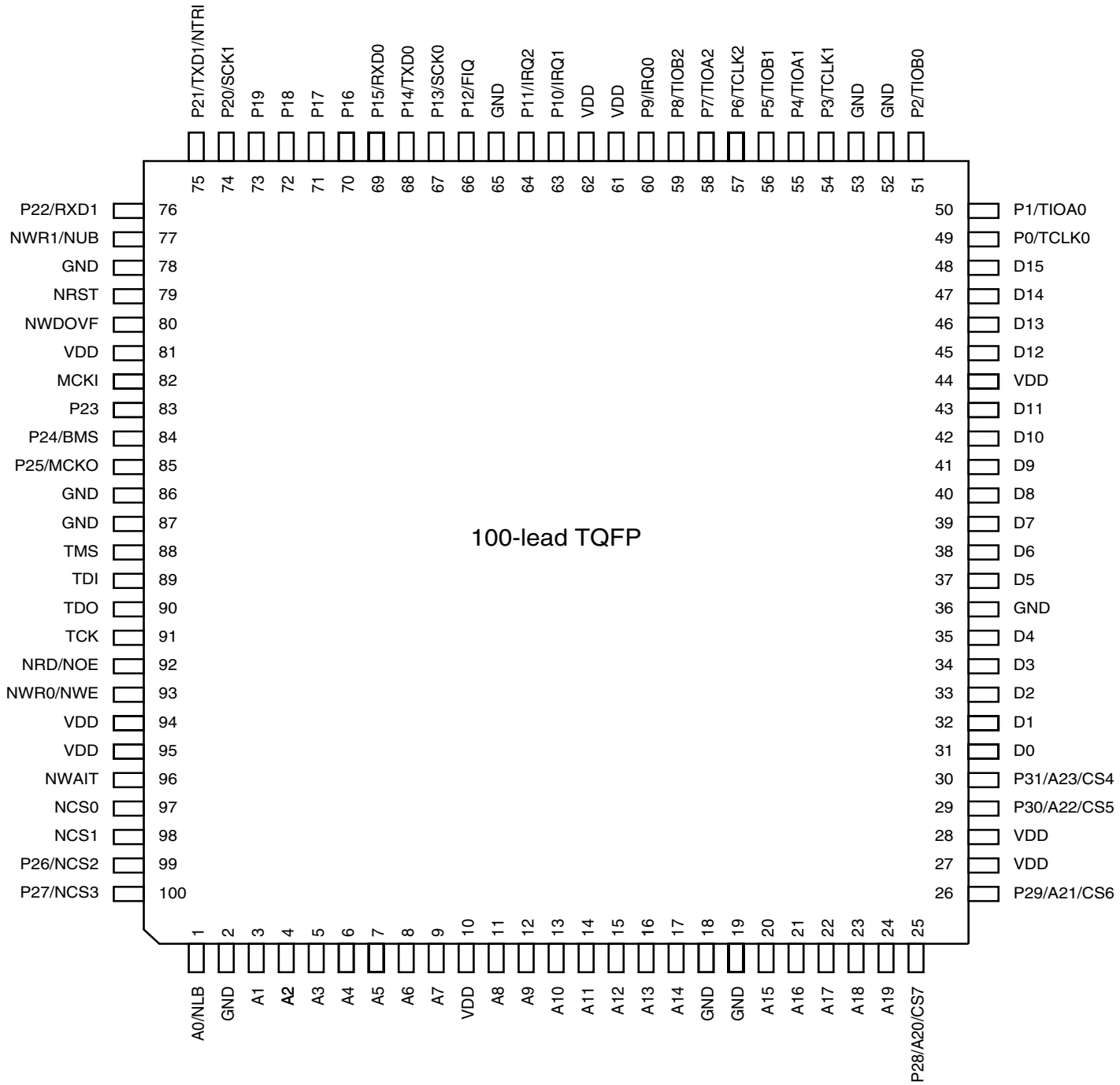
AT91R40807 Summary

Rev. 1345DS–ATARM–02/02

Note: This is a summary document. A complete document is available on our web site at www.atmel.com.

Pin Configuration

Figure 1. AT91R40807 Pinout (Top View)



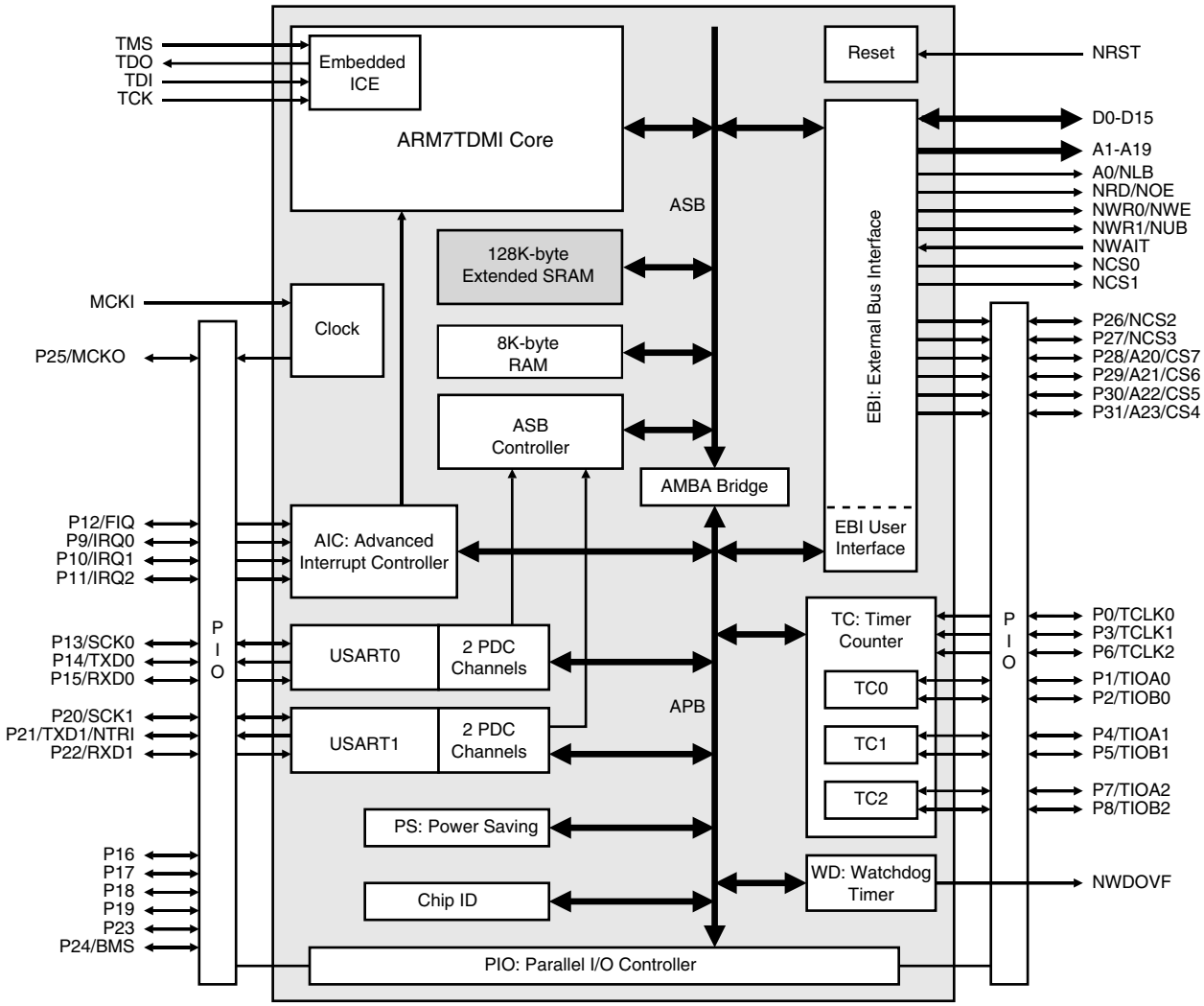
Pin Description

Table 1. AT91R40807 Pin Description

Module	Name	Function	Type	Active Level	Comments
EBI	A0 - A23	Address Bus	Output	–	All valid after reset
	D0 - D15	Data Bus	I/O	–	
	NCS0 - NCS3	Chip Select	Output	Low	
	CS4 - CS7	Chip Select	Output	High	A23 - A20 after reset
	NWR0	Lower Byte 0 Write Signal	Output	Low	Used in Byte Write option
	NWR1	Upper Byte 1 Write Signal	Output	Low	Used in Byte Write option
	NRD	Read Signal	Output	Low	Used in Byte Write option
	NWE	Write Enable	Output	Low	Used in Byte Select option
	NOE	Output Enable	Output	Low	Used in Byte Select option
	NUB	Upper Byte Select	Output	Low	Used in Byte Select option
	NLB	Lower Byte Select	Output	Low	Used in Byte Select option
	NWAIT	Wait Input	Input	Low	
	BMS	Boot Mode Select	Input	–	Sampled during reset
AIC	FIQ	Fast Interrupt Request	Input	–	PIO-controlled after reset
	IRQ0 - IRQ2	External Interrupt Request	Input	–	PIO-controlled after reset
TC	TCLK0 - TCLK2	Timer External Clock	Input	–	PIO-controlled after reset
	TIOA0 - TIOA2	Multipurpose Timer I/O pin A	I/O	–	PIO-controlled after reset
	TIOB0 - TIOB2	Multipurpose Timer I/O pin B	I/O	–	PIO-controlled after reset
USART	SCK0 - SCK1	External Serial Clock	I/O	–	PIO-controlled after reset
	TXD0 - TXD1	Transmit Data Output	Output	–	PIO-controlled after reset
	RXD0 - RXD1	Receive Data Input	Input	–	PIO-controlled after reset
PIO	P0 - P31	Parallel I/O Line	I/O	–	
WD	NWDOVF	Watchdog overflow	Output	Low	Open-drain
Clock	MCKI	Master Clock Input	Input	–	Schmidt trigger
	MCKO	Master Clock Output	Output	–	
Reset	NRST	Hardware Reset Input	Input	Low	Schmidt trigger
	NTRI	Tri-state Mode Select	Input	Low	Sampled during reset
ICE	TMS	Test Mode Select	Input	–	Schmidt trigger, internal pull-up
	TDI	Test Data Input	Input	–	Schmidt trigger, internal pull-up
	TDO	Test Data Output	Output	–	
	TCK	Test Clock	Input	–	Schmidt trigger, internal pull-up
Power	VDD	Power	Power	–	
	GND	Ground	Ground	–	

Block Diagram

Figure 2. AT91R40807



Architectural Overview

The AT91R40807 microcontroller integrates an ARM7TDMI with Embedded ICE interface, memories and peripherals. The architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). Designed for maximum performance and controlled by the memory controller, the ASB interfaces the ARM7TDMI processor with the on-chip 32-bit memories, the External Bus Interface (EBI) and the AMBA™ Bridge. The AMBA Bridge drives the APB, which is designed for accesses to on-chip peripherals and optimized for low power consumption.

The AT91R40807 microcontroller implements the ICE port of the ARM7TDMI processor on dedicated pins, offering a complete, low-cost and easy-to-use debug solution for target debugging.

Memories

The AT91R40807 microcontroller embeds 136K bytes of internal SRAM. The internal memory is directly connected to the 32-bit data bus and is single-cycle accessible. This provides maximum performance of 36 MIPS at 40 MHz by using the ARM instruction set of the processor, minimizing system power consumption and improving on the performance of separate memory solutions.

The AT91R40807 microcontroller features an External Bus Interface (EBI), which enables connection of external memories and application-specific peripherals. The EBI supports 8- or 16-bit devices and can use two 8-bit devices to emulate a single 16-bit device. The EBI implements the early read protocol, enabling faster memory accesses than standard memory interfaces.

Peripherals

The AT91R40807 microcontroller integrates several peripherals, which are classified as system or user peripherals. All on-chip peripherals are 32-bit accessible by the AMBA Bridge, and can be programmed with a minimum number of instructions. The peripheral register set is composed of control, mode, data, status and enable/disable/status registers.

An on-chip Peripheral Data Controller (PDC) transfers data between the on-chip USARTs and on- and off-chip memories address space without processor intervention. Most importantly, the PDC removes the processor interrupt handling overhead, making it possible to transfer up to 64K contiguous bytes without reprogramming the start address, thus increasing the performance of the microcontroller, and reducing the power consumption.

System Peripherals

The External Bus Interface (EBI) controls the external memory or peripheral devices via an 8- or 16-bit data bus and is programmed through the APB. Each chip select line has its own programming register.

The Power-saving (PS) module implements the Idle mode (ARM7TDMI core clock stopped until the next interrupt) and enables the user to adapt the power consumption of the microcontroller to application requirements (independent peripheral clock control).

The Advanced Interrupt Controller (AIC) controls the internal interrupt sources from the internal peripherals and the four external interrupt lines (including the FIQ), to provide an interrupt and/or fast interrupt request to the ARM7TDMI. It integrates an 8-level priority controller and, using the Auto-vectoring feature, reduces the interrupt latency time.

The Parallel Input/Output Controller (PIO) controls up to 32 I/O lines. It enables the user to select specific pins for on-chip peripheral input/output functions, and general-purpose input/output signal pins. The PIO controller can be programmed to detect an interrupt on a signal change from each line.

The Watchdog (WD) can be used to prevent system lock-up if the software becomes trapped in a deadlock.

The Special Function (SF) module integrates the Chip ID, the Reset Status and the Protect registers.

User Peripherals

Two USARTs, independently configurable, enable communication at a high baud rate in synchronous or asynchronous mode. The format includes start, stop and parity bits and up to 8 data bits. Each USART also features a Timeout and a Time Guard register, facilitating the use of the two dedicated Peripheral Data Controller (PDC) channels.

The 3-channel, 16-bit Timer Counter (TC) is highly-programmable and supports capture or waveform modes. Each TC channel can be programmed to measure or generate different kinds of waves, and can detect and control two input/output signals. The TC has also three external clock signals.

Associated Documentation

The AT91R40807 is a part of the AT91X40 Series microcontrollers, a member of the Atmel AT91 16/32-bit microcontroller family which is based on the ARM7TDMI processor core. Table 2 contains details of associated documentation for further reference.

Table 2. Associated Documentation

Product	Information	Document Title
AT91R40807	Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI (Thumb) Datasheet
	External memory interface mapping Peripheral operations Peripheral user interfaces	AT91x40 Series Datasheet
	DC characteristics Power consumption Thermal and reliability considerations AC characteristics	AT91R40807 Electrical Characteristics
	Product overview Ordering information Packaging information Soldering profile	AT91R40807 Summary Datasheet (this document)

Product Overview

Power Supply

The AT91R40807 microcontroller has a unique type of power supply pin – VDD. The VDD pin supplies the I/O pads and the device core. The supported voltage range on V_{DD} is 1.8V to 3.6V.

Input/Output Considerations

The AT91R40807 accepts voltage levels up to the power supply limit on the pads.

After the reset, the peripheral I/Os are initialized as inputs to provide the user with maximum flexibility. It is recommended that in any application phase the inputs to the AT91R40807 microcontroller be held at valid logic levels to minimize the power consumption.

Master Clock

The AT91R40807 microcontroller has a fully static design and work on the Master Clock (MCK), provided on the MCKI pin from an external source.

The Master Clock is also provided as an output of the device on the pin MCKO, which is multiplexed with a general-purpose I/O line. While NRST is active, MCKO remains low. After the reset, the MCKO is valid and outputs an image of the MCK signal. The PIO controller must be programmed to use this pin as standard I/O line.

Reset

Reset restores the default states of the user interface registers (defined in the user interface of each peripheral), and forces the ARM7TDMI to perform the next instruction fetch from address zero. Except for the program counter the ARM7TDMI registers do not have defined reset states.

NRST Pin

NRST is active low-level input. It is asserted asynchronously, but exit from reset is synchronized internally to the MCK. The signal presented on MCKI must be active within the specification for a minimum of 10 clock cycles up to the rising edge of NRST to ensure correct operation.

The first processor fetch occurs 80 clock cycles after the rising edge of NRST.

Watchdog Reset

The watchdog can be programmed to generate an internal reset. In this case, the reset has the same effect as the NRST pin assertion, but the pins BMS and NTRI are not sampled. Boot mode and Tri-state mode are not updated. If the NRST pin is asserted and the Watchdog triggers the internal reset, the NRST pin has priority.

Emulation Functions

Tri-state Mode

The AT91R40807 provides a Tri-state mode, which is used for debug purposes. This enables the connection of an emulator probe to an application board without having to desolder the device from the target board. In Tri-state mode, all the output pin drivers of the AT91R40807 microcontroller are disabled.

To enter Tri-state mode, the pin NTRI must be held low during the last 10 clock cycles before the rising edge of NRST. For normal operation the pin NTRI must be held high during reset, by a resistor of up to 400K Ohm.

NTRI is multiplexed with I/O line P21 and USART 1 serial data transmit line TXD1.

Standard RS232 drivers generally contain internal 400K Ohm pull-up resistors. If TXD1 is connected to a device not including this pull-up, the user must make sure that a high-level is tied on NTRI while NRST is asserted.

JTAG/ICE Debug

ARM Standard Embedded In-circuit Emulation is supported via the JTAG/ICE port. The pins TDI, TDO, TCK and TMS are dedicated to this debug function and can be connected to a host computer via the external ICE interface.

In ICE Debug mode, the ARM7TDMI core responds with a non-JTAG chip ID that identifies the microcontroller. This is not fully IEEE1149.1 compliant.

Memory Controller

The ARM7TDMI processor address space is 4G bytes. The memory controller decodes the internal 32-bit address bus and defines three address spaces:

- Internal memories in the four lowest megabytes
- Middle space reserved for the external devices (memory or peripherals) controlled by the EBI
- Internal peripherals in the four highest megabytes

In any of these address spaces, the ARM7TDMI operates in Little-Endian mode only.

Internal Memories

The AT91R40807 microcontroller integrates 8K bytes of primary internal SRAM. All internal memories are 32 bits wide and single-clock cycle accessible. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one cycle. Fetching Thumb or ARM instructions is supported and internal memory can store twice as many Thumb instructions as ARM ones.

The primary SRAM bank is mapped at address 0x0 (after the remap command), allowing ARM7TDMI exception vectors between 0x0 and 0x20 to be modified by the software. The rest of the bank can be used for stack allocation (to speed up context saving and restoring) or as data and program storage for critical algorithms.

The AT91R40807 also integrates an extended memory bank of 128K bytes at address 0x0010 0000. Placing the SRAM on-chip and using the 32-bit data bus bandwidth maximizes the microcontroller performance and minimizes the system power consumption. The 32-bit bus increases the effectiveness of the use of the ARM instruction set, and the ability of processing data that is wider than 16-bit, thus making optimal use of the ARM7TDMI advanced performance.

Being able to dynamically update application software in the 128-Kbyte SRAM adds an extra dimension to the AT91R40807. This 128-Kbyte SRAM can also be used to validate the code to be stored in the on-chip ROM memory prior to mass production of the AT91M40807. At system boot, the code is downloaded from external nonvolatile memory to this on-chip extended SRAM. In order to prevent accidental write to the extended SRAM during the ROM emulation, a write detection feature has been implemented.

The AT91R40807 microcontroller ROM version (AT91M40807) integrates 128K bytes of internal ROM at address 0x0010 0000. The ROM version offers a reduced-cost option for high-volume applications in which the software is stable.

Boot Mode Select

The ARM reset vector is at address 0x0. After the NRST line is released, the ARM7TDMI executes the instruction stored at this address. This means that this address must be mapped in nonvolatile memory after the reset.

The input level on the BMS pin during the last 10 clock cycles before the rising edge of the NRST selects the type of boot memory. The Boot Mode depends on BMS (see Table 3).

The AT91R40807 supports boot in on-chip extended SRAM, for the purpose of emulating ROM versions. In this case, the microcontroller must first boot from external nonvolatile memory, and ensure that a valid program is downloaded in the on-chip

extended SRAM. Then, the NRST must be reasserted by external circuitry after the level on the pin BMS is changed.

The pin BMS is multiplexed with the I/O line P24 that can be programmed after reset like any standard PIO line.

Table 3. Boot Mode Select

BMS	Boot Memory
1	Internal 32-bit extended SRAM
0	External 16-bit memory on NCS0

Remap Command

The ARM vectors (Reset, Abort, Data Abort, Prefetch Abort, Undefined Instruction, Interrupt, Fast Interrupt) are mapped from address 0x0 to address 0x20. In order to allow these vectors to be redefined dynamically by the software, the AT91R40807 Microcontrollers use a remap command that enables switching between the boot memory and the internal primary SRAM bank addresses. The remap command is accessible through the EBI User Interface, by writing one in RCB of EBI_RCR (Remap Control Register). Performing a remap command is mandatory if access to the other external devices (connected to chip-selects 1 to 7) is required. The remap operation can only be changed back by an internal reset or an NRST assertion.

Abort Control

The abort signal providing a Data Abort or a Prefetch Abort exception to the ARM7TDMI is asserted when accessing an undefined address in the EBI address space.

No abort is generated when reading the internal memory or by accessing the internal peripherals, whether the address is defined or not.

External Bus Interface

The External Bus Interface handles the accesses between addresses 0x0040 0000 and 0xFFC0 0000. It generates the signals that control access to the external devices, and can be configured from eight 1-Mbyte banks up to four 16-Mbyte banks. It supports byte-, half-word- and word- aligned accesses.

For each of these banks, the user can program:

- Number of wait states
- Number of data float times (wait time after the access is finished to prevent any bus contention in case the device is too long in releasing the bus)
- Data bus-width (8-bit or 16-bit).
- With a 16-bit wide data bus, the user can program the EBI to control one 16-bit device (Byte Access Select mode) or two 8-bit devices in parallel that emulate a 16-bit memory (Byte Write Access mode).

The External Bus Interface features also the Early Read Protocol, configurable for all the devices, that significantly reduces access time requirements on an external device in the case of single-clock cycle access.

Peripherals

The AT91R40807 peripherals are connected to the 32-bit wide Advanced Peripheral Bus. Peripheral registers are only word accessible – byte and half-word accesses are not supported. If a byte or a half-word access is attempted, the memory controller automatically masks the lowest address bits and generates an word access.

Each peripheral has a 16-Kbyte address space allocated (the AIC only has a 4-Kbyte address space).

Peripheral Registers

The following registers are common to all peripherals:

- Control Register – write only register that triggers a command when a one is written to the corresponding position at the appropriate address. Writing a zero has no effect.
- Mode Register – read/write register that defines the configuration of the peripheral. Usually has a value of 0x0 after a reset.
- Data Registers – read and/or write register that enables the exchange of data between the processor and the peripheral.
- Status Register – read only register that returns the status of the peripheral.
- Enable/Disable/Status Registers – shadow command registers. Writing a one in the Enable Register sets the corresponding bit in the Status Register. Writing a one in the Disable Register resets the corresponding bit and the result can be read in the Status Register. Writing a bit to zero has no effect. This register access method maximizes the efficiency of bit manipulation, and enables modification of a register with a single non-interruptible instruction, replacing the costly read-modify-write operation.

Unused bits in the peripheral registers are shown as "–" and must be written at 0 for upward compatibility. These bits read 0.

Peripheral Interrupt Control

The Interrupt Control of each peripheral is controlled from the status register using the interrupt mask. The status register bits are ANDed to their corresponding interrupt mask bits and the result is then ORed to generate the Interrupt Source signal to the Advanced Interrupt Controller.

The interrupt mask is read in the Interrupt Mask Register and is modified with the Interrupt Enable Register and the Interrupt Disable Register. The enable/disable/status (or mask) makes it possible to enable or disable peripheral interrupt sources with a non-interruptible single instruction. This eliminates the need for interrupt masking at the AIC or core level in real-time and multi-tasking systems.

Peripheral Data Controller

The AT91R40807 microcontroller has a 4-channel PDC dedicated to the two on-chip USARTs. One PDC channel is dedicated to the receiver and one to the transmitter of each USART.

The user interface of a PDC channel is integrated in the memory space of each USART. It contains a 32-bit Address Pointer Register (RPR or TPR) and a 16-bit Transfer Counter Register (RCR or TCR). When the programmed number of transfers are performed, a status bit indicating the end of transfer is set in the USART Status Register and an interrupt can be generated.

System Peripherals

PS: Power-saving

The Power-saving feature optimizes power consumption, enabling the software to stop the ARM7TDMI clock (idle mode), restarting it when the module receives an interrupt (or reset). It also enables on-chip peripheral clocks to be enabled and disabled individually, matching power consumption and application need.

AIC: Advanced Interrupt Controller

The Advanced Interrupt Controller has an 8-level priority, individually maskable, vectored interrupt controller, and drives the NIRQ and NFIQ pins of the ARM7TDMI from:

- The external fast interrupt line (FIQ)
- The three external interrupt request lines (IRQ0-IRQ2)
- The interrupt signals from the on-chip peripherals.

The AIC is largely programmable offering maximum flexibility, and its vectoring features reduce the real-time overhead in handling interrupts.

The AIC also features a spurious vector, which reduces spurious interrupt handling to a minimum, and a protect mode that facilitates the debug capabilities.

PIO: Parallel I/O Controller

The AT91R40807 microcontroller has 32 programmable I/O lines. Six pins are dedicated as general-purpose I/O pins. Other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The PIO controller enables generation of an interrupt on input change and insertion of a simple input glitch filter on any of the PIO pins.

WD: Watchdog

The Watchdog is built around a 16-bit counter and is used to prevent system lock-up if the software becomes trapped in a deadlock. It can generate an internal reset or interrupt, or assert an active level on the dedicated pin NWDOVF. All programming registers are password-protected to prevent unintentional programming.

SF: Special Function

The AT91R40807 microcontroller provide registers that implement the following special functions.

- Chip identification
- RESET status
- Protect mode
- Write protection for the AT91R40807 internal 128-Kbyte memory

User Peripherals

USART: Universal Synchronous/ Asynchronous Receiver Transmitter

The AT91R40807 microcontroller provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters.

Each USART has its own baud rate generator, and two dedicated Peripheral Data Controller channels. The data format includes a start bit, up to 8 data bits, an optional programmable parity bit and up to 2 stop bits.

The USART also features a Receiver Timeout register, facilitating variable length frame support when it is working with the PDC, and a Time Guard register, used when interfacing with slow remote equipment.

TC: Timer Counter

The AT91R40807 microcontroller features a Timer Counter block that includes three identical 16-bit timer counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

The Timer Counter can be used in Capture or Waveform mode, and all three counter channels can be started simultaneously and chained together.

Ordering Information

Table 4. Ordering Information

Ordering Code	Package	Operation Range
AT91R40807-33AI	TQFP 100	Industrial (-40°C to 85°C)

Packaging Information

Figure 3. 100-lead Thin Quad Flat Pack Package Drawing

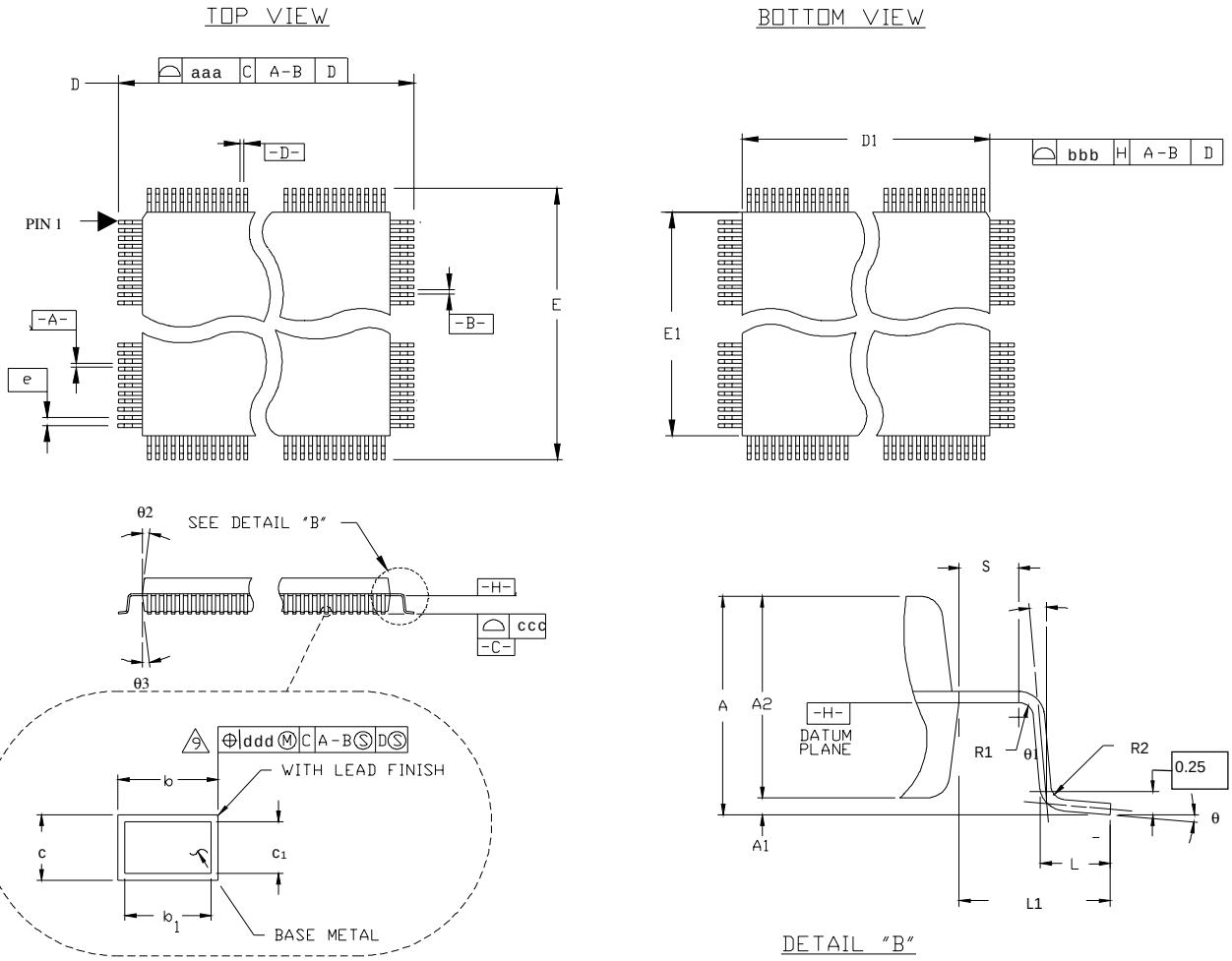


Table 5. Common Dimensions (mm)

Symbol	Min	Nom	Max
c	0.09		0.2
c1	0.09		0.16
L	0.45	0.6	0.75
L1		1.00 REF	
R2	0.08		0.2
R1	0.08		
S	0.2		
q	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
Tolerances of form and position			
aaa		0.2	
bbb		0.2	

Table 6. Lead Count Dimensions (mm)

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Nom	Max	Min	Nom	Max			
100	16.0	14.0	0.17	0.22	0.27	0.17	0.2	0.23	0.50	0.10	0.06

Table 7. Device and 100-lead TQFP Package Maximum Weight

739	mg

Soldering Profile

Table 8 gives the recommended soldering profile from J-STD-20.

Table 8. Soldering Profile

	Convection or IR/Convection	VPR
Average Ramp-up Rate (183°C to Peak)	3°C/sec. max.	10°C/sec.
Preheat Temperature 125°C ±25°C	120 sec. max	
Temperature Maintained Above 183°C	60 sec. to 150 sec.	
Time within 5°C of Actual Peak Temperature	10 sec. to 20 sec.	60 sec.
Peak Temperature Range	220 +5/-0°C or 235 +5/-0°C	215 to 219°C or 235 +5/-0°C
Ramp-down Rate	6°C/sec.	10°C/sec.
Time 25°C to Peak Temperature	6 min. max	

Small packages may be subject to higher temperatures if they are reflowed in boards with larger components. In this case, small packages may have to withstand temperatures of up to 235°C, not 220°C (IR reflow).

Recommended package reflow conditions depend on package thickness and volume. See Table 9.

Table 9. Recommended Package Reflow Conditions (1, 2, 3)

Parameter	Temperature
Convection	235 +5/-0°C
VPR	235 +5/-0°C
IR/Convection	235 +5/-0°C

When certain small thin packages are used on boards without larger packages, these small packages may be classified at 220°C instead of 235°C.

Notes:
1. The packages are qualified by Atmel by using IR reflow conditions, not convection or VPR.
2. By default, the package level 1 is qualified at 220°C (unless 235°C is stipulated).
3. The body temperature is the most important parameter but other profile parameters such as total exposure time to hot temperature or heating rate may also influence component reliability.

A maximum of three reflow passes is allowed per component.

Document Details

Title	AT91R40807 Summary
Literature Number	1345S

Revision History

Version A	**Publication Date:** Jan-00
Version B	**Publication Date:** Mar-00
Version C	**Publication Date:** May-00
Version D	**Publication Date:** 21-Jan-02
Revisions Since Previous Version	
All pages.	Reformatted.
Page: 9	Added information to section Internal Memories
Page: 14	Change in Table 4
Page: 16	Added Table 7, Package Weight
Page: 17	Added section Soldering Profile

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