

Features

General

- High-performance, Low-power secureAVR™ Core Enhanced RISC Architecture
 - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- With an ISO14443 Contactless only interface
- Power-saving Wait and Very Low Power Stop Modes
- Power-up Detection
- Available in Wafers, Contactless Modules or Inlays and Industry-standard Packages
- Compliant with Master Card PayPass™ / VISA Specifications

Contactless Mode

- Contactless Interface Controller (CIC) with Full Support for ISO/IEC 14443 Type A and B Protocol
- Supply Voltage Clamp and Regulation
- Full-bridge Power Rectification
- On-chip Tuning Capacitance: 20pF up to 120pF
- 13.56 MHz Clock Extraction
- 6.78 MHz Internal Bus Frequency
- Reader-to-card:
 - ISO/IEC Type A: 100% ASK Modulation and Modified Miller Bit Coding
 - ISO/IEC Type B: 10% ASK Modulation and NRZ Bit Coding
- Card-to-reader:
 - ISO/IEC Type A: Generation of 847.5KHz Subcarrier with OOK Modulation and Manchester Bit Coding
 - ISO/IEC Type B: Modulation of Incoming RF Carrier by Resistive Load Switching / Generation of 847.5KHz Subcarrier with BPSK Modulation / NRZ data Encoding
 - Baud Rates: 106Kbps, 212 Kbps and 424 Kbps
- RF Frame: Up to 256 bytes

Memory

- 64K Bytes of ROM Program Memory
- 04K Bytes of EEPROM, Including 64 OTP Bytes and 192 Bit-addressable Bytes
 - 1 to 64-byte Program/Erase, 2 ms Program, 2 ms Erase
 - Endurance: 500,000 Write/Erase Cycles at 25°C, 10 Years Data Retention
- 1K Bytes of RAM + 256 Bytes of DMA dedicated RAM

Peripherals

- Programmable Internal Oscillator (Up to 20 MHz for internal CPU Clock)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 8-vector Interrupt Controller
- Hardware DES and Triple DES DPA/DEMA Resistant
- Checksum Accelerator
- CRC 16 & 32 Engine (Compliant with ISO/IEC 3309)
- DMA Controller (Used to Speed-Up Data Transfers when Communicating via the Contactless Interface)

Security

- Dedicated Hardware for Protection Against SPA/DPA/DEMA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Environmental Protection Systems, Temperature Monitor, Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)
- Security Certification Targeted: Common Criteria EAL4+



Secure Microcontroller for Smart Cards

AT90SC 6404RFT Summary

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Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Development Tools

- Voyager Emulation Platform (ATV4 Advanced) to Support Software Development
- IAR Embedded Workbench® V3.20c Debugger or Atmel's AVR Studio® Version 4.07 or Above
- Software Libraries and Application Notes

Description

The AT90SC6404RFT is a low-power, high-performance, 8-/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR enhanced RISC architecture and with a contactless interface.

By executing powerful instructions in a single clock cycle, the AT90SC6404RFT achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

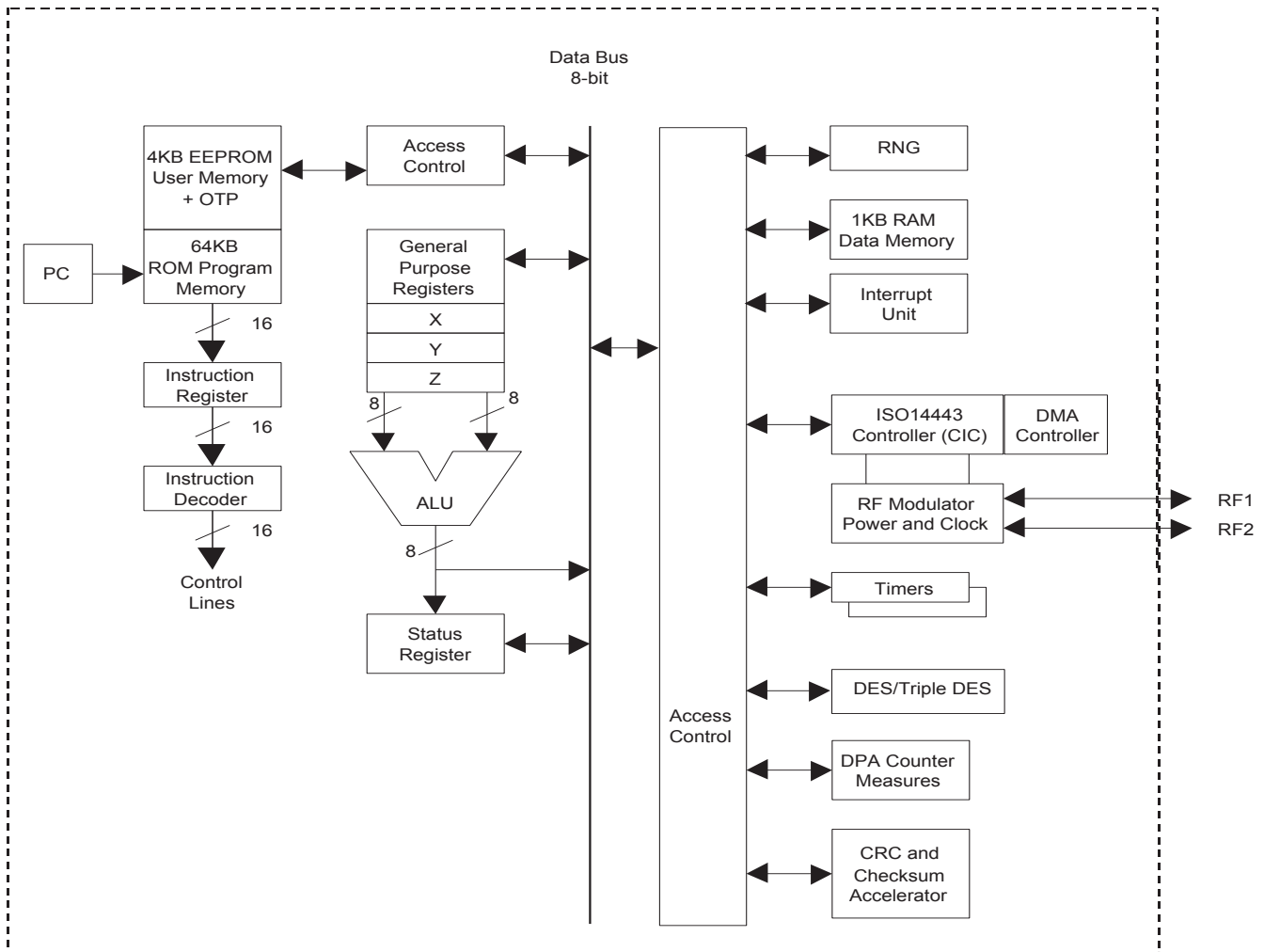
The AT90SC6404RFT uses the secureAVR architecture that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data as well as a number of new functional and security features. The AT90SC6404RFT features 04K bytes of high-performance EEPROM (fast erase/write time, high endurance). The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system.

Additional security features include temperature protection logic, logical scrambling on program data and addresses, power analysis countermeasures, and memory accesses controlled by a supervisor mode.

This product is specifically designed for Smart Cards and targets Transport and Banking applications.

Figure 1 shows a block diagram of the AT90SC6404RFT.

Figure 1. Block diagram of AT90SC6404RFT.





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