Features

- DC/DC Step-up Converter (BOOST) 3.3V to 5.2V, 1A, up to 90% Efficiency. Can be Used as BUCK/BOOST in SEPIC Configuration
- DC/DC Step-down (BUCK) Synchronous Converter 0.9V to 3.4V, 500mA, up to 90% Efficiency, Pulse Skipping Capabilities for High Efficiency at Light Load Currents
- Two Low-Drop-Out Regulators 1.3V, 1.5V to 1.8V, 2.5V to 2.8V (100 mV Step), 3.3V, 200 mA Maximum Load
- Ultra-low Power Real-time Clock (RTC) and Backup Battery Management
  - 2.6V RTC LDO for Backup Battery Charging
  - 32 kHz Crystal RTC Oscillator (1 µA)
  - RTC Circuit for Time and Date Information
- Activation of the Power Management Modules via Dedicated Enable Pin
- Automatic Start-up Sequences, POK Signal Indicating When Start-up is Completed
- Activation and Control of the Power Management Modules in Dynamic Mode (via SPI or TWI) or in Static Mode (On/Off of the Four Power Supplies)
- ITB Signal Indicating Short-circuits in DC/DC Converters
- Very Low Quiescent Current
- Minimum External Components Count
- Supply: from 2.8V to 5.25V (typ: Li-Ion Battery 3V to 4.2V)
- Available in a 32-pin 5x5 QFN Package
- Applications Include:
  - WLAN Portable Devices
  - Multimedia Devices
  - Portable Music Players

1. Description

The AT73C224-x is a family of ultra low cost Power Management Unit, available in a small outline QFN 5x5mm package.

The AT73C224-x family is optimized for portable applications, typically powered by a Li-Ion battery. The AT73C224-x device is also suitable to operate from a standard 3.3V to 5.25V voltage rail. It includes four power supplies and a very low power Real-time Clock (RTC). In normal mode (main battery present), the backup battery is recharged through a 2.6V RTC LDO.

The AT73C224-x series offer different automatic start-up sequences (with varying orders of power-on and specific default output values) and different soft management modes: dynamic (via SPI or TWI) with register access or static, with access to power on/off of the four power supplies.

Each AT73C224-x device is equipped with a very low power bandgap reference, low power 32 kHz and 1 MHz oscillators and an internal LDO used to generate the internal supply (VINT) equal to 2.8V. Auxiliary cells, such as a power-on reset (POR) and a voltage monitor are used to control the system power-on (battery plugged in) and power-off (battery unplugged).

The four power supplies are named: BOOST1, BUCK2, LDO3 and LDO4.

Table 1-1 lists the different devices available in the AT73C224-x series.

Power Management and Analog Companions (PMAAC)

AT73C224-A
AT73C224-B
AT73C224-C
AT73C224-D
AT73C224-E
AT73C224-F
AT73C224-G
AT73C224-H

4x Channels Power Supply:
DC/DC BOOST
DC/DC BUCK
2x LDOs
RTC

6266A–PMAAC–08-Sep-08

For more details concerning the Automatic start-up sequences, see Section 5.2.

For more details concerning the Management Modes, see Section 5.3.

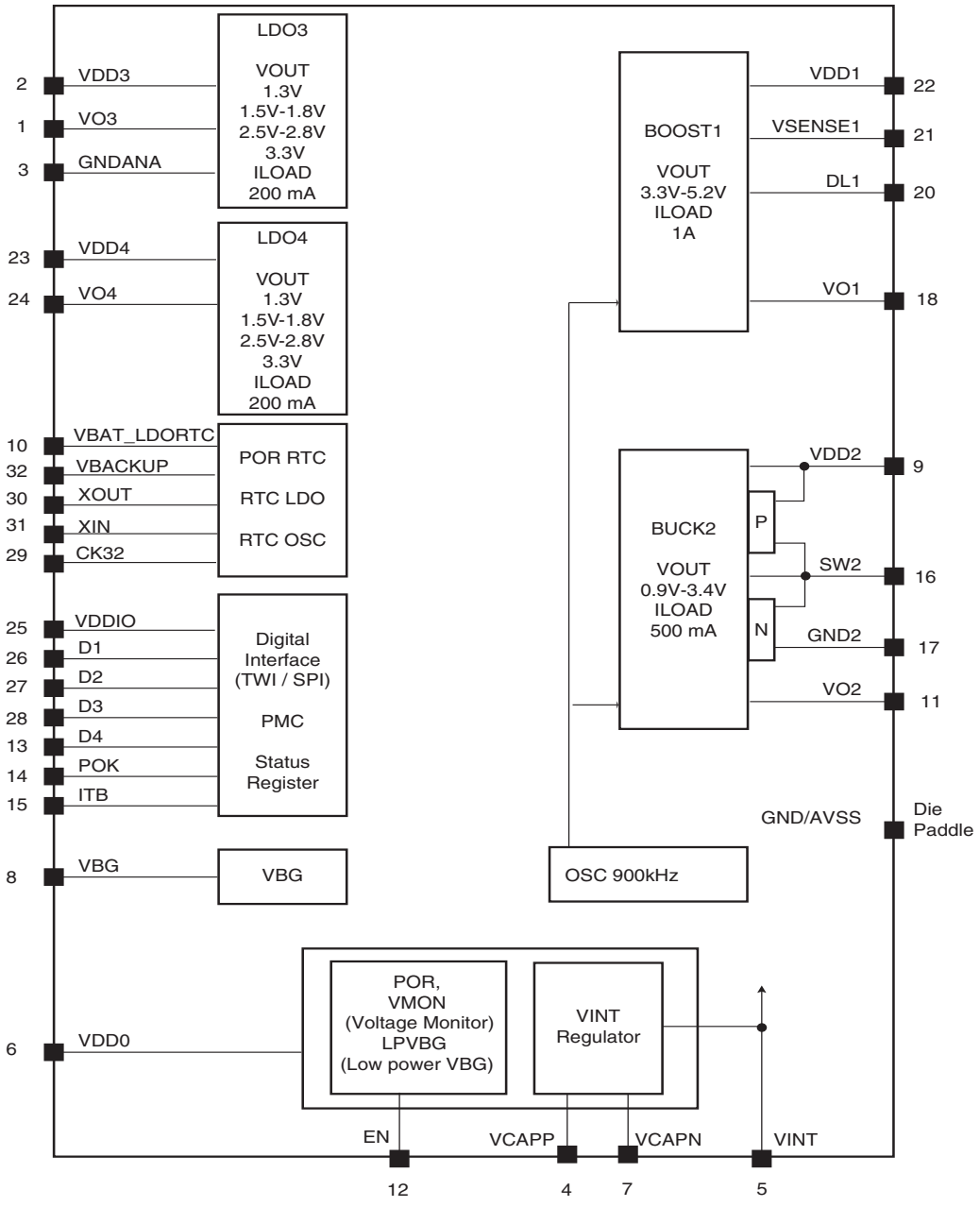
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Table 1-1. AT73C224-x device series

Part Number	Automatic Start-up Sequence Order of power-on and output default values.	Management Mode	Comments
AT73C224-A	1 - BUCK2= 1.8V 2 - LDO4 = 2.8V 3 - LDO3 = 2.7V	Dynamic	BOOST1 can be activated after Start-up sequence by a user command.
AT73C224-B	1 - BUCK2 = 1.2V 2 - LDO4 = 1.8V 3 - LDO3 = 1.8V	Dynamic	BOOST1 can be activated after Start-up sequence by a user command.
AT73C224-C	1 - LDO4 = 2.8V 2 - BUCK2 = 1.8V 3 - LDO3 = 2.7V	Dynamic	BOOST1 can be activated after Start-up sequence by a user command.
AT73C224-D	1 - LDO4 = 1.8V 2 - BUCK2 = 1.2V 3 - LDO3 = 1.8V	Dynamic	BOOST1 can be activated after Start-up sequence by a user command.
AT73C224-E	1 - BOOST11 = 5.2V 2 - LDO4 = 3.3V 3 - LDO3 = 3V	Dynamic	BUCK2 can be activated after Start-up sequence by a user command. LDO3 & LDO4 are supplied by BOOST1. (See Section 4. “Application examples”, Figure 4-3 on page 7: Application Schematic 3.)
AT73C224-F	1 - BUCK2 = 1.8V 2 - LDO4 = 2.8V 3 - LDO3 = 2.7V	Static	Same as AT73C224-A.
AT73C224-G	1 - LDO4 = 2.8V 2 - BUCK2= 1.8V 3- LDO3 = 2.7V	Static	Same as AT73C224-C.
AT73C224-H	1 - BOOST1 = 5.2V 2 - LDO4 = 3.3V 3 - LDO3 = 3V	Static	Same as AT73C224-E.

2. Block Diagram

Figure 2-1. Block Diagram



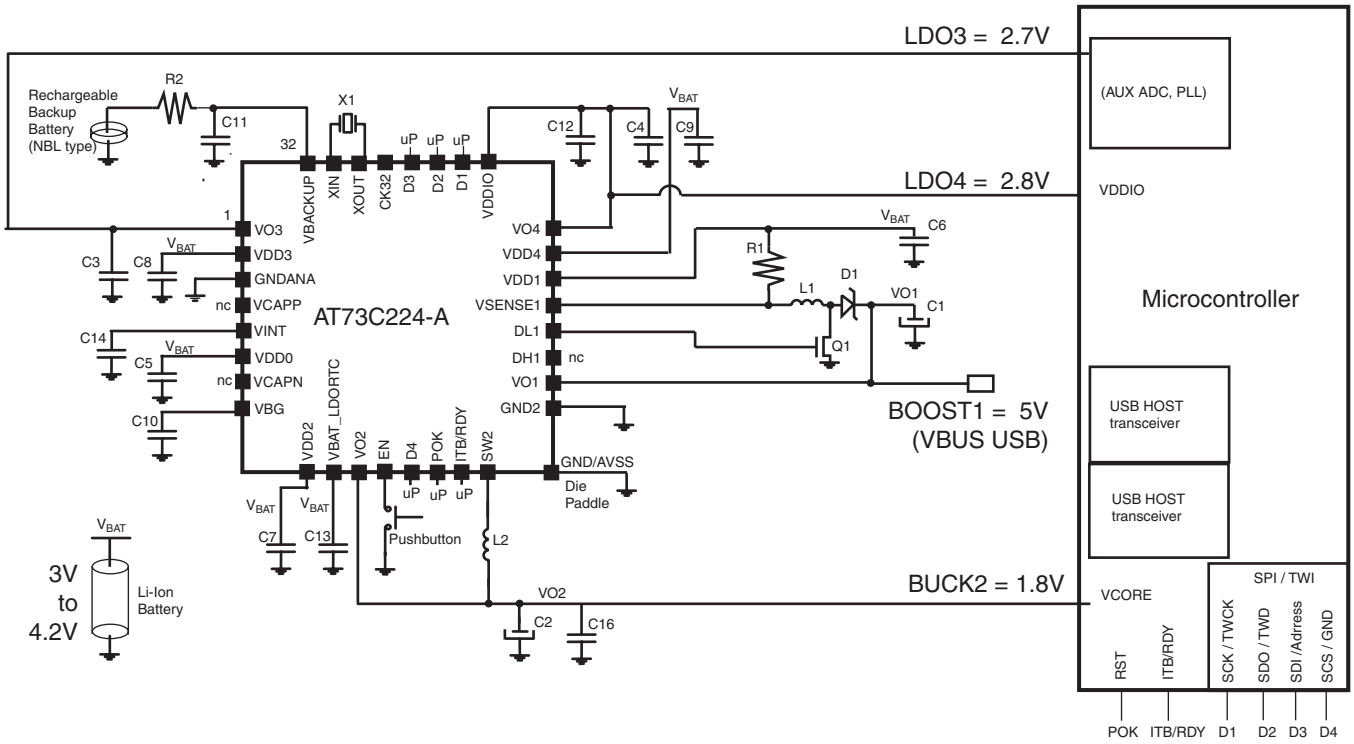
3. Pinout

Table 3-1. AT73C224 Pinout

Pin Name	I/O	Pin #	Type	Function	Comments
VO3	O	1	Analog	LDO3 output voltage	Ext. 2.2 µF capacitor (mandatory)
VDD3	PS	2	Power	LDO3 supply voltage	
GNDANA	PS	3	Ground	Analog ground	
VCAPP	I/O	4	Analog	Not connected	
VINT	PS	5	Power	Output of the internal LDO	Ext. 470 nF capacitor (mandatory)
VDD0	PS	6	Analog	Supply of the internal LDO	Must be connected to the main battery (mandatory)
VCAPN	I/O	7	Analog	Not connected	
VBG	O	8	Analog	Bandgap reference voltage	Should not be resistively loaded
VDD2	PS	9	Power	BUCK2 supply voltage	
VBAT_LDORTC	PS	10	Power	LDO_RTC Supply voltage	Must be connected to the main battery (mandatory)
VO2	I	11	Analog	BUCK2 output voltage	
EN	I	12	Digital	Enable signal	Internal 100 KΩ pull up
D4	I	13	Digital	Digital interface	Internal 100 KΩ pull up
POK	O	14	Digital	Power Ok: indicates when start-up is completed	
ITB/RDY	I/O	15	Digital	User Interrupt, GPIO and Shutdown control	Internal 100 KΩ pull up
SW2	O	16	Analog	BUCK2 inductor (NMOS switcher output)	
GND2	PS	17	Ground	BUCK2 ground	
VO1	I	18	Analog	BOOST1 output voltage	
DH1	O	19	Analog	Not connected	
DL1	O	20	Analog	BOOST1 NMOS control signal	
VSENSE1	I	21	Analog	BOOST1 current limitation sense voltage	
VDD1	PS	22	Power	BOOST1 supply voltage	Must be connected to the main battery
VDD4	PS	23	Power	LDO4 supply voltage	
VO4	O	24	Analog	LDO4 output voltage	Ext. 2.2 µF capacitor (mandatory)
VDDIO	PS	25	Digital supply	Supply voltage for Digital I/O	
D1	I	26	Digital	Digital interface	open drain
D2	I/O	27	Digital	Digital interface	open drain
D3	I	28	Digital	Digital interface	open drain
CK32	O	29	Digital	32 kHz RTC output clock	
XOUT	I/O	30	Analog	RTC crystal oscillator output	
XIN	I/O	31	Analog	RTC crystal oscillator input	
VBACKUP	O	32	Analog	Backup Battery and RTC supply	
GND/AVSS	PS	33	Ground	Main G_{ND} and AV_{SS} ground	die paddle connected to ground (mandatory)

4. Application examples

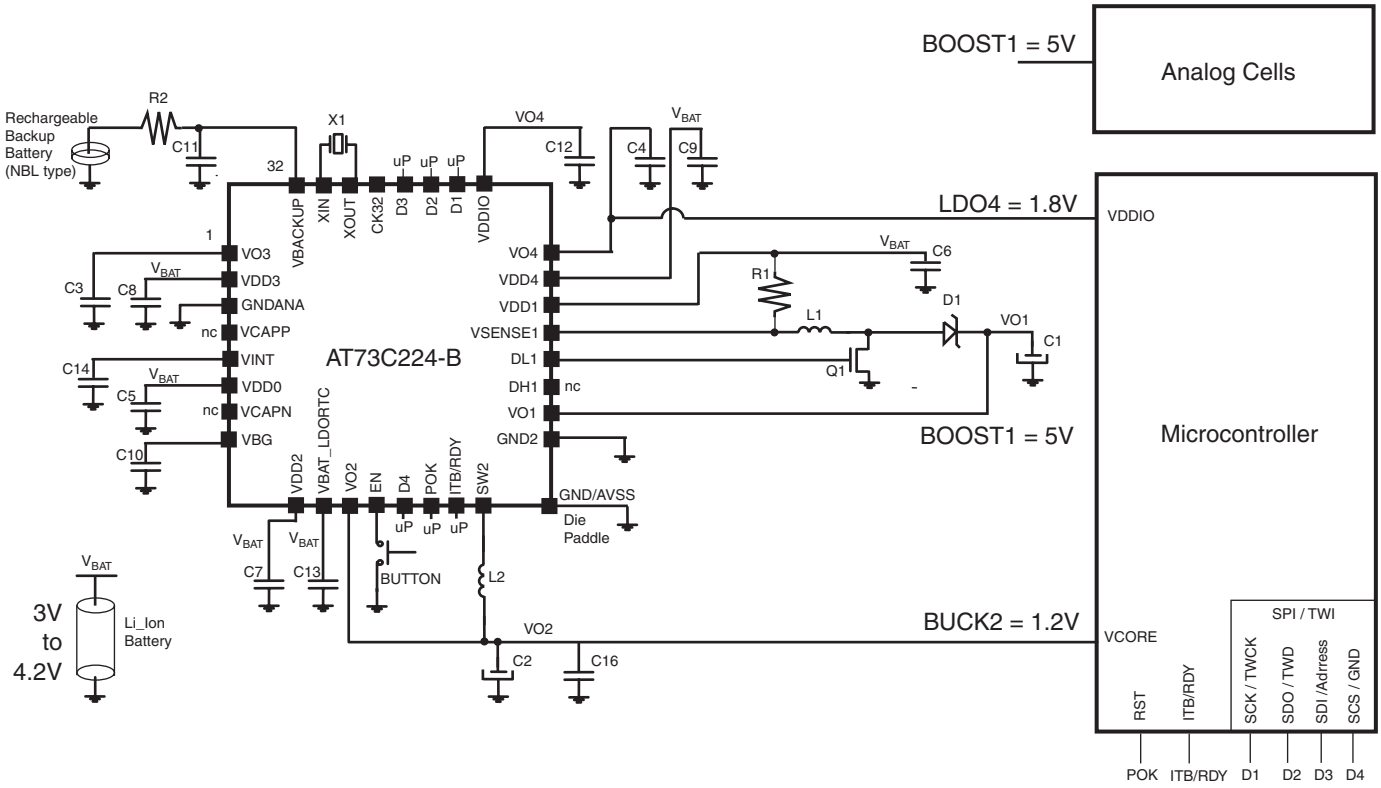
Figure 4-1. Application Schematic 1: Microcontroller with 5V VBUS for 2 USB Host Transceivers



In the Application Schematic 1, the AT7373C224-A is used: the BOOST(VO1) supplies the “VBUS” of two USB transceivers, the BUCK(VO2) supplies the digital core of the microcontroller, the LDO3 supplies the I/Os of the microcontroller and LDO4 supplies analog cells, such as auxiliary ADC or PLL.

For external components, see Table 4-1.

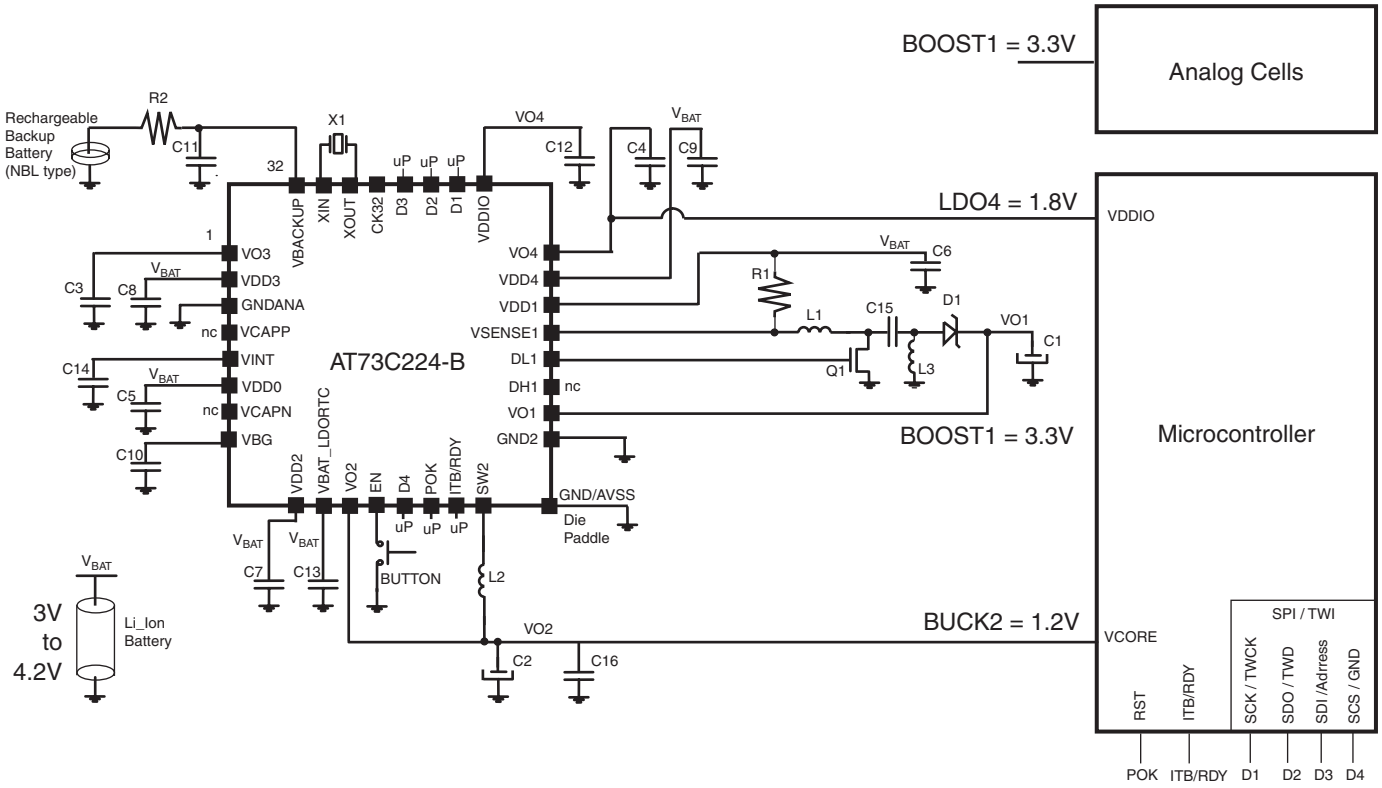
Figure 4-2. Application Schematic 2: Supply of a Microprocessor and External Analog Cells



In the Application Schematic 2, the AT73C224-B is used: the BOOST (VO1) supplies the “VBUS” of one USB transceiver and supplies also LDO3 and LDO4. The BUCK(VO2) supplies the digital core of the microcontroller and the LDOs supply the I/Os and Analog cells, such as auxiliary ADC or PLL.

For external components, see Table 4-1.

Figure 4-3. Application Schematic 3: BOOST in SEPIC Configuration (BUCK/BOOST)



In the Application Schematic 3, the BOOST (VO1) is in SEPIC configuration (BUCK/BOOST) and generates a 3.3V output voltage for analog cells. The BUCK (VO2) supplies the core of the microcontroller, and LDO4 supplies the I/Os.

Note that, in the SEPIC configuration, the maximum load current on VO1 should not exceed 300 mA.

For external components, see Table 4-1.

Table 4-1. External Components

Schematic reference	Reference	Manufacturer	Value
C1	Tantalum TPS Case B	AVX®	100 µF
C2	Tantalum TPS Case A	AVX	33 µF
C3, C4	GRM155R60J225ME15 C1005X5R0J225MT	Murata® TDK	2.2 µF
C6	GRM21BR60J226ME39 C2012X5R0J226MT	Murata TDK	22 µF
C5, C7, C8, C9, C11, C13	GRM155R60J105KE19 C1005X5R0J105KT	Murata TDK	1 µF
C10	GRM155R61A104KA01 C0603X5R0J104KT	Murata TDK	100 nF
C12, C14	GRM155R60J474KE18 C1005X5R1A474KT	Murata TDK	470 nF
C15	GRM188R60J475KE19 C1608X5R0J475KT	Murata TDK	4.7 µF
C16	GRM188R60J106ME47 C1608X5R0J106MT	Murata TDK	10 µF
L1	744773022	Wurth® Elektronik	2.2 µH
L1, L3 (in SEPIC config.)	744773068	Wurth Elektronik	6.8 µH
L2	B82467-G0682-M	Epcos®	6.8 µH
D1	MBRM120LT1	On Semiconductor®	
Q1	Si1470DH	Vishay®	
X1	FX135B-327	Fox	32.768 kHz
R1 (can be printed on the board (Cu line))	LR2010R050J	Welwyn	50 mΩ
R2	MR-CRG0402J2k2	Tyco™ Electronics	2 kΩ

5. Detailed Description

The AT73C224-x is a family of Power Management Units with four power supplies and an ultra low-power Real-time Clock.

By choosing a specific ordering code “x” from A to H, different automatic start-up sequences and management modes can be selected.

The start-up sequence includes the order of power-on, as well as the default value of the power supplies (see Section 5.2 ”Automatic Start-up Sequences and Shut-down”). The user can afterwards change this default value via SPI or TWI, if the dynamic mode has been chosen (see Section 5.3 ”Digital Control and Protocol”).

5.1 Core

The core of the AT73C224-x device integrates the following blocks:

- Power-On-Reset for the backup battery.
- Internal switch and LDO dedicated to the backup battery. The output of the LDO_RTC is set to 2.6V and the switch is on when the main battery higher than 2.8V (charge of the backup battery).See Section 7.7 for electrical details.
- Real-Time-Clock digital bloc + 32 kHz oscillator.
- Power-On-Reset for the main battery.
- Voltage Monitor (VMON) of the main battery.
- Digital Power Management Control (PMC) for automatic start-up sequences. Digital output POK indicates when start-up is completed, whereas ITB digital output signal informs the user (typically the microcontroller) of a default in the DC/DCs (short-circuit) or too low main battery value.
- TWI and SPI protocol blocs.
- DC/DC Step-up converter BOOST1: A 3.3V to 5.2V(100 mV step), 1A, asynchronous DC/DC Step-up Converter available for overall system requirements. The DC/DC can be implemented through proper external components in BUCK/BOOST (SEPIC) configuration. The output voltage can be programmed via the internal registers. BOOST1 is supplied directly by the battery.
- DC/DC Step-down converter BUCK2: A 0.9V to 3.4V, 500 mA fully integrated synchronous PWM DC/DC Step-down Converter. The output voltage can be programmed via the internal registers. A Pulse Skipping mode is available in order to improve efficiency at very light load current values. In order to guarantee very low supply voltage functionality, the controller is supplied by the max voltages between the main battery and the output of BOOST1 (VO1). BUCK2 can be directly supplied by the battery or by the output of BOOST1.
- LDO3: A 1.3V, 1.5V to 1.8V (100 mV of step), 2.5V to 2.8V (100 mV of step), 3.3V, 200 mA – Low Drop out regulators. The output voltage can be programmed via the internal registers. LDO3 can work with supply from 1.8V up to 5.5V. This LDO can be supplied by the battery, by the output of BOOST1, or by the output of BUCK2.
- LDO4: same functionality than LDO3.
- Main Bandgap: 1.18V reference voltage.
- 900 kHz Oscillator.
- Internal LDO (VINT) at 2.8V for internal supply.

5.2 Automatic Start-up Sequences and Shut-down

5.2.1 Start-up/Wakeup

If the backup battery (only) is present, the RTC is running (1.2 µA). This mode is called “Backup mode”. When the main battery is plugged in and voltage is higher than 2.8V, the LDO_RTC recharges the backup battery through an internal switch (if the main battery is lower than 2.8V, nothing happens, RTC still running). This mode is called “Standby mode”. Note that when the battery is plugged in (and higher than 2.8V), a reset of the RTC is performed only if the backup battery was lower than 1.8V.

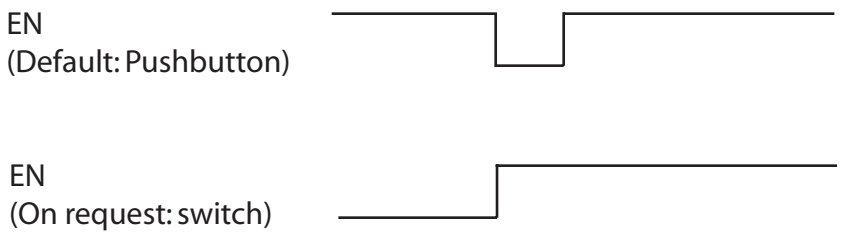
Now, the system waits for wake-up information coming from the pushbutton (EN pin) or an RTC alarm. When one of the previous conditions occurs, the automatic start-up sequence starts (without any external commands).

Different automatic start-up sequences can be chosen from the AT73C224-x family (see Figure 5-1 on page 11 and Figure 5-2 on page 12).

When the automatic start-up sequence has been completed, the POK signal (which is an open drain signal) goes high, thus implementing a sort of POR for the user (i.e., a microcontroller) and enters into “Normal mode”.

Note: Power On is controlled by default by an external pushbutton, connected on EN pin (the EN pad has an internal 100 kΩ pull up). A switch can also be used as shown bellow but should be a request from the customer

.



5.2.2 Shut-down

Static and Dynamic modes are explained in detail in Section 5.3.

5.2.2.1 Static Mode

In Static mode, the Power-off condition is an OR between the following conditions: main battery lower than 2.8V or electrical default in the DC/DC (short-circuit). When Power-off condition occurs, POK signal is cleared, then the AT73C224-x device waits for the signal ITB/RDY to shut down all power supplies.

5.2.2.2 Dynamic Mode

In Dynamic mode, Power-off condition is an OR between the following conditions: electrical default in the DC/DC (short-circuit) or software shutdown. When main battery lower than 2.8V, an interrupt is generated on signal ITB/RDY. It is the responsibility of the host microcontroller to perform a software shut-down by properly writing the AT73C224-x device registers through the serial interface. After that, the POK signal is cleared, and all is turned off. A check on the push-button is then performed to assure that it has been released, thus avoiding continuous on-off-on behavior. The “normal” shutdown is performed by software. Note that the microcontroller has to write the proper register to enable the power off (see Section 6. ”Register Tables”).

Figure 5-1 illustrates the complete automatic start-up sequence of the AT73C224-A and AT73C224-F, whereas Figure 5-2 illustrates the automatic start-up sequence of the other AT73C224-x device versions.

Figure 5-1. Start up Sequence of the AT73C224-A and AT73C224-F

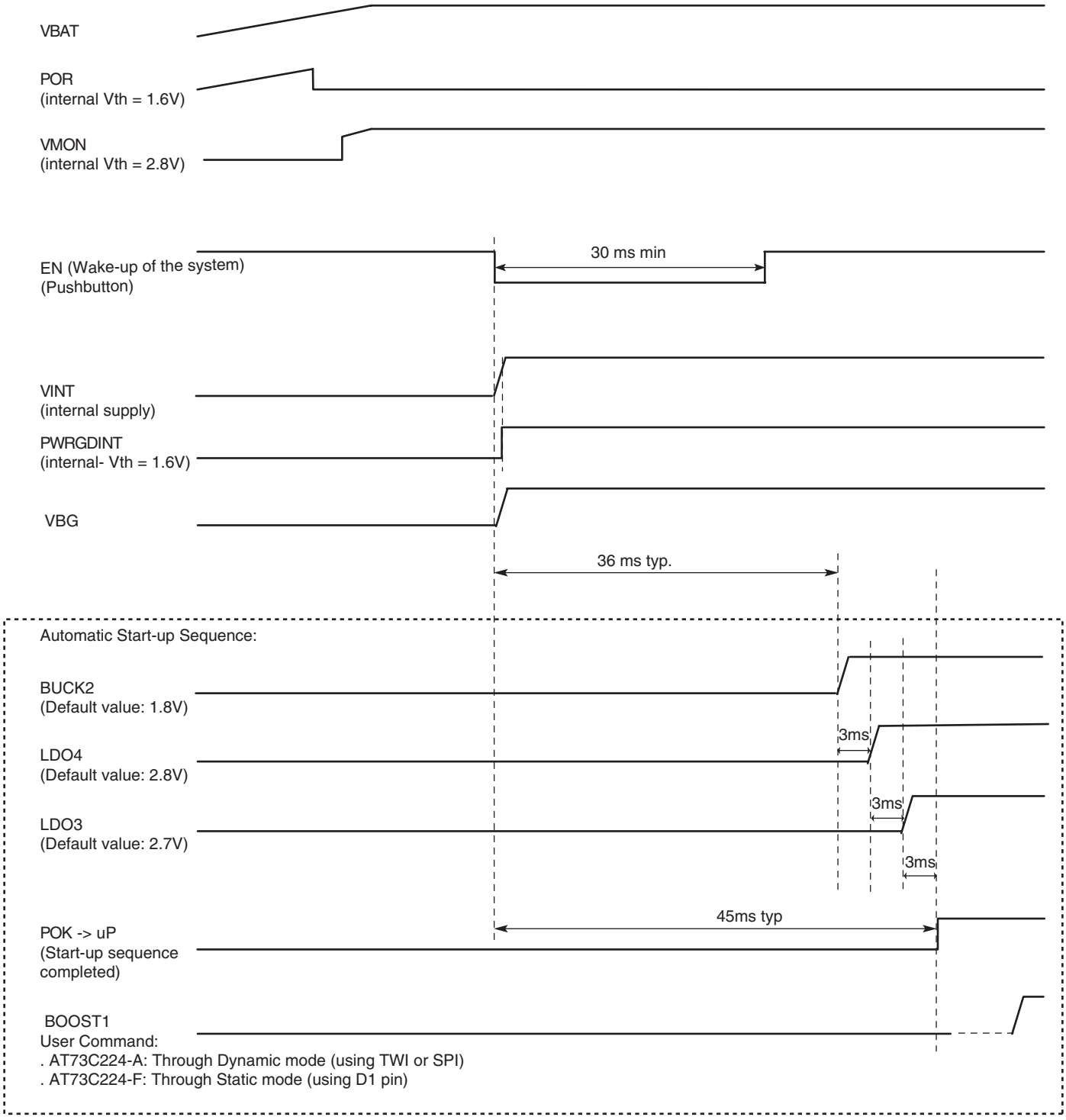
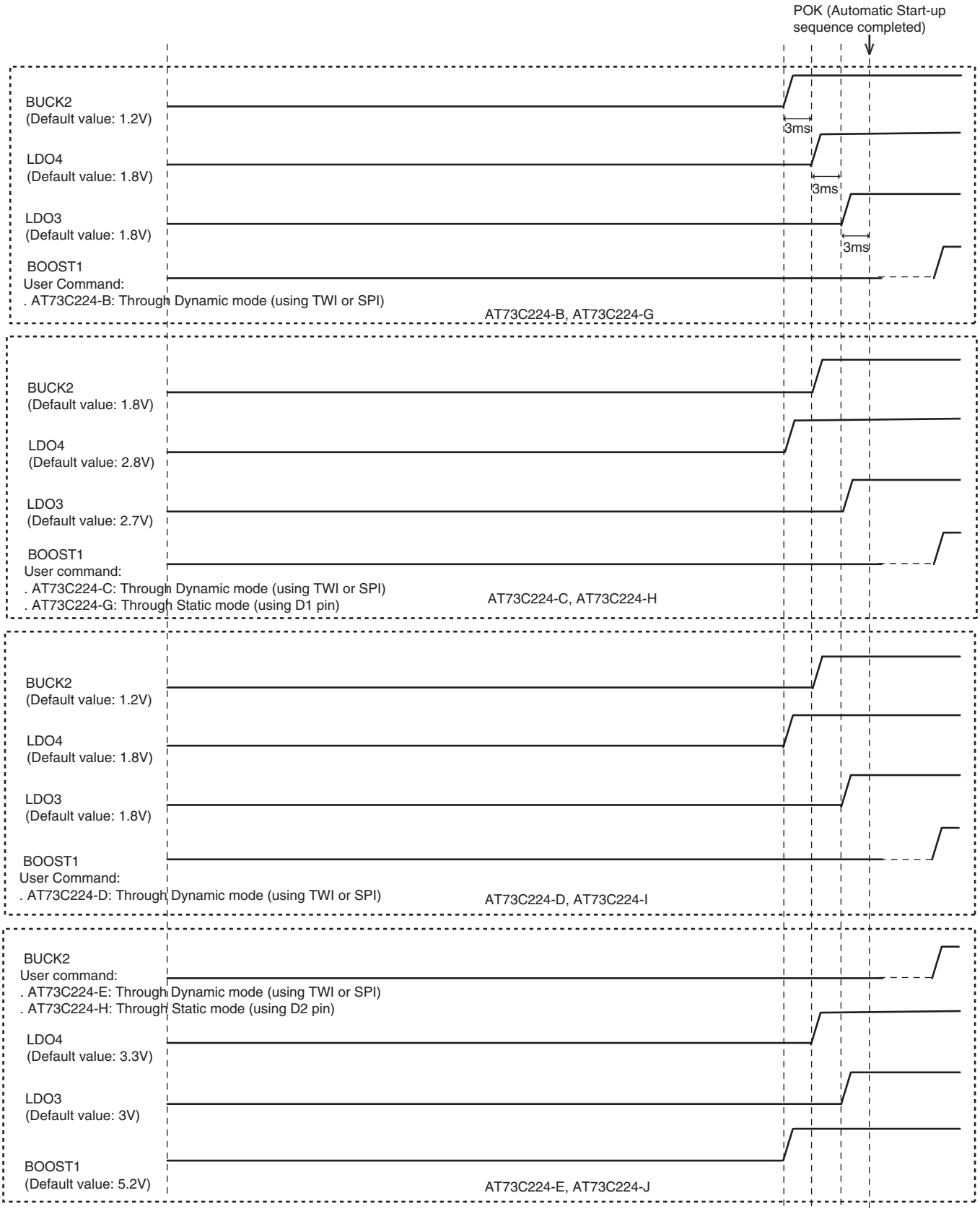


Figure 5-2. Automatic Start-up Sequence of all Other Versions of the AT73C224-x Device Series



5.3 Digital Control and Protocol

The AT73C224-x family offers a choice of devices in static mode or dynamic mode (see Table 1-1 on page 2). In dynamic mode, the user can manage the chip via SPI or TWI. The selection between SPI or TWI is done at start-up via the D4 pin (see Section 5.3.2 on page 14).

5.3.1 Static Mode

When the AT73C224-x is established in Static Mode, the digital interface signals, D1 to D4, directly drive the enable of the four supplies. During start-up, these enable signals are driven by the internal state machine. To ensure a safe transition between the start-up state and the established state, a handshake protocol must be respected. This transition period is especially important in a microcontroller environment, as the microcontroller controlling the D1-D4 signals may require an unknown period of time to actually drive these pins.

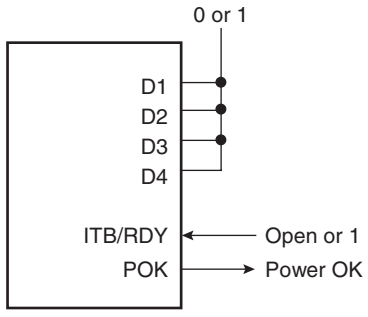
In Static Mode, the ITB/RDY pin is configured as an input with controllable pull-up resistor. When the internal state machine completes the supply start-up, it latches the value of ITB/RDY and then sets the POK signal to 1. This means that start-up is accomplished. The state machine then checks for changes on ITB/RDY. If no changes are detected, the control of the four supply channels remains with the state machine. If a change is detected the internal pullup is disconnected and the control is passed on to D1-D4, with the assignment shown in Table 5-2 below.

Table 5-1. D1-D4 Signal Assignment

Digital Interface Signal	Supply Enable
D1	Enables BOOST1
D2	Enables BUCK2
D3	Enables LDO3
D4	Enables LDO4

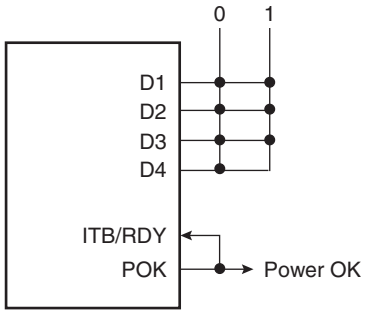
The illustrations in Figure 5-3, Figure 5-5 and Figure 5-5 represent possible static mode scenarios.

Figure 5-3. Fully Static Mode



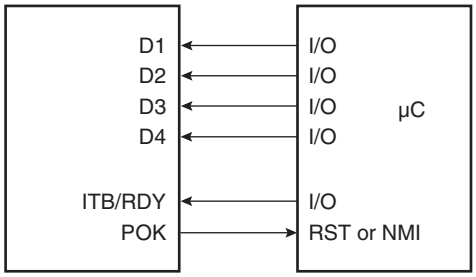
Since ITB/RDY is 1 or open (weak internal pullup), the state of each supply channel is determined by the internal state machine (Automatic Start-up sequence and default values for the three power supplies). In this configuration, the 4th power supply is off and can not be used. D1-D4 is not considered, but must be valid. The POK signal can be used as a global system reset.

Figure 5-4. Configurable Static Mode



The state of each channel is determined by the internal state machine during the start-up sequence. POK is looped back onto ITB/RDY. When this signal changes from 0 to 1 (i.e., the start-up is completed), the control of each supply channel is passed on to D1-D4. This allows changing the output values defined by the state machine. This mode can be used when the 4th channel is needed.

Figure 5-5. GPIO (µC Controlled)



When the system is powered, the microcontroller is not necessarily well configured and may be unable to drive D1-D4 correctly. Since ITB/RDY is not actively controlled, its state is an unknown logic level. If ITB/RDY is in hi-Z, the weak internal pullup pulls the level to 1. The power channels are controlled by the internal state machine. After some initialization time, the microcontroller configures its GPIOs to drive D1-D4 as wished. At the end of the software configuration, the microcontroller changes the level of ITB/RDY to 0 in order to get control on the four power channels through D1-D4.

5.3.2 Dynamic Mode

For the devices of the AT73C224-x family that work in dynamic mode, supply management can be performed by the SPI or TWI digital interface. Selection between the two digital interfaces is done through D4 pin when the AT73C224-x is enabled. Pin D4 is a digital input pin that features a controllable pull-up resistor with active low control signal. When the AT73C224-x starts, the pullup is disabled until a push button event is detected. The state machine enables the pull-up resistor on D4, waits for a time and then checks back on the value on the pad.

- If D4 is high (i.e., the level externally applied on D4 is HZ or logic 1), SPI interface is selected. D4 will become SCS.
- If D4 is low (i.e., D4 is externally grounded), TWI interface is selected. D4 is not used.

After signal dynamic has been determined the state machine disables the pull-up resistor to save power and the D4 pin can be normally used (if SPI has been selected).

The selection between SPI versus TWI is performed once, each time the start-up sequence is executed. A timing diagram of the interface selection is shown in Figure 5-6. Care must be taken to leave enough time between the activation of the pullup and the moment when D4 is sampled back. This time is necessary to load the capacitance of the net layout where D4 is connected through the pull-up resistor (100 kΩ typ.). This time is in the order of magnitude of 1 µs (10 pF * 100 kΩ), i.e. only a few cycles of the 900 kHz oscillator are needed.

Figure 5-6. Dynamic Mode Interface Selection

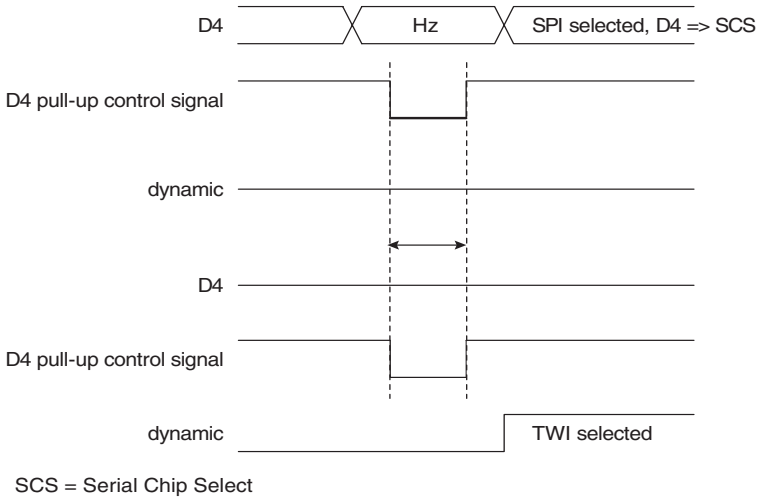


Table 5-2. Digital Interface Selection

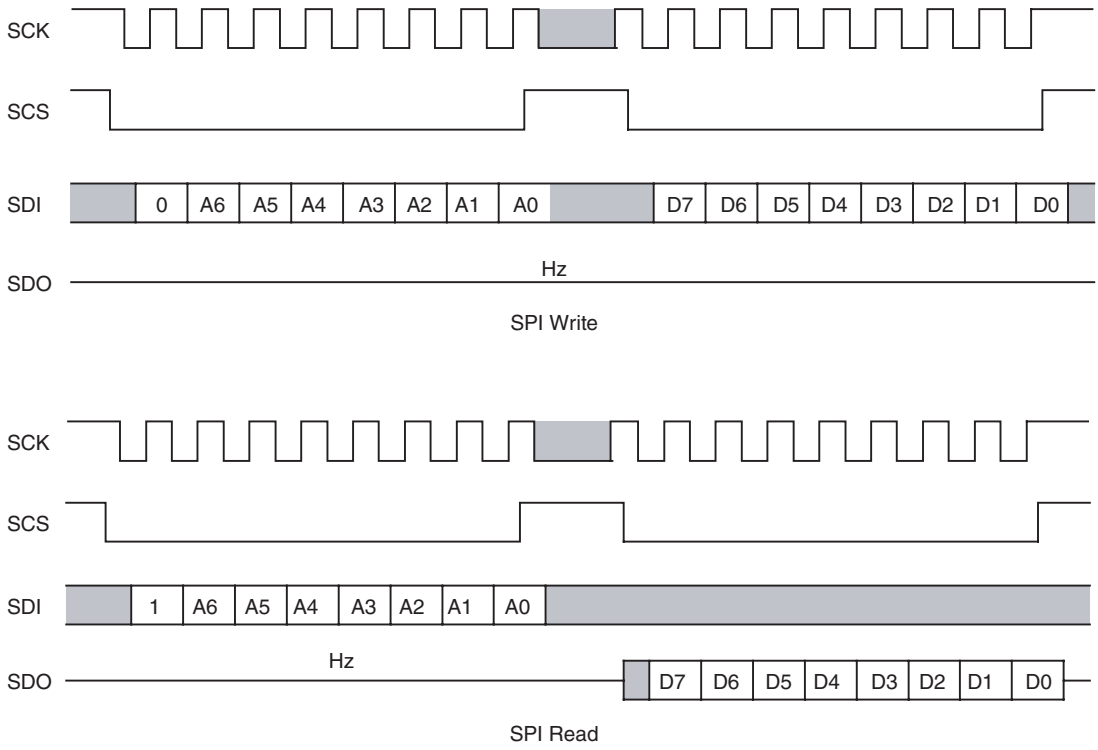
Digital Signal Interface	Pad	SPI Selection		TWI Selection	
		Signal	Direction	Signal	Direction
D1	I	SCK	In	TWCK	In
D2	BIDIR	SDO	Out	TWD	I/O
D3	I	SDI	In	Select the 7-bit fixed address	In
D4[1]	I	SCS	In	grounded	-

Note: 1. On D4, I = Input pad with controllable pull-up resistor.

5.3.2.1 SPI Operation

When SPI mode is selected, the control interface to the AT73C224-x chip is a 4-wire interface modeled after commonly available microcontroller and serial-peripheral devices. The interface consists of a serial clock (SCK), chip select (SCS), serial data input (SDI) and serial data output (SDO). Data is transferred one byte at a time with each register access consisting of a pair of byte transfers. Figure 5-7 below illustrates read and write operations in SPI mode.

Figure 5-7. SPI Read and Write Operations



The first byte of a pair is the command/address byte. The most significant bit of this byte indicates register read when 1 and register write when 0. The remaining seven bits of the command/address byte indicate the address of the register to be accessed.

The second byte of the pair is the data byte. During a read operation, the SDO becomes active and the 8-bit contents of the register are driven out MSB first. The SDO will be in high impedance on either the falling edge of SCK following the LSB or the rising edge of SCS, whichever occurs first.

SDI is a don't care during the data portion of read operations. During write operations, data is driven into the AT73C224-x via the SDI pin, MSB first. The SDO pin will remain in high impedance during write operations. Data always transitions with the falling edge of the clock and is latched on the rising edge. The clock should return to a logic high when no transfer is in progress.

- **Continuous clocking**: In normal operation, the SCK should not transition out of byte transfer periods. However, in test mode, the SCK is used as the main clock. This implies that all data transfers must be controlled by the assertion of the SCS pin.
- **3-wire operation**: SDI and SDO can be treated as two separate lines or wired together if the master is capable of tri-stating its output during the data-byte transfer of a read operation.
- **SCK vs internal clock rates**: It is very likely that the bit rate commanded by SCK will be much higher than the internal clock (900 kHz/64) used to read and write the registers. This implies that a minimal delay between byte transfers must be imposed to allow some time to decode the address and actually access the physical register. It is **not acceptable** to sample SCK with the internal clock.

5.3.2.2 *TWI Operation*

The TWI interface allows a microcontroller to proceed to read or write accesses to the internal registers of the AT73C224-x. Unlike the SPI, the TWI operation is based on a standard which defines a data-link layer and an addressing scheme. The TWI implementation used in the AT73C224-x conforms to this standard, with the following restrictions:

- slave only
- bit rate: 400 kbps max
- 7-bit fixed address: the default value is **1001001** (D3 is high). But the external D3 bit can modify it. When D3 is low, the 7-bit fixed address is **1001000**.
- TWCK is an input pin for the clock
- TWD is a bidirectional pin driving (open drain with external resistor connected to V_{DDIO}) or receiving the serial data.

The data put on TWD line must be 8 bits long. Data is transferred MSB first. Each byte must be followed by an acknowledgement. Each transfer begins with a Start condition and terminates with a STOP condition.

- A high-to-low transition on TWD while TWCK is high defines a START condition.
- A low-to-high transition on TWD while TWCK is high defines a STOP condition.

Figure 5-8. TWI Start/Stop Condition

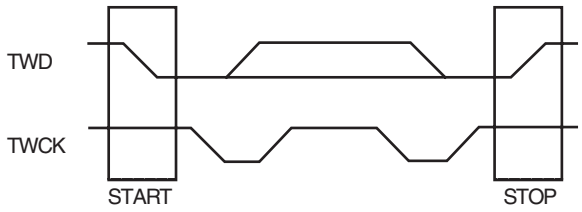
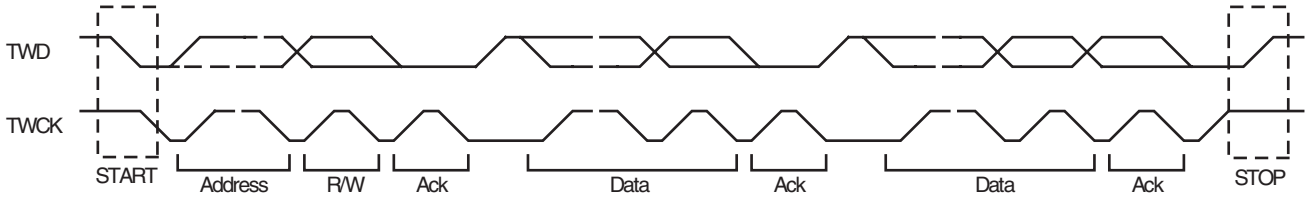


Figure 5-9. TWI Protocol



After the host initiates a START condition, it sends the 7-bit slave address, as defined above, to notify the slave device. A Read/Write bit follows (Read = 1, Write = 0). The device acknowledges each received byte. The first byte sent after device address and R/W bit is the address of the device register the host wants to read or write. For a write operation, the data follows the internal address. For a read operation, a repeated START condition needs to be generated followed by a read on the device.

Write and Read operations are shown in Figure 5-8 and Figure 5-9.

The TWI abbreviations are defined below.

S = Start	A = Acknowledge
P = Stop	N = Not Acknowledge
W = Write	ADDR = Device Address
R = Read	IADDR = Internal Address

Figure 5-10. Write Operation



Figure 5-11. Read Operation



5.3.3 Interrupt Controller

In dynamic mode, the ITB/RDY pin is an output and operates as an interrupt to an external microcontroller. The output logic is active low (a 0 level means interrupt).

Several sources can potentially trigger an interrupt:

- the RTC, when a real-time alarm event occurs (see Section 7.8 ”Real-time Clock (RTC)” for more details)
- the push-button, when its state changes
- the power monitor, when it detects a failure or main battery lower than 2.7V
- the boost, when it detects a failure
- the buck, when it detects a failure

Each of these sources can be individually masked to disable the corresponding interrupt. All the interrupt logic can also be globally disabled when the microcontroller needs to enter an uninterruptible state. The interrupt enable/disable logic is controlled through two independent registers. Refer to Section 6. ”Register Tables” for detailed register and bit assignment. IRQ_EN is used to enable the interrupts, while IRQ_DIS is used to disable the interrupts. This strategy allows the controlling software to handle the interrupt mask completely independently for each interrupt source while avoiding read-modify-write operations. The register IRQ_MSK can be read to know the current interrupt mask.

The sequence shown below in Table 5-3 shows an example of interrupt masking/unmasking.

Table 5-3. Interrupt Masking/Unmasking

Action	What it Does	Contents of IRQ_MSK
Reset	Disables all interrupts individually and globally.	00000000
Write 00000101 in IRQ_EN	Enables the RTC interrupt and the power failure interrupt individually. The interrupts are still globally masked, no interrupt can be triggered yet.	00000101
Write 00000000 in IRQ_EN	Nothing happens, only bits set at one have an effect.	00000101
Write 10000000 in IRQ_EN	Enables the interrupts globally. The ITB pin will toggle to 0 if either the RTC or the power monitor requests an interrupt.	10000101
Write 00000001 in IRQ_DIS	Disables the RTC interrupt. The power failure interrupt remains active.	10000100

Once the interrupt request is active on the ITB/RDY pin, the microcontroller has to handle it. To determine the reason for being interrupted, it reads the interrupt status register IRQ_STA (this action resets ITB/RDY). In this register, each potential interrupt source has a bit which indicates if it is responsible for triggering the request.

Once the source is identified, the microcontroller performs the handling routine in an application-dependant manner. It then needs to acknowledge the interrupt source to avoid being interrupted again for the same reason.

6. Register Tables

Default values appear beneath the bit fields in the register description tables that follow.

6.1 System Registers

6.1.1 7-bit Fixed Address for TWI

Register Name: TWIADDR
Access Type: Read-only
Address: 0x01

7	6	5	4	3	2	1	0
ALT	ADDR						
1	1	0	0	1	0	0	1

- **ADDR:**

Reads the TWI address currently in use. This field can be used to check the connectivity of the TWI, or to identify the AT73C224-x device. When ALT bit is 0, ADDR contains the alternate address (0x48). When ALT is 1, ADDR contains the default address (0x49).

- **ALT:**

Indicates if the TWI address is the default or the alternate.

0: the default address is selected.

1: the alternate address is selected.

The reset value depends on the configuration of the fuses. When the fuses are blank, the reset value is 0 (manufacturing default).

6.1.2 Button Status Register

Register Name: BT_SR
Access Type: Read-only
Address: 0x02

7	6	5	4	3	2	1	0
–	–	–	–	–	–	HIGH	LOW
						0	0

- **Low:**

0: the button input has not been seen low.

1: the button input has been seen low.

- **High:**

0: the button input has not been seen high.

1: the button input has been seen high.

6.1.3 Button Status Clear Command Register

Register Name: BT_SCCR
Access Type: Write-only
Address: 0x03

7	6	5	4	3	2	1	0
–	–	–	–	–	–	HIGH	LOW
						0	0

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **Low:**

0: no effect.

1: clears LOW in BT_SR.

- **High:**

0: no effect.

1: clears HIGH in BT_SR.

6.1.4 Button Interrupt Enable Register

Register Name: BT_IER
Access Type: Write-only
Address: 0x04

7	6	5	4	3	2	1	0
–	–	–	–	–	–	HIGH	LOW
						0	0

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **Low:**

0: no effect.

1: the button low interrupt is enabled.

- **High:**

0: no effect.

1: the button high interrupt is enabled.

6.1.5 Button Interrupt Disable Register

Register Name: BT_IDR
Access Type: Write-only
Address: 0x05

7	6	5	4	3	2	1	0
–	–	–	–	–	–	HIGH	LOW
						0	0

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **Low:**

0: no effect.

1: the button low interrupt is disabled.

- **High:**

0: no effect.

1: the button high interrupt is disabled.

6.1.6 Button Interrupt Mask Register

Register Name: BT_IMR
Access Type: Read-only
Address: 0x06

7	6	5	4	3	2	1	0
–	–	–	–	–	–	HIGH	LOW
						0	0

- **Low:**

0: the button low interrupt is disabled.

1: the button low interrupt is enabled.

- **High:**

0: the button low interrupt is disabled.

1: the button low interrupt is enabled.

6.1.7 Software Shutdown Command Register

Register Name: SHUTDN
Access Type: Write-only
Address: 0x07

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	LOW
							0

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

0: no effect.

1: shutdown the whole chip.

6.2 PMU Registers

6.2.1 BOOST Command Register

Register Name: BST_CLR
Access Type: Read/Write
Address: 0x10

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	EN(*)

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **EN:**

Writing EN to 1 starts the BOOST/SEPIC converter.

Writing En to 0 stops the BOOST/SEPIC converter.

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2).

6.2.2 BOOST Configuration Register

Register Name: BST_CFG
Access Type: Read/Write
Address: 0x11

7	6	5	4	3	2	1	0
–	–	–	–	ISHORT			
				1	0	1	1

- **ISHORT:**

Selects the overcurrent threshold. When the external sense resistor is 50 mOhms, the lookup table below applies.

ISHORT	Threshold (Amps)
0000b	0.5
0001b	1.0
0010b	1.5
0011b	2.0
0100b	2.5
0101b	3.0
0110b	3.5
0111b	4.0
1000b	4.5
1001b	5.0
1010b	5.5
1011b	6.0
1100b	6.5
1101b	7.0

At the startup, it is recommended to put 1 Amp over current threshold in order not to generate a reset of the product.

6.2.3 BOOST Voltage Register

Register Name: BST_VOLT
Access Type: Read/Write
Address: 0x12

7	6	5	4	3	2	1	0
–	–	VOUT(*)					

- **VOUT:**

Selects the output voltage of the regulator following the table below. VOUT should always be higher than VDD1 in BOOS T configuration (Application schematic 1). It can be programmed lower in SEPIC configuration (Application Schematic 2).

V_{OUT} [5:0]	V_{OUT} [V]	V_{OUT} [5:0]	V_{OUT} [V]
000000	not permitted	010101	3.3
000001	not permitted	010110	3.4
000010	not permitted	010111	3.5
000011	not permitted	011000	3.6
000100	not permitted	011001	3.7
000101	not permitted	011010	3.8
000110	not permitted	011011	3.9
000111	not permitted	011100	4.0
001000	not permitted	011101	4.1
001001	not permitted	011110	4.2
001010	not permitted	011111	4.3
001011	not permitted	100000	4.4
001100	not permitted	100001	4.5
001101	not permitted	100010	4.6
001110	not permitted	100011	4.7
001111	not permitted	100100	4.8
010000	not permitted	100101	4.9
010001	not permitted	100110	5.0
010010	not permitted	100111	5.1
010011	not permitted	101000	5.2
010100	3.2	—	

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2). The chosen value should always be higher than the supply of the cell (VDD1).

6.2.4 BUCK2 Control Register

Register Name: BCK_CTROL
Access Type: Read/Write
Address: 0x13

7	6	5	4	3	2	1	0
–	–	–	–	–	–	BYP	EN(*)

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **EN:**

Writing EN to 1 starts the BUCK converter.

Writing EN to 0 stops the BUCK converter.

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2).

- **BYP:**

Writing BYP to 1 puts the BUCK2 output voltage to VDD2.

Writing BYP to 0 configures the BUCK2 in Normal operation (default).

6.2.5 BUCK2 Configuration Register

Register Name: BCK_CFG
Access Type: Read/Write
Address: 0x14

7	6	5	4	3	2	1	0
OUTZ	SLIM	MODE		ISHORT			
1	1	0	0	1	0	0	0

- **ISHORT:**

Selects the overcurrent threshold. When the external sense resistor is 50 mOhms, the lookup table below applies.

ISHORT	Threshold (Amps)
0000b	1.01
0001b	1.08
0010b	1.15
0011b	1.22
0100b	1.29
0101b	1.36
0110b	1.43
0111b	1.5
1000b	1.57
1001b	1.64
1010b	1.71
1011b	1.78
1100b	1.85
1101b	1.92
1110b	1.99
1111b	2.06

- **MODE:**

Selects the PWM pulse skipping mode.

MODE	Operation
00	Auto
01	PWM
10	Pulse skipping
11	Pass-through

- **SLIM:**

Selects the power-up mode.

0: current limitation.

1: slow start.

- **OUTZ:**

Defines the state of the voltage output when the converter is off.

0: the output is forced to ground.

1: the output is left floating (Hz).

6.2.6 BUCK2 Voltage Register

Register Name: BCK_VOLT
Access Type: Read/Write
Address: 0x15

7	6	5	4	3	2	1	0
–	–	–	VOUT(*)				

- **VOUT:**

Selects the output voltage of the regulator following the table below.

V_{OUT} [4:0]	V_{OUT} [V]	V_{OUT} [4:0]	V_{OUT} [V]
00000	0.9	10000	1.28
00001	1.0	10001	1.42
00010	1.1	10010	1.56
00011	1.2	10011	1.7
00100	1.3	10100	1.86
00101	1.4	10101	2.00
00110	1.5	10110	2.14
00111	1.6	10111	2.29
01000	1.7	11000	2.43
01001	1.8	11001	2.57
01010	1.9	11010	2.71
01011	2.0	11011	2.86
01100	2.1	11100	3.00
01101	2.2	11101	3.14
01110	2.3	11110	3.30
01111	2.4	11111	3.42

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2).

6.2.7 LDO3 Control Register

Register Name: LDO3_CTRL
Access Type: Read/Write
Address: 0x16

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	EN(*)

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **EN:**

Writing EN to 1 starts the LDO3 regulator.

Writing EN to 0 stops the LDO3 regulator.

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2).

6.2.8 LDO3 Configuration Register

Register Name: LDO3_CFG
Access Type: Read/Write
Address: 0x17

7	6	5	4	3	2	1	0
–	–	–	–	–	MODE	OUTZ	–
					1	1	

- **OUTZ:**

Defines the state of the voltage output when the regulator is off.

0: the output is forced to ground.

1: the output is left floating (Hz).

This bit should be at 1 when LDO is on.

- **MODE:**

0: RF mode, I_{MAX} = 100 mA.

1: Smoother mode, I_{MAX} = 200 mA.

6.2.9 LDO3 Voltage Register

Register Name: LDO3_VOLT
Access Type: Read/Write
Address: 0x18

7	6	5	4	3	2	1	0
–	–	–	–	VOUT(*)			

- **VOUT**

Selects the output voltage of the regulator following the table below.

V_{OUT} [3:0]	V_{OUT} [V]
1000	1.3
0000	1.5
0001	1.6
0010	1.7
0011	1.8
0100	2.5
0101	2.6
0110	2.7
0111	2.8
1001	3.3
1010	4.9
others	–

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2).

6.2.10 LDO4 Control Register

Register Name: LDO4_CTRL
Access Type: Read/Write
Address: 0x19

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	EN(*)

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **EN:**

Writing EN to 1 starts the LDO4 regulator.

Writing EN to 0 stops the LDO4 regulator.

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2).

6.2.11 LDO4 Configuration Register

Register Name: LDO4_CFG
Access Type: Read/Write
Address: 0x1A

7	6	5	4	3	2	1	0
–	–	–	–	–	MODE	OUTZ	–
					1	1	

- **OUTZ:**

Defines the state of the voltage output when the regulator is off.

0: the output is forced to ground.

1: the output is left floating (Hz).

This bit should be at 1 when LDO is on.

- **MODE:**

0: RF mode, I_{MAX} = 100 mA.

1: Smoother mode, I_{MAX} = 200 mA.

6.2.12 LDO4 Voltage Register

Register Name: LDO4_VOLT
Access Type: Read/Write
Address: 0x1B

7	6	5	4	3	2	1	0
–	–	–	–	VOUT(*)			
				0	1	1	1

- **VOUT**

Selects the output voltage of the regulator following the table below.

V_{OUT}[3:0]	V_{OUT} [V]
1000	1.3
0000	1.5
0001	1.6
0010	1.7
0011	1.8
0100	2.5
0101	2.6
0110	2.7
0111	2.8
1001	3.3
1010	4.9
others	–

(*): Default value depends on the chosen AT73C224-x device (see Section 5.2).

6.2.13 PMU Status Register

Register Name: PMU_SR
Access Type: Read-only
Address: 0x1C

7	6	5	4	3	2	1	0
–	–	PF2	PG2	–	PF1	PG1	SHORT1
0	0	0	0	0	0	0	0

- **SHORT1:**

0: no overcurrent condition.

1: an overcurrent condition has been detected on the BOOST/SEPIC1 converter.

- **PG1:**

0: no power good condition on BOOST/SEPIC1.

1: the power good condition has been met on BOOST/SEPIC1.

- **PF1:**

0: no power failure condition on BOOST/SEPIC1.

1: the power failure condition has been met on BOOST/SEPIC1.

- **PG2:**

0: no power good condition on BUCK2.

1: the power good condition has been met on BUCK2.

- **PF2:**

0: no power failure condition on BUCK2.

1: the power failure condition has been met on BUCK2.

6.2.14 PMU Status Clear Command Register

Register Name: PMU_SCCR
Access Type: Write-only
Address: 0x1D

7	6	5	4	3	2	1	0
–	–	PF2	PG2	–	PF1	PG1	SHORT1
		–	–		–	–	–

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **SHORT1:**

0: no effect.

1: clears SHORT1 in the PMU_SR.

- **PG1:**

0: no power good condition on BOOST/SEPIC1.

1: clears PG1 in the PMU_SR.

- **PF1:**

0: no effect.

1: clears PF1 in the PMU_SR.

- **PG2:**

0: no effect.

1: clears PG2 in the PMU_SR.

- **PF2:**

0: no effect.

1: clears PF2 in the PMU_SR.

6.2.15 PMU Interrupt Enable Register

Register Name: PMU_IER
Access Type: Write-only
Address: 0x1E

7	6	5	4	3	2	1	0
–	–	PF2	PG2	–	PF1	PG1	SHORT1
–	–	0	0	–	0	0	0

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **SHORT1:**

0: no effect.

1: the overcurrent detection interrupt on BOOST/SEPIC1 is enabled.

- **PG1:**

0: no effect.

1: the power good interrupt of BOOST/SEPIC1 is enabled.

- **PF1:**

0: no effect.

1: the power fail interrupt of BOOST/SEPIC1 is enabled.

- **PG2:**

0: no effect.

1: the power good interrupt of BUCK2 is enabled.

- **PF2:**

0: no effect.

1: the power fail interrupt of BUCK2 is enabled.

6.2.16 PMU Interrupt Disable Register

Register Name: PMU_IDR
Access Type: Write-only
Address: 0x1F

7	6	5	4	3	2	1	0
–	–	PF2	PG2	–	PF1	PG1	SHORT1
		–	–		–	–	–

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **SHORT1:**

0: no effect.

1: the overcurrent detection interrupt on BOOST/SEPIC1 is disabled.

- **PG1:**

0: no effect.

1: the power good interrupt of BOOST/SEPIC1 is disabled.

- **PF1:**

0: no effect.

1: the power fail interrupt of BOOST/SEPIC1 is disabled.

- **PG2:**

0: no effect.

1: the power good interrupt of BUCK2 is disabled.

- **PF2:**

0: no effect.

1: the power fail interrupt of BUCK2 is disabled.

6.2.17 PMU Interrupt Mask Register

Register Name: PMU_IMR
Access Type: Read-only
Address: 0x20

7	6	5	4	3	2	1	0
–	–	PF2	PG2	–	PF1	PG1	SHORT1
		0	0		0	0	0

A minimum of 3 clock cycles of 15 kHz clock must be waited after any read operation before doing a new register access.

- **SHORT1:**

0: the overcurrent detection interrupt on BOOST/SEPIC1 is disabled.

1: the overcurrent detection interrupt on BOOST/SEPIC1 is enabled.

- **PG1:**

0: the power good interrupt of BOOST/SEPIC1 is disabled.

1: the power good interrupt of BOOST/SEPIC1 is enabled.

- **PF1:**

0: the power fail interrupt of BOOST/SEPIC1 is disabled.

1: the power fail interrupt of BOOST/SEPIC1 is enabled.

- **PG2:**

0: the power good interrupt of BUCK2 is disabled.

1: the power good interrupt of BUCK2 is enabled.

- **PF2:**

0: the power fail interrupt of BUCK2 is disabled.

1: the power fail interrupt of BUCK2 is enabled.

6.3 Interrupt Registers

6.3.1 Interrupt Enable Register

Register Name: IRQ_EN
Access Type: Write-only
Address: 0x30

7	6	5	4	3	2	1	0
ALL	–	DC2	DC1	–	PWR	PB	RTC
–		–	–		–	–	–

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **RTC:**

Enables the RTC interrupt when written to 1.

Writing 0 has no effect.

- **PB:**

Enables the push-button interrupt when written to 1.

Writing 0 has no effect.

- **PWR:**

Enables the power failure interrupt when written to 1.

Writing 0 has no effect

- **DC1:**

Enables the BOOST/SEPIC1 interrupt when written to 1.

Writing 0 has no effect.

- **DC2:**

Enables the BUCK2 interrupt when written to 1.

Writing 0 has no effect.

- **ALL:**

Writing to 1 globally enables all the interrupt sources that had been previously enabled individually. The interrupt setting for each source is restored.

Writing 0 has no effect.

6.3.2 Interrupt Disable Register

Register Name: IRQ_DIS
Access Type: Write-only
Address: 0x31

7	6	5	4	3	2	1	0
ALL	–	DC2	DC1	–	PWR	PB	RTC
–		–	–		–	–	–

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access.

- **RTC:**

Disables the RTC interrupt when written to 1.

Writing 0 has no effect.

- **PB:**

Disables the push-button interrupt when written to 1.

Writing 0 has no effect.

- **PWR:**

Disables the power failure interrupt when written to 1.

Writing 0 has no effect

- **DC1:**

Disables the BOOST/SEPIC1 interrupt when written to 1.

Writing 0 has no effect.

- **DC2:**

Disables the BUCK2 interrupt when written to 1.

Writing 0 has no effect.

- **ALL:**

Writing to 1 globally disables all the interrupt sources. The individual setting of each interrupt source is saved.

Writing 0 has no effect.

6.3.3 Interrupt Mask Register

Register Name: IRQ_MSK
Access Type: Read-only
Address: 0x32

7	6	5	4	3	2	1	0
ALL	–	DC2	DC1	–	PWR	PB	RTC
0	0	0	0	0	0	0	0

This register summarizes the result of the successive interrupt enable/disable commands performed by writing into IRQ_EN/IRQ_DIS.

- **RTC:**

0: the RTC interrupt is masked.

1: the RTC interrupt is unmasked.

- **PB:**

0: the push-button interrupt is masked.

1: the push-button interrupt is unmasked.

- **PWR:**

0: the power failure interrupt is masked.

1: the power failure interrupt is unmasked.

- **DC1:**

0: the BOOST/SEPIC1 interrupt is masked.

1: the BOOST/SEPIC1 interrupt is unmasked.

- **DC2:**

0: the BUCK2 interrupt is masked.

1: the BUCK2 interrupt is unmasked.

- **ALL:**

0: the interrupt sources are globally masked.

1: the interrupt sources are globally unmasked.

6.3.4 Interrupt Status Register

Register Name: IRQ_STA
Access Type: Read-only
Address: 0x33

7	6	5	4	3	2	1	0
–	–	DC2	DC1	–	PWR	PB	RTC
0	0	0	0	0	0	0	0

A minimum of 3 clock cycles of 15 kHz clock must be waited after any write operation before doing a new register access. Reading IRQ de-asserts the ITB signal.

- **RTC:**

1: signals a pending interrupt request from the RTC.

- **PB:**

1: signals a pending interrupt request from the push-button.

- **PWR:**

1: signals a pending interrupt request from the power monitor.

- **DC1:**

1: signals a pending interrupt request from the BOOST/SEPIC1.

- **DC2:**

1: signals a pending interrupt request from the BUCK2.

6.4 RTC Registers

6.4.1 RTC Control Register

Register Name: RT_CR
Access Type: Read/Write
Address: 0x40

7	6	5	4	3	2	1	0
CALEVSEL		TIMEVSEL		–	–	UPDCAL	UPDTIM
0	0	0	0			0	0

- **UPDTIM:**

Writing 1 requests the RTC to stop the time counter so that it can be safely updated. The time counter is actually stopped only when ACKUPD is set in RTC_SR.

Writing 0 restarts the time counter.

- **UPDCAL:**

Writing 1 requests the RTC to stop the calendar counter so that it can be safely updated. The calendar counter is actually stopped only when ACKUPD is set in RTC_SR.

Writing 0 restarts the calendar counter.

- **TIMEVSEL:**

Selects the type of event to cause TIMEV to change in RTC_SR.

00	minute change
01	hour change
10	every day at midnight
11	every day at noon

- **CALEVSEL:**

Selects the type of event to cause CALEV to change in RTC_SR.

00	week change	every Monday	at time 00:00:00
01	month change	every 1st of each month	at time 00:00:00
10 11	year change	every 1st of January	at time 00:00:00

6.4.2 RTC Reset Register

Register Name: RT_RR
Access Type: Read/Write

Address: 0x41

7	6	5	4	3	2	1	0
RST	–	–	–	–	–	–	–
0							

RST:

RST = 0, Normal Operation

RST=1, Reset the RTC

6.4.3 RTC Mode Register

Register Name: RT_MR
Access Type: Read/Write
Address: 0x44

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	HRMOD
							0

- **HRMOD:**

0: 24-hour mode.

1: 12-hour mode.

The three **Time** writing registers are only writable concomitantly and must be written in the order as shown below:

1. **RT_SEC**
2. **RT_MIN**
3. **RT_HOUR**

6.4.4 Real-time Second Register

Register Name: RT_SEC
Access Type: Read/Write
Address: 0x48

7	6	5	4	3	2	1	0
–	SEC						
	0	0	0	0	0	0	0

- **SEC:**

The range is 0-59 encoded in Binary Coded Decimal (BCD). The lowest four bits encode the units, the higher bits encode the tens.

This field must not be written unless the time counter has been stopped.

6.4.5 Real-time Minute Register

Register Name: RT_MIN
Access Type: Read/Write
Address: 0x49

7	6	5	4	3	2	1	0
–	MIN						
	0	0	0	0	0	0	0

- **MIN**

The range is 0-59 encoded in BCD. The lowest four bits encode the units, the higher bits encode the tens. This field must not be written unless the time counter has been stopped.

6.4.6 Real-time Hour Register

Register Name: RT_HOUR
Access Type: Read/Write
Address: 0x4A

7	6	5	4	3	2	1	0
–	AMPM	HOUR					
	0	0	0	0	0	0	0

- **HOUR:**

Depending on bit AMPM, the range can be 1-12 or 0-23, encoded in BCD. The lowest four bits encode the units, the higher bits encode the tens. This field must not be written unless the time counter has been stopped.

- **AMPM:**

This bit controls/reflects the AM/PM indicator in 12-hour mode.

0: AM.

1: PM.

The four **Date** writing registers are only writable concomitantly and must be written in the order as shown below:

1. **RT_CENT**
2. **RT_YEAR**
3. **RT_MONTH**
4. **RT_DATE**

6.4.7 Real-time Century Register

Register Name: RT_CENT
Access Type: Read/Write
Address: 0x4C

7	6	5	4	3	2	1	0
–	–	CENT					
		0	1	1	0	0	1

- **CENT:**

The range is 19 - 20, encoded in BCD. The lowest four bits encode the units, the higher bits encode the tens.

6.4.8 Real-time Year Register

Register Name: RT_YEAR
Access Type: Read/Write
Address: 0x4C

7	6	5	4	3	2	1	0
YEAR							
1	0	0	1	1	0	0	0

- **YEAR:**

The range is 1 - 12, encoded in BCD. The lowest four bits encode the units, the higher bits encode the tens.

6.4.9 Real-time Month Register

Register Name: RT_Month
Access Type: Read/Write
Address: 0x4E

7	6	5	4	3	2	1	0
DAY			MONTH				
1	0	0	0	0	0	0	1

- **MONTH:**

The range is 1 - 12, encoded in BCD. The lowest four bits encode the units, the higher bits encode the tens.

- **DAY:**

The range is 1-7 and represents the day of the week. The relationship between the coding of this field and the actual day of the week, is user-defined. Especially, writing to this bit has no effect on the date counter.

6.4.10 Real-time Date Register

Register Name: RT_DATE
Access Type: Read/Write
Address: 0x4F

7	6	5	4	3	2	1	0
DAY			DATE				
1	0	0	1	1	0	0	0

- **DATE:**

The range is 1 - 31, encoded in BCD and represents the day of the month. The lowest four bits encode the units, the higher bits encode the tens.

The three **Time Alarm** writing registers are only writable concomitantly and must be written in the order as shown below:

1. **RT_SECA**
2. **RT_MINA**
3. **RT_HOURA**

6.4.11 Real-time Second Alarm Register

Register Name: RT_SECA
Access Type: Read/Write
Address: 0x50

7	6	5	4	3	2	1	0
SECEN	SEC						
0	0	0	0	0	0	0	0

- **SEC:**

This field is the alarm field corresponding to the BCD-encoded second counter.

- **SECEN**

0: the second-matching alarm is disabled.

1: the second-matching alarm is enabled.

6.4.12 Real-time Minute Alarm Register

Register Name: RT_MINA
Access Type: Read/Write
Address: 0x51

7	6	5	4	3	2	1	0
MINEN	MIN						
0	0	0	0	0	0	0	0

- **MIN:**

This field is the alarm field corresponding to the BCD-encoded minute counter.

- **MINEN**

0: the minute-matching alarm is disabled.

1: the minute-matching alarm is enabled.

6.4.13 Real-time Hour Alarm Register

Register Name: RT_HOURA
Access Type: Read/Write
Address: 0x52

7	6	5	4	3	2	1	0
HOUREN	AMPM	HOUR					
0	0	0	0	0	0	0	0

- **HOUR:**

This field is the alarm field corresponding to the BCD-encoded hour counter.

- **AMPM:**

This field is the alarm field corresponding to the BCD-encoded hour counter.

- **HOUREN**

0: the hour-matching alarm is disabled.

1: the hour-matching alarm is enabled.

The two **Date Alarm** writing registers are only writable concomitantly and must be written in the order as shown below:

1. **RT_MONTHA**
2. **RT_DATEA**

6.4.14 Real-time Month Alarm Register

Register Name: RT_MONTHA
Access Type: Read/Write
Address: 0x56

7	6	5	4	3	2	1	0
MTHEN	–	–	MONTH				
0			0	0	0	0	1

- **MONTH:**

This field is the alarm field corresponding to the BCD-encoded month counter.

- **MTHEN**

0: the month-matching alarm is disabled.

1: the month-matching alarm is enabled.

6.4.15 Real-time DATE Alarm Register

Register Name: RT_DATEA
Access Type: Read/Write
Address: 0x56

7	6	5	4	3	2	1	0
DATEEN	–	DATE					
0		0	0	0	0	0	1

- **DATE:**

This field is the alarm field corresponding to the BCD-encoded day of the month counter.

- **DATEEN:**

0: the day of the month-matching alarm is disabled.

1: the day of the month-matching alarm is enabled.

6.4.16 RTC Status Register

Register Name: RTC_SR
Access Type: Read-only
Address: 0x58

7	6	5	4	3	2	1	0
–	–	–	CALEV	TIMEV	SEC	ALARM	ACKUPD
			0	0	0	0	0

- **ACKUPD:**

0: time and calendar registers should not be updated.

1: time and calendar can be updated safely (clock stopped).

- **ALARM:**

0: no alarm matching condition occurred.

1: an alarm matching condition occurred.

- **SEC:**

0: no second event has occurred since last clear.

1: at least one second event occurred since last clear.

- **TIMEV:**

0: no time event has occurred since last clear.

1: at least one time event occurred since last clear.

The time event is selected by the TIMEVSEL field in RTC_CR and can be any of the following events: minute change, hour change, noon, midnight (day change).

- **CALEV:**

0: no calendar event occurred since last clear.

1: at least one calendar event occurred since last clear.

The calendar event is selected in the CALEVSEL field in RTC_CR and can be any of the following events: week change, month change, or year change.

6.4.17 RTC Status Clear Command Register

Register Name: RTC_SCCR
Access Type: Write-only
Address: 0x5C

7	6	5	4	3	2	1	0
–	–	–	CALCLR	TIMCLR	SECCLR	ALRCLR	ACKCLR
			0	0	0	0	0

- **ACKCLR:**

0: no effect.

1: clears the ACKUPD bit in RTC_SR.

- **ALCLR:**

0: no effect.

1: clears the ALARM bit RTC_SR.

- **SECCLR:**

0: no effect.

1: clears the SEC bit RTC_SR.

- **TIMCLR:**

0: no effect.

1: clears the TIMEV bit RTC_SR.

- **CALCR:**

0: no effect.

1: clears the CALEV bit RTC_SR.

6.4.18 RTC Interrupt Enable Register

Register Name: RTC_IER
Access Type: Write-only
Address: 0x60

7	6	5	4	3	2	1	0
–	–	–	CALEN	TIMEN	SECEN	ALREN	ACKEN
			0	0	0	0	0

- **ACKEN:**

0: no effect.

1: the acknowledge for update interrupt is enabled.

- **ALREN:**

0: no effect.

1: the alarm interrupt is enabled.

- **SECEN:**

0: no effect.

1: the second periodic interrupt is enabled.

- **TIMEN:**

0: no effect.

1: the selected time event interrupt is enabled.

- **CALEN:**

0: no effect.

1: the selected calendar event interrupt is enabled.

6.4.19 RTC Interrupt Disable Register

Register Name: RTC_IDR
Access Type: Write-only
Address: 0x64

7	6	5	4	3	2	1	0
–	–	–	CALDIS	TIMDIS	SECDIS	ALRDIS	ACKDIS
			0	0	0	0	0

- **ACKDIS:**

0: no effect.

1: the acknowledge for update interrupt is disabled.

- **ALRDIS:**

0: no effect.

1: the alarm interrupt is disabled.

- **SECDIS:**

0: no effect.

1: the second periodic interrupt is disabled.

- **TIMDIS:**

0: no effect.

1: the selected time event interrupt is disabled.

- **CALDIS:**

0: no effect.

1: the selected calendar event interrupt is disabled.

6.4.20 RTC Interrupt Mask Register

Register Name: RTC_IMR
Access Type: Read-only
Address: 0x68

7	6	5	4	3	2	1	0
–	–	–	CAL	TIM	SEC	ALR	ACK
			0	0	0	0	0

- **ACK:**

0: the acknowledge for update interrupt is disabled.

1: the acknowledge for update interrupt is enabled.

- **ALR:**

0: the alarm interrupt is disabled.

1: the alarm interrupt is enabled.

- **SEC:**

0: the second periodic interrupt is disabled.

1: the second periodic interrupt is enabled.

- **TIM:**

0: the selected time event interrupt is disabled.

1: the selected time event interrupt is enabled.

- **CAL:**

0: the selected calendar event interrupt is disabled.

1: the selected calendar event interrupt is enabled.

6.4.21 RTC Valid Entry Register

Register Name: RTC_VER
Access Type: Read-only
Address: 0x6C

7	6	5	4	3	2	1	0
–	–	–	–	NVCALA	NVTIMA	NVCAL	NVTIM

- **NVTIM:**

0: no invalid data has been detected in the time registers.

1: invalid data has been detected.

- **NVCAL:**

0: no invalid data has been detected in the calendar registers.

1: invalid data has been detected.

- **NVTIMA:**

0: no invalid data has been detected in the time alarm registers.

1: invalid data has been detected.

- **NVCALA:**

0: no invalid data has been detected in the calendar alarm registers.

1: invalid data has been detected.

7. Electrical Characteristics

With external components as listed in Table 4-1, Ta = -40°C to 85°C typical values are at Ta = 25°C (unless otherwise specified).

7.1 Absolute Maximum Ratings

Table 7-1. Absolute Maximum Ratings

Operating Temperature (Industrial).....-40°C to + 85°C
Storage Temperature.....-55°C to + 150°C
Power Supply Input.....-0.3V to + 5.5V
I/O Input..... -0.3V to + 5.5V
ESD (all pins)-.....2 KV

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Table 7-2. Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Operating Temperature		-40	85	°C
Power Supply Input		2.8	5.25	V

7.3 Digital I/Os

Digital I/Os are supplied by VDDIO. VDDIO is an input and must be externally connected.

.

Table 7-3. VDDIO Referred Digital I/Os

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDIO	Operating Supply Voltage		1.75	3.6	5.25	V
V_{IL}	Input Low Level Voltage		-0.3		0.3x VDDIO	V
V_{IH}	Input High Level Voltage		0.7x VDDIO		VDDIO + 0.3	V
V_{OL}	Output Low Level Voltage		0.75x VDDIO			V
V_{OH}	Output high Level Voltage				0.25x VDDIO	V
Io	Output Current				8	mA
Rp	Pull-Up or Pull Down resistance	when applicable	90	120	150	kΩ

VDDIO referred pins EN, D1, D3, D4: CMOS inputs. Only VIH and VIL parameters are applicable.

VDDIO referred pins POK: CMOS output. Only VOL, VOH parameters are applicable.

VDDIO referred pin ITB, D2: CMOS BiDir. All parameters applicable.

7.4 Current Consumption Versus Modes

Table 7-4. Quiescent Current in Different Operating Modes

Status	Conditions	Battery Current	
		Typ	Max
Off	No battery is present	N/A	N/A
Backup mode	No Main Battery is present Backup battery present (and charged): . Running: RTC (dig + oscillator 32 kHz) - supply: vbackup pin	 1 µA	 2 µA
Stand by	Main Battery plugged in and higher than 2.8V Backup battery present (and charged) . Power supplies off (BOOST1, BUCK2, LDO3, LDO4) . Running: RTC, LDO_RTC - supply: vbat_ldortc POR, LPBG, VMON - supply: vdd0 pin	 4µA 9µA	 7µA 17µA

7.5 BOOST1: Step-up Converter

Table 7-5. BOOST1 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD1	Operating Supply Voltage		2.8	3.6	5.25	V
Fs	Converter Frequency		400	900	1400	kHz
I_O	Load Current				1	A
VO1	Output Voltage	BST_VOLT register (@12) - Step 100 mV VDD1 < VO1	3.2		5.2	V
Error	Output voltage precision	Iload > 100 mA	-10		-10	%
I_{sc}	Shutdown Current	BST_CLR register (@10); EN = 0			1	µA
I_{LIM}	Current Limitation	BST_CFG register (@11)	0.5		7(1)	A
η2.8_3.3_1A	Efficiency at VDD1 = 2.8 V	I_O = 1 A, VDD1 = 2.8V, VO1 = 3.3V		90		%
h3.6_5.2_1A	Efficiency at VDD1 = 3.6 V	I_O = 1 A, VDD1 = 3.3V, VO1 = 5.2V		85		%
t_{START}	Start-up Time	No load		200		µs
$\Delta V_{O1_5.2V}$	Ripple Voltage	peak-to-peak, I_O = 1 A, VO1 = 5.2V Bandwidth = 20 MHz		200		mV
$\Delta V_{O1_5.2V}$	Static Line Regulation	VDD1: 2.8 to 4.2V - I_O = 1 A - VO1 = 5.2V		200		mV
$\Delta V_{O1_5.2V}$	Static Load Regulation	VDD1: 3.6V - I_O: 100 mA to 900 mA - VO1 = 5.2V		50		mV

Note: 1. Before the BOOST is turned on, it is recommended to establish low current limitation (typic: 1 Amp) to avoid current peak on main supply.

7.5.1 BOOST1: Typical Characteristics

Figure 7-1. Efficiency BOOST1 - VO1 = 5V -

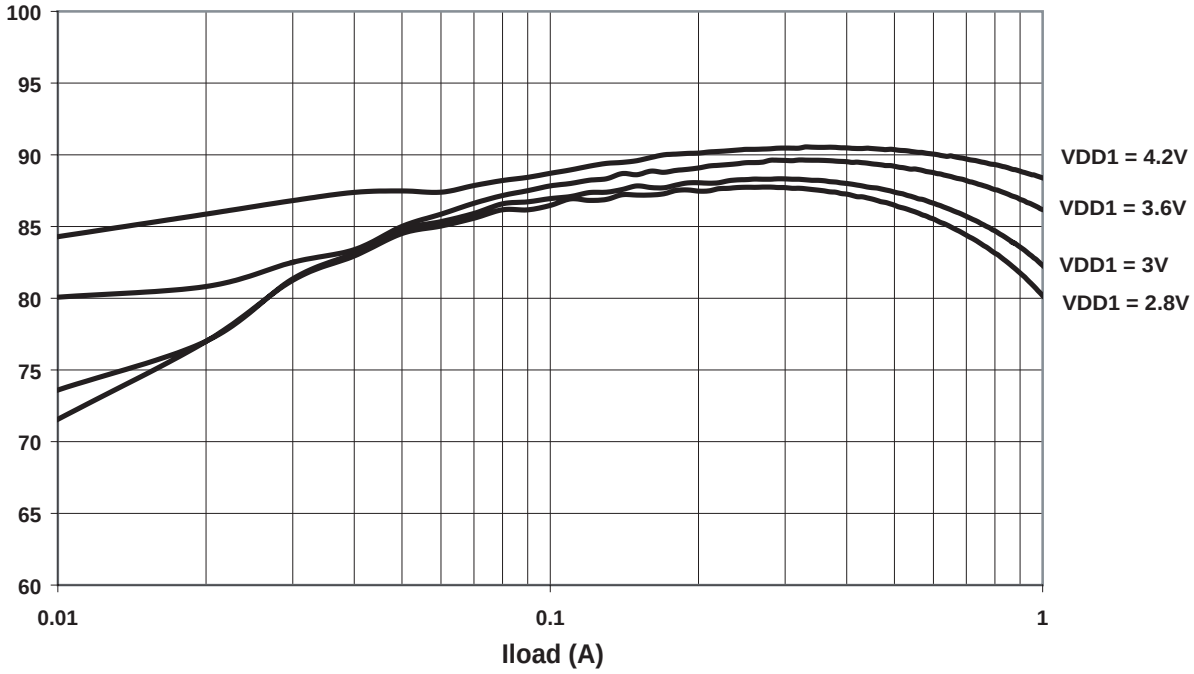
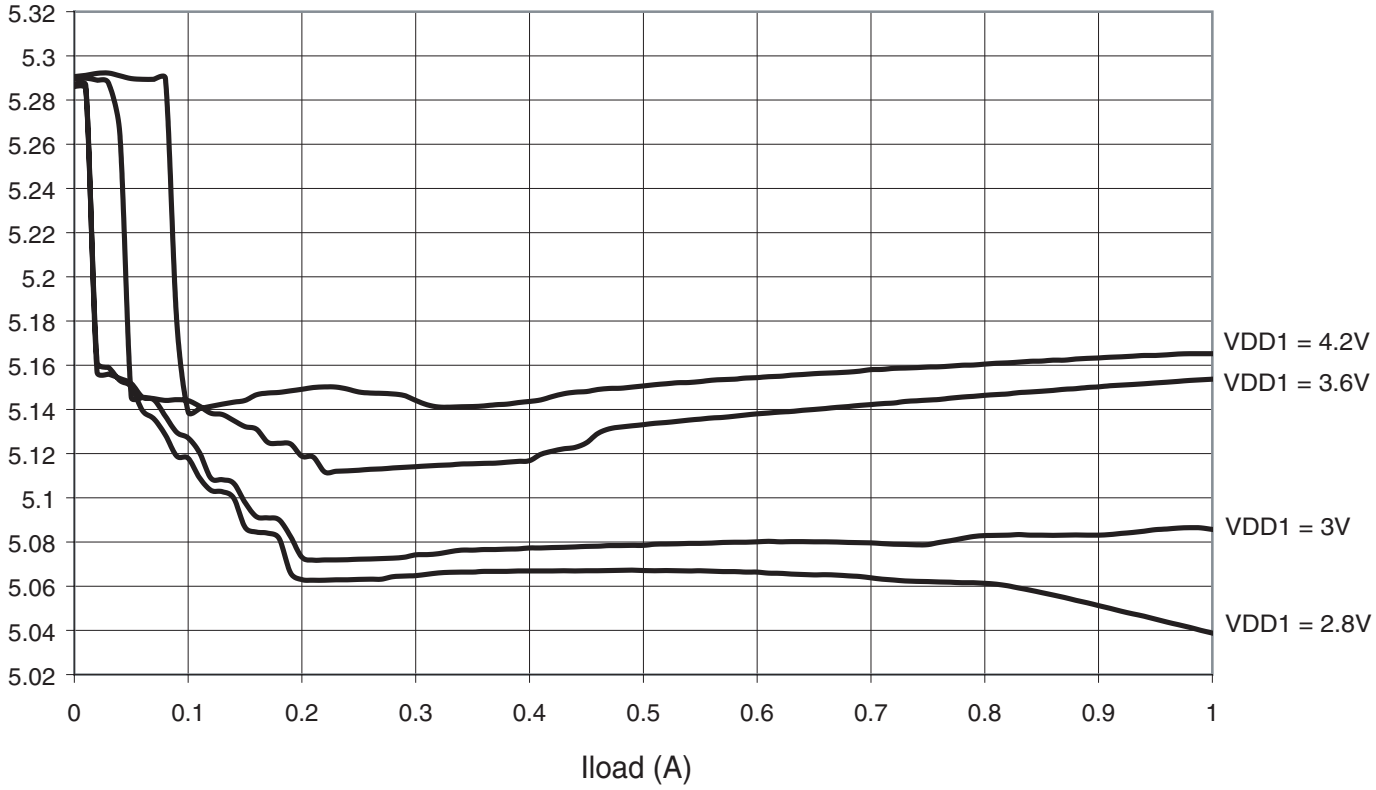


Figure 7-2. Load Regulation BOOST1 - VO1 = 5V -



The BOOST1 cell can be implemented using proper external components. (See Figure 4-3 “Application Schematic 3: BOOST in SEPIC Configuration (BUCK/BOOST)”.)

7.6 BUCK2: Step-down Converter

Table 7-6. BUCK2 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD2	Operating Supply Voltage		2.8	3.6	5.25	V
Fs	Converter Frequency	PWM mode	400	900	1400	kHz
I_{LOAD}	Load Current				0.5	A
VO2	Output Voltage	BCK_VOLT register (@15) - Step 100mV VDD2 > (VO2 + 0.2V)	0.9(1)		3.4	V
Error	Output Voltage Precision		-10		10	%
I_{SC}	Shutdown Current	BCK_CTROL register (@13), EN = 0		1	6	µA
I_{STB}	Stand-by Current	BCK_CTROL register (@13), EN = 1, clock not present		20	50	µA
I_{MAX}	Short Circuit Current	BCK_CFG register (@14)	1		2	A
$I_{PWM-PSK}$	PWM – Pulse SKipping Current Threshold	Automatic mode- VDD2 = 3.6V- VO2 = 1.8V		70		mA
Δv	Ripple Voltage	PWM mode		10		mV
T_R	Rise Time	Bandgap already started, slow-start power up selected		1		ms
ΔV_{DC}	Static Line Regulation	I_{LOAD} = 500 mA, VDD2 from 2.8V to 5V PWM mode		80		mV
ΔV_{DC}	Static Load Regulation	1 mA <iload<500 mA, PWM mode		40		mV

Note: 1. for device commanded in Dynamic Mode only. For devices commanded in Static Mode, the minimum voltage is 1.8V.

The BUCK2 is a Pulse Width Modulator (PWM) / Pulse-Skipping (PSK) synchronous regulator that can be used to provide an accurate 0.9V to 3.4V programmable output voltage at 500 mA of maximum load current.

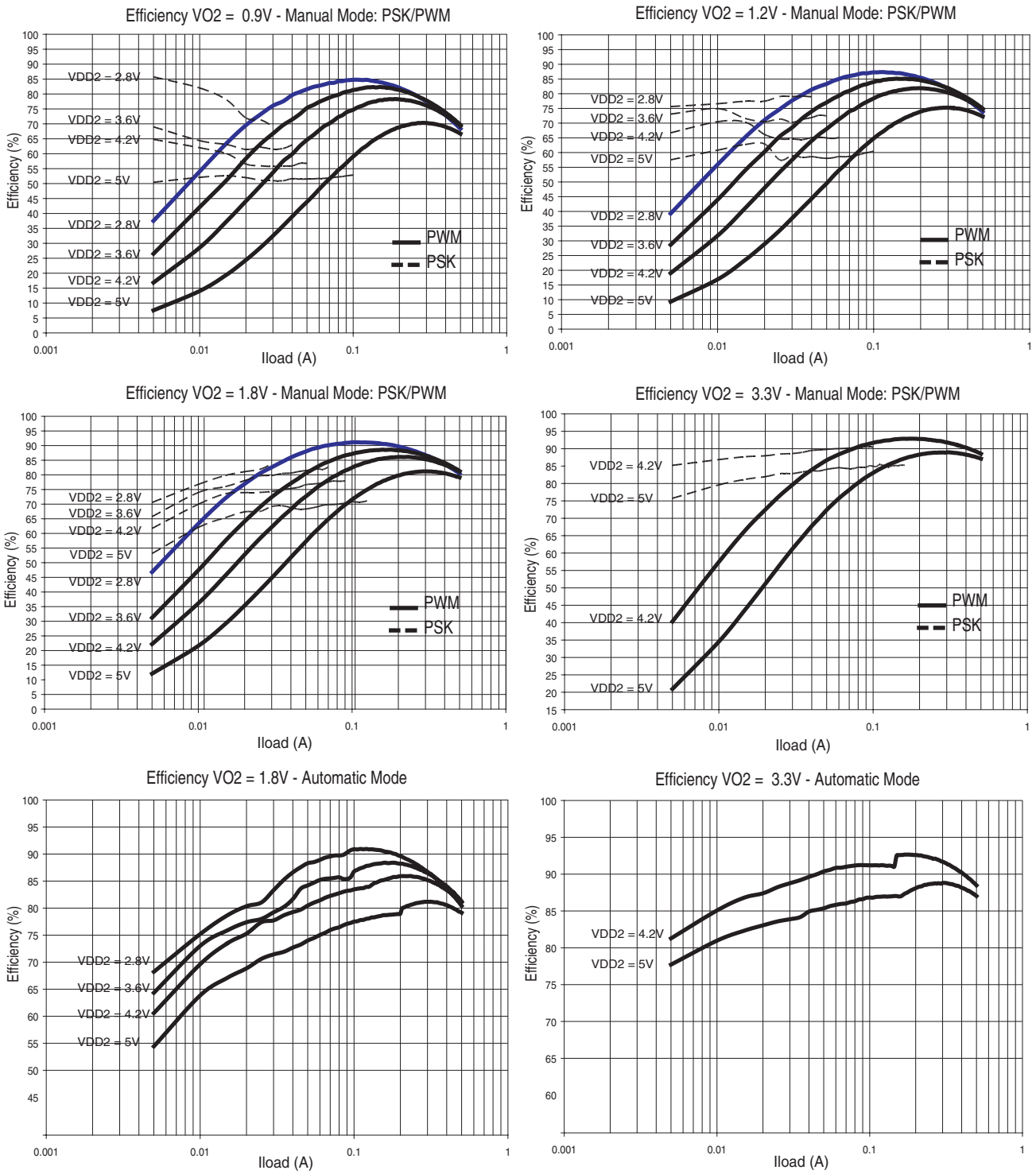
Integrated current sensing is used to sense the DC/DC converter load current used for the over-current circuit protection and for the PWM / PSK mode selector.

By default, the BUCK2 is in Automatic Mode: according to the load current value, the regulator is either in Pulse-Skipping mode (light load) or in PWM mode (high load). In dynamic mode, the user can select PWM or PSK mode, using the bits 4 and 5 of the BCK_CFG register (see Section 6 Register Tables).

Note that the Automatic mode should not be used for output voltages below 1.8V.

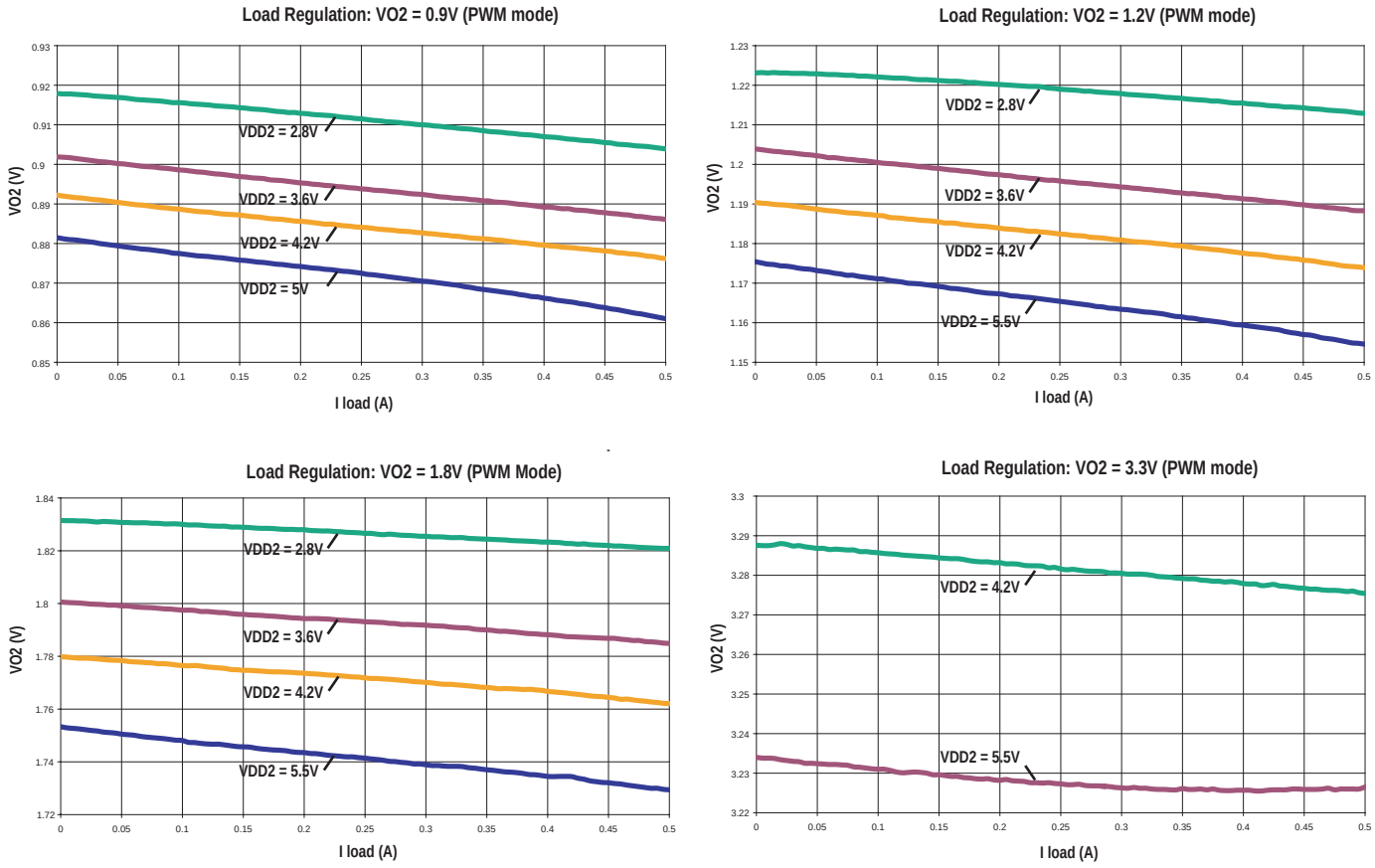
7.6.1 BUCK2: Typical Characteristics

Figure 7-3. Efficiency Manual/Automatic Modes



7.6.2 BUCK2: Load Regulation of VO2

Figure 7-4. Load Regulation



7.7 LDO3 & LDO4

LDO3 and LDO4 are low-drop-out voltage regulators that can provide a 1.3V, 1.5V to 1.8V (step 100 mV), 2.5V to 2.8V (100 mV step) or 3.3V output voltage.

Two kinds of applications are defined: “RF” mode (high PSRR and low noise) with 100 mA maximum load and “Smoother” mode with 200 mA maximum load.

By default, the LDOs are configured in RF mode. If the load is higher than 100 mA, the user should pass into Smoother mode (see the register tables in Section 6.2.8 ”LDO3 Configuration Register” and Section 6.2.11 ”LDO4 Configuration Register”).

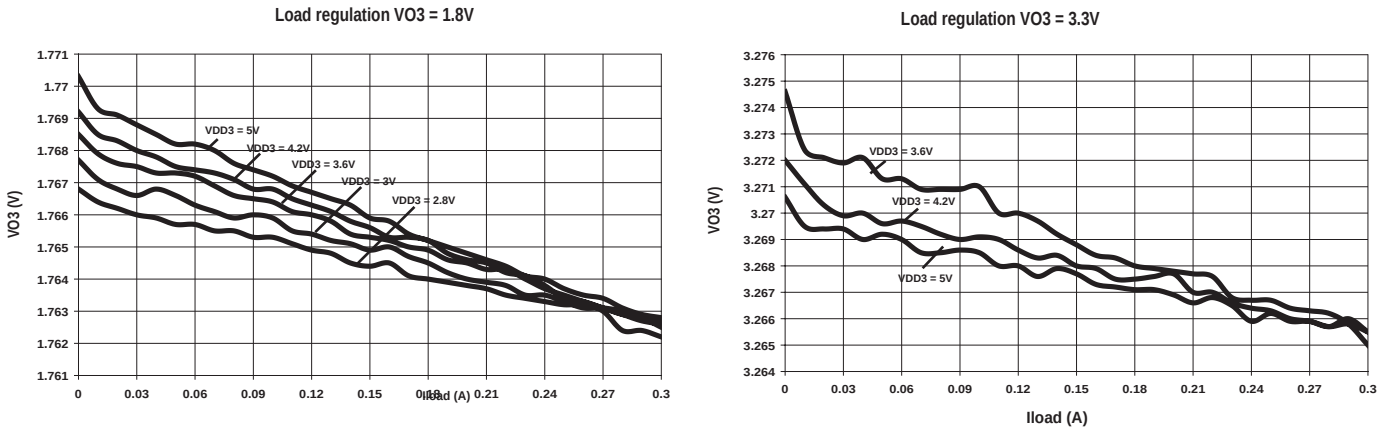
An external 2.2 µF ceramic capacitor is needed for the stability of each LDO.

Table 7-7. LDO3 and LDO4 Electrical Characteristics

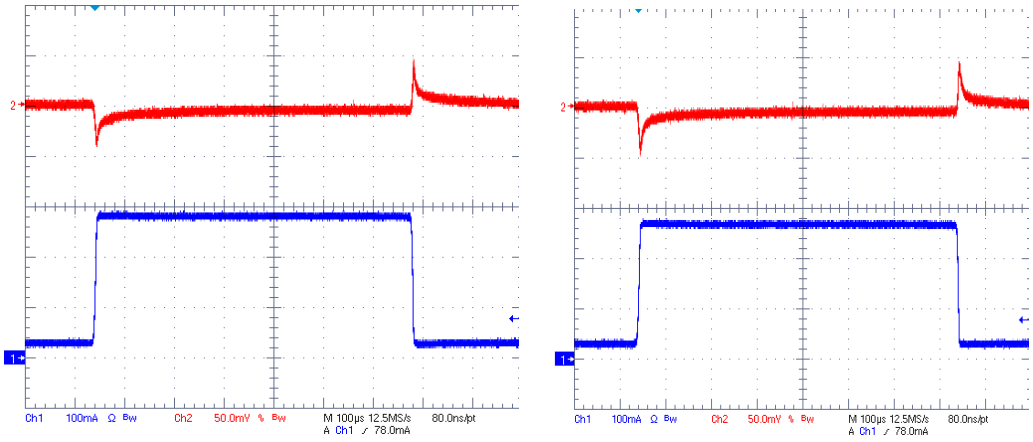
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD3&4	Operating Supply Voltage		2.8	3.6	5.25	V
I_{LOAD_S}	Smoother Load current	In Smoother mode	0		200	mA
I_{LOAD_RF}	RF Load current	In RF mode	0		100	mA
VO3, VO4	Output Voltage	Selection in LDO3_VOLT @ 18 and LDO4_VOLT @ 1B VDD3 > VO3 + 200mV VDD4 > VO4 + 200mV	1.3		3.3	V
ΔV_o	Accuracy	I_{LOAD}=10mA	-8		8	%
I_{SC}	Shutdown Current	GND output (LDO3_CFG@17 and LDO4_CFG@1A)			1	µA
I_{QQ}	Quiescent Current	No load		20		µA
t_R	Rise Time			100		µs
ΔV_{DC}	Line Regulation Static	2.8V < VDD3 < 5.25V, full load		10		mV
ΔV_{DC}	Load Regulation Static	10 mA <I_{LOAD} <100 mA		10	5	mV
n	Output Noise	In RF mode Bandwidth: [22 - 80kHz]		1.5		µVrms
PSRR	Power Supply Rejection Ratio	In RF mode: I_{LOAD}=100mA, 100 Hz I_{LOAD}=100mA, 1kHz I_{LOAD}=100mA, 10kHz I_{LOAD}=100mA, 100kHz		 70 65 55 45		 dB dB dB dB

7.7.1 LDO3 and LDO4: Typical Characteristics

Figure 7-5. LDO Load Regulation



Shown below is VO3 Ripple (same as VO4) in response to a load current pulse from 10 mA to 200 mA.



Channel 2: VO3 = 1.8V and VO3 = 3.3V (50mV/div)

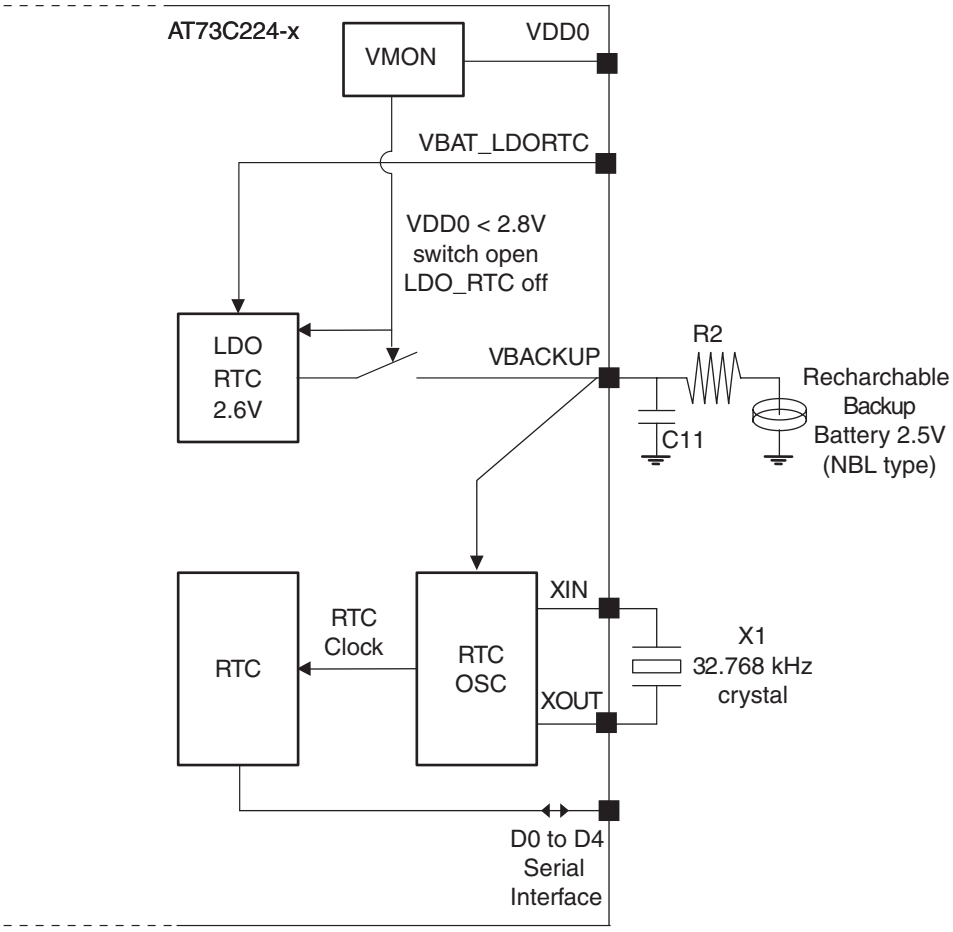
Channel 1: Iload = 10 mA - 200 mA (100 mA/div)

7.8 Real-time Clock (RTC)

The Real-time Clock architecture is shown in Figure 7-6 and is comprised of the following blocks: 2.6V LDO_RTC voltage regulator with backup switch, RTC oscillator and RTC block.

7.8.1 Block Diagram

Figure 7-6. RTC Block Diagram



The LDO_RTC is used to charge the backup battery at 2.6V. When the main battery is plugged in, the LDO is enabled and the backup switch is closed, thus charging the battery. If the VBACKUP initial value is lower than the minimum backup voltage admissible (1.8V typical), an active low reset is generated on reset signal.

The C11 capacitor is used for LDO compensation while the R2 resistor limits the charge current for the backup battery.

The RTC oscillator is suited to work with a 32.768 kHz crystal oscillator and generates the 32.768 kHz clock for the RTC. The RTC block provides seconds, minutes, hours, days, date, month, and year information. RTC time data is stored into a register that can be accessed via the AT73C224-x device serial interface.

7.8.2 LDO RTC

Table 7-8. LDO RTC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_LDORTC}	Operating Supply Voltage		2.8		5.25	V
V_{BACKUP}	Output Voltage	Vbat_ldortc present	2.55	2.6	2.65	V
I_{OUT}	Load Current	Dc load current			2	mA
I_{QQ}	Battery Quiescent Current	en = 1		3	5	µA
I_{BKQQ}	Backup Battery Quiescent Current	en = 0		200	300	nA
I_{SC}	Shutdown Current				1	µA
T_S	Start-up Time				1	ms
V_{TH}	Reset Threshold	reset is active low		1.8		V

The LDO_Backup is a low drop out voltage regulator that is used to charge a 2.5V RTC rechargeable backup battery (type NBL621). The max load current is 2 mA. An external 1 µF ceramic capacitor (C11) is needed for compensation.

7.8.3 RTC Oscillator

Table 7-9. RTC Oscillator Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BACKUP}	Supply voltage		1.75		2.65	
F_{CK}	Operating frequency			32.768		kHz
Duty	Duty cycle		40	50	60	%
Ton	Startup time				900	ms
V_{SIN}	Level sinus wave on xin	R_S = 50 KΩ	160	260	360	mVpp
D_{RV}	Drive level	R_S = 50 KΩ			0.1	µW
I	Current dissipation	OFF			5	nA
		ON		0.8	2	µA
A_{CC}	Accuracy	T = 25 °C			3	mn/month
R_S	Equivalent series resistance	Crystal @ 32.768kHz			50	kΩ
C_{MT}	Motional capacitance	Crystal @ 32.768kHz	1		3	fF
C_{SHUNT}	Shunt capacitance	Crystal @ 32.768kHz	0.6		2	pF
C_{LOAD}	Load capacitance	Crystal @ 32.768kHz	6		12.5	pF

The RTC Oscillator is a low-frequency, 2-Pad, Pierce-type Xtal oscillator, optimized for 32.768 kHz crystal. For operation with 6 pF load capacitance crystals, no external components are needed on “xin” and “xout”. It may be necessary to add external capacitors on “xin” and “xout” to ground in special cases, for example, to exactly set the frequency or for crystals with a load capacitance superior to 6 pF. The “clock” output is low during standby. “xin” and “xout” must not be used to drive other circuitry.

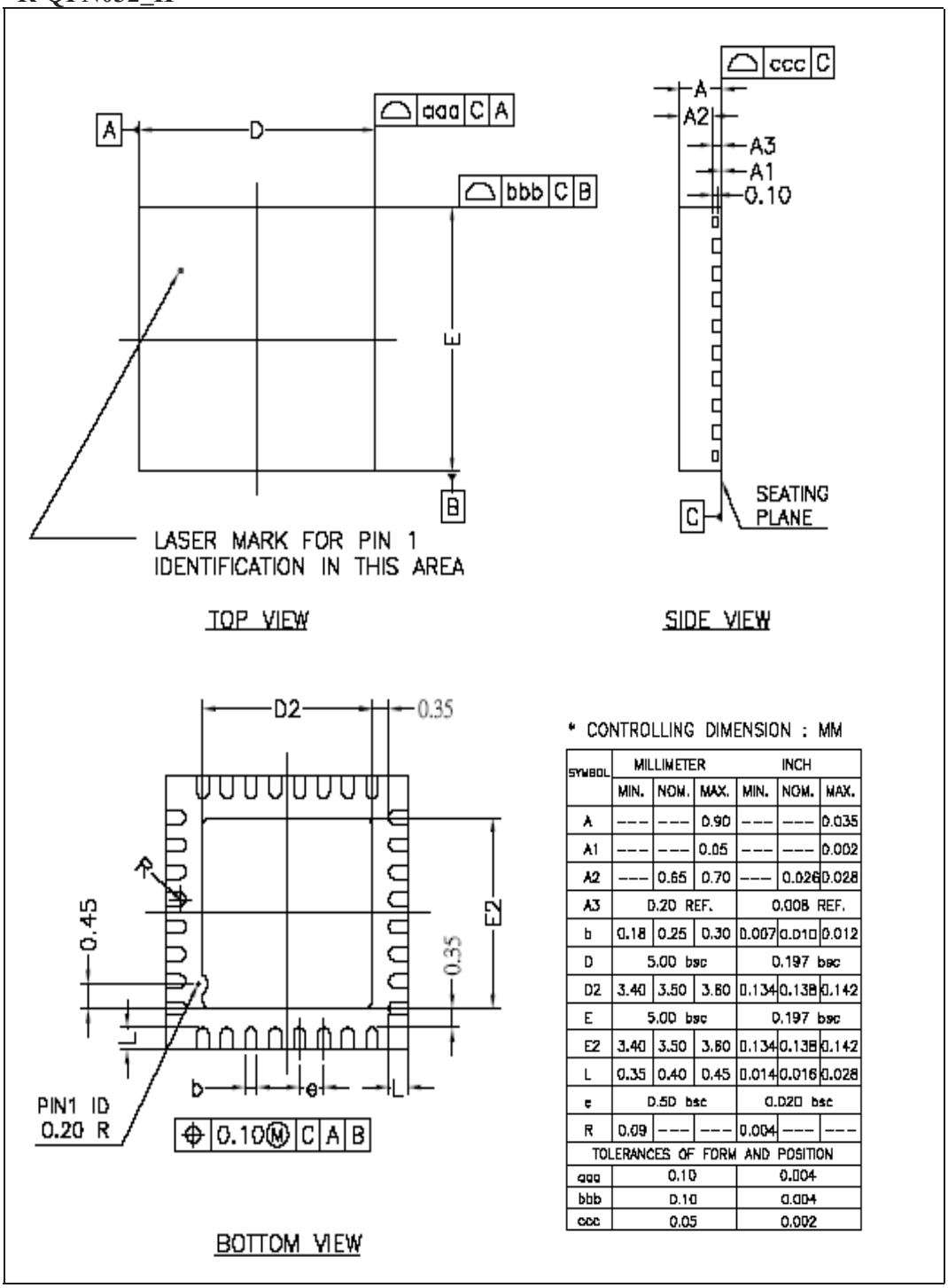
7.9 VINT

One external capacitor (47 0nF) is necessary on VINT pin for functionality of the internal LDO supply. This voltage should not be used by the user.

8. Package Drawing

Figure 8-1. QFN 32-lead Package Drawing (all dimensions in millimeters)

R-QFN032_H



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 bsc			0.197 bsc		
D2	3.40	3.50	3.60	0.134	0.138	0.142
E	5.00 bsc			0.197 bsc		
E2	3.40	3.50	3.60	0.134	0.138	0.142
L	0.35	0.40	0.45	0.014	0.016	0.028
e	0.50 bsc			0.020 bsc		
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

9. Revision History

Doc. Rev.	Comments	Change Request Ref.
6266A	First issue.	

Table of Contents

Features *1*

1 Description *1*

2 Block Diagram *3*

3 Pinout *4*

4 Application examples *5*

5 Detailed Description *9*

5.1 Core 9

5.2 Automatic Start-up Sequences and Shut-down 10

5.3 Digital Control and Protocol 13

6 Register Tables *20*

6.1 System Registers 20

6.2 PMU Registers 23

6.3 Interrupt Registers 39

6.4 RTC Registers 43

7 Electrical Characteristics *57*

7.1 Absolute Maximum Ratings 57

7.2 Recommended Operating Conditions 57

7.3 Digital I/Os 58

7.4 Current Consumption Versus Modes 58

7.5 BOOST1: Step-up Converter 59

7.6 BUCK2: Step-down Converter 62

7.7 LDO3 & LDO4 65

7.8 Real-time Clock (RTC) 67

7.9 VINT 69

8 Package Drawing *70*

9 Revision History *71*

Table of Contents ..... *i*

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