Features

- **Operating Voltage: 3.3V**
- **Access Time:**
  - **15 ns for 3.3V biased only (AT60142F)**
  - **17 ns for 5V Tolerant (AT60142FT)**
- **Very Low Power Consumption**
  - **Active: 650 mW (Max) @ 15 ns, 540 mW (Max) @ 25 ns**
  - **Standby: 3.5 mW (Typ)**
- **Wide Temperature Range: -55 to +125°C**
- **TTL-Compatible Inputs and Outputs**
- **Asynchronous**
- **Designed on 0.25 µm Radiation Hardened Process**
- **No Single Event Latch Up below LET Threshold of 80 MeV/mg/cm^2**
- **Tested up to a Total Dose of 300 krads (Si) according to MIL-STD-883 Method 1019**
- **500 Mils Wide FP36 Package**
- **ESD Better than 4000V for the AT60142F**
- **ESD Better than 2000V for the AT60142FT**
- **Quality Grades: ESCC, QML-Q or V with smd 5962-05208**

Description

The AT60142F/FT are very low power CMOS static RAM organized as 524 288 x 8 bits.

Atmel brings the solution to applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments, or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the AT60142F/FT combine an extremely low standby supply current (Typical value = 1 mA) with a fast access time at 15 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The F version is biased at 3.3 V and is not 5V tolerant: it is available to 15 ns specification.

The FT version is a variant allowing for 5V tolerance: it is available in 17 ns specification.

The AT60142F/FT are processed according to the methods of the latest revision of the MIL PRF 38535 or ESCC 9000.

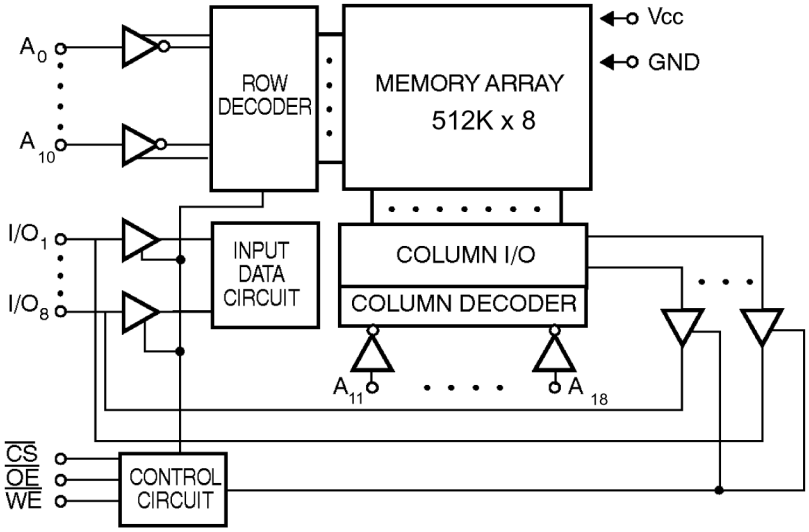
It is produced on a radiation hardened 0.25 µm CMOS process.

Rad Hard 512K x 8 Very Low Power CMOS SRAM

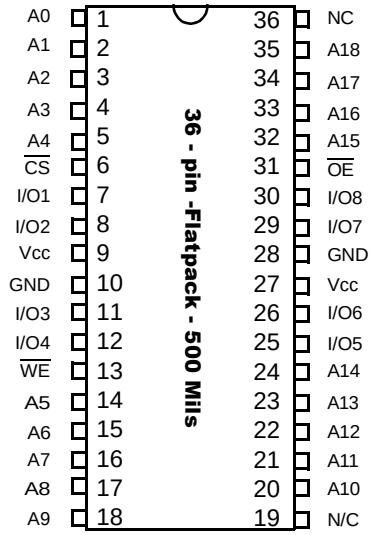
AT60142F AT60142FT

Rev. 4408A–AERO–02/05

Block Diagram



Pin Configuration



Pin Description

Table 1. Pin Names

Name	Description
A0 - A18	Address Inputs
I/O1 - I/O8	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground

Table 2. Truth Table[1]

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	Z	Deselect/ Power-down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	Z	Output Disable

Note: 1. L=low, H=high, X= H or H, Z=high impedance.

Electrical Characteristics

Absolute Maximum Ratings*

Supply Voltage to GND Potential:	-0.5V + 4.6V
DC Input Voltage:	GND -0.5V to 4.6V(1)
DC Output Voltage High Z State:	GND -0.5V to 4.6V
Storage Temperature:	-65°C to + 150°C
Output Current Into Outputs (Low):	20 mA
Electro Statics Discharge Voltage(2):	> 4000V (MIL STD 883D Method 3015.3)

*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. 7V for FT version.
2. For AT60142F. It is better than 2000V for AT60142FT.

Military Operating Range

	Operating Voltage	Operating Temperature
Military	3.3 $\pm$ 0.3V	-55°C to + 125°C

Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
Vcc	Supply voltage	3	3.3	3.6	V
GND	Ground	0.0	0.0	0.0	V
V_{IL}	Input low voltage	GND - 0.3	0.0	0.8	V
V_{IH}	Input high voltage	2.2	–	V_{CC} + 0.3(1)	V

Note: 1. FT version: 5.5V in DC, 5.8V in transient conditions.

Capacitance

Parameter	Description	Min	Typ	Max	Unit
C_{in}(1)	Input low voltage	–	–	12	pF
C_{out}(1)	Output high voltage	–	–	12	pF

Note: 1. Guaranteed but not tested.

DC Parameters

Parameter	Description	Minimum	Typical	Maximum	Unit
I_{IX} (1)	Input leakage current	-1	–	1	µA
I_{OZ}(1)	Output leakage current	-1	–	1	µA
I_{IH}(2) at 5.5V	Input Leakage Current	-1	–	10	µA
I_{OZH}(2) at 5.5V	Output Leakage Current	-1	–	10	µA
V_{OL}(3)	Output low voltage	–	–	0.4	V
V_{OH}(4)	Output high voltage	2.4	–	–	V

1. GND < V_{IN} < V_{CC}, GND < V_{OUT} < V_{CC} Output Disabled.
2. FT version only: V_{IN} = 5.5V, V_{OUT} = 5.5V, Output Disabled.
3. V_{CC} min. I_{OL} = 8 mA.
4. V_{CC} min. I_{OH} = -4 mA.

Consumption

Symbol	Description	TAVAV/TAVAW Test Condition	AT60142F-15	AT60142FT-17	Unit	Value
I_{CCSB} (1)	Standby Supply Current	–	2.5	2.5	mA	max
I_{CCSB1} (2)	Standby Supply Current	–	2	2	mA	max
I_{CCOP}(3) Read	Dynamic Operating Current	15 ns 17 ns 25 ns 50 ns 1 µs	180 - 150 75 10	- 170 150 75 10	mA	max
I_{CCOP}(4) Write	Dynamic Operating Current	15 ns 17 ns 25 ns 50 ns 1 µs	150 - 130 120 100	- 145 130 120 100	mA	max

1. $\overline{CS} \geq V_{IH}$
2. $\overline{CS} \geq V_{CC}$ - 0.3V
3. F = $1/_{TAVAV}$, I_{out} = 0 mA, $\overline{WE}$ = $\overline{OE}$ = V_{IH}, V_{IN} = GND/V_{CC}, V_{CC} max.
4. F = $1/_{TAVAW}$, I_{out} = 0 mA, $\overline{W}$ = V_{IL}, $\overline{OE}$ = V_{IH} , V_{IN} = GND/V_{CC}, V_{CC} max.

AC Characteristics

Temperature Range: ..... -55 +125°C

Supply Voltage: ..... 3.3 ±0.3V

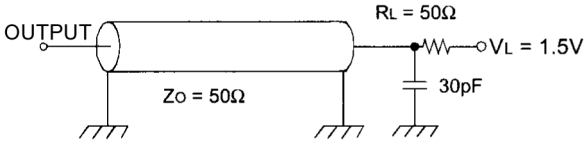
Input Pulse Levels: ..... GND to 3.0V

Input Rise and Fall Times: ..... 3ns (10 - 90%)

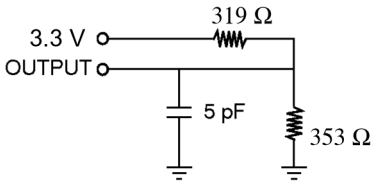
Input and Output Timing Reference Levels: 1.5V

Output Loading I_{OL}/I_{OH}: ..... See Figure 1

Figure 1. AC Test Loads Waveforms



General



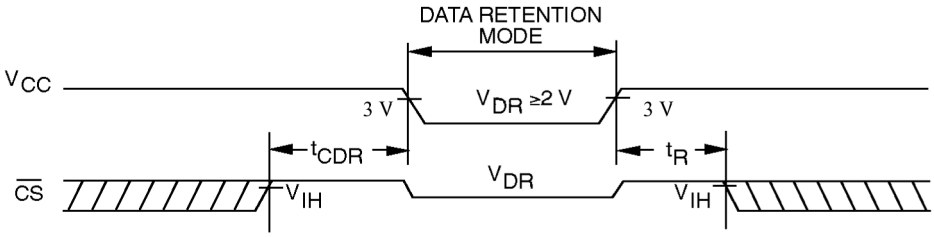
Specific (thz, tlz, twhz, tow, tolz, tohz)

Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. During data retention chip select $\overline{CS}$ must be held high within V_{CC} to V_{CC} -0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions $\overline{CS}$ and $\overline{OE}$ must be kept between V_{CC} + 0.3V and 70% of V_{CC}.
4. The RAM can begin operation > t_R ns after V_{CC} reaches the minimum operation voltages (3V).

Figure 2. Data Retention Timing



Data Retention Characteristics

Parameter	Description	Min	Typ T_A = 25°C	Max	Unit
V_{CCDR}	V_{CC} for data retention	2.0	–	–	V
t_{CDR}	Chip deselect to data retention time	0.0	–	–	ns
t_R	Operation recovery time	t_{AVAV} (1)	–	–	ns
I_{CCDR} (2)	Data retention current	–	0.700	1.5	mA

1. T_{AVAV} = Read cycle time.
2. $\overline{CS}$ = V_{CC}, V_{IN} = GND/V_{CC}.

Write Cycle

Symbol	Parameter	AT60142F-15	AT60142FT-17	Unit	Value
TAVAW	Write cycle time	15	17	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	8	8	ns	min
TDVWH	Data set-up time	7	7	ns	min
TELWH	$\overline{CS}$ low to write end	12	12	ns	min
TWLQZ	Write low to high Z[1]	6	7	ns	max
TWLWH	Write pulse width	8	8	ns	min
TWHAX	Address hold from end of write	0	0	ns	min
TWHDX	Data hold time	0	0	ns	min
TWHQX	Write high to low Z[1]	3	3	ns	min

Notes: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See “AC Test Loads Waveforms” on page 6.)

Read Cycle

Symbol	Parameter	AT60142F-15	AT60142FT-17	Unit	Value
TAVAV	Read cycle time	15	17	ns	min
TAVQV	Address access time	15	17	ns	max
TAVQX	Address valid to low Z	5	5	ns	min
TELQV	Chip-select access time	15	17	ns	max
TELQX	$\overline{CS}$ low to low Z[1]	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z[1]	6	7	ns	max
TGLQV	Output Enable access time	6	8	ns	max
TGLQX	$\overline{OE}$ low to low Z[1]	2	2	ns	min
TGHQZ	$\overline{OE}$ high to high Z [1]	5	6	ns	max

Notes: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See “AC Test Loads Waveforms” on page 6.)

Figure 3. Write Cycle 1. $\overline{WE}$ Controlled, $\overline{OE}$ High During Write

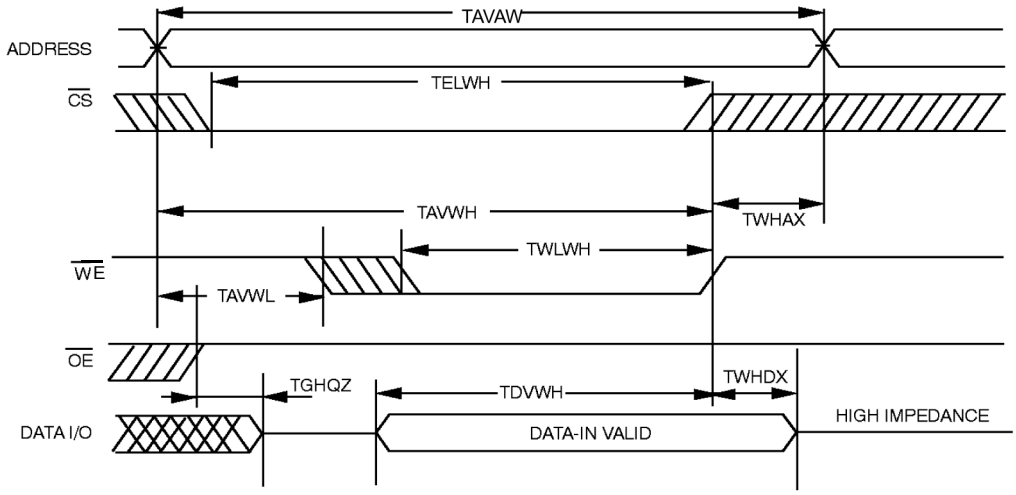


Figure 4. Write Cycle 2. $\overline{WE}$ Controlled, $\overline{OE}$ Low

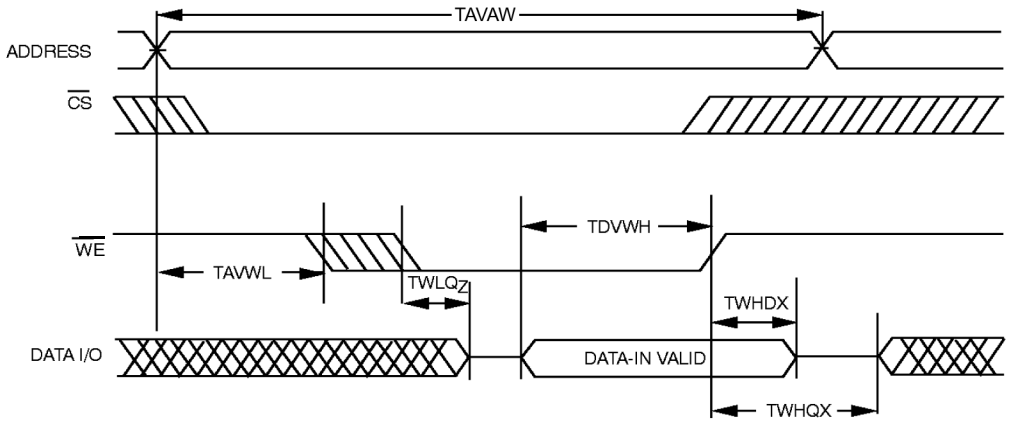
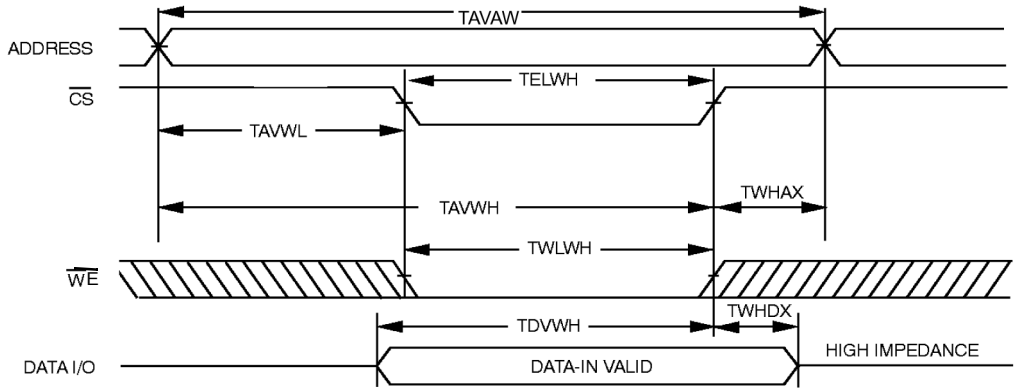


Figure 5. Write Cycle 3. $\overline{CS}$ Controlled[1]



Note: The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{W}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in active mode. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$= V_{IH}.

Figure 6. Read Cycle nb 1: Address Controlled ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

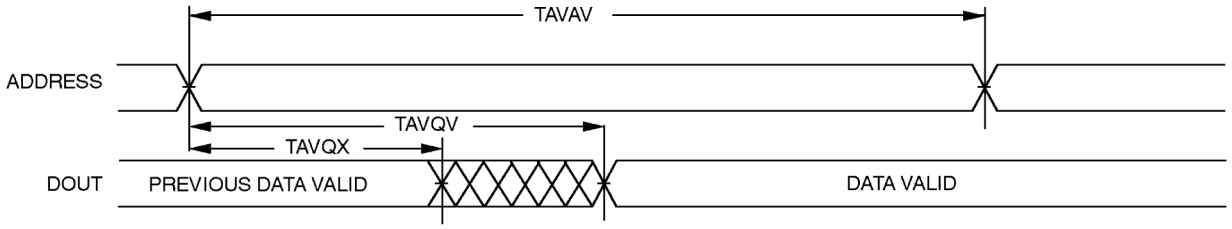
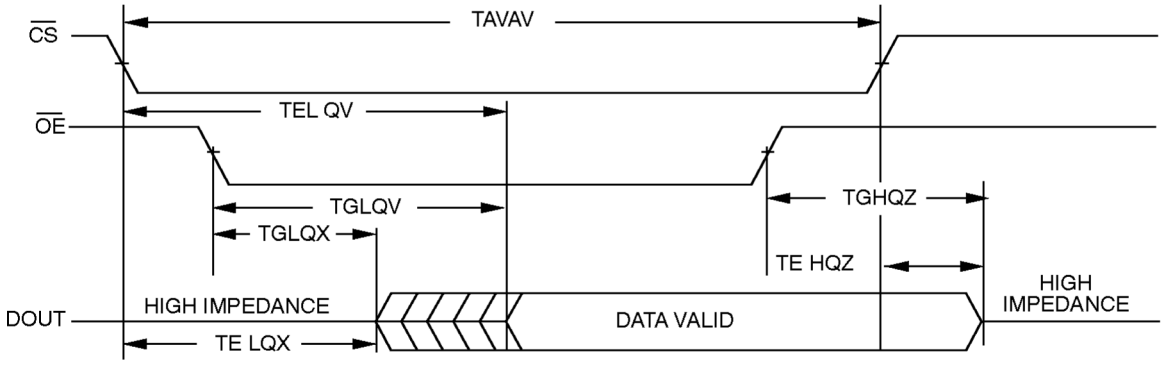


Figure 7. Read Cycle nb 2: Chip Select Controlled ($\overline{WE}$ = V_{IH})



Ordering Information

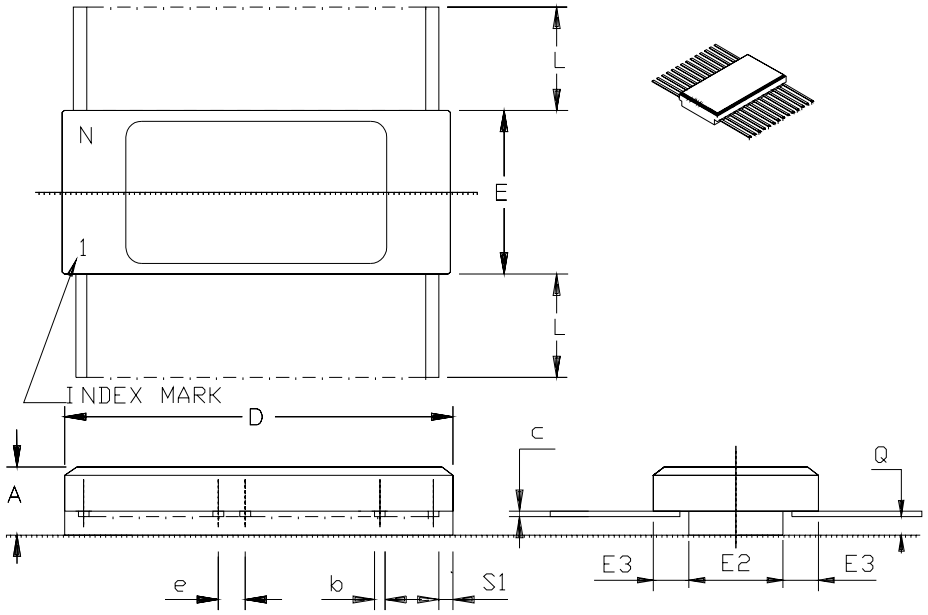
Part Number	Temperature Range	Speed	Package	Flow
AT60142F-DC15M-E	25°C	15 ns/3.3V	FP36.5	Engineering Samples
5962-0520802QXC	-55° to +125°C	15 ns/3.3V	FP36.5	QML Q
5962-0520802VXC	-55° to +125°C	15 ns/3.3V	FP36.5	QML V
5962R0520802VXC	-55° to +125°C	15 ns/3.3V	FP36.5	QML V RHA
AT60142F-DC15SSB	-55° to +125°C	15 ns/3.3V	FP36.5	ESCC
AT60142F-DD15M-E(1)	25°C	15 ns/3.3V	Die	Engineering Samples
AT60142F-DD15MMQ(1) (2)	-55° to +125°C	15 ns/3.3V	Die	QML Q
AT60142F-DD15SMV(1) (2)	-55° to +125°C	15 ns/3.3V	Die	QML V
AT60142FT-DC17M-E	25°C	17 ns/5V tol.	FP36.5	Engineering Samples
5962-0520801QXC	-55° to +125°C	17 ns/5V tol.	FP36.5	QML Q
5962-0520801VXC	-55° to +125°C	17 ns/5V tol.	FP36.5	QML V
5962R0520801VXC	-55° to +125°C	17 ns/5V tol.	FP36.5	QML V RHA
AT60142FT-DC17SSB	-55° to +125°C	17 ns/5V tol.	FP36.5	ESCC
AT60142FT-DD17M-E(1)	25°C	17 ns/5V tol.	Die	Engineering Samples
AT60142FT-DD17MMQ(1) (2)	-55° to +125°C	17 ns/5V tol.	Die	QML Q
AT60142FT-DD17SMV(1) (2)	-55° to +125°C	17 ns/5V tol.	Die	QML V

Note: 1. Contact Atmel for availability.

2. Will be replaced by SMD part number when available.

Package Drawings

36-lead Flat Pack (500 Mils)



	MM		INCH	
	Min	Max	Min	Max
A	2.29	3.05	.090	.120
b	0.38	0.51	.015	.020
c	0.10	0.18	.004	.007
D	---	23.62	---	.930
E	11.99	12.40	.472	.488
E2	8.89	---	.350	---
E3	0.76	---	.030	---
e	1.27 BSC		.050 BSC	
L	7.75	8.26	.305	.325
Q	0.66	1.14	.026	.045
S1	0.13	---	.005	---
N	36		36	

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