Features

- Single Voltage Read/Write Operation: 1.65V to 1.95V
- Access Time – 90 ns
- Sector Erase Architecture
  - Fifteen 32K Word (64K Bytes) Sectors with Individual Write Lockout
  - Eight 4K Word (8K Bytes) Sectors with Individual Write Lockout
- Fast Byte/Word Program Time – 12 µs
- Fast Sector Erase Time – 300 ms
- Suspend/Resume Feature for Erase and Program
  - Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector
  - Supports Reading Any Byte/Word in the Non-suspending Sectors by Suspending Programming of Any Other Byte/Word
- Low-power Operation
  - 12 mA Active
  - 13 µA Standby
- $\overline{\text{Data}}$ Polling, Toggle Bit, Ready/$\overline{\text{Busy}}$ for End of Program Detection
- $\overline{\text{RESET}}$ Input for Device Initialization
- Sector Lockdown Support
- TSOP and CBGA Package Options
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Minimum 100,000 Erase Cycles
- Common Flash Interface (CFI)
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT49SV802A(T) is a 1.8-volt 8-megabit Flash memory organized as 524,288 words of 16 bits each or 1,048,576 bytes of 8 bits each. The x16 data appears on I/O0 - I/O15; the x8 data appears on I/O0 - I/O7. The memory is divided into 23 sectors for erase operations. The AT49SV802A(T) is offered in a 48-lead TSOP and a 48-ball CBGA package. The device has $\overline{\text{CE}}$ and $\overline{\text{OE}}$ control signals to avoid any bus contention. This device can be read or reprogrammed using a single power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see “Sector Lockdown” on page 7).

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory. The end of a program or an erase cycle is detected by the READY/$\overline{\text{BUSY}}$ pin, $\overline{\text{Data}}$ Polling or by the toggle bit.

8-megabit (512K x 16/ 1M x 8) 1.8-volt Only Flash Memory

AT49SV802A
AT49SV802AT

Preliminary

3522C–FLASH–3/05

A six-byte command (Enter Single Pulse Program Mode) sequence to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Byte/Word Program) is exited by powering down the device, or by pulsing the $\overline{\text{RESET}}$ pin low for a minimum of 500 ns and then bringing it back to V_{CC}. Erase, Erase Suspend/Resume and Program Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

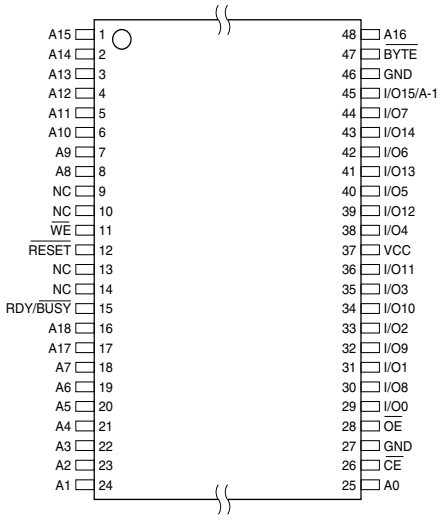
The $\overline{\text{BYTE}}$ pin controls whether the device data I/O pins operate in the byte or word configuration. If the $\overline{\text{BYTE}}$ pin is set at logic “1”, the device is in word configuration, I/O0 - I/O15 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$.

If the $\overline{\text{BYTE}}$ pin is set at logic “0”, the device is in byte configuration, and only data I/O pins I/O0 - I/O7 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$. The data I/O pins I/O8 - I/O14 are tri-stated, and the I/O15 pin is used as an input for the LSB (A-1) address function.

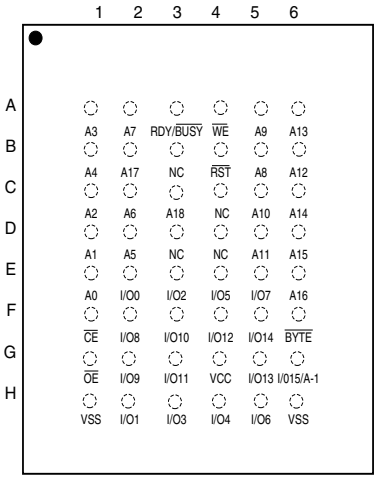
2. Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Reset
RDY/$\overline{BUSY}$	READY/$\overline{BUSY}$ Output
I/O0 - I/O14	Data Inputs/Outputs
I/O15 (A-1)	I/O15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
$\overline{BYTE}$	Selects Byte or Word Mode
NC	No Connect

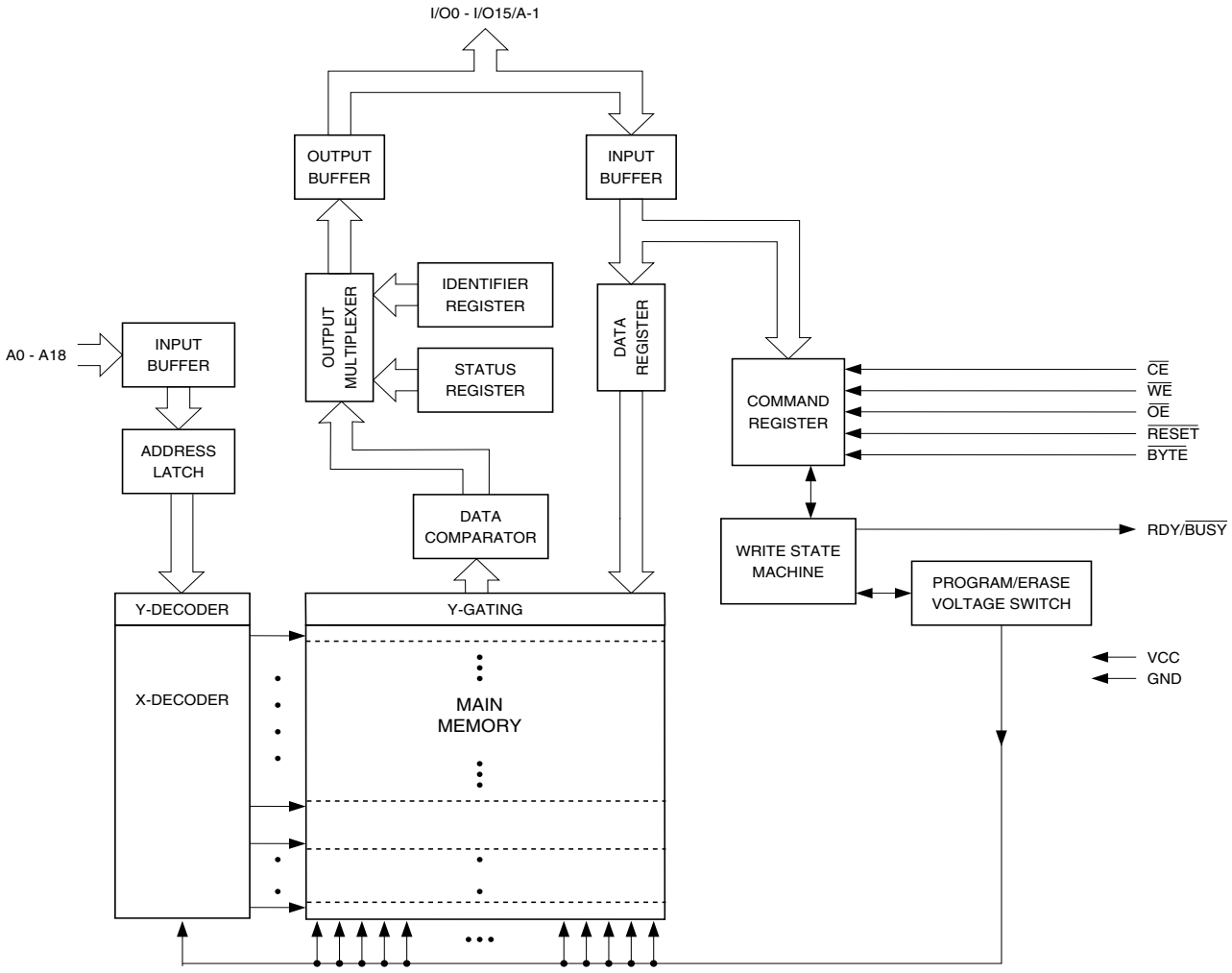
2.1 TSOP Top View (Type 1)



2.2 CBGA Top View (Ball Down)



3. Block Diagram



4. Device Operation

4.1 Read

The AT49SV802A(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Command Sequences

When the device is first powered on, it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the "Command Definition Table" on page 13 (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$

or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

4.3 Reset

A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs.

4.4 Erasure

Before a byte/word can be reprogrammed, it must be erased. The erased state of memory bits is a logical “1”. The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

4.4.1 Chip Erase

The entire device can be erased at one time by using the six-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the sector lockdown has been enabled, the chip erase will not erase the data in the sector that has been locked out; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

4.4.2 Sector Erase

As an alternative to a full chip erase, the device is organized into 23 sectors (SA0 - SA22) that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched on the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a sector is t_{SEC}. When the sector programming lockdown feature is not enabled, the sector will erase (from the same Sector Erase command). An attempt to erase a sector that has been protected will result in the operation terminating immediately.

4.5 Byte/Word Programming

Once a memory block is erased, it is programmed (to a logical “0”) on a byte-by-byte or on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is completed after the specified t_{BP} cycle time. The $\overline{Data}$ Polling feature or the Toggle Bit feature may be used to indicate the end of a program cycle. If the erase/program status bit is a “1”, the device was not able to verify that the erase or program operation was performed successfully.

4.6 Program/Erase Status

The device provides several bits to determine the status of a program or erase operation: I/O2, I/O5, I/O6 and I/O7. The "Status Bit Table" on page 12 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the AT49SV802A(T) contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, "00" or "01". If the configuration register is set to "00", the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a "01", a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a "00" or to a "01", any unsuccessful program or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is "00". Using the four-bus cycle Set Configuration Register command as shown in the "Command Definition Table" on page 13, the value of the configuration register can be changed. Voltages applied to the $\overline{\text{RESET}}$ pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

4.6.1 $\overline{\text{Data}}$ Polling

The AT49SV802A(T) features $\overline{\text{Data}}$ Polling to indicate the end of a program cycle. If the status configuration register is set to a "00", during a program cycle an attempted read of the last byte/word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle. Please see "Status Bit Table" on page 12 for more details.

If the status bit configuration register is set to a "01", the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The $\overline{\text{Data}}$ Polling status bit must be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 4-1 and 4-2 on page 10.

4.6.2 Toggle Bit

In addition to $\overline{\text{Data}}$ Polling the AT49SV802A(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see "Status Bit Table" on page 12 for more details.

The toggle bit status bit should be used in conjunction with the erase/program status bit as shown in the algorithm in Figures 4-3 and 4-4 on page 11.

4.6.3 Erase/Program Status Bit

The device offers a status bit on I/O5, which indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a “1”, the device is unable to verify that an erase or a byte/word program operation has been successfully performed. If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a “0” while the erase or program operation is still in progress. Please see “Status Bit Table” on page 12 for more details.

4.7 Sector Lockdown

Each sector has a programming lockdown feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockdown feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector’s usage as a write-protected region is optional to the user.

At power-up or reset, all sectors are unlocked. To activate the lockdown for a specific sector, the six-bus cycle Sector Lockdown command must be issued. Once a sector has been locked down, the contents of the sector is read-only and cannot be erased or programmed.

4.7.1 Sector Lockdown Detection

A software method is available to determine if programming of a sector is locked down. When the device is in the software product identification mode (see “Software Product Identification Entry/Exit” sections on page 24), a read from address location 00002H within a sector will show if programming the sector is locked down. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockdown feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

4.7.2 Sector Lockdown Override

The only way to unlock a sector that is locked down is through reset or power-up cycles. After power-up or reset, the content of a sector that is locked down can be erased and reprogrammed.

4.8 Erase Suspend/Erase Resume

The Erase Suspend command allows the system to interrupt a sector or chip erase operation and then program or read data from a different sector within the memory. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

4.9 Program Suspend/Program Resume

The Program Suspend command allows the system to interrupt a programming operation and then read data from a different byte/word within the memory. After the Program Suspend command is given, the device requires a maximum of 20 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read data from any other byte/word that is not contained in the sector in which the programming operation was suspended. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same.

4.10 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see "Operating Modes" on page 17 (for hardware operation) or "Software Product Identification Entry/Exit" sections on page 24. The manufacturer and device codes are the same for both modes.

4.11 128-bit Protection Register

The AT49SV802A(T) contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the "Command Definition Table" on page 13. To lock out block B, the four-bus cycle Lock Protection Register command must be used as shown in the "Command Definition Table". Data bit D1 must be zero during the fourth bus cycle. All other data bits during the fourth bus cycle are don't cares. To determine whether block B is locked out, the Status of block B protection command is given. If data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. Please see the "Protection Register Addressing Table" on page 14 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether block B is protected or not, or reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

4.12 RDY/$\overline{\text{BUSY}}$

An open-drain READY/$\overline{\text{BUSY}}$ output pin provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open-drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line. Please see "Status Bit Table" on page 12 for more details.

4.13 Common Flash Interface (CFI)

CFI is a published, standardized data structure that may be read from a flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters, and functions supported by the device. CFI is used to allow the system to learn how to interface to the flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to address 55h. The CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in "Common Flash Interface Definition Table" on page 25. To exit the CFI Query mode, the product ID exit command must be given.

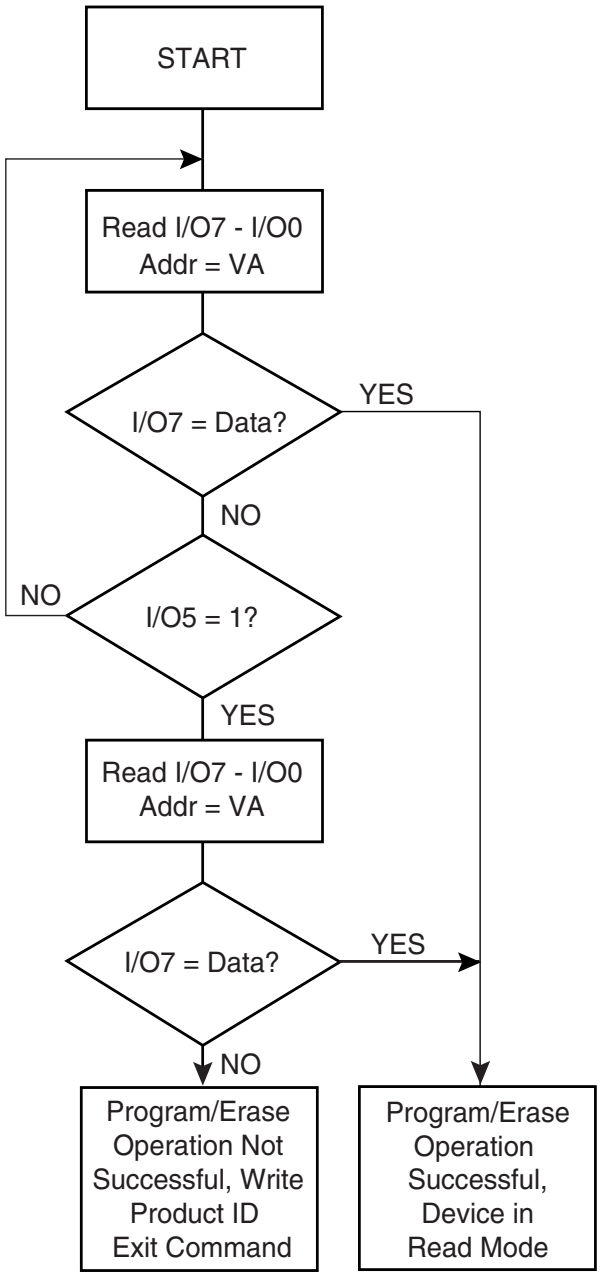
4.14 Hardware Data Protection

The Hardware Data Protection feature protects against inadvertent programs to the AT49SV802A(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.65V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles.

4.15 Input Levels

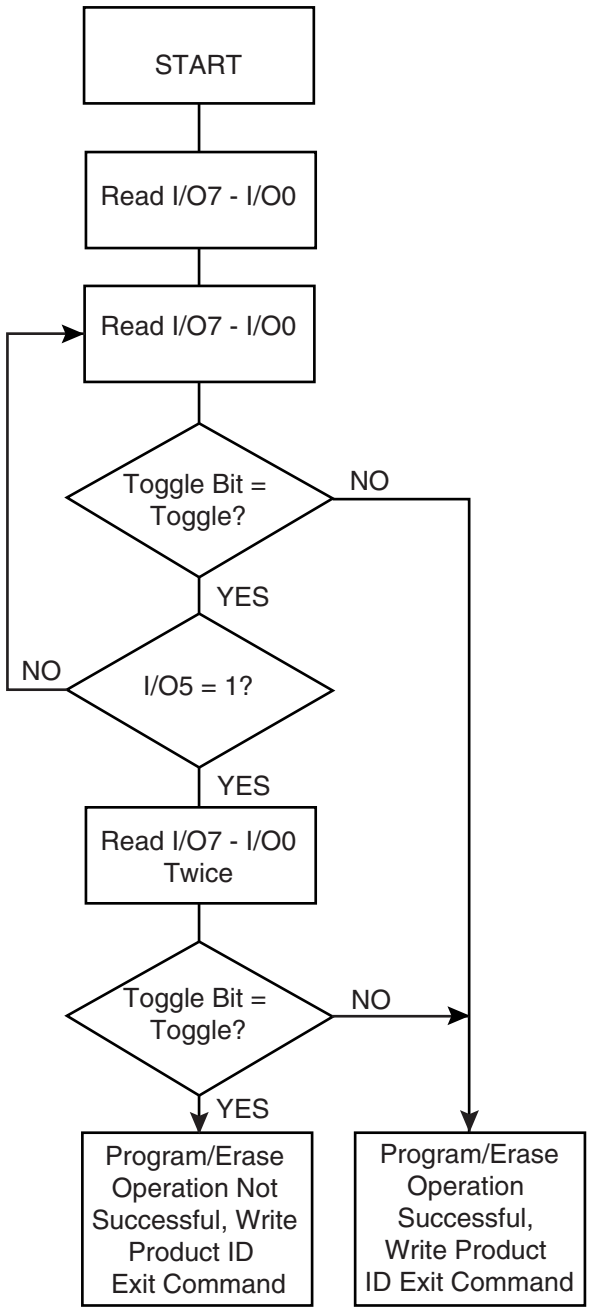
While operating with a 1.65V to 1.95V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

Figure 4-1. $\overline{\text{Data}}$ Polling Algorithm (Configuration Register = 00)



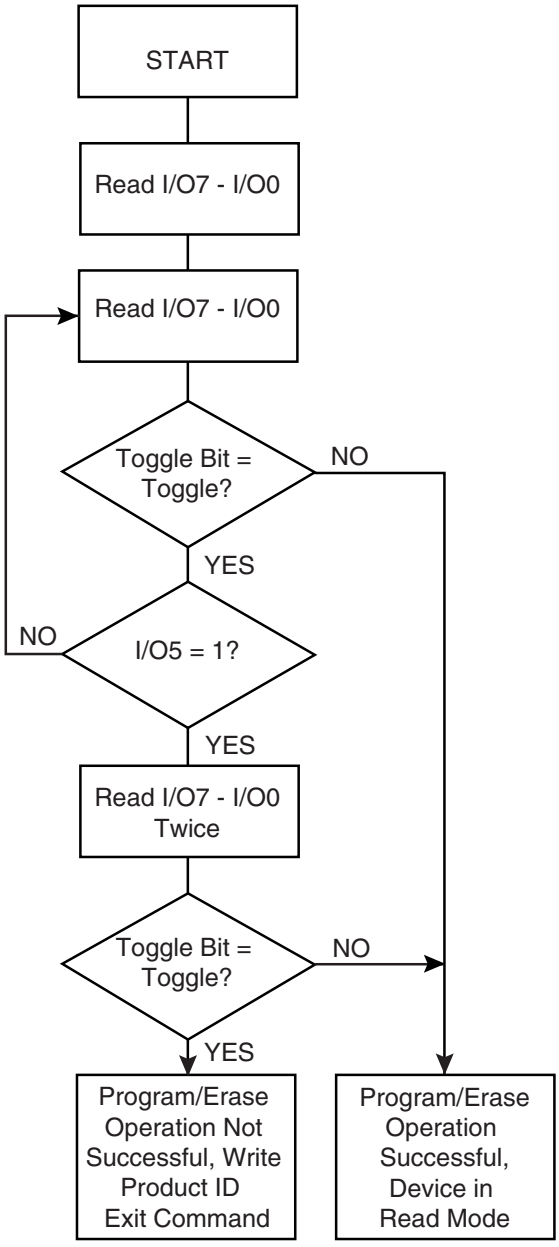
Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 4-2. $\overline{\text{Data}}$ Polling Algorithm (Configuration Register = 01)



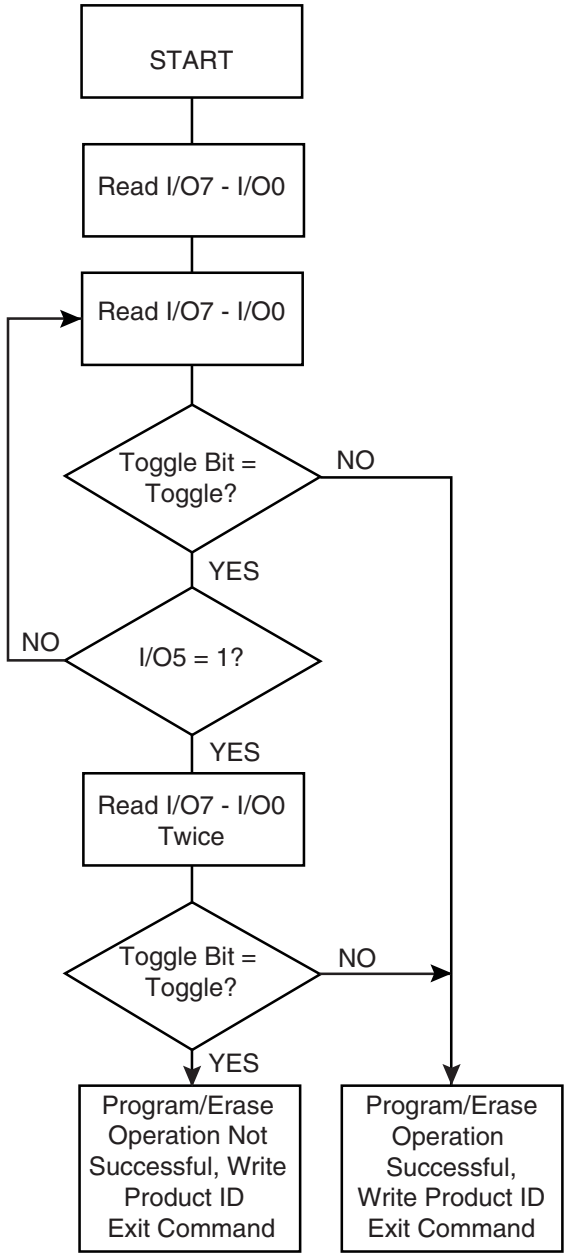
Note:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

Figure 4-3. Toggle Bit Algorithm (Configuration Register = 00)



Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

Figure 4-4. Toggle Bit Algorithm (Configuration Register = 01)



Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

5. Status Bit Table

	Status Bit					
	I/O7	I/O7	I/O6	I/O5[1]	I/O2	RDY/$\overline{\text{BUSY}}$
Configuration Register	**00**	**01**	**00/01**	**00/01**	**00/01**	**00/01**
Programming	$\overline{\text{I/O7}}$	0	TOGGLE	0	1	0
Erasing	0	0	TOGGLE	0	TOGGLE	0
Erase Suspended & Read Erasing Sector	1	1	1	0	TOGGLE	1
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	1
Erase Suspended & Program Non-erasing Sector	$\overline{\text{I/O7}}$	0	TOGGLE	0	TOGGLE	0
Erase Suspended & Program Suspended and Reading from Non-suspended Sectors	DATA	DATA	DATA	DATA	DATA	1
Program Suspended & Read Programming Sector	I/O7	1	1	0	TOGGLE	1
Program Suspended & Read Non-programming Sector	DATA	DATA	DATA	DATA	DATA	1

Note: 1. I/O5 switches to a “1” when a program or an erase operation has exceeded the maximum time limits or when a program or sector erase operation is performed on a protected sector.

6. Command Definition Table

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[3][4]	30
Byte/Word Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Enter Single Pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single Pulse Byte/Word Program	1	Addr	D_{IN}										
Sector Lockdown	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	SA[3][4]	60
Erase/Program Suspend	1	XXX	B0										
Erase/Program Resume	1	XXX	30										
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit[5]	3	555	AA	AAA	55	555	F0[8]						
Product ID Exit[5]	1	XXX	F0[8]										
Program Protection Register	4	555	AA	AAA	55	555	C0	Addr	D_{IN}				
Lock Protection Register – Block B	4	555	AA	AAA	55	555	C0	080	X0				
Status of Block B Protection	4	555	AA	AAA	55	555	90	80	D_{OUT}[6]				
Set Configuration Register	4	555	AA	AAA	55	555	D0	XXX	00/01[7]				
CFI Query	1	X55	98										

Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). In word operation I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A11 - A0 (Hex). Address A18 through A11 are don't care in the word mode. Address A18 through A11 and A-1 are don't care in the byte mode.
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. SA = sector address. Any byte/word address within a sector can be used to designate the sector address (see pages 15 - 16 for details).
4. Once a sector is in the lockdown mode, data in the protected sector cannot be changed unless the chip is reset or power cycled.
5. Either one of the Product ID Exit commands can be used.
6. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
7. The default state (after power-up) of the configuration register is "00".
8. Bytes of data other than F0 may be used to exit the Product ID mode. However, it is recommended that F0 be used.

7. Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on V_{PP} with Respect to Ground	-0.6V to +13.0V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8. Protection Register Addressing Table

Word	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
0	Factory	A	1	0	0	0	0	0	0	1
1	Factory	A	1	0	0	0	0	0	1	0
2	Factory	A	1	0	0	0	0	0	1	1
3	Factory	A	1	0	0	0	0	1	0	0
4	User	B	1	0	0	0	0	1	0	1
5	User	B	1	0	0	0	0	1	1	0
6	User	B	1	0	0	0	0	1	1	1
7	User	B	1	0	0	0	1	0	0	0

Note: All address lines not specified in the above table must be “0” when accessing the protection register, i.e., A18 - A8 = 0.

9. AT49SV802A – Sector Address Table

Sector	Size (Bytes/Words)	x8 Address Range (A18 - A-1)	x16 Address Range (A18 - A0)
SA0	8K/4K	000000 - 001FFF	00000 - 00FFF
SA1	8K/4K	002000 - 003FFF	01000 - 01FFF
SA2	8K/4K	004000 - 005FFF	02000 - 02FFF
SA3	8K/4K	006000 - 007FFF	03000 - 03FFF
SA4	8K/4K	008000 - 009FFF	04000 - 04FFF
SA5	8K/4K	00A000 - 00BFFF	05000 - 05FFF
SA6	8K/4K	00C000 - 00DFFF	06000 - 06FFF
SA7	8K/4K	00E000 - 00FFFF	07000 - 07FFF
SA8	64K/32K	010000 - 01FFFF	08000 - 0FFFF
SA9	64K/32K	020000 - 02FFFF	10000 - 17FFF
SA10	64K/32K	030000 - 03FFFF	18000 - 1FFFF
SA11	64K/32K	040000 - 04FFFF	20000 - 27FFF
SA12	64K/32K	050000 - 05FFFF	28000 - 2FFFF
SA13	64K/32K	060000 - 06FFFF	30000 - 37FFF
SA14	64K/32K	070000 - 07FFFF	38000 - 3FFFF
SA15	64K/32K	080000 - 08FFFF	40000 - 47FFF
SA16	64K/32K	090000 - 09FFFF	48000 - 4FFFF
SA17	64K/32K	0A0000 - 0AFFFF	50000 - 57FFF
SA18	64K/32K	0B0000 - 0BFFFF	58000 - 5FFFF
SA19	64K/32K	0C0000 - 0CFFFF	60000 - 67FFF
SA20	64K/32K	0D0000 - 0DFFFF	68000 - 6FFFF
SA21	64K/32K	0E0000 - 0EFFFF	70000 - 77FFF
SA22	64K/32K	0F0000 - 0FFFFF	78000 - 7FFFF

10. AT49SV802AT – Sector Address Table

Sector	Size (Bytes/Words)	x8 Address Range (A18 - A-1)	x16 Address Range (A18 - A0)
SA0	64K/32K	000000 - 00FFFF	00000 - 07FFF
SA1	64K/32K	010000 - 01FFFF	08000 - 0FFFF
SA2	64K/32K	020000 - 02FFFF	10000 - 17FFF
SA3	64K/32K	030000 - 03FFFF	18000 - 1FFFF
SA4	64K/32K	040000 - 04FFFF	20000 - 27FFF
SA5	64K/32K	050000 - 05FFFF	28000 - 2FFFF
SA6	64K/32K	060000 - 06FFFF	30000 - 37FFF
SA7	64K/32K	070000 - 07FFFF	38000 - 3FFFF
SA8	64K/32K	080000 - 08FFFF	40000 - 47FFF
SA9	64K/32K	090000 - 09FFFF	48000 - 4FFFF
SA10	64K/32K	0A0000 - 0AFFFF	50000 - 57FFF
SA11	64K/32K	0B0000 - 0BFFFF	58000 - 5FFFF
SA12	64K/32K	0C0000 - 0CFFFF	60000 - 67FFF
SA13	64K/32K	0D0000 - 0DFFFF	68000 - 6FFFF
SA14	64K/32K	0E0000 - 0EFFFF	70000 - 77FFF
SA15	8K/4K	0F0000 - 0F1FFF	78000 - 78FFF
SA16	8K/4K	F20000 - F3FFFF	79000 - 79FFF
SA17	8K/4K	F40000 - F5FFFF	7A000 - 7AFFF
SA18	8K/4K	F60000 - F7FFFF	7B000 - 7BFFF
SA19	8K/4K	F80000 - F9FFFF	7C000 - 7CFFF
SA20	8K/4K	FA0000 - FBFFFF	7D000 - 7DFFF
SA21	8K/4K	FC0000 - FDFFFF	7E000 - 7EFFF
SA22	8K/4K	FE0000 - FFFFFF	7F000 - 7FFFF

11. DC and AC Operating Range

		AT49SV802A(T)-90
Operating Temperature (Case)	Ind.	-40°C - 105°C
V_{CC} Power Supply		1.65V to 1.95V

12. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	High-Z
Program Inhibit	X	X	V_{IH}	V_{IH}		
	X	V_{IL}	X	V_{IH}		
Output Disable	X	V_{IH}	X	V_{IH}		High-Z
Reset	X	X	X	V_{IL}	X	High-Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
					A1 - A18 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]
Software[5]				V_{IH}	A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code[4]
					A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to "Program Cycle Waveforms" on page 22.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH (x8); 001FH (x16), Device Code: 00C4H - AT49SV802A; 00C6H - AT49SV802AT.
5. See details under "Software Product Identification Entry/Exit" on page 24.

13. DC Characteristics

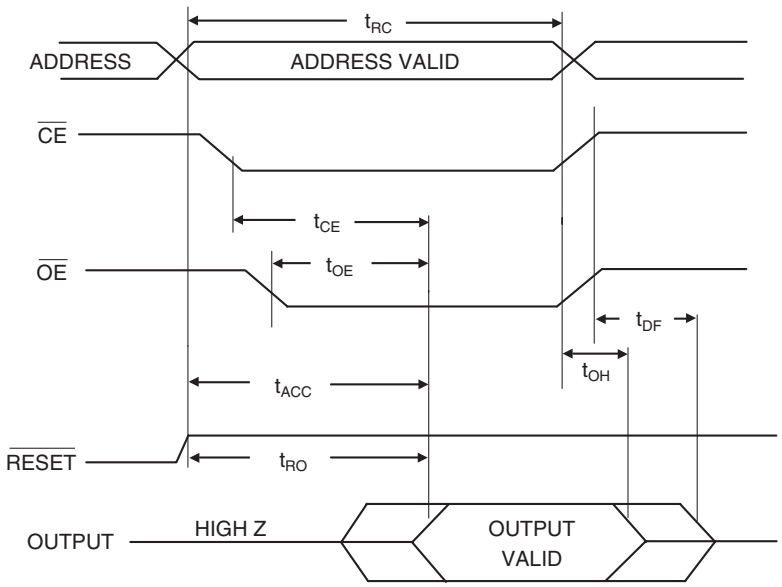
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			2	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		13	25	µA
I_{CC} (1)	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		12	25	mA
I_{CC1}	V_{CC} Programming Current				40	mA
V_{IL}	Input Low Voltage				0.4	V
V_{IH}	Input High Voltage		V_{CC} – 2.0			V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.25	V
V_{OL2}	Output Low Voltage	I_{OL} = 100 µA			0.10	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	1.4			V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA	V_{CC} – 0.1			V

Note: 1. In the erase mode, I_{CC} is 45 mA.

14. AC Read Characteristics

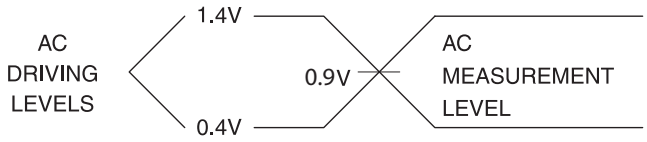
Symbol	Parameter	AT49SV802A(T)-90		Units
		Min	Max	
t_{RC}	Read Cycle Time	80		ns
t_{ACC}	Address to Output Delay		90	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		90	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	90	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		100	ns

15. AC Read Waveforms[1][2][3][4]



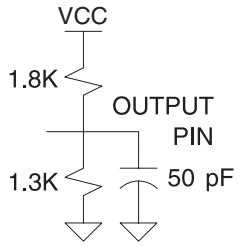
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

16. Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

17. Output Test Load



18. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

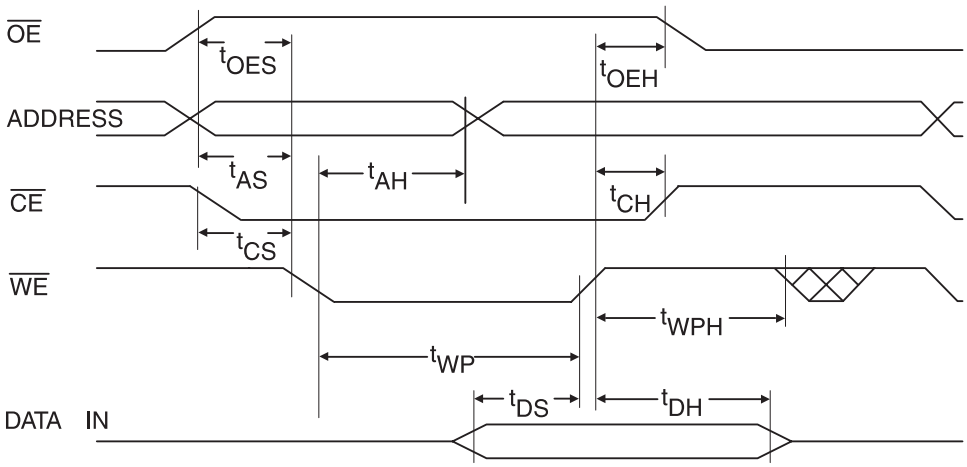
Note: This parameter is characterized and is not 100% tested.

19. AC Byte/Word Load Characteristics

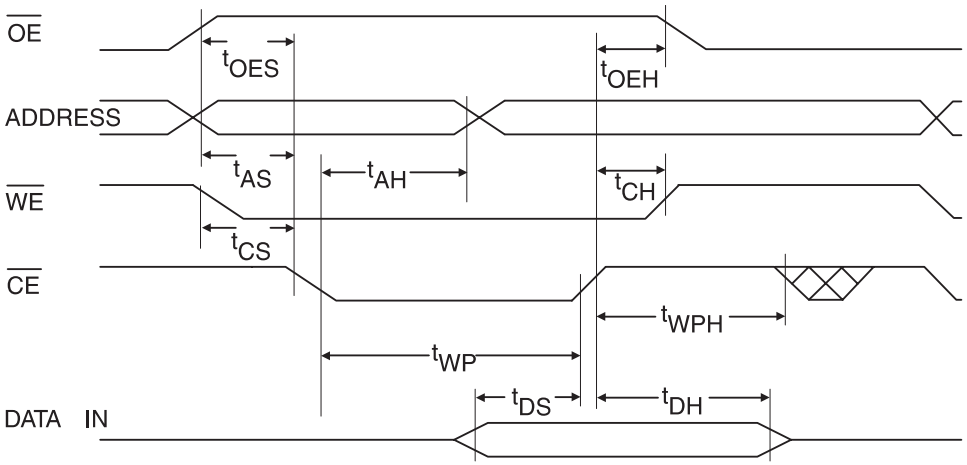
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	35		ns
t_{DS}	Data Setup Time	35		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	35		ns

20. AC Byte/Word Load Waveforms

20.1 $\overline{WE}$ Controlled



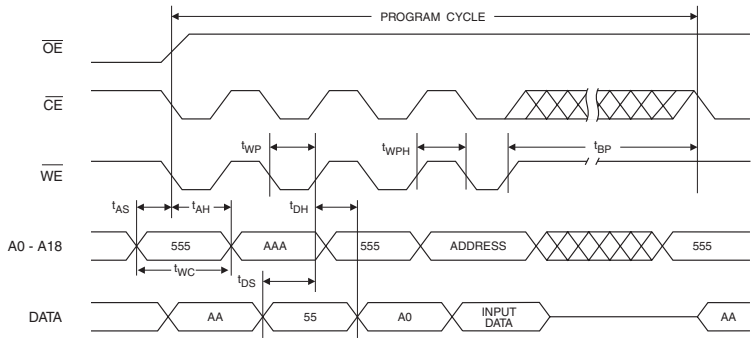
20.2 $\overline{CE}$ Controlled



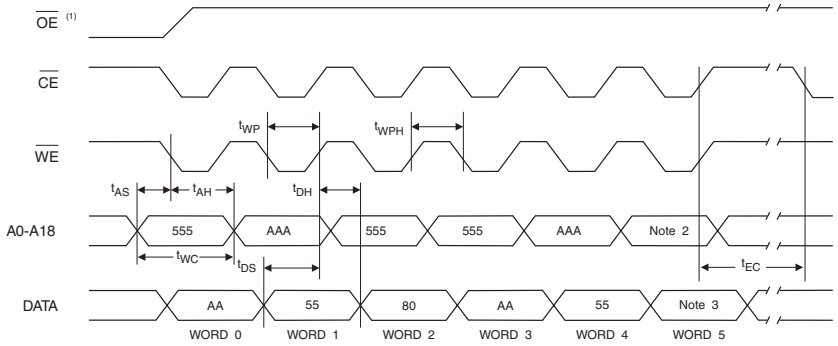
21. Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte/Word Programming Time		12	200	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	35			ns
t_{DS}	Data Setup Time	35			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	35			ns
t_{WPH}	Write Pulse Width High	35			ns
t_{WC}	Write Cycle Time	70			ns
t_{RP}	$\overline{\text{Reset}}$ Pulse Width	500			ns
t_{EC}	Chip Erase Cycle Time		13		seconds
t_{SEC1}	Sector Erase Cycle Time (4K Word Sectors)		0.3	3.0	seconds
t_{SEC2}	Sector Erase Cycle Time (32K Word Sectors)		1.0	5.0	seconds
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			10	µs

22. Program Cycle Waveforms



23. Sector or Chip Erase Cycle Waveforms



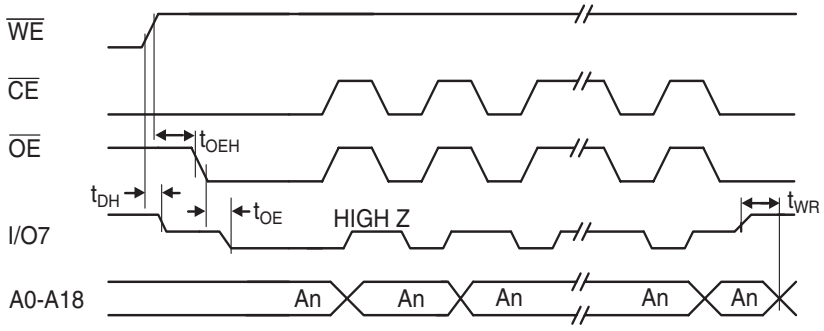
Notes:
1. $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under "Command Definition Table" on page 13.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

24. $\overline{\text{Data}}$ Polling Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 19.

25. $\overline{\text{Data}}$ Polling Waveforms

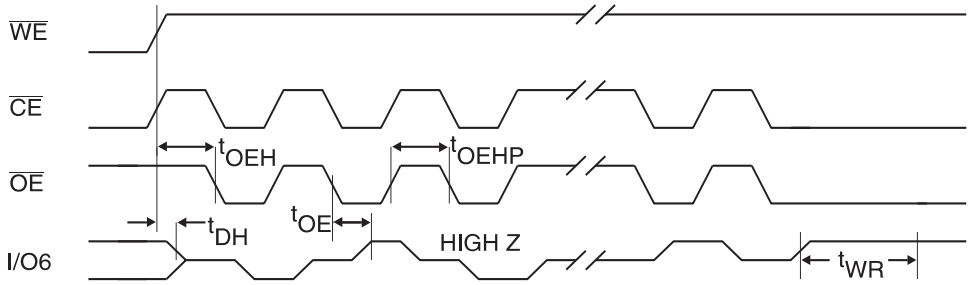


26. Toggle Bit Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

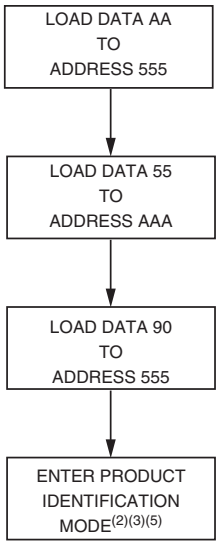
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 19.

27. Toggle Bit Waveforms(1)(2)(3)

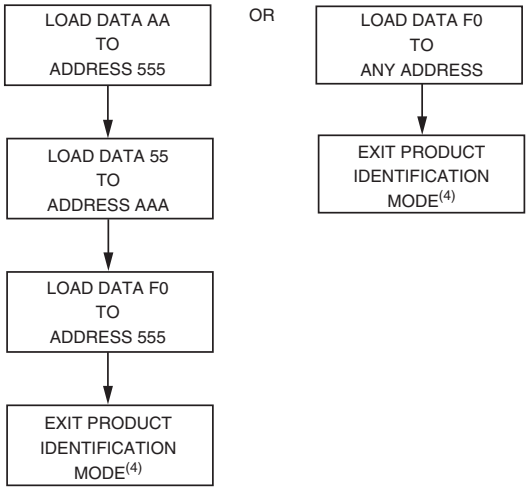


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

28. Software Product Identification Entry[1]

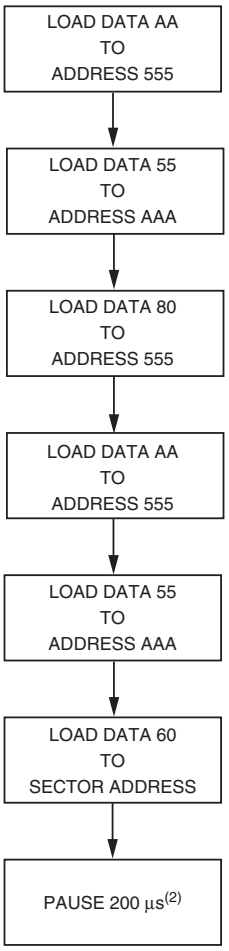


29. Software Product Identification Exit[1][6]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A11 - A0 (Hex), A-1, and A11 - A18 (Don't Care).
2. A1 - A18 = V_{IL}. Manufacturer Code is read for A0 = V_{IL}; Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH(x8); 001FH(x16)
   Device Code:00C4H - AT49SV802A;
   00C6H - AT49SV802AT.
6. Either one of the Product ID Exit commands can be used.

30. Sector Lockdown Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A11 - A0 (Hex), A-1, and A11 - A18 (Don't Care).
2. Sector Lockdown feature enabled.

31. Common Flash Interface Definition Table

Address [x16 Mode]	Address [x8 Mode]	Data	Comments
10h	20h	0051h	"Q"
11h	22h	0052h	"R"
12h	24h	0059h	"Y"
13h	26h	0002h	
14h	28h	0000h	
15h	2Ah	0041h	
16h	2Ch	0000h	
17h	2Eh	0000h	
18h	30h	0000h	
19h	32h	0000h	
1Ah	34h	0000h	
1Bh	36h	0017h	V_{CC} min write/erase
1Ch	38h	0019h	V_{CC} max write/erase
1Dh	3Ah	0000h	V_{PP} min voltage – No V_{PP}
1Eh	3Ch	0000h	V_{PP} max voltage – No V_{PP}
1Fh	3Eh	0004h	Typ word write – 12 µs
20h	40h	0000h	
21h	42h	000Ah	Typ block erase: 1,000 ms
22h	44h	000Eh	Typ chip erase: 13,000 ms
23h	46h	0004h	Max word write/typ time
24h	48h	0000h	N/A
25h	4Ah	0002h	Max block erase/typ block erase
26h	4Ch	0002h	Max chip erase/typ chip erase
27h	4Eh	0014h	Device size
28h	50h	0002h	x8/x16 device
29h	52h	0000h	x8/x16 device
2Ah	54h	0000h	Multiple byte write not supported
2Bh	56h	0000h	Multiple byte write not supported
2Ch	58h	0002h	2 regions, X = 2
2Dh	5Ah	000Eh	64K bytes, Y = 14
2Eh	5Ch	0000h	64K bytes, Y = 14
2Fh	5Eh	0000h	64K bytes, Z = 256
30h	60h	0001h	64K bytes, Z = 256
31h	62h	0007h	8K bytes, Y = 7
32h	64h	0000h	8K bytes, Y = 7
33h	66h	0020h	8K bytes, Z = 32

31. Common Flash Interface Definition Table (Continued)

Address [x16 Mode]	Address [x8 Mode]	Data	Comments
34h	68h	0000h	8K bytes, Z = 32
Vendor Specific Extended Query			
41h	82h	0050h	"P"
42h	84h	0052h	"R"
43h	86h	0049h	"I"
44h	88h	0031h	Major version number, ASCII
45h	8Ah	0030h	Minor version number, ASCII
46h	8Ch	0087h	Bit 0 – chip erase supported, 0 – no, 1 – yes Bit 1 – erase suspend supported, 0 – no, 1 – yes Bit 2 – program suspend supported, 0 – no, 1 – yes Bit 3 – simultaneous operations supported, 0 – no, 1 – yes Bit 4 – burst mode read supported, 0 – no, 1 – yes Bit 5 – page mode read supported, 0 – no, 1 – yes Bit 6 – queued erase supported, 0 – no, 1 – yes Bit 7 – protection bits supported, 0 – no, 1 – yes
47h	8Eh	0000h (top) or 0001h (bottom)	Bit 8 – top ("0") or bottom ("1") boot block device undefined bits are "0"
48h	90h	0000h	Bit 0 – 4-word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8-word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – continuos burst, 0 – no, 1 – yes Undefined bits are "0"
49h	92h	0000h	Bit 0 – 4-word page, 0 – no, 1 – yes Bit 1 – 8-word page, 0 – no, 1 – yes Undefined bits are "0"
4Ah	94h	0080h	Location of protection register lock byte, the section's first byte
4Bh	96h	0003h	# of bytes in the factory prog section of prot register – 2*n
4Ch	98h	0003h	# of bytes in the user prog section of prot register – 2*n

32. Ordering Information

32.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	25	0.025	AT49SV802A-90CI AT49SV802A-90TI	48C19 48T	Industrial (-40° to 105°C)
90	25	0.025	AT49SV802AT-90CI AT49SV802AT-90TI	48C19 48T	Industrial (-40° to 105°C)

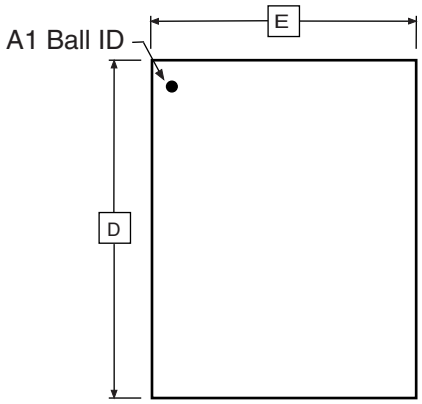
32.2 Green Package Option (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	25	0.025	AT49SV802A-90CU AT49SV802A-90TU	48C19 48T	Industrial (-40° to 105°C)

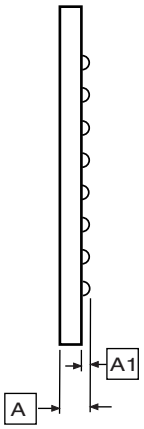
Package Type	
48C19	48-ball, Plastic Chip-Size Ball Grid Array Package (CBGA)
48T	48-lead, Plastic Thin Small Outline Package (TSOP)

33. Packaging Information

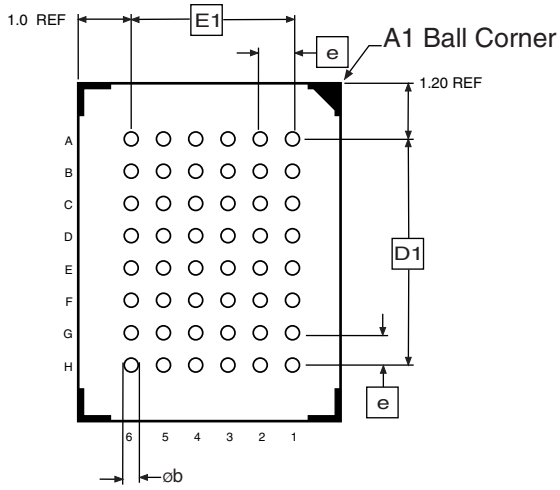
33.1 48C19 – CBGA



Top View



Side View



Bottom View

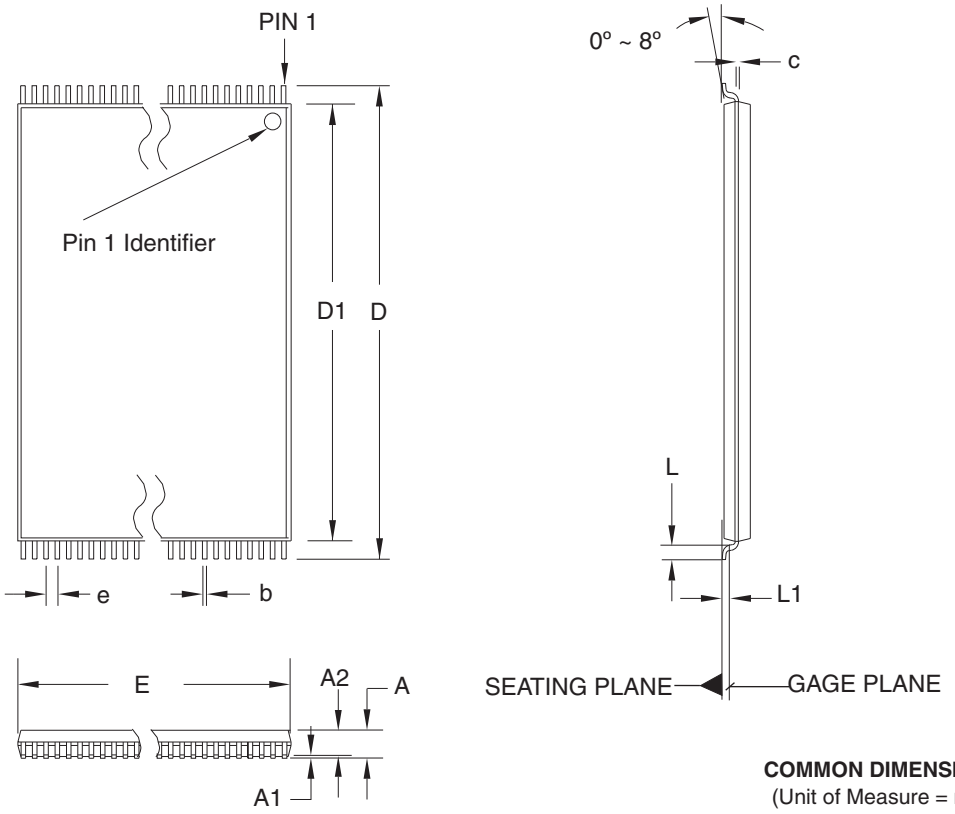
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
E	5.90	6.00	6.10	
E1		4.0 TYP		
D	7.90	8.00	8.10	
D1		5.6 TYP		
A	–	–	1.0	
A1	0.22	–	–	
e		0.80 BSC		
øb		0.40 TYP		

7/2/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**48C19**, 48-ball (6 x 8 Array), 0.80 mm Pitch, 6.0 x 8.0 x 1.0 mm Chip-scale Ball Grid Array Package (CBGA)	48C19	A

33.2 48T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	11.90	12.00	12.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**48T**, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	48T	B

34. Revision History

Revision No.	History
Revision A – November 2004	• Initial Release
Revision B – November 2004	• Changed the speed from 80 ns to 90 ns. • Changed the maximum temperature from 85°C to 105°C.
Revision C – March 2005	• Added Green Package Options (Pb/Halide-free).

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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