Atmel AT30TSE002B

Integrated Temperature Sensor with SEEPROM

DATASHEET

Features

- Integrated Temperature Sensor (TS) + 2-Kbit Serial EEPROM
- JEDEC (JC42.4) SO-DIMM SPD + TS compliant
- Standard voltage operation
  - Optimized for voltage range: 2.7V to 3.6V
- 100khz and 400khz compatibility
- 2-wire serial interface: I^2C/SMBus™ compatible
  - SMBus Timeout supported
- Schmitt Trigger, filtered inputs for noise suppression
- Industry standard green (Pb/Halide-free/RoHS compliant) package options
  - 8-lead Very Very Thin DFN (2 x 3 x 0.8mm)

Serial EEPROM Features

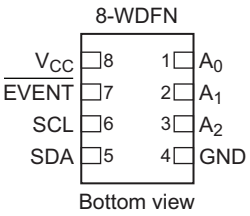
- Permanent and reversible software write protection for the first-half of the array
  - Software procedure to verify write protect status
- Internally organized as one block of 256-bytes (256 x 8)
- Supports byte and page write operation
  - Write 1, 2, 3, and up to 16 bytes at a time
- Self-timed write cycle (5ms max)
- High-reliability
  - Endurance: 1 million write cycles
  - Data retention: 100 years
- Low operating current
  - EEPROM write ~1.5mA (typical)
  - EEPROM read ~ 0.2mA (typical)

Temperature Sensor Features

- 11-bit ADC temp-to-digital converter with 0.125°C resolution
- Programmable hysteresis threshold: off, 0°C, 1.5°C, 3°C, and 6 °C
- B-grade accuracy
  - ±1°C (max.) for +75°C to +95°C
  - ±2°C (max.) for +40°C to +125°C
  - ±3°C (max.) for -20°C to +125°C
- Low operating current
  - Temperature sensor active ~ 0.2mA (typical)

Figure 1. Pin Configuration

Pin	Function
A_0, A_1, A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
Temperature Alert	$\overline{\text{EVENT}}$
GND	Ground
V_{CC}	Power Supply



1. Description

Atmel® AT30TSE002B is a combination Serial EEPROM and temperature sensor device containing 2048-bits of Serially Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 256-bytes of eight bits each and could be used to store memory module and vendor information. The EEPROM operation is tailored specifically for DRAM Memory Modules Serial Presence Detect (SPD). The first 128-bytes of the memory incorporate a permanent and a reversible software Write Protection (WP) feature. Once the permanent software WP is enabled, by sending a special command, it cannot be reversed. However, once the reversible software WP is enabled, it can be reversed by sending a special command.

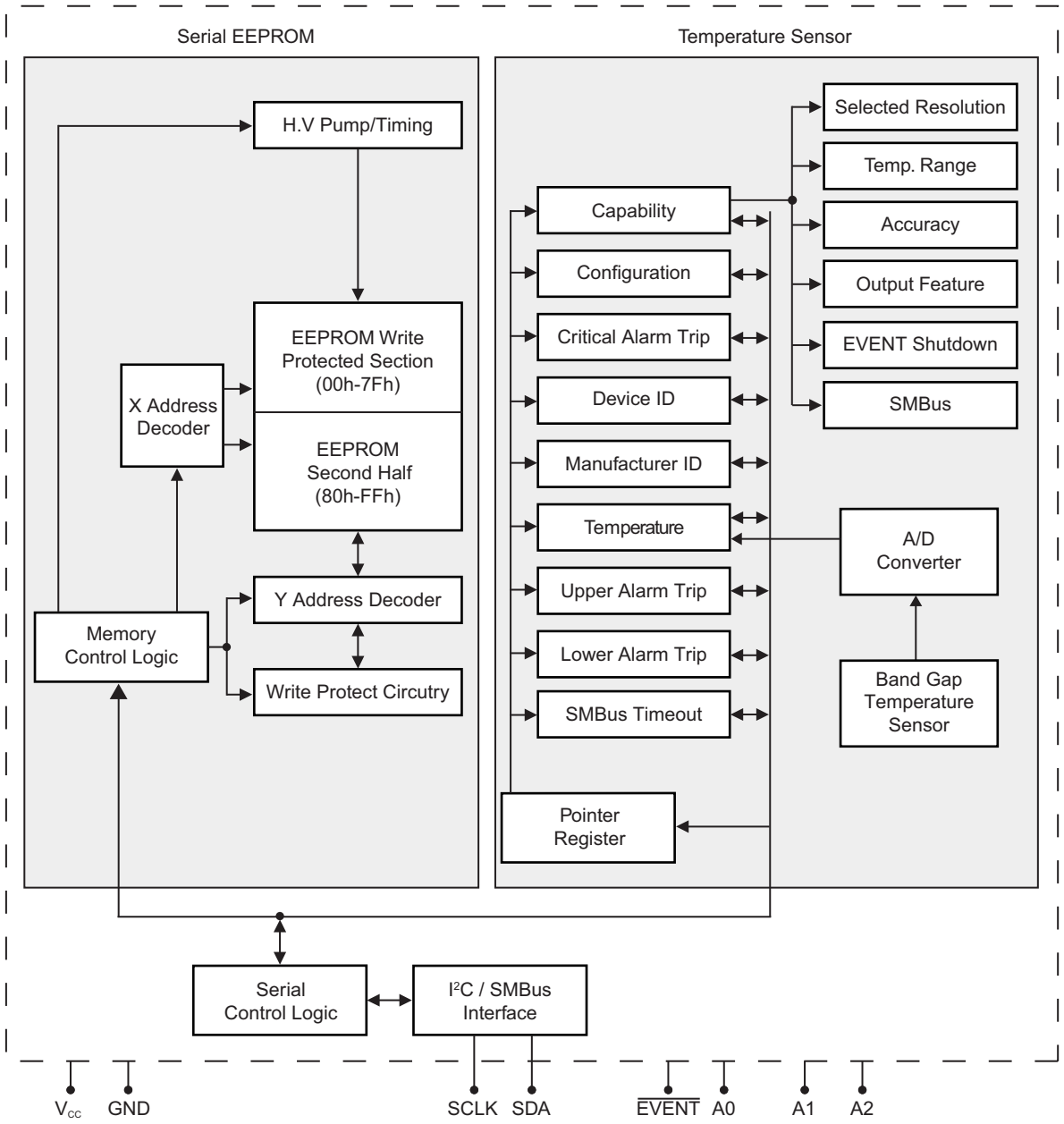
The integrated temperature sensor converts temperatures from -20°C to +125°C to a digital word and provides an accuracy of ±1°C (max.) in the temperature range +75°C to +95°C. The temperature sensor continuously monitors temperature and updates data in the temperature register at least eight times per second. Temperature data is latched internally by the device and may be read by software via a microcontroller at anytime. The AT30TSE002B has flexible user programmable internal registers to configure the temperature sensor performance and response to over temperature conditions. The device contains programmable high, low, and critical temperature limits. The device $\overline{\text{EVENT}}$ pin is configured as active low and can be configured to operate as an interrupt or as a comparator output. Manufacturer and Device ID registers provide the ability to confirm the identity of the device. The AT30TSE002B supports the industry standard 2-wire I^2C/ SMBus serial interface to include time out feature to help prevent system lock-ups.

2. Absolute Maximum Ratings*

Operating Temperature	- 40°C to +125°C
Storage Temperature	- 65°C to + 150°C
Voltage on any pin with respect to ground	- 1.0 V +5.0V
Pin A_0	- 1.0 V +12V
Maximum Operating Voltage	4.3V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram



4. Pin Description

AT30TSE002B requires no external components for operation except for pull-up resistors on SCL, SDA, and $\overline{\text{EVENT}}$ pins. In order to provide effective noise protection and filtering, it is recommended that a decoupling capacitor of 0.1µF be used and is located as close as possible to the device between V_{CC} and ground pins.

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Device Addresses (A_2, A_1, A_0): The A_2, A_1, and A_0 pins are device address inputs that are hardwired (directly to GND or to V_{CC}) for compatibility with 2-wire devices. When the pins are hardwired, as many as eight devices may be addressed on a single bus system. A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A_2, A_1, and A_0 pins will be internally pulled to GND. However, Atmel recommends always connecting the address pins to a known state by direct connection to ground or V_{CC}, but if using a pull-up resistor, Atmel recommends using 10kΩ or less.

The A_0 pin is also overvoltage tolerant, allowing up to 10V for software write protection functionality. (See Section 6. through Section 9.)

Temperature Alert Output ($\overline{\text{EVENT}}$): The $\overline{\text{EVENT}}$ pin outputs a signal when the temperature goes beyond the user-programmed temperature limits and be configured in one of three modes; either Interrupt, Comparator, or Critical Alarm modes.

The $\overline{\text{EVENT}}$ pin is an open-drain output and requires a pull-up resistor for proper operation (see Section 10.).

Table 4-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 100 kHz, V_{CC} = +3.0V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/output Capacitance (SDA), $\overline{\text{EVENT}}$	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, and SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is ensured by characterization only.

Table 4-2. DC Characteristics

Applicable over recommended operating range: T_{AI} = –20°C to +125°C, V_{CC} = +2.7v to +3.6V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.7		3.6	V
Supply Current						
I_{CC}	EEPROM Read V_{CC} = 3.6V (2)	100kHz		0.4	1.0	mA
I_{CC}	EEPROM Write V_{CC} = 3.6V (2)	100kHz		1.5	3.0	mA
I_{CC}	Temp. Sensor V_{CC} = 3.6V	EEPROM Inactive		0.2	0.5	mA
I_{CC}	Timeout Active V_{CC} = 3.6V	EEPROM Inactive, Temp. Sensor Shutdown		0.2	0.5	mA
I_{SB}	Standby Current V_{CC} =3.6V(3)	V_{in} = V_{HV} = or V_{SS}		1.6	4.0	µA
I_{LI}	Input Leakage Current	V_{in} = V_{HV} = or V_{SS}		0.1	2.0	µA
I_{LO}	Output Leakage Current	V_{in} = V_{HV} = or V_{SS}		0.1	2.0	µA
V_{IL}	Input Low Level(1)		-0.6		V_{HV} x 0.3	V
V_{IH}	Input High Level(1)		V_{HV} x0.7		V_{HV} + 0.5	V
V_{OL}	Output Low level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{HV}	High Voltage Input A0	Pin = A_0; V_{HV} - $V_{CC} \geq$ 4.8V	7		10	V
V_{HYST}	Input Hysteresis (SDA, SCL)		0.05 x V_{CC}			V
T_{CONV}	Temp. Sensor Conversion Time			75	125	ms
T_{RES}	Temp. Sensor Resolution			0.25		°C
Temperature Sensor Accuracy						
T_{ACCUR}	+75°C < Ta < +95°C		-1.0	±0.5	+1.0	°C
T_{ACCUR}	+40°C < Ta < +125°C		-2.0	±1	+2.0	°C
T_{ACCUR}	-20°C < Ta < +125°C		-3.0	±2	+3.0	°C
T_{CONV}	Temp. Sensor Conversion Time			75	125	ms
T_{RES}	Temp. Sensor Resolution			0.25		°C

Notes:
1. V_{IL} min and V_{IH} max are reference only and are not tested.
2. Sensor in shutdown mode.
3. EEPROM inactive, sensor in shutdown mode.

Table 4-3. AC Characteristics

Applicable over recommended operating range:
T_{AI} = –20°C to +125°C, V_{CC} = +2.7v to +3.6V, CL = 1 TTL Gate and 100µF (unless otherwise noted)

Symbol	Parameter	Min	Max	Min	Max	Units
F_{SCL}	Clock Frequency, SCL	10[2]	100	10[2]	400	kHz
T_{LOW}	Clock Pulse Width Low	4.7		1.2		us
T_{HIGH}	Clock Pulse Width High	4.0		0.6		us
T_R	Inputs Rise Time[1]		1.0		0.3	us
T_F	Inputs Fall Time[1]		300		300	ns
$T_{SU.DAT}$	Data In Set-up Time	200		100		ns
$T_{HD.DI}$	Data In Hold Time	0		0.0		us
$T_{HD.DAT}$	Data Out Hold Time	200	3450	200	900	ns
T_{BUF}	Time the bus must be free before a new transmission can start[1]	4.7		1.2		us
$T_{SU.STA}$	Start Set-up Time	4.7		0.6		us
$T_{HD.STA}$	Start Hold Time	4.0		0.6		us
$T_{SU.STO}$	Stop Set-up Time	4.7		0.6		us
T_I	Noise Suppression Time[1]		100		50	ns
T_{OUT}	SMBus Timeout Time	25	35	25	35	ms
T_{WR}	Write Cycle Time		5		5	ms
EEPROM Endurance[1]	25°C, Page Mode	1 Million				Write cycles

Notes: 1. This parameter is ensured by characterization only.
2. The minimum frequency is specified at 10Khz to avoid activating the timeout feature.

5. Memory Organization

AT30TSE002B, 2K Serial EEPROM: The 2K memory is internally organized with 16 pages of 16-bytes each. Random word addressing requires an 8-bit data word address.

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. (See Figure 6-4) Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 6-5).

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the Stop command will place the device in a standby power mode (see Figure 6-5).

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The device sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Standby Mode: The AT30TSE002B features a low-power standby mode which is enabled:

a. Upon power-up.

b. After the receipt of the Stop bit and the completion of any internal operations. The temperature sensor must be disabled by the user for low-power standby mode.

2-wire Software Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Create a start bit condition.
2. Clock nine cycles.
3. Create another start bit followed by stop bit condition as shown below.

The device is ready for next communication after the above steps have been completed.

Figure 6-1. 2-wire Software Reset

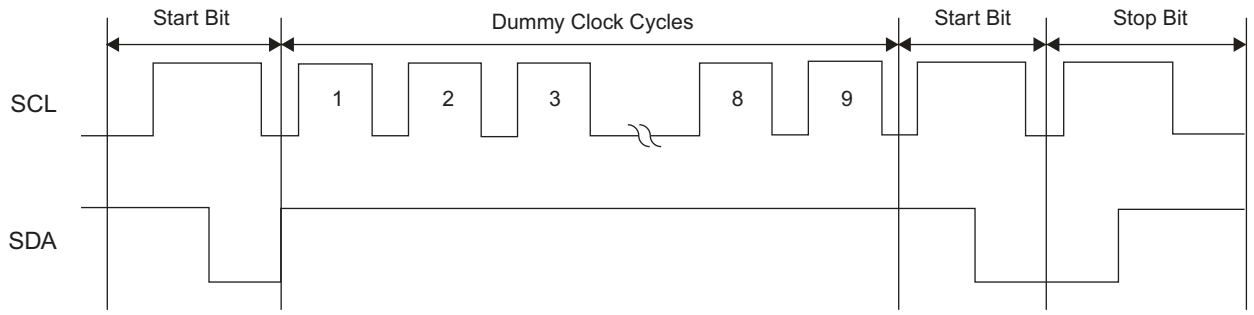


Figure 6-2. Bus Timing SCL
Serial Clock SDA: Serial Data I/O

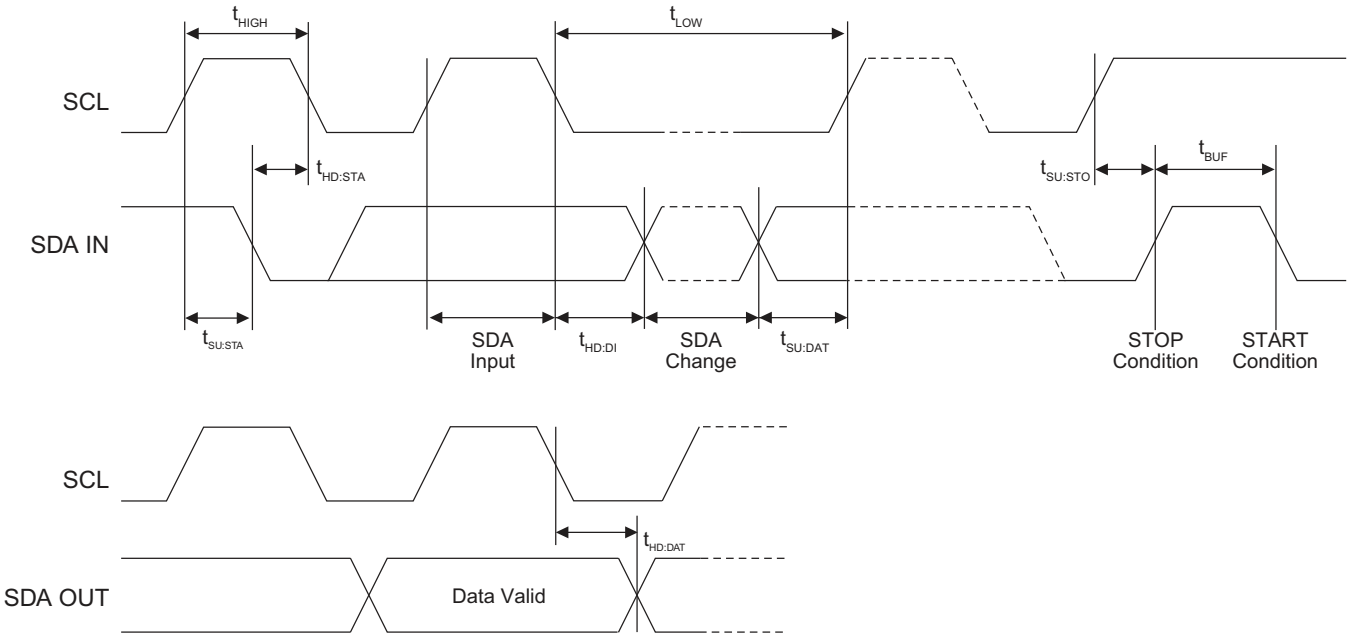


Figure 6-3. Write Cycle Timing SCL
Serial Clock SDA: Serial Data I/O

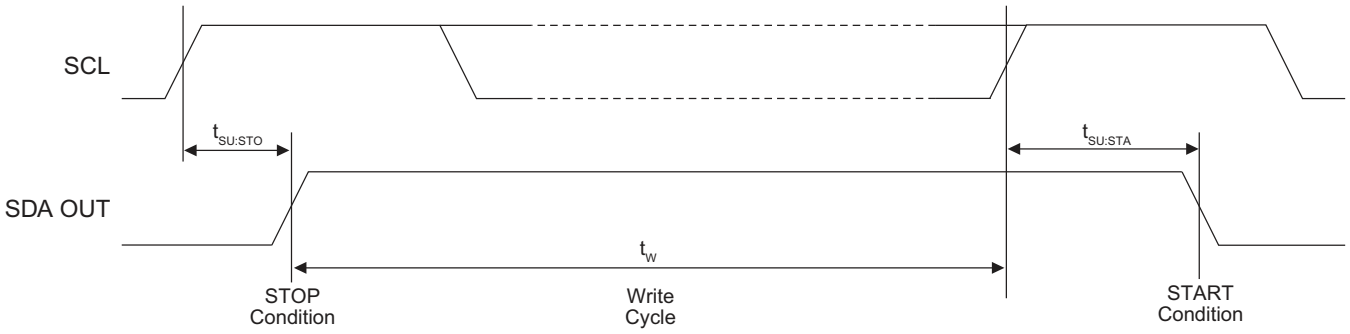


Figure 6-4. Data Validity

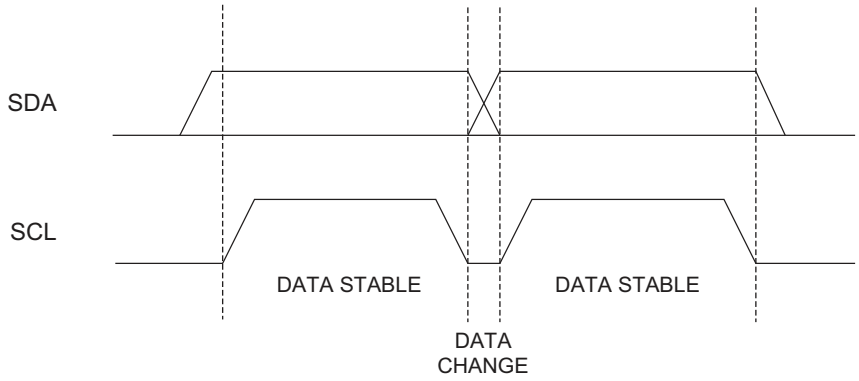


Figure 6-5. Start and Stop Condition

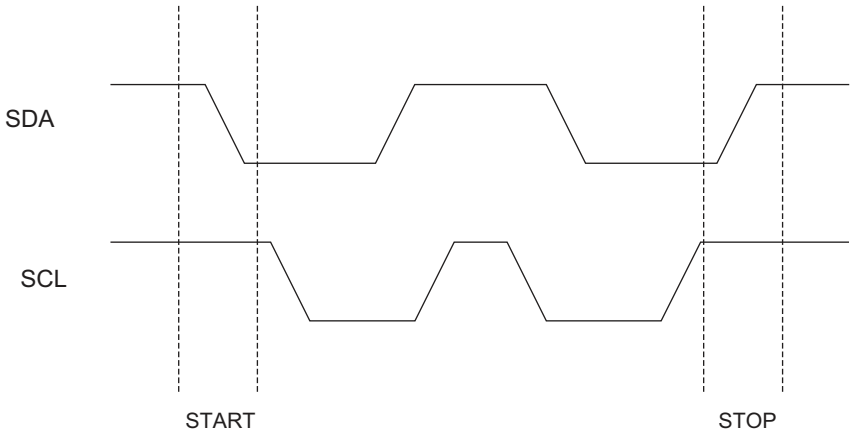
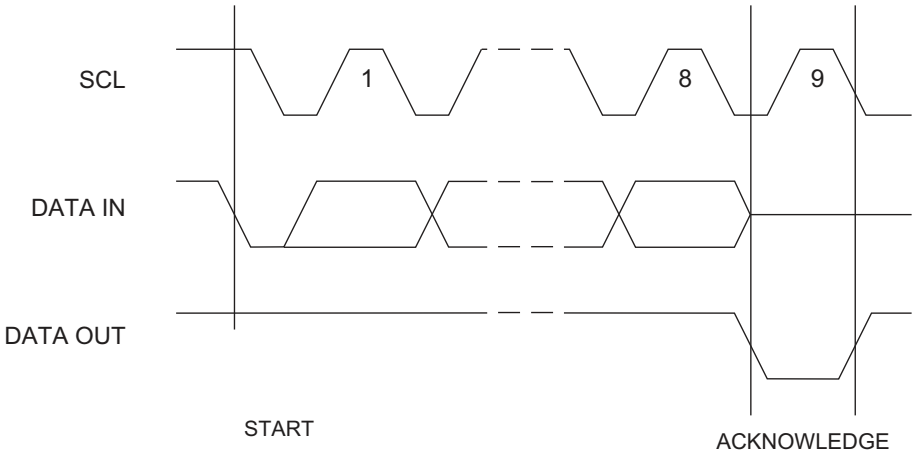


Figure 6-6. Output Acknowledge



7. Device Addressing

AT30TSE002B device requires an 8-bit device address word following a start condition to enable the chip to access either the Temperature Sensor or EEPROM functions (See Table 7-1).

Table 7-1. Control/Device Address Word

Device	Control / Device Address Word							
	Device ID				Device Address Bits			R/W
	B7	B6	B5	B4	A2	A1	A0	B0
EEPROM	1	0	1	0	X	X	X	X
Temperature Sensor	0	0	1	1				
EEPROM Write Protection	0	1	1	0				

Note: 1. X = User Selectable

The EEPROM device address word consists of a mandatory one-zero sequence for the first four most significant bits (‘1010’) for normal read and write operations, a ‘0110’ for writing to the EEPROM write protect register and ‘0011’ for Temperature Sensor operations. The next three bits are the A2, A1 and A0 device address bits for the AT30TSE002B device. These three bits must match their corresponding hard-wired input pins. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and an EEPROM write operation is selected if this bit is low. Upon a compare of the device address, the device will output a zero, called an Acknowledge (ACK). If a compare is not made, the chip will not ACK and will return to a standby state. The EEPROM will not ACK if the write protect register has been programmed and the control code is ‘0110’.

8. EEPROM Write Operations

Byte Write: A write operation requires an 8-bit data word address following the device address word and ACK. Upon receipt of this address, the EEPROM will again respond with an ACK and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output an ACK and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 13-2 and Figure 13-3).

The device will acknowledge a write command, but not write the data, if the software write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

Page Write: The 2K EEPROM device is capable of 16-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 13-3). The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page. The device will acknowledge a write command, but not write the data, if the software write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

Acknowledge (ACK) Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, ACK polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

9. EEPROM Write Protection

The device supports permanent and reversible software write protection and once enabled, write protects the first-half of the array (00H - 7FH).

Permanent Software Write Protection: The software write protection is enabled by sending a command similar to a normal write command; to the device which programs the permanent write protect register. The write protect register is programmed by sending a write command with the device address of '0110' with the address and data bit being don't cares (see Figure 12-5 and Table 12-1). Once the software write protection has been enabled, the device will no longer acknowledge the '0110' control byte. The software write protection cannot be reversed even if the device is powered down. The write cycle time must be observed.

Reversible Software Write Protection: The reversible software write protection is enabled by sending a command, similar to a normal write command; to the device which programs the reversible write protect register. The write protect register is programmed by sending a write command '01100010' with pins A_2 and A_1 tied to ground or no connect and pin A_0 connected to V_{HV} (see Figure 12-6 and Table 12-1). The reversible write protection can be reversed by sending a command '01100110' with pin A_2 tied to ground or no connect, pin A_1 tied to V_{CC} and pin A_0 tied to V_{HV} (see Figure 12-6 and Table 12-1).

10. Temperature Sensor Functional Description

AT30TSE002B consists of a Delta-Sigma Analog to Digital Converter (ADC) with a band gap type temperature sensor that monitors and updates its own temperature reading at least eight times per second converting the readings into digital data bits and latching them into a temperature register that can be read via 2-wire I^2C/SMBus serial interface. The device communicates over a 2-wire I^2C/SMBus interface with the bus master or controller consisting of a serial clock (SCL) and serial bidirectional data bus (SDA) with clock frequencies up to 400Khz. The bus master or controller generates the SCL signal and is used by the AT30TSE002B to receive and send serial data on the SDA line with the most significant bit transferred first. A pull-up resistor is required on the SDA pin since it has an open drain configuration.

10.1 $\overline{\text{EVENT}}$ Output

The $\overline{\text{EVENT}}$ pin has three operating modes depending on configuration settings. They are Interrupt, Comparator, and Critical Alarm (Crit_Alarm) modes.

In the Interrupt mode, once a temperature reaches a boundary limit, the AT30TSE002B asserts the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin will remain asserted until software clears the interrupt by writing a one to the EVTCLR bit five in the configuration register. When the temperature drops below specified limits, the device returns back to either interrupt or comparator mode as programmed in the configuration register's EVTMOD bit zero.

In the comparator mode, the $\overline{\text{EVENT}}$ pin remains asserted until the error condition that caused the pin to be asserted no longer exists and the $\overline{\text{EVENT}}$ pin will clear itself. In the Crit_Alarm mode, when the measured temperature exceeds Crit_Alarm trip limit, the $\overline{\text{EVENT}}$ pin will remain asserted until the temperature drops below Crit_Alarm limit minus hysteresis (See Figure 11-1). All event thresholds use hysteresis as programmed in the configuration register.

10.2 Alarm Window

The alarm window consists of the Upper Alarm Trip Register and Lower Alarm Trip Register. The Upper Alarm Trip Register holds the upper temperature trip point and the Lower Alarm Trip Register holds the lower temperature trip point. After the $\overline{\text{EVENT}}$ pin control is enabled, the $\overline{\text{EVENT}}$ output will be triggered upon entering and exiting from this window.

10.3 Temperature Sensor Power-on Default

The AT30TSE002B has an internal Power-On Reset (POR) circuit. When the supply voltage drops below the POR threshold, the device will reset to the following power-on default conditions:

- Sensor starts monitoring temperature continuously.
- Address Pointer Register = 00h.
- Upper / Lower Alarm Trip registers and Crit_Alarm registers are set to 0°C.
- $\overline{\text{EVENT}}$ register cleared and pulled high by external pull up resistor.
- Operational mode is comparator.
- $\overline{\text{EVENT}}$ hysteresis is 0°C.
- SMBus register =00h.

10.4 Device Initialization

The AT30TSE002B Temperature Sensor has programmable registers that, upon device power-on, are initialized to zero. Table 11-1 shows the Power-On register default values. The $\overline{\text{EVENT}}$ output is defaulted to deasserted state and comparator mode.

Note: The Upper Alarm Trip, Lower Alarm Trip, Critical Alarm Trip, and Configuration registers need to be programmed to desired values before temperature sensor can properly function.

10.5 SMBus Timeout

The AT30TSE002B supports the SMBus timeout feature for temperature sensor operations if enabled via setting the SMBus register (see Section 11.10). This feature helps prevent potential system bus hang-ups by resetting the serial interface if SCL stays low for a time specified by the t_{OUT} parameter. This requires a minimum SCL clock speed of 10Khz as specified in the SMBus specification to avoid any timeout issues.

11. Register Descriptions

This section describes all the temperature sensor registers that are used in AT30TSE002B. The AT30TSE002B has several registers that are user accessible and or programmable and used for latching temperature readings, storing high and low temperature limits, configuring the hysteresis threshold and reporting status.

These registers include the Capability Register, Upper Alarm Trip Register, Lower Alarm Trip Register, Critical Alarm Trip Register, Temperature Register, Manufacturer Identification Register, Device Identification Register, and SMBus Register. The AT30TSE002B uses an 8-bit Pointer Register to access these registers and all other registers contain 16-bits.

Table 11-1 indicates the write/read access capability of each register. Reading from a write only register will result in reading zero data and writing to read-only register will have no impact even though the write sequence was acknowledged by the device.

Table 11-1. Register Summary

Register				Power-up Default Register Data (hex)
Address (hex)	Read / Write	Register Name	Section	
n/a	W	Address Pointer	11.1	00h
00h	R	Capability	11.2	00F7h
01h	R / W	Configuration	11.3	0000h
02h	R / W	Upper Alarm Trip	11.4	0000h
03h	R / W	Lower Alarm Trip	11.5	0000h
04h	R / W	Critical Alarm Trip	11.6	0000h
05h	R	Temperature Data	11.7	n/a
06h	R	Manufacturer I.D.	11.8	001Fh
07h	R	Device I.D. / Device Revision	11.9	8201h
08h to 21h	R / W	Reserved (1)	n/a	0000h
22h	R / W	SMBus Timeout	11.10	0000h
23h to FFh	R / W	Reserved (1)	n/a	0000h

Note: 1. Write operations to reserve registers should be avoided as it may cause undesirable results.

11.1 Address Pointer Register

The AT30TSE002B uses a Pointer Register to select and access the 16-bit data registers shown in Table 11-1. The Pointer Register is an 8-bit write only register (See Table 11-2). The power-on default value is 00h which is the address location for the capability register.

Table 11-2. Address Pointer Register

Bit	7	6	5	4	3	2	1	0
Symbol	Pointer Bits							
R/W	W	W	W	W	W	W	W	W
Default Value	0	0	0	0	0	0	0	0

11.2 Capability Register (16-bit Read Only, Address = 00h)

AT30TSE002B is capable of measuring temperature with ±1°C over the active range and ±2°C over the monitor range. This register is a 16-bit read-only register used to specify the capabilities of the temperature sensor. The Capability Register functions are described in Table 11-3 and Table 11-4.

Table 11-3. Capability Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Default Value	0	0	0	0	0	0	0	0
R / W Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EVSD	TMOUT	V_{HV}	TPRES		RANGE	SACC	ICAP
Default Value	1	1	1	1	0	1	1	1
R / W Access	R	R	R	R	R	R	R	R

Table 11-4. Capability Register Bit Description

Bit	Symbol	Description
15:8	RFU	***Reserved*** for ***Future Use.*** Must be zero.
7	EVSD	**Event Output Status during shutdown mode:** 1 = The $\overline{\text{EVENT}}$ pin output is deasserted (not driven) when entering shutdown mode and will resume status update immediately upon exiting shutdown. In addition, the EVTSTS bit in the configuration register will be cleared when entering shutdown mode and will resume status update immediately upon exiting shutdown.
6	TMOUT	**Bus Timeout:** 1 = Supported within the SMBus compatible range 25 to 35ms (power-up default).
5	V_{HV}	**High Voltage Support for A_0 pin:** 1 = A_0 pin supports a voltage up to 10V (power-up default).
4:3	TPRES	**Temperature Resolution:** 10 = Supports 0.125°C
2	RANGE	1 = Can read temperatures below 0°C and sets appropriate sign bit.
1	SACC	**Supported Accuracy:** 1 = Supports B grade accuracy of ± 1°C over the active range (75°C to 95°C) and 2°C over the monitor range (40°C to 125°C).
0	ICAP	**Interrupt Capability:** 1 = Has alarm and critical trip interrupt capability.

11.3 Configuration Register (16-bit Read/Write, Address = 01h)

The AT30TSE002B contains a 16-bit Configuration Register allowing the user to set key operational features of the Temperature Sensor. The Configuration Register functions are described in Table 11-5, Table 11-6, and Figure 11-1.

Table 11-5. Configuration Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	RFU					HYSTENB		SHTDWN
Default Value	0	0	0	0	0	0	0	0
R / W Access	R	R	R	R	R	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CRTALML	WINLOCK	EVTCLR	EVTSTS	EVTOUT	CRITEVT	EVTPOL	EVTMOD
Default Value	0	0	0	0	0	0	0	0
R / W Access	R/W	R/W	W	R	R/W	R/W	R/W	R/W

Table 11-6. Configuration Register Bit Description

Bit	Symbol	Description
15:11	RFU	***Reserved*** for ***Future Use*** and must be zero.
10:9	HYSTENB	**Hysteresis Enable**: 00 = 0°C Disable Hysteresis (default power-on condition) 01 = 1.5°C Enable Hysteresis 10 = 3.0°C Enable Hysteresis 11 = 6.0°C Enable Hysteresis The purpose of these bits is to control the hysteresis applied to the alarm trip point boundaries. The above hysteresis applies to all limits when temperature drops below the user specified alarm trip points. Note: Hysteresis applies to decreasing temperature only. Once ambient temperature is above a given threshold, it must drop below the boundary limit minus hysteresis in order for a comparator $\overline{\text{EVENT}}$ to be cleared. Example: If these bits are set to '01' for 1.5°C and the Upper Alarm Trip limit is set to 85°C, as temperature rises above 85°C, bit 14 of temperature register will be set to a one. Bit 14 will remain set until the ambient temperature drops below the threshold (85°C) minus the hysteresis value or 83.5°C. Note: Hysteresis is also applied to the $\overline{\text{EVENT}}$ pin functionality. When either of the Crit_Alarm Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
8	SHTDWN	**Shutdown Mode:** 0 = Temperature sensor enabled for continuous conversion (power-on default). 1 = Temperature sensor disabled. In shutdown mode, the temperature sensor is not active and will not generate interrupts or update temperature data. The $\overline{\text{EVENT}}$ pin is deasserted (not driven). When either of the Crit_Alarm Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
7	CRTALML	**Crit_Alarm Trip Lock bit:** Locks the Critical Alarm Trip Register from being updated. 0 = Crit_Alarm Trip Register can be updated (power-on default). 1 = Crit_Alarm Trip Register is locked and cannot be updated. Once set, it can be only be cleared to zero by internal POR which occurs when the device is powered off and then powered on.
6	WINLOCK	**Alarm Window Lock bit:** 0 = Upper and Lower Alarm Trip Registers can be updated (Power-on default). 1 = Upper and Lower Alarm Trip Registers are locked and cannot be updated. Once set, it can be only be cleared to zero by internal POR when device is powered off then powered on.
5	EVTCLR	**$\overline{\text{EVENT}}$ Clear:** This bit is a write only bit and will read zero. This bit can clear the $\overline{\text{EVENT}}$ pin after it has been enabled and is self clearing. 0 = has no effect (power-on default). 1 = clears (releases) the active $\overline{\text{EVENT}}$ pin in interrupt mode. This bit is ignored when in comparator mode.

Table 11-6. Configuration Register Bit Description (Continued)

Bit	Symbol	Description
4	EVTSTS	**$\overline{\text{EVENT}}$ Pin Output Status:** 0 = The $\overline{\text{EVENT}}$ Output is not asserted by the device (power-on default). 1 = The $\overline{\text{EVENT}}$ Output is asserted due to an alarm trip condition. Note: This bit will be cleared when entering shutdown mode and will resume status update immediately upon exiting shutdown.
3	EVTOUT	**$\overline{\text{EVENT}}$ Output Control:** This bit, when set, prevents the $\overline{\text{EVENT}}$ pin from generating an interrupt. 0 = The $\overline{\text{EVENT}}$ output is disabled and will not generate interrupts (power-on default). 1 = The $\overline{\text{EVENT}}$ output is enabled. When either of the Crit_Alarm Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
2	CRITEVT	**Critical Temperature Only:** 0 = The $\overline{\text{EVENT}}$ output is asserted for the Upper, Lower, and Critical Alarms (power-on default). 1 = The $\overline{\text{EVENT}}$ output is asserted for only Critical Alarm when ambient temperature > Crit_Alarm trip boundary. When the Alarm Window lock bit is set, this bit cannot be altered until unlocked.
1	EVTPOL	**$\overline{\text{EVENT}}$ Polarity:** 0 = Active Low (power-on default). A pull-up resistor is required on this pin to set inactive state. 1 = Active High. When either of the Crit_Alarm Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked
0	EVTMOD	**$\overline{\text{EVENT}}$ Mode:** 0 = The $\overline{\text{EVENT}}$ pin will operate in Comparator mode (power-on default). 1 = The $\overline{\text{EVENT}}$ pin will operate in Interrupt mode. When either of the Crit_Alarm Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.

Any JEDEC TSE2002av compliant temperature sensor can be configured to report an over temperature limit condition to the host system via its $\overline{\text{EVENT}}$ pin. These temperature sensors have the default value for all temperature alarm thresholds set at 0°C.

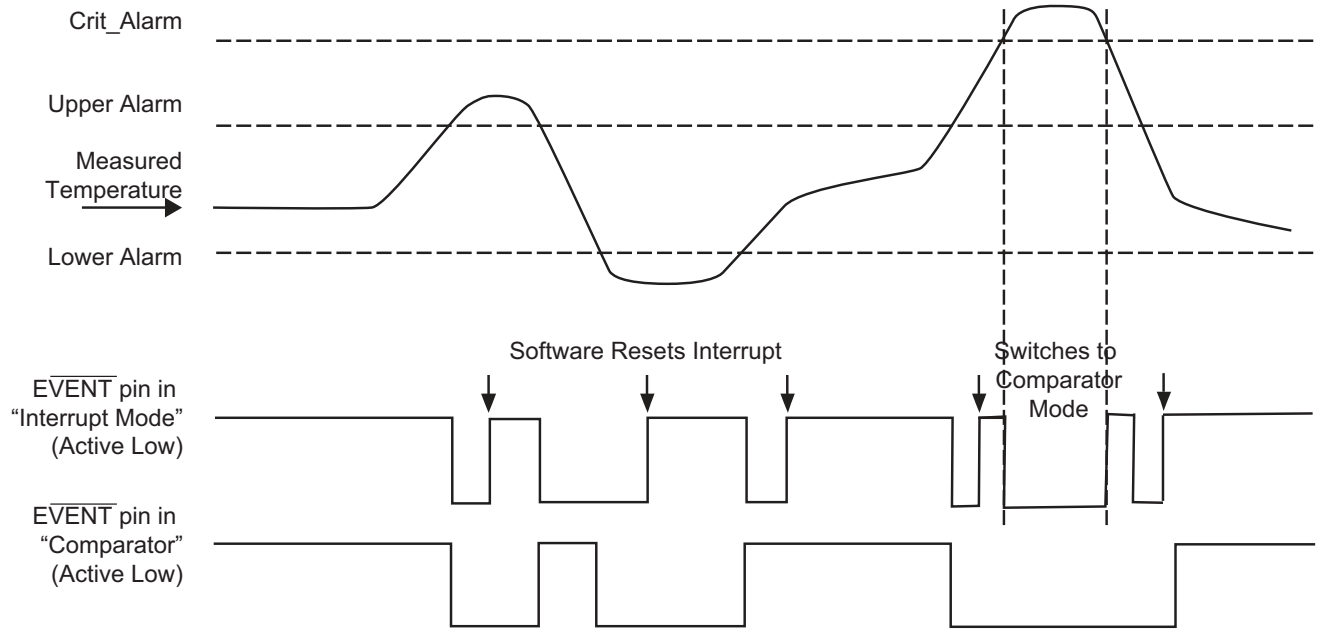
Often, if a system designer determines to utilize only the Critical Alarm temperature threshold to trigger an Event, it is likely he would only setup the Critical Alarm temperature threshold to a proper value while leaving the Upper Alarm temperature threshold unchanged at the default (0°C).

Due to some ambiguity in the TSE2002av specification, it is possible a temperature sensor can process bit three (Event Output Control) of the Configuration register first while others process bit two (Critical Temperature only) first from the Configuration register. If both bits are set to Logic 1 state concurrently and bit three is processed first, the Event output would be enabled before learning the Upper Alarm temperature threshold should be ignored. Since the Upper Alarm temperature threshold is often left unchanged at 0°C if it is not used and if the temperature sensor operates in a greater than 0°C environment, it naturally outputs an Event condition. Sometime later, after bit two is also processed, the temperature sensor would ignore the Upper Alarm temperature threshold and deassert the Event output if the ambient temperature has not exceeded the Critical Alarm temperature threshold; however, for a system that triggers action off this Event output, this correction has arrived too late.

To remedy this ambiguity in the TSE2002av specification, one must avoid setting both bit two and three of the Configuration register to Logic 1 concurrently. Instead, bit two should be set first before bit three in separate commands to offer universal compatibility if the system is designed to only trigger off the Critical Alarm temperature threshold.

Please see the Atmel Application Note, "Utilizing a Digital Temperature Sensor in a DDR3 DIMM," for more details.

Figure 11-1. $\overline{\text{EVENT}}$ Pin Mode Functionality



11.4 Upper Alarm Trip Register (16-bit Read/Write, Address = 02h)

The Upper Alarm Trip Register holds the user programmed upper temperature boundary trip point in 11-bit twos complement format (0.25°C resolution) that can be used to monitor ambient temperature in an operating window (See Table 11-7 and Table 11-8). When the temperature increases above this trip point, or drops below, or is equal to the trip point (minus any hysteresis set), then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). This register becomes read-only if the Alarm Window Lock bit (WINLOCK) bit six in the configuration register is set to a one.

Table 11-7. Upper Alarm Trip Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	ALMWINH			
Default Value	0	0	0	0	0	0	0	0
R / W access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ALMWINH						RFU	
Default Value	0	0	0	0	0	0	0	0
R / W access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 11-8. Upper Alarm Trip Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as zero.
12	SIGN	**Sign bit:** 0 = Ambient temperature is greater than or equal to 0°C. 1= Ambient temperature is less than 0°C.
11:2	ALMWINH	**Upper Alarm Trip temperature bits:** Represented in two's complement format.
0:1	RFU	***Reserved*** for ***Future Use***. Read as zero.

11.5 Lower Alarm Trip Register (16-bit Read/Write, Address = 03h)

The Lower Alarm Trip Register holds the user programmed lower temperature boundary trip point in 11-bit twos complement format (0.25°C resolution) that can be used to monitor ambient temperature in an operating window (See Table 11-9 and Table 11-10). When temperature decreases below this trip point minus any hysteresis set or increases to meet or exceed this trip point, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled).

This register becomes read-only if the Alarm Window Lock bit (WINLOCK) bit six in the Configuration register is set to a one.

Table 11-9. Lower Alarm Trip Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	ALMWINL			
Default Value	0	0	0	0	0	0	0	0
R / W access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ALMWINL						RFU	
Default Value	0	0	0	0	0	0	0	0
R / W access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 11-10. Lower Alarm Trip Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as zero.
12	SIGN	**Sign bit:** 0 = Ambient temperature is greater than or equal to 0°C. 1 = Ambient temperature is less than 0°C.
11:2	ALMWINL	**Lower Alarm Trip temperature bits:** Represented in twos complement format.
0:1	RFU	***Reserved*** for ***Future Use***. Read as zero.

11.6 Critical Alarm Trip Register (16-bit Read/Write, Address = 04h)

The Critical Alarm Trip Register holds the user programmed Critical Alarm temperature boundary trip point in 11-bit twos complement format (0.25°C resolution) that can be used to monitor ambient temperature (See Table 11-11 and Table 11-12). When the temperature increases above this trip point, the $\overline{\text{EVENT}}$ pin will be asserted (if enabled). It will remain asserted until temperature decreases below or equal to the trip point minus any hysteresis set. This register becomes read only if the Critical Alarm Trip Lock Bit (CRTALML) bit seven in the configuration register is set to a one.

Table 11-11. Critical Alarm Trip Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	CRITEVT			
Default Value	0	0	0	0	0	0	0	0
R / W access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CRITEVT						RFU	
Default Value	0	0	0	0	0	0	0	0
R / W access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 11-12. Critical Alarm Trip Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as zero.
12	SIGN	**Sign bit:** 0 = Ambient temperature is greater than or equal to 0°C. 1 = Ambient temperature is less than 0°C.
11:2	CRITEVT	**Critical Alarm Trip temperature bits:** Represented in two's complement format.
0:1	RFU	***Reserved*** for *Future Use*. Read as zero.

11.7 Temperature Register (16-bit Read-only, Address = 05h)

The Temperature Register holds the internal temperature measurement data represented in 11-bit twos complement word format allowing for resolution equal to 0.125°C (least significant bit). The upper three bits (15, 14, and 13) of the temperature register indicates the trip status of the current temperature and most important, are not affected by the status of the output of the $\overline{\text{EVENT}}$ pin (See Table 11-13 and Table 11-14).

Table 11-13. Temperature Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	CRITHIGH	ALMHIGH	ALMLOW	SIGN	128°C	64°C	32°C	16°C
Default Value	0	0	0	0	0	0	0	0
R / W access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0.125°C	RFU
Default Value	0	0	0	0	0	0	0	0
R / W access	R	R	R	R	R	R	R	R

Table 11-14. Temperature Register Bit Description

Bit	Symbol	Description
15	CRITHIGH	0 = Ambient temperature is less than the Critical Alarm Trip Register setting. 1 = Ambient temperature is greater than or equal to Critical Alarm Trip Register setting. When this bit is set one, it will automatically clear once the measured temperature decreases below or is equal to the trip point minus any hysteresis set.
14	ALMHIGH	0 = Ambient temperature is below the Upper Alarm Trip register setting. 1 = Ambient temperature is above the Upper Alarm Trip register setting. When the bit is set one, it will automatically clear once the measured temperature decreases below or is equal to the trip point minus any hysteresis set.
13	ALMLOW	0 = Ambient temperature is above the Lower Alarm Trip register setting. 1 = Ambient temperature is below the Lower Alarm Trip register setting. When the bit is set one, it will automatically clear once the measured temperature increases above or is to equal to the trip point.
12	SIGN	**Sign bit:** 0 = Ambient temperature is greater than or equal to 0°C. 1 = Ambient temperature is less than 0°C.
11:1	TEMP	**Ambient Temperature bits:** Represented in twos complement format. The encoding of bits B11 through B2 is the same as in the Alarm Trip Registers.
0	RFU	***Reserved*** for ***Future Use***. Read as zero.

11.7.1 Temperature Register Format

This section will clarify the temperature register format and temperature bit value assignments used for temperature for the following registers: Upper Alarm Trip, Lower Alarm Trip, Critical Alarm Trip, and Temperature Data Registers. The temperatures expressed in the Upper Alarm Trip, Lower Alarm Trip, Critical Alarm Trip, and Temperature Data Registers are indicated in twos complement format. In each of the trip registers, bits 12 through bit two are used for temperature settings, or in the case of the temperature register, holds the internal temperature measurement with bits 12 through bit one allowing 0.125ºC resolution.

Table 11-15 indicates the temperature register's assigned bit values used for temperature. Table 11-15 below shows examples for temperature register bit values for various temperature readings.

Table 11-15. Temperature Register Format

Bit Position	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Value	SIGN	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0.125°C	X

Table 11-16. Temperature Register Examples

Temperature Register Value Examples	
Temperature	**Binary (Bit 15 – Bit 0)**
+125°C	xxx0 0111 1101 00xx
+99.75°C	xxx0 0110 0011 11xx
+85°C	xxx0 0101 0101 00xx
+39°C	xxx0 0010 0111 00xx
+15.75°C	xxx0 0000 1111 11xx
+0.25°C	xxx0 0000 0000 01xx
0°C	xxx0 0000 0000 00xx
-0.25°C	xxx1 1111 1111 11xx
-1°C	xxx1 1111 1110 00xx
-20°C	xxx1 1110 1100 00xx

11.8 Manufacturer ID Register (16-bit Read-only, Address = 06h)

This register is used to identity the manufacturer of the product. The manufacturer ID for the AT30TSE002B is 001Fh (See Table 11-17).

Table 11-17. Manufacturer ID Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	Manufacturer ID							
Default Value	0	0	0	0	0	0	0	0
R / W access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Manufacturer ID							
Default Value	0	0	0	1	1	1	1	1
R / W access	R	R	R	R	R	R	R	R

11.9 Device ID Register (16-bit Read-only, Address = 07h)

The upper or high order byte is used to specify the device identification and the other byte is used to specify device revision. The Device ID for the AT30TSE002B is 8201h (See Table 11-18).

Table 11-18. Device ID Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	Device ID							
Default Value	1	0	0	0	0	0	1	0
R / W access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Device Revision							
Default Value	0	0	0	0	0	0	0	1
R / W access	R	R	R	R	R	R	R	R

11.10 SMBus Register (16-bit Write/Read only, Address = 22h)

The SMBus Register allows the user to enable or disable the SMBus time out feature (See Table 11-19 and Table 11-20).

Table 11-19. SMBus Register Bit Distribution

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Default Value	0	0	0	0	0	0	0	0
R / W access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SMBOUT	RFU						
Default Value	0	0	0	0	0	0	0	0
R / W access	R/W	R	R	R	R	R	R	R

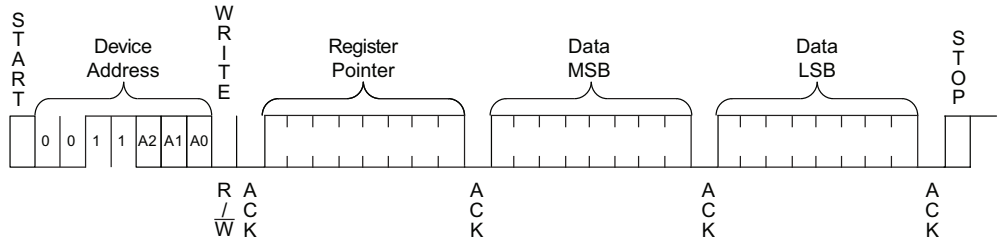
Table 11-20. SMBus Register Bit Distribution

Bit	Symbol	Description
15:8	RFU	***Reserved*** for ***Future Use***. Read as zero.
7	SMBOUT	**SMBus Timeout:** 0 = SMBus Timeout is enabled. 1 = SMBus Timeout is disabled. When enabled, timeout is active for temperature sensor operations. When either of the Crit_Alarm Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
6:0	RFU	***Reserved*** for ***Future Use***. Read as zero.

12. TS Write Operations

Writing to the AT30TSE002B Temperature register set is accomplished through a modified write operation for two data bytes. To maintain 2-wire compatibility, the 16-bit register is accessed through a pointer register, requiring the write sequence to include an address pointer in addition to the device address. This indicates the storage location for the next two bytes received. Table 12-1 shows an entire write transaction on the bus.

Figure 12-1. TS Register Write Operation



12.1 TS Read Operations

Reading data from the TS may be accomplished in one of two ways:

- If the location latched in the pointer register is correct (for normal operation it is expected the same address will be read repeatedly for temperature), the read sequence may consist of a device address from the bus master followed by two bytes of data from the device; or
- The pointer register is loaded with the correct register address, and the data is read. The sequence to preset the pointer register is shown in Figure 12-4, and the preset pointer read is shown in Figure 12-3. If it is desired to read random address each cycle, the complete pointer write, word read sequence is shown in Figure 12-4.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (No ACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

Figure 12-2. Write to Pointer Register

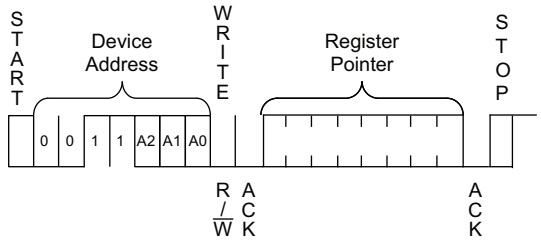


Figure 12-3. Preset Pointer Register Word Read

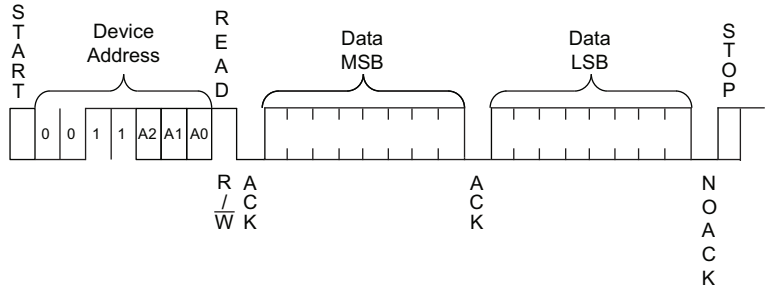


Figure 12-4. 2-wire Pointer Write Register Word Read

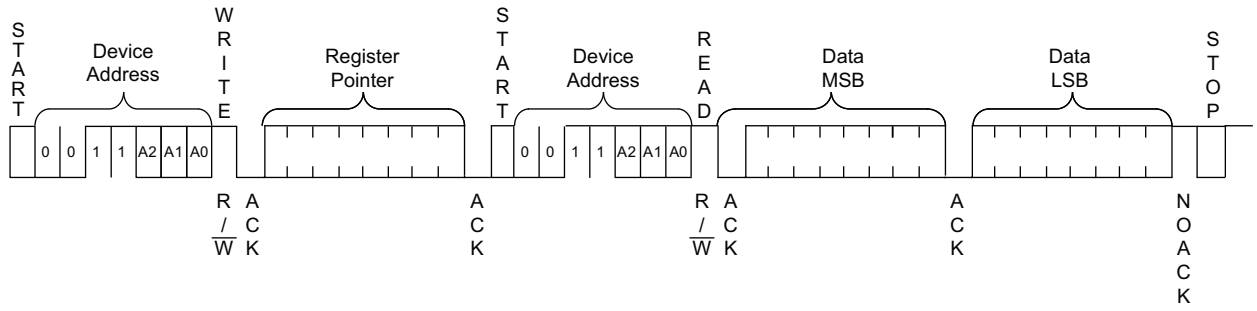
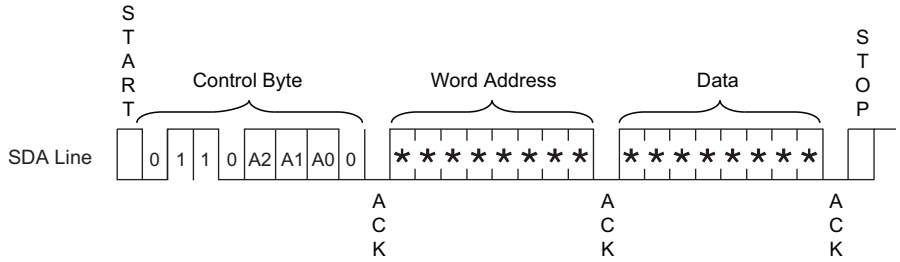
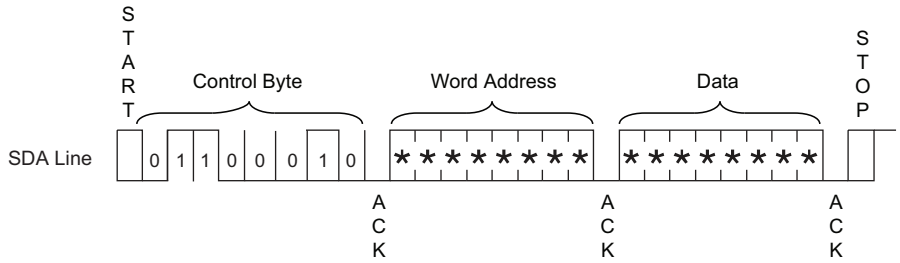


Figure 12-5. Setting Permanent Write Protect Register (PSWP)



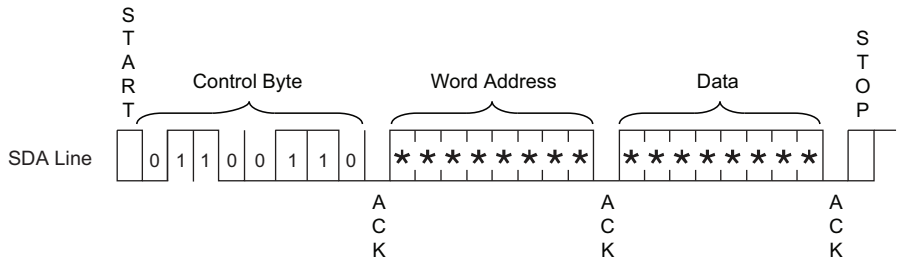
* = Dummy bit

Figure 12-6. Setting Reversible Write Protect Register (RSWP)



* = Dummy bit

Figure 12-7. Clearing Reversible Write Protect Register (RSWP)



* = Dummy bit

Table 12-1. EEPROM Write Protection

Command	Pin			Preamble							R/W
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
Set PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	0
Set RSWP	0	0	VHV	0	1	1	0	0	0	1	0
Clear RSWP	0	1	VHV	0	1	1	0	0	1	1	0

Table 12-2. VHV

	Min	Max	Units
VHV	7	10	V

Table 12-3. EEPROM Software Write Protection

Command	R/W Bit	Permanent Write Protect Register PSWP	Reversible Write Protect Register RSWP	Acknowledgement from Device	Action from Device
1010	R	X	X	ACK	
1010	W	Programmed	X	ACK	Can write to second Half (80H - FFH) only.
1010	W	X	Programmed	ACK	Can write to second Half (80H - FFH) only.
1010	W	Not Programmed	Not Programmed	ACK	Can write to full array.
Read PSWP	R	Programmed	X	No ACK	Stop – Indicates Permanent Write Protect Register is programmed.
Read PSWP	R	Not Programmed	X	ACK	Read out data don't care. Indicates PSWP Register is not programmed.
Set PSWP	W	Programmed	X	No ACK	Stop – Indicates Permanent Write Protect Register is programmed.
Set PSWP	W	Not Programmed	X	ACK	Program Permanent Write Protect Register (irreversible).
Read RSWP	R	X	Programmed	No ACK	Stop – Indicates Reversible Write Protect Register is programmed.
Read RSWP	R	X	Not Programmed	ACK	Read out data don't care. Indicates RSWP Register is not programmed.
Set RSWP	W	X	Programmed	No ACK	Stop – Indicates Reversible Write Protect Register is programmed.
Set RSWP	W	X	Not Programmed	ACK	Program Reversible Write Protect Register (reversible).
Clear RSWP	W	Programmed	X	No ACK	Stop – Indicates Permanent Write Protect Register is programmed.
Clear RSWP	W	Not Programmed	X	ACK	Clear (unprogram) Reversible Write Protect Register (reversible).

13. EEPROM Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read, and sequential read.

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. To end the command, the microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 13-4).

Random Read: A random read requires a dummy byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. To end the command, the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 13-5).

Sequential Read: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an ACK. As long as the EEPROM receives an ACK, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 13-6).

Permanent Write Protect Register (PSWP) Status: To find out if the register has been programmed, the same procedure is used as to program the register except that the R/W bit is set to one. If the device sends an acknowledge, then the permanent write protect register has not been programmed; otherwise, it has been programmed and the device is permanently write protected at the first half of the array.

Table 13-1. PSWP Status

	Pin			Preamble							R/W
Command	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
Read PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	1

Reversible Write Protect Register (RSWP) Status: To find out if the register has been programmed, the same procedure is used as to program the register except that the R/W bit is set to one. If the device sends an acknowledge, then the reversible write protect register has not been programmed; otherwise, it has been programmed and the device is write protected (reversible) at the first half of the array.

Figure 13-1. EEPROM Device Address

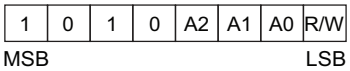


Figure 13-2. EEPROM Byte Write

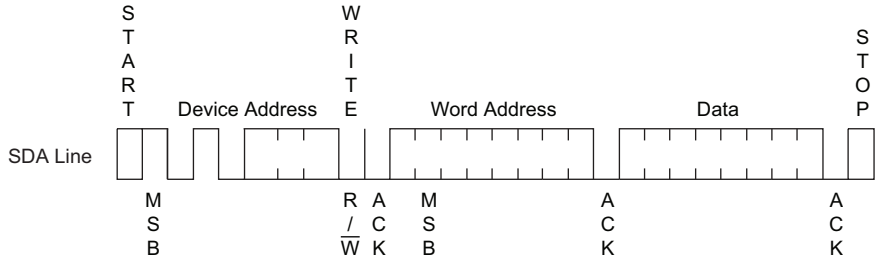


Figure 13-3. EEPROM Page Write

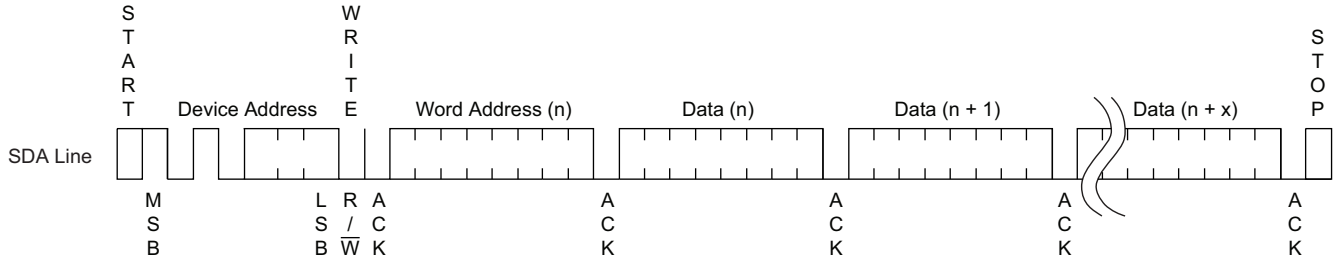


Figure 13-4. EEPROM Current Address Read

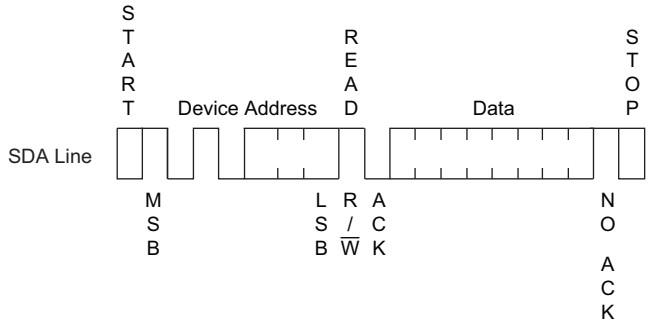


Figure 13-5. EEPROM Random Read

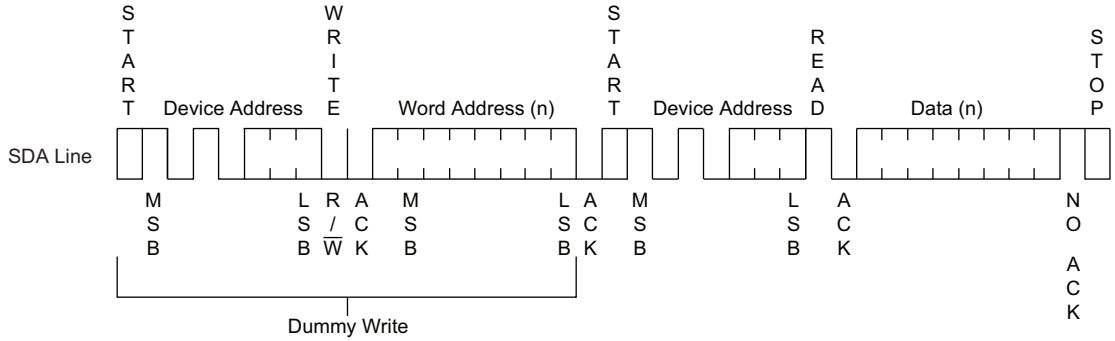
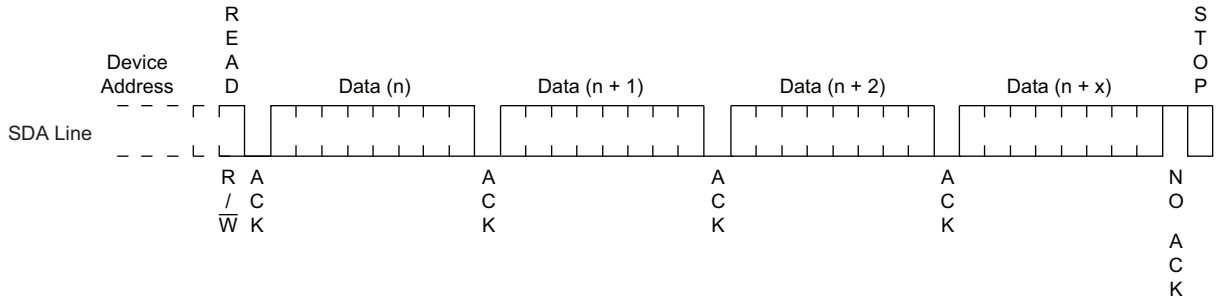


Figure 13-6. EEPROM Sequential Read



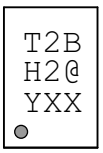
14. Part Marking

14.1 WDFN Marking

AT30TSE002B: Package Marking Information

8-lead UDFN

2.0 x 3.0 mm Body



Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

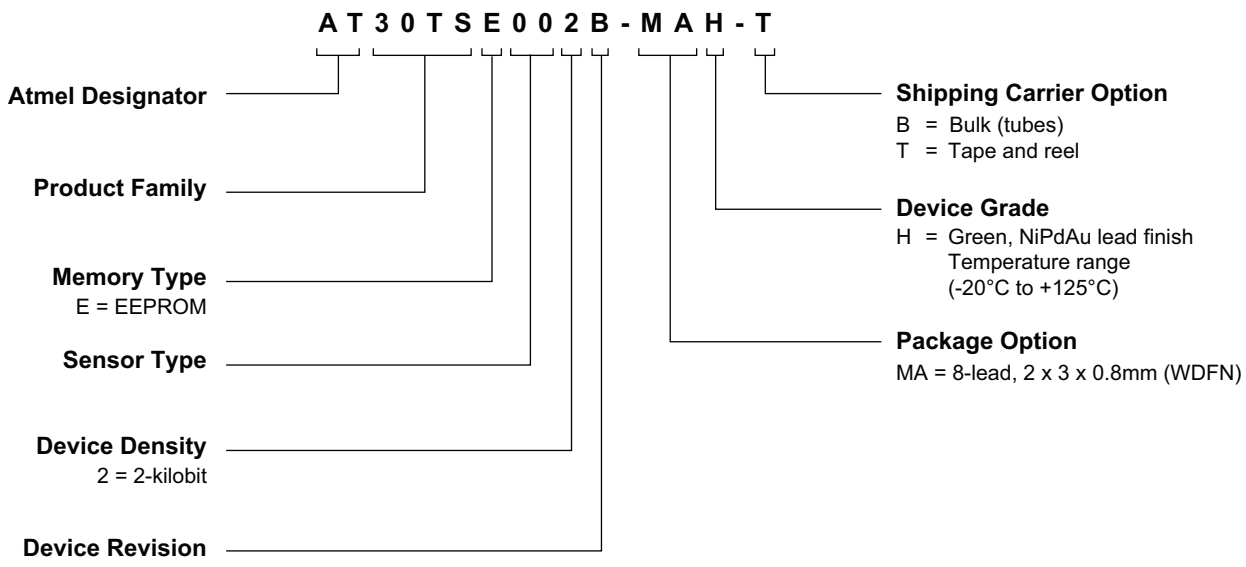
Catalog Number Truncation			
AT30TSE002B		Truncation Code: T2B	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	2: 2.7V min
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		H: Industrial/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

5/14/12

Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	30TSE002BSM, AT30TSE002B Package Marking Information	30TSE002BSM	D

15. Ordering Information

15.1 Ordering Code Detail



15.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

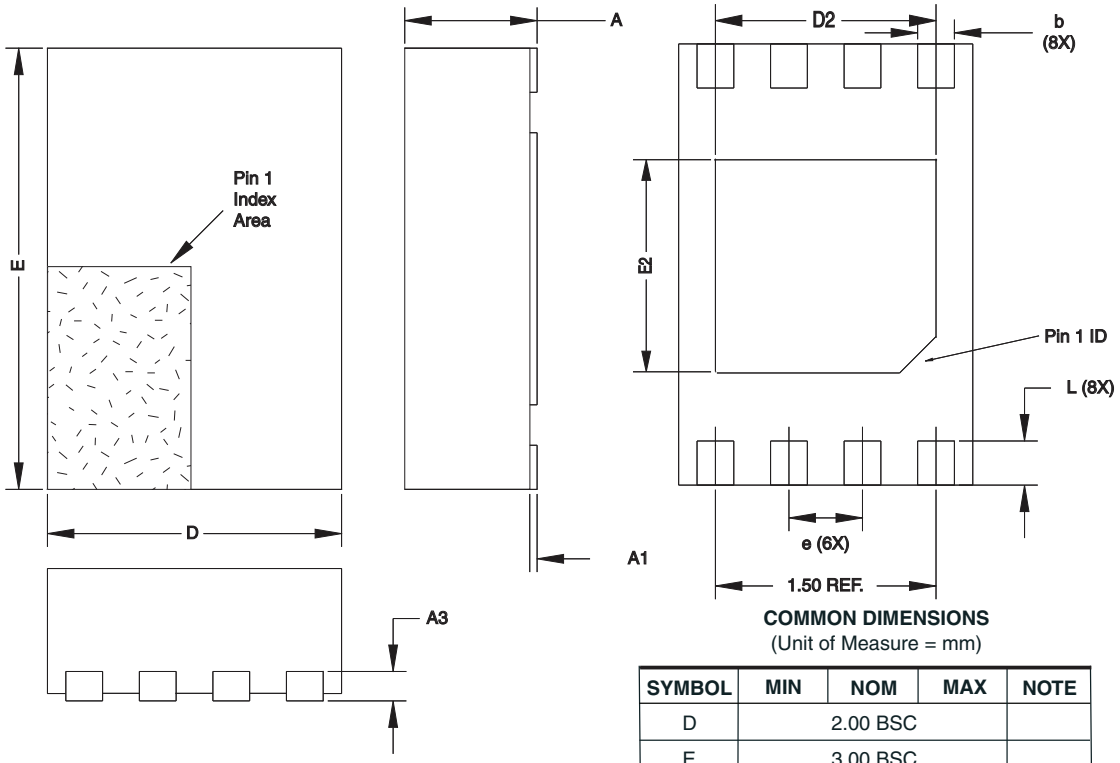
Ordering Code	Package	Lead Finish	Operating Voltage	Max. Freq. (KHz)	Operational Range
AT30TSE002B-MAH-T	8M2	NiPdAu	2.7V to 3.6V	400	–20°C to 125°C

Note: 1. T = Tape and reel
- WDFN = 5K per reel

Package Type	
8M2	8-lead, 2 x 3 x 0.8mm, Thermally Enhanced Plastic Very Very Thin Dual Flat No Lead (WDFN)

16. Package Drawings

16.1 8M2 – 8-lead WDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.35	1.40	1.45	
E2	1.25	1.30	1.35	
A	0.70	0.75	0.80	
A1	0.0	0.02	0.05	
A3		0.20 REF		
L	0.35	0.40	0.45	
e		0.50 BSC		
b	0.18	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, WCED-3, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

6/12/09

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8M2, 8-lead** 2.0x3.0 mm Body, 0.50 mm Pitch, WDFN, Very Very Thin, Dual No Lead Package (Sawn)	YDL	8M2	A

17. Revision History

Doc. Rev.	Date	Comments
8711G	05/2012	Add JEDEC TSE2002av compliant paragraphs after the Configuration Register Bit Description table. Update template.
8711F	03/2011	WDFN marking added “2” and @ = location of assembly.
8711E	12/2010	Update Table, “Register Summary,” 00D7h to 00F7H. Correct cross reference in EEPROM Write Protection and TS WRITE Operations sections. Change note under Green Package Options table.
8711D	08/2010	Update R to R / W for 22h in Register Summary table. Correct cross references in EEPROM Write Operations.
8711C	07/2010	Section 12.2, change part number to -MAH-T from -MA-T.
8711B	05/2010	Add statement in Section 2 before Serial Clock definition.
8711A	04/2010	Initial document release.

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