Features

- Fast Read Access Time - 90 ns
- Five-Volt-Only Reprogramming
- Sector Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 512 Sectors (128 bytes/sector)
  - Internal Address and Data Latches for 128 Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Sector Program Cycle Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability CMOS Technology
  - 1000 Program Cycles per Sector
  - 10-Year Data Retention
- Single 5 V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges

512K (64K x 8) 5-Volt Only CMOS Flash PEROM

Description

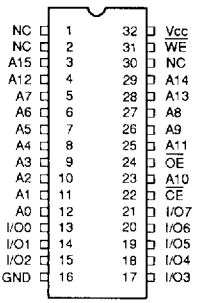
The AT29C512 is a five-volt-only in-system Flash Programmable and Erasable Read Only Memory (PEROM). Its 512K of memory is organized as 65,536 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

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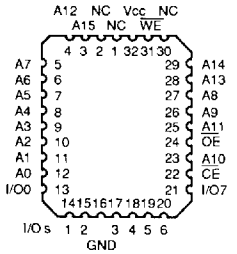
Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View



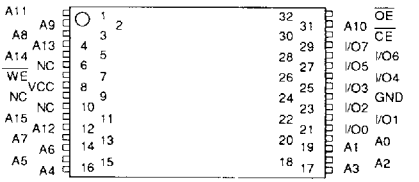
PLCC and LCC Top View



Note: PLCC package pin 30 is a DON'T CONNECT.

TSOP Top View

Type 1



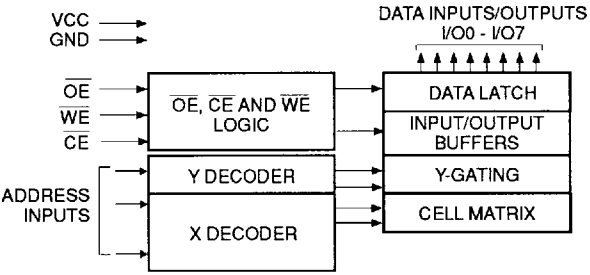
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Description (Continued)

To allow for simple in-system reprogrammability, the AT29C512 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C512 is performed on a sector basis; 128 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Block Diagram



Device Operation

READ: The AT29C512 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: Byte loads are used to enter the 128 bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

PROGRAM: The device is reprogrammed on a sector basis. If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A15 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C512. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the sector program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high.

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Device Operation (Continued)

The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 128 bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C512 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{DATA}$ POLLING: The AT29C512 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C512 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. This parameter is characterized and is not 100% tested

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D.C. and A.C. Operating Range

		AT29C512-90	AT29C512-12	AT29C512-15	AT29C512-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1-A15 = V_{IL}, A9 = V_H,[3] A0 = V_{IL}	Manufacturer Code[4]
				A1-A15 = V_{IL}, A9 = V_H,[3] A0 = V_{IH}	Device Code[4]
Software[5]				A0 = V_{IL}	Manufacturer Code[4]
				A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V
4. Manufacturer Code: 1F, Device Code: 5D
5. See details under Software Product Identification Entry/Exit.

D.C. Characteristics

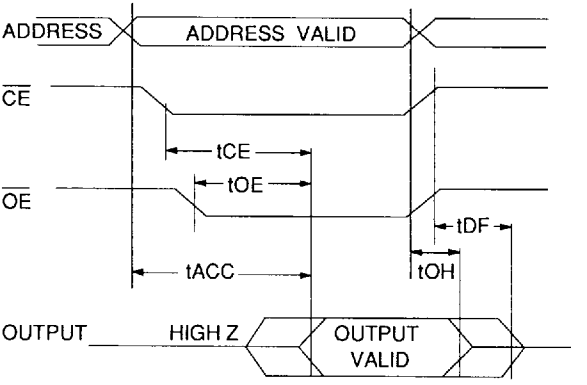
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3 V to V_{CC}	Com.		100	µA
			Ind., Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5 V		4.2		V

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A.C. Read Characteristics

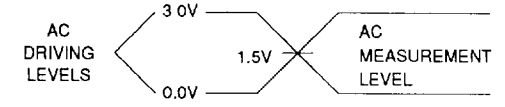
Symbol	Parameter	AT29C512-90		AT29C512-12		AT29C512-15		AT29C512-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120		150		200	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	0	80	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



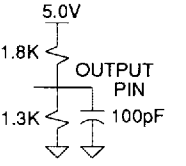
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load

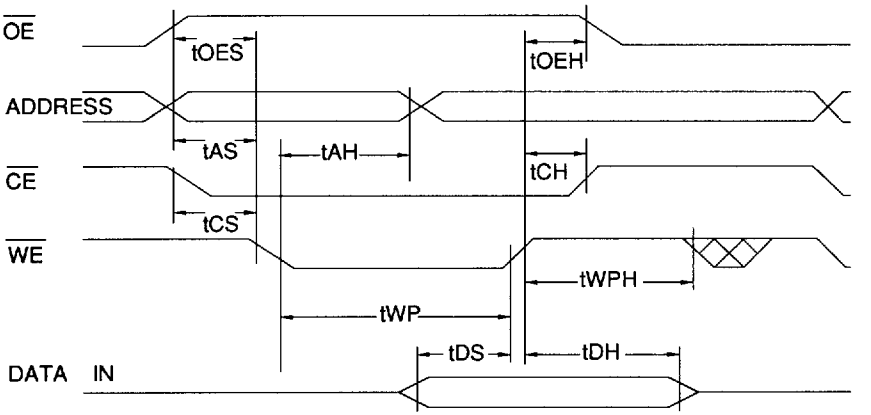


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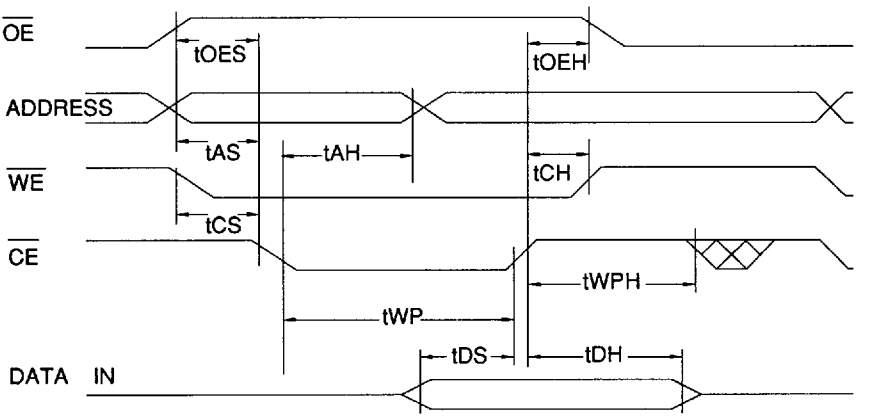
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



A.C. Byte Load Waveforms- $\overline{CE}$ Controlled

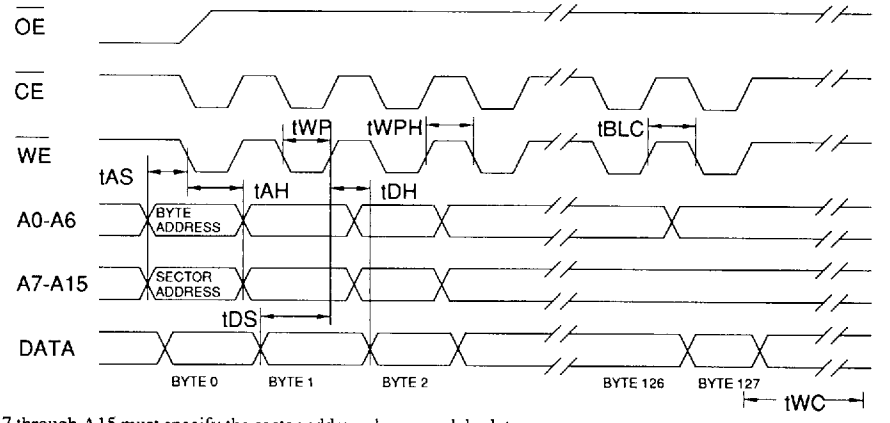


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Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

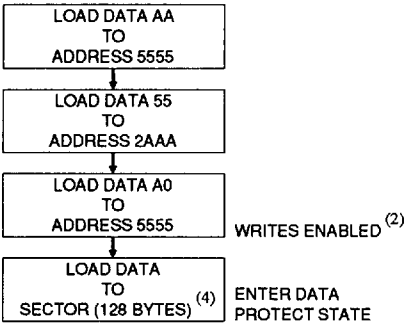
Program Cycle Waveforms



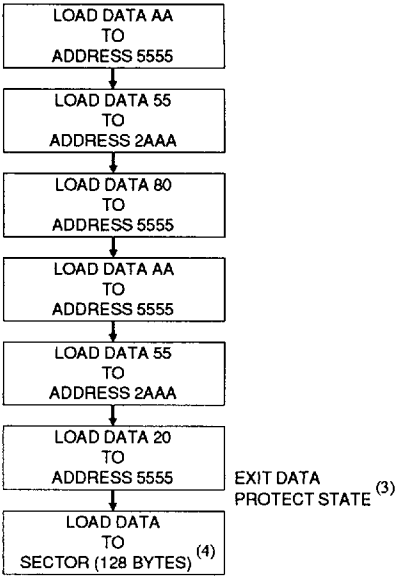
Notes: A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the sector being programmed will be erased to FF.

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Software Data Protection Enable Algorithm [1]

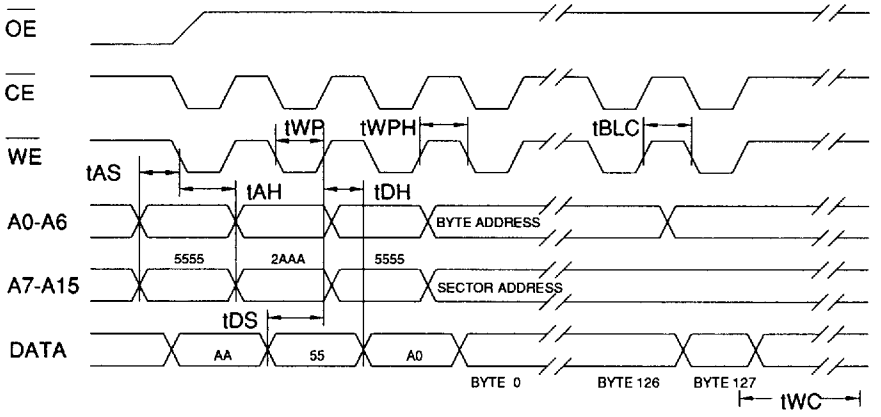


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 128 bytes of data MUST BE loaded.

Software Protected Program Cycle Waveform



Notes: A7 through A15 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the sector being programmed will be erased to FF.

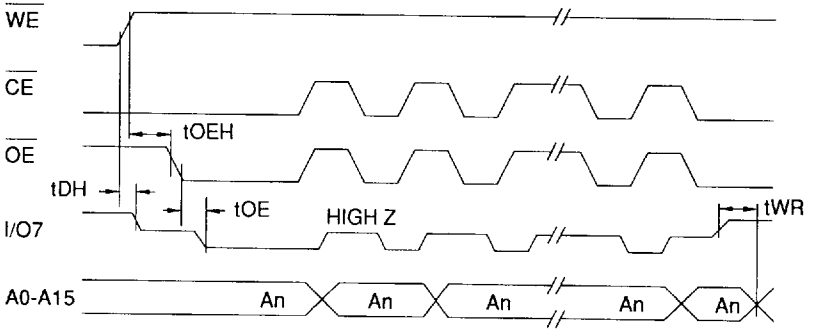
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$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]			100	ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in A.C. Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

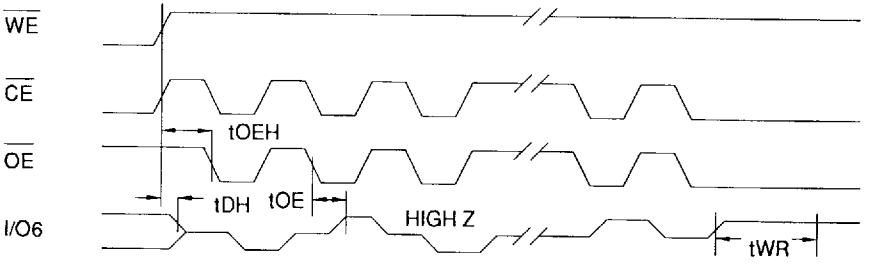


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes. 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in A.C. Read Characteristics.

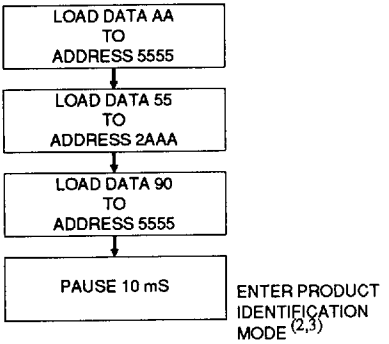
Toggle Bit Waveforms



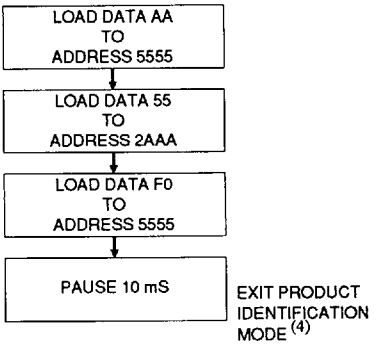
Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary

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Software Product Identification Entry [1]



Software Product Identification Exit [1]

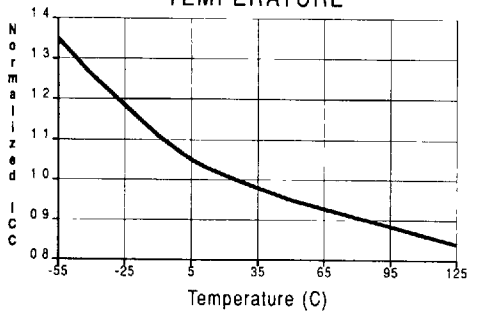


Notes for software product identification:

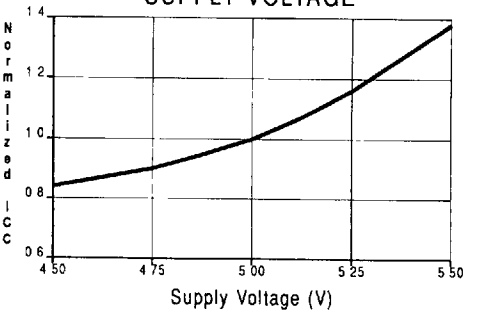
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A15 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: 5D

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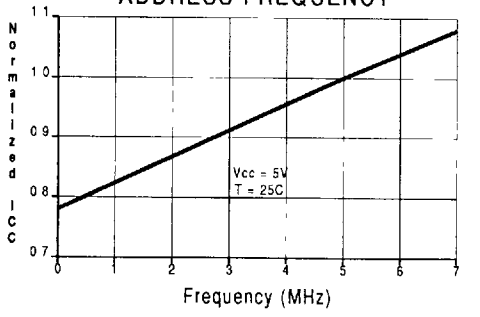
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



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Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.1	AT29C512-90DC AT29C512-90JC AT29C512-90PC	32D6 32J 32P6	Commercial (0° to 70°C)
90	50	0.3	AT29C512-90DI AT29C512-90JI AT29C512-90PI	32D6 32J 32P6	Industrial (-40° to 85°C)
120	50	0.1	AT29C512-12DC AT29C512-12JC AT29C512-12PC AT29C512-12TC	32D6 32J 32P6 32T	Commercial (0° to 70°C)
120	50	0.3	AT29C512-12DI AT29C512-12JI AT29C512-12PI	32D6 32J 32P6	Industrial (-40° to 85°C)
			AT29C512-12DM	32D6	Military (-55°C to 125°C)
			AT29C512-12DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	50	0.1	AT29C512-15DC AT29C512-15JC AT29C512-15PC AT29C512-15TC	32D6 32J 32P6 32T	Commercial (0° to 70°C)
150	50	0.3	AT29C512-15DI AT29C512-15JI AT29C512-15PI	32D6 32J 32P6	Industrial (-40° to 85°C)
			AT29C512-15DM	32D6	Military (-55°C to 125°C)
			AT29C512-15DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	AT29C512-20DC AT29C512-20JC AT29C512-20PC	32D6 32J 32P6	Commercial (0° to 70°C)
200	50	0.3	AT29C512-20DI AT29C512-20JI AT29C512-20PI	32D6 32J 32P6	Industrial (-40° to 85°C)
			AT29C512-20DM	32D6	Military (-55°C to 125°C)
			AT29C512-20DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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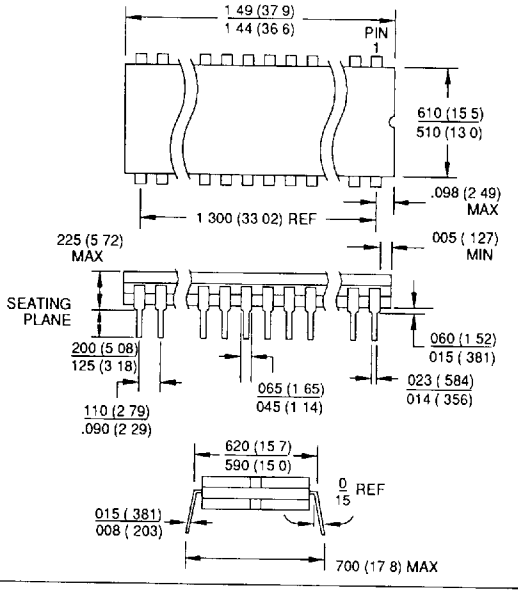
Ordering Information

	Package Type
32D6	32 Lead, 0 600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32 Lead, Thin Small Outline Package (TSOP)

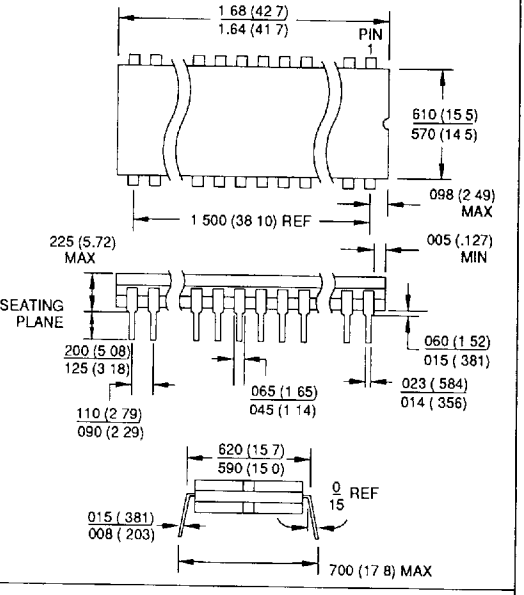
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Packaging Information

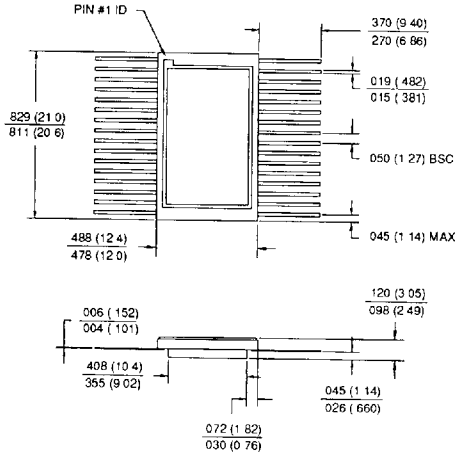
28D6, 28 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-10 CONFIG 1



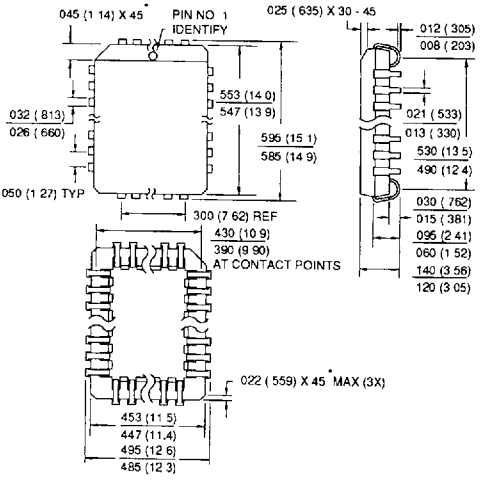
32D6, 32 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 CONFIG A



32F, 32 Lead, Non-Windowed,
Ceramic Bottom Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-18 CONFIG B
JEDEC OUTLINE MO-115



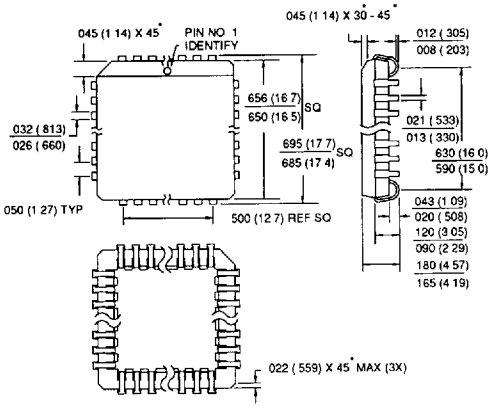
32J, 32 Leadd, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-52 AC



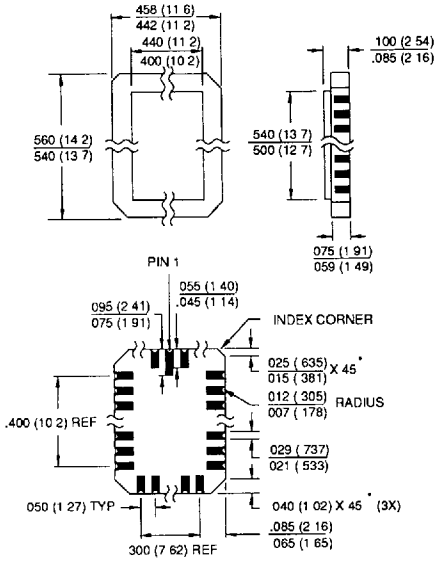
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Packaging Information

44J, 44 Leadd, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-47 AC

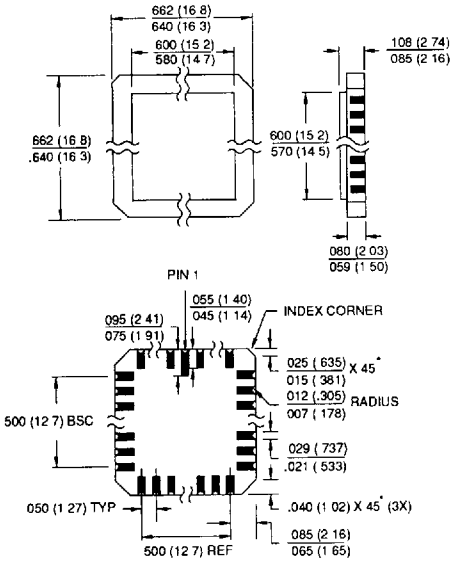


32L, 32 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*



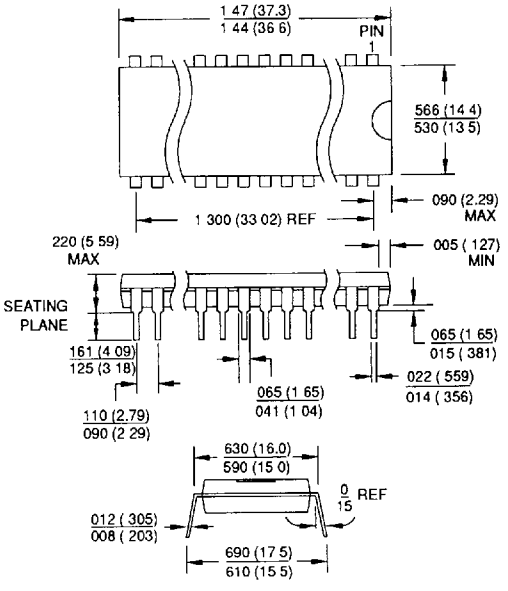
*Ceramic lid standard unless specified

44L, 44 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*



*Ceramic lid standard unless specified.

28P6, 28 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

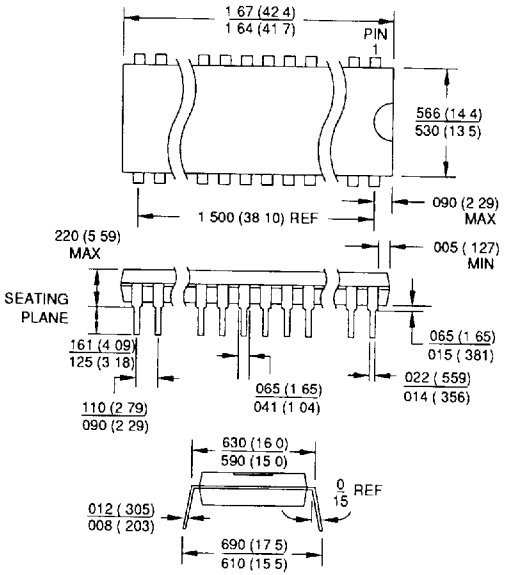


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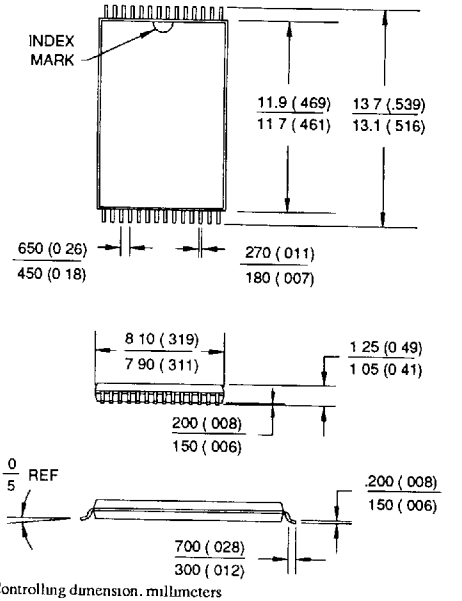
1074177 0007046 082

Packaging Information

32P6, 32 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

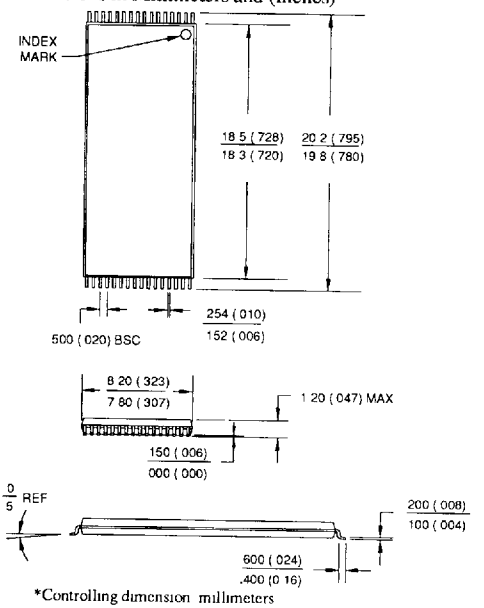


28T, 28 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches)*



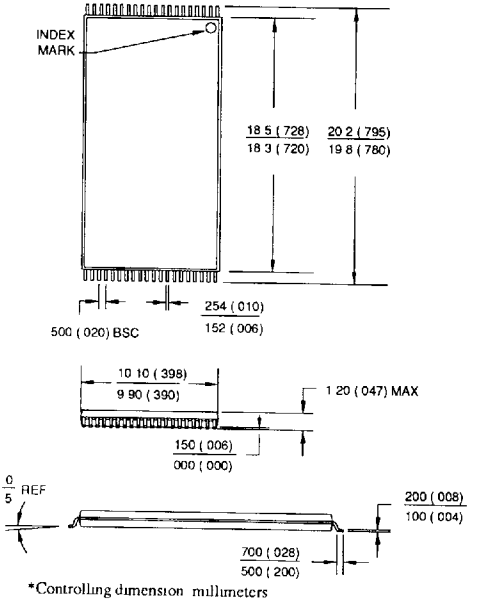
*Controlling dimension: millimeters

32T, 32 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

40T, 40 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches)*

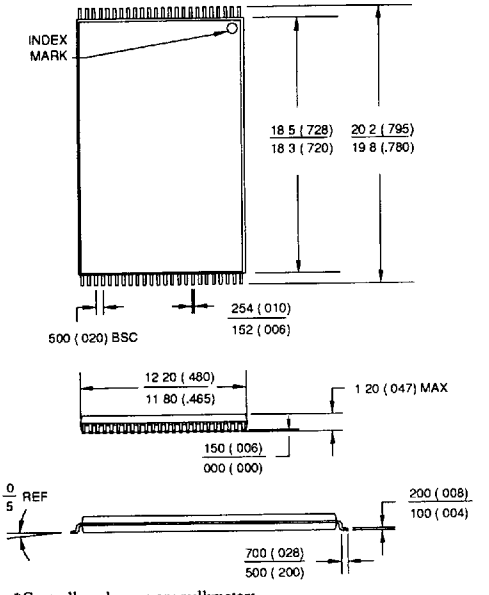


*Controlling dimension: millimeters

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Packaging Information

48T, 48 Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

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