## Features

- Fast read access time – 90ns
- Dual voltage range operation
  - Unregulated battery power supply range, 2.7V to 3.6V, or
  - Standard power supply range, 5V ± 10%
- Compatible with JEDEC standard Atmel® AT27C010
- Low-power CMOS operation
  - 20µA max standby (less than 1µA, typical) for $V_{CC}$ = 3.6V
  - 29mW max active at 5MHz for $V_{CC}$ = 3.6V
- JEDEC standard package
  - 32-lead PLCC
- High-reliability CMOS technology
  - 2,000V ESD protection
  - 200mA latchup immunity
- Rapid programming algorithm – 100µs/byte (typical)
- CMOS- and TTL-compatible inputs and outputs
  - JEDEC standard for LVTTL and LVBO
- Integrated product identification code
- Industrial temperature range
- Green (Pb/halide-free) packaging option

# 1Mb (128K x 8) Unregulated Battery Voltage, One-time Programmable, Read-only Memory

## Atmel AT27BV010

## 1. Description

The Atmel AT27BV010 is a high-performance, low-power, low-voltage 1,048,576-bit, one-time programmable, read-only memory (OTP EPROM) organized as 128K by 8 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

The innovative Atmel design techniques provide fast speeds that rival 5V parts, while keeping the low power consumption of a 3V supply. At $V_{CC}$ = 2.7V, any byte can be accessed in less than 90ns. With a typical power draw of only 18mW at 5MHz and $V_{CC}$ = 3V, the AT27BV010 consumes less than one-fifth the power of a standard, 5V EPROM. Standby mode supply current is typically less than 1µA at 3V. The AT27BV010 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV010 is available in an industry-standard, JEDEC-approved, one-time programmable (OTP) PLCC package. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27BV010 operating with $V_{CC}$ at 3.0V produces TTL-level outputs that are compatible with standard TTL logic devices operating at $V_{CC}$ = 5.0V. At $V_{CC}$ = 2.7V, the part is compatible with JEDEC-approved, low-voltage battery operation (LVBO) interface specifications. The device is also capable of standard, 5V operation, making it ideally suited for dual supply range systems or card products that are pluggable in both 3V and 5V hosts.

The AT27BV010 has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The integrated product identification code electronically identifies the device and manufacturer.

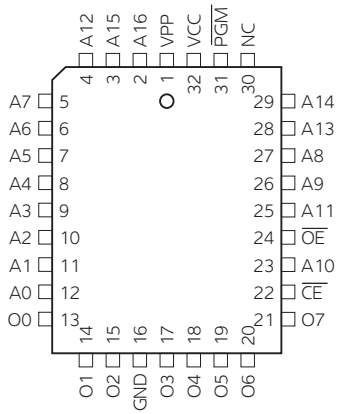
0344I–EPROM–4/11

This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages. The AT27BV010 programs in exactly the same way as a standard, 5V AT27C010, and uses the same programming equipment.

## 2. Pin configurations

| Pin name | Function |
|---|---|
| A0 - A16 | Addresses |
| O0 - O7 | Outputs |
| $\overline{CE}$ | Chip enable |
| $\overline{OE}$ | Output enable |
| $\overline{PGM}$ | Program strobe |
| NC | No connect |

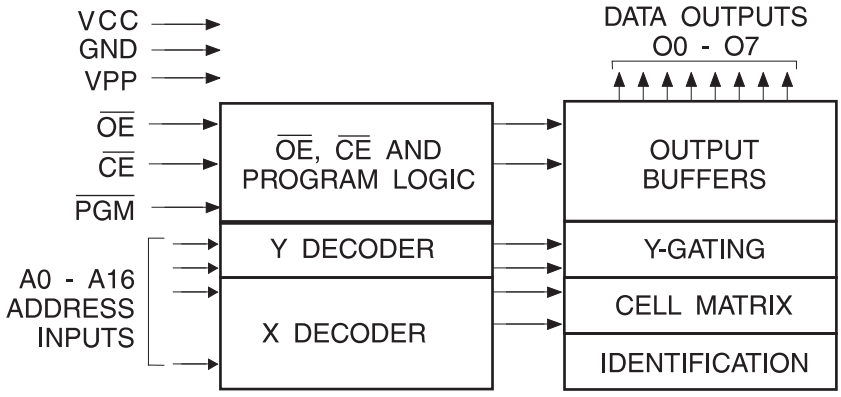
32-lead PLCC
Top view




## 3. System considerations

Switching between active and standby conditions via the chip enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1µF, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the $V_{CC}$ and ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7µF bulk electrolytic capacitor should be utilized, again connected between the $V_{CC}$ and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Figure 3-1. Block diagram



## 4. Absolute maximum ratings*

| | |
|---|---|
| Temperature under bias | -40°C to +85°C |
| Storage temperature | -65°C to +125°C |
| Voltage on any pin with respect to ground | -2.0V to +7.0V(1) |
| Voltage on A9 with respect to ground | -2.0V to +14.0V(1) |
| $V_{PP}$ supply voltage with respect to ground | -2.0V to +14.0V(1) |

*NOTICE: Stresses beyond those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC}$ + 0.75V DC, which may be exceeded if certain precautions are observed (consult application notes), and which may overshoot to +7.0V for pulses of less than 20ns.

## 5. AC and DC charcteristics

Table 5-1. Operating mode

| Mode/Pin | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | Ai | $V_{PP}$ | $V_{CC}$ | Outputs |
|---|---|---|---|---|---|---|---|
| Read(2) | $V_{IL}$ | $V_{IL}$ | X(1) | Ai | X | $V_{CC}$ | $D_{OUT}$ |
| Output disable(2) | X | $V_{IH}$ | X | X | X | $V_{CC}$ | High Z |
| Standby(2) | $V_{IH}$ | X | X | X | X | $V_{CC}$ | High Z |
| Rapid program(3) | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Ai | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |
| PGM verify(3) | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | Ai | $V_{PP}$ | $V_{CC}$ | $D_{OUT}$ |
| PGM inhibit(3) | $V_{IH}$ | X | X | X | $V_{PP}$ | $V_{CC}$ | High Z |
| Product identification(3)(5) | $V_{IL}$ | $V_{IL}$ | X | A9 = $V_H$(4)<br>A0 = $V_{IH}$ or $V_{IL}$<br>A1 - A16 = $V_{IL}$ | X | $V_{CC}$ | Identification code |

Note: 1. X can be $V_{IL}$ or $V_{IH}$.
2. Read, output disable, and standby modes require 2.7V ≤ $V_{CC}$ ≤ 3.6V or 4.5V ≤ $V_{CC}$ ≤ 5.5V.
3. Refer to programming characteristics. Programming modes require $V_{CC}$ = 6.5V.
4. $V_H$ = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low ($V_{IL}$) except A9, which is set to $V_H$, and A0, which is toggled low ($V_{IL}$) to select the manufacturer's identification byte and high ($V_{IH}$) to select the device code byte.

Table 5-2. DC and AC operating conditions for read operation

| | Atmel AT27BV010-90 |
|---|---|
| Industrial operating temperature (case) | -40°C - 85°C |
| $V_{CC}$ power supply | 2.7V to 3.6V |
| | 5V ± 10% |

Table 5-3. DC and operating characteristics for read operation

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ = 2.7V to 3.6V | | | | | |
| $I_{LI}$ | Input load current | $V_{IN}$ = 0V to $V_{CC}$ | | ±1 | µA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$ = 0V to $V_{CC}$ | | ±5 | µA |
| $I_{PP1}$ (2) | $V_{PP}$ (1) read/standby current | $V_{PP}$ = $V_{CC}$ | | 10 | µA |
| $I_{SB}$ | $V_{CC}$ (1) standby current | $I_{SB1}$ (CMOS), $\overline{CE}$ = $V_{CC}$ ± 0.3V | | 20 | µA |
| | | $I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V | | 100 | µA |
| $I_{CC}$ | $V_{CC}$ active current | f = 5MHz, $I_{OUT}$ = 0mA, $\overline{CE}$ = $V_{IL}$, $V_{CC}$ = 3.6V | | 8 | mA |
| $V_{IL}$ | Input low voltage | $V_{CC}$ = 3.0 to 3.6V | -0.6 | 0.8 | V |
| | | $V_{CC}$ = 2.7 to 3.6V | -0.6 | 0.2 x $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage | $V_{CC}$ = 3.0 to 3.6V | 2.0 | $V_{CC}$ + 0.5 | V |
| | | $V_{CC}$ = 2.7 to 3.6V | 0.7 x $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2.0mA | | 0.4 | V |
| | | $I_{OL}$ = 100µA | | 0.2 | V |
| | | $I_{OL}$ = 20µA | | 0.1 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -2.0mA | 2.4 | | V |
| | | $I_{OH}$ = -100µA | $V_{CC}$ - 0.2 | | V |
| | | $I_{OH}$ = -20µA | $V_{CC}$ - 0.1 | | V |
| $V_{CC}$ = 4.5V to 5.5V | | | | | |
| $I_{LI}$ | Input load current | $V_{IN}$ = 0V to $V_{CC}$ | | ±1 | µA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$ = 0V to $V_{CC}$ | | ±5 | µA |
| $I_{PP1}$ (2) | $V_{PP}$ (1) read/standby current | $V_{PP}$ = $V_{CC}$ | | 10 | µA |
| $I_{SB}$ | $V_{CC}$ (1) standby current | $I_{SB1}$ (CMOS), $\overline{CE}$ = $V_{CC}$ ± 0.3V | | 100 | µA |
| | | $I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V | | 1 | mA |
| $I_{CC}$ | $V_{CC}$ active current | f = 5MHz, $I_{OUT}$ = 0mA, $\overline{CE}$ = $V_{IL}$ | | 25 | mA |
| $V_{IL}$ | Input low voltage | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -400µA | 2.4 | | V |

Notes: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$, and removed simultaneously with or after $V_{PP}$.

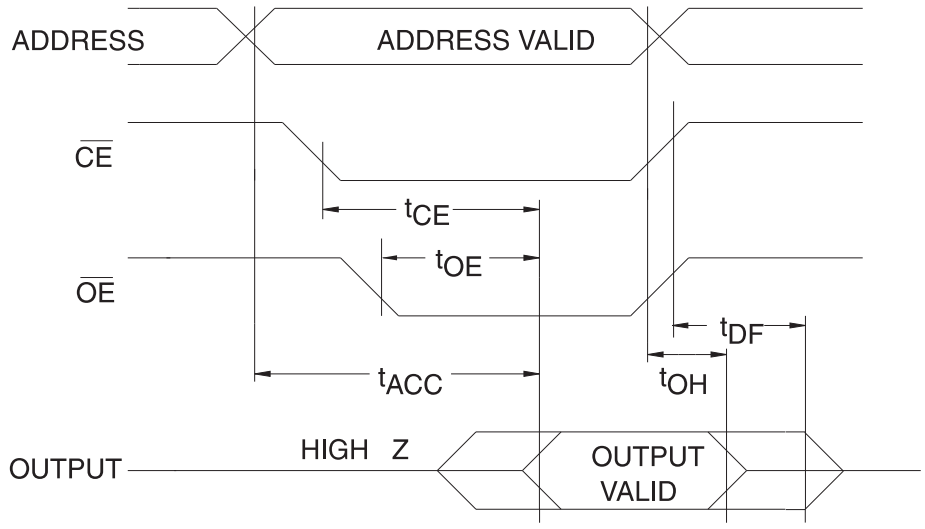
2. $V_{PP}$ may be connected directly to $V_{CC}$, except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP}$.

Table 5-4. AC characteristics for read operation

$V_{CC}$ = 2.7V to 3.6V and 4.5V to 5.5V

| Symbol | Parameter | Condition | -90 | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{ACC}$ (3) | Address to output delay | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | 90 | ns |
| $t_{CE}$ (2) | $\overline{CE}$ to output delay | $\overline{OE}$ = $V_{IL}$ | | 90 | ns |
| $t_{OE}$ (2)(3) | $\overline{OE}$ to output delay | $\overline{CE}$ = $V_{IL}$ | | 50 | ns |
| $t_{DF}$ (4)(5) | $\overline{OE}$ or $\overline{CE}$ high to output float, whichever occurred first | | | 40 | ns |
| $t_{OH}$ | Output hold from address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first | | 0 | | ns |

Figure 5-1. AC waveforms for read operation (1)




Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
3. $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the address is valid without impact on $t_{ACC}$.
4. This parameter is only sampled, and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Figure 5-2. Input test waveform and measurement level

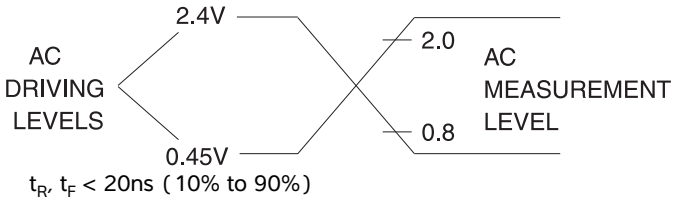
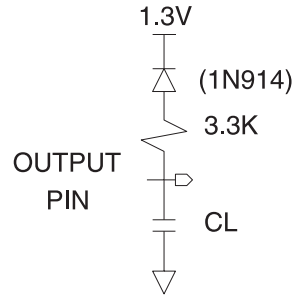


Figure 5-3. Output test load




Note: CL = 100pF
including jig capacitance.

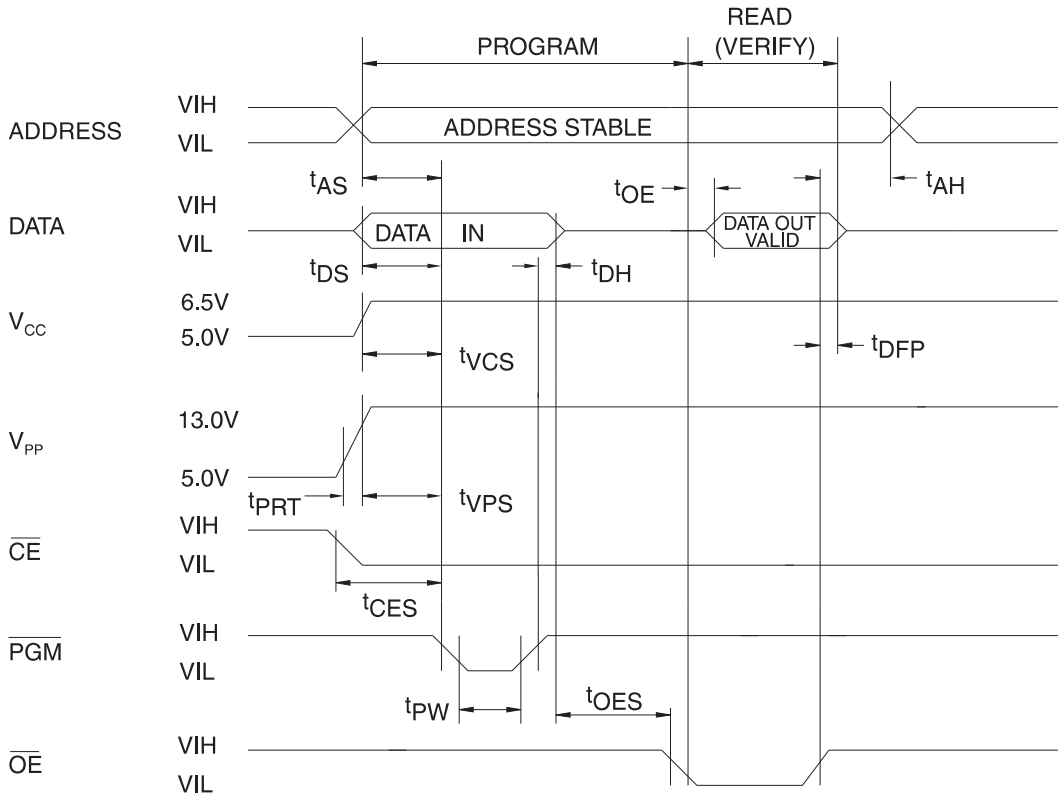
Table 5-5. Pin capacitance

f = 1MHz, T = 25°C[1]

| Symbol | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 8 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled, and is not 100% tested.

Figure 5-4. Programming waveforms[1]




Notes: 1. The input timing reference is 0.8V for $V_{IL}$ and 2.0V for $V_{IH}$.

2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device, but must be accommodated by the programmer.

3. When programming the Atmel AT27BV010, a 0.1µF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients.

Table 5-6. DC programming charcteristics

$T_A$ = 25 ± 5°C, $V_{CC}$ = 6.5 ± 0.25V, $V_{PP}$ = 13.0 ± 0.25V

| Symbol | Parameter | Test conditions | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{LI}$ | Input load current | $V_{IN} = V_{IL}, V_{IH}$ | | ±10 | µA |
| $V_{IL}$ | Input low level | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input high level | | 2.0 | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -400µA | 2.4 | | V |
| $I_{CC2}$ | $V_{CC}$ supply current (program and verify) | | | 40 | mA |
| $I_{PP2}$ | $V_{PP}$ supply current | $\overline{CE} = \overline{PGM} = V_{IL}$ | | 20 | mA |
| $V_{ID}$ | A9 product identification voltage | | 11.5 | 12.5 | V |

Table 5-7. AC programming charcteristics

$T_A$ = 25 ± 5°C, $V_{CC}$ = 6.5 ± 0.25V, $V_{PP}$ = 13.0 ± 0.2V

| Symbol | Parameter | Test conditions[1] | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{AS}$ | Address setup time | Input rise and fall times: (10% to 90%) 20ns<br>Input pulse levels: 0.45V to 2.4V<br>Input timing reference level: 0.8V to 2.0V<br>Output timing reference level: 0.8V to 2.0V | 2 | | µs |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | µs |
| $t_{OES}$ | $\overline{OE}$ setup time | | 2 | | µs |
| $t_{DS}$ | Data setup time | | 2 | | µs |
| $t_{AH}$ | Address hold time | | 0 | | µs |
| $t_{DH}$ | Data hold time | | 2 | | µs |
| $t_{DFP}$ | $\overline{OE}$ high to output float delay[2] | | 0 | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ setup time | | 2 | | µs |
| $t_{VCS}$ | $V_{CC}$ setup time | | 2 | | µs |
| $t_{PW}$ | $\overline{PGM}$ program pulse width[3] | | 95 | 105 | µs |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | 150 | ns |
| $t_{PRT}$ | $V_{PP}$ pulse rise time during programming | | 50 | | ns |

Notes:
1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously with or after $V_{PP}$.
2. This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
3. Program pulse width tolerance is 100µsec ± 5%.

Table 5-8. The Atmel AT27BV010 integrated product identification code[1]

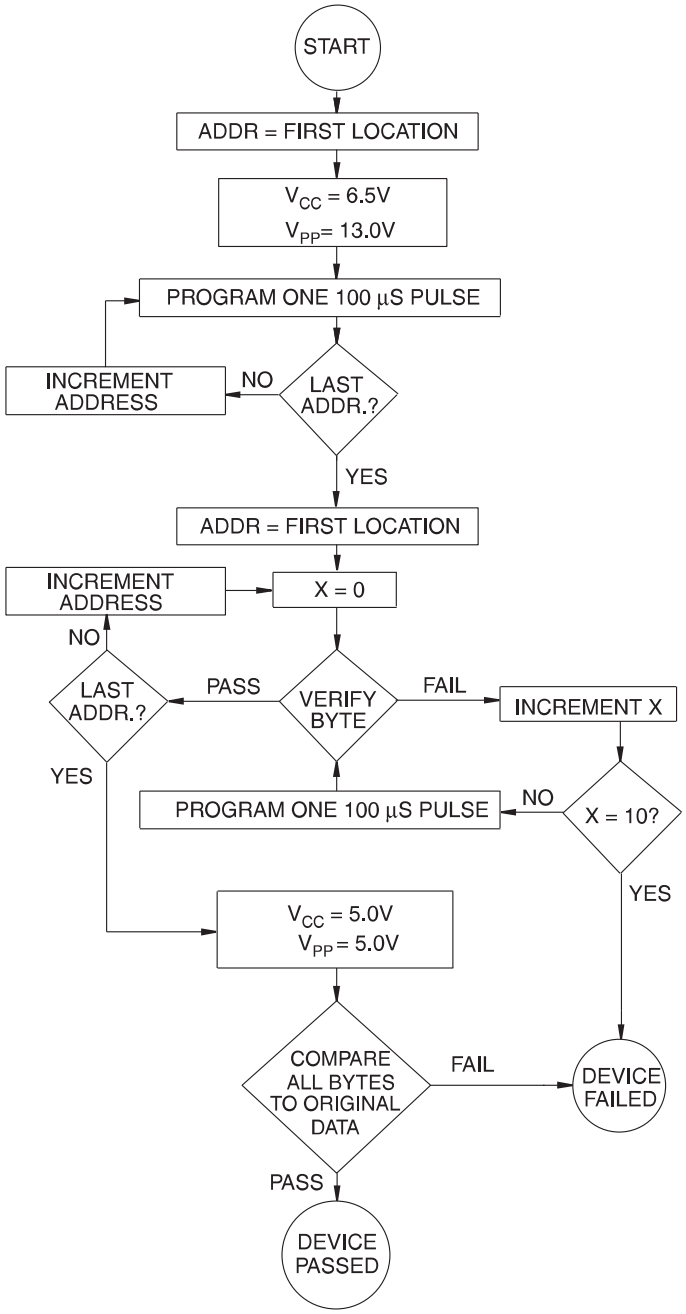
| Codes | Pins | | | | | | | | | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| | A0 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | |
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E |
| Device type | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |

Note: 1. The Atmel AT27BV010 has the same product identification code as the Atmel AT27C010. Both are programming compatible.

# 6. Rapid programming algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. $V_{CC}$ is raised to 6.5V and $V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $V_{PP}$ is then lowered to 5.0V and $V_{CC}$ to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Figure 6-1. Rapid programming algorithm



# 7. Ordering Information

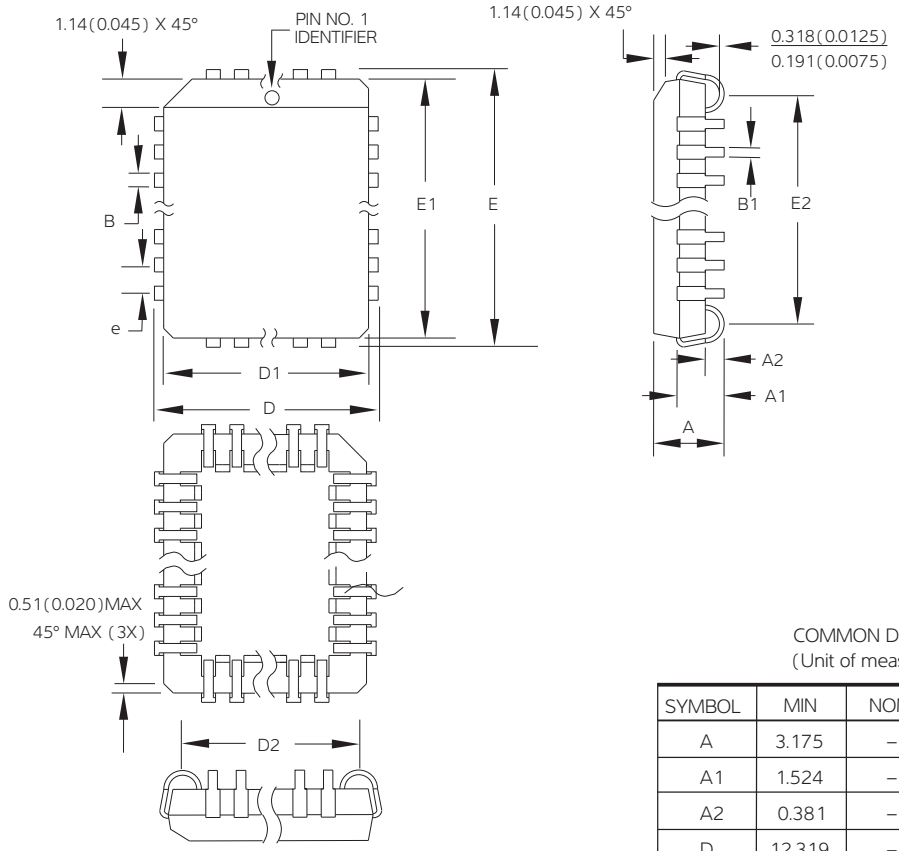
## Green package (Pb/hailde-free)

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) $V_{CC}$ = 3.6V | | Atmel ordering code | Lead finish | Package | Operation range |
|---|---|---|---|---|---|---|
| | Active | Standby | | | | |
| 90 | 8 | 0.02 | AT27BV010-90JU | Matte tin | 32J | Industrial (-40°C to 85°C) |

| Package types | |
|---|---|
| 32J | 32-lead, plastic, J-leaded chip carrier (PLCC) |

# 8. Packaging information

## 32J – PLCC




COMMON DIMENSIONS
(Unit of measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 3.175 | – | 3.556 | |
| A1 | 1.524 | – | 2.413 | |
| A2 | 0.381 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.354 | – | 11.506 | Note 2 |
| D2 | 9.906 | – | 10.922 | |
| E | 14.859 | – | 15.113 | |
| E1 | 13.894 | – | 14.046 | Note 2 |
| E2 | 12.471 | – | 13.487 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.10mm) maximum.

10/04/01

| Package Drawing Contact: packagedrawings@atmel.com | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| | 32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC) | 32J | B |

# 9. Revision history

| Doc. rev. | Date | Comments |
|---|---|---|
| 0344I | 04/2011 | Remove TSOP and VSOP packages<br>Add lead finish to ordering information |
| 0344H | 12/2007 | |

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