Features

- **Serial Peripheral Interface (SPI) Compatible**
- **Supports SPI Modes 0 (0,0) and 3 (1,1)**
  - **Data Sheet Describes Mode 0 Operation**
- **Low-voltage and Standard-voltage Operation**
  - **V_{CC} = 1.8V to 5.5V**
- **20 MHz Clock Rate (5V)**
- **8-byte Page Mode**
- **Block Write Protection**
  - **Protect 1/4, 1/2, or Entire Array**
- **Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection**
- **Self-timed Write Cycle (5 ms max)**
- **High Reliability**
  - **Endurance: One Million Write Cycles**
  - **Data Retention: 100 Years**
- **Green (Pb/Halogen-free/Rohs Compliant) Packaging Options**
- **Die Sales: Wafer Form, Waffle Pack, Bumped Wafers**

Description

The AT25010B/020B/040B provides 1024/2048/4096 bits of serial electrically erasable programmable read-only memory (EEPROM) organized as 128/256/512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25010B/020B/040B is available in space saving, JEDEC SOIC, UDFN, TSSOP, XDFN and VFBGA packages.

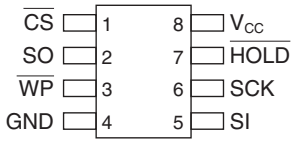
The AT25010B/020B/040B is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.

Block write protection is enabled by programming the status register with one of four blocks of write protection. Separate Program Enable and Program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

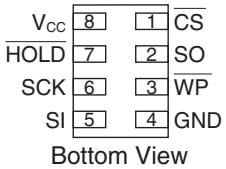
Table 0-1. Pin Configuration

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

SOIC, TSSOP

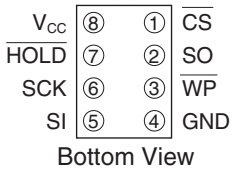


8-lead UDFN, XDFN



Bottom View

8-ball VFBGA



Bottom View

SPI Serial EEPROM

1K (128x8)

2K (256x8)

4K (512x8)

AT25010B
AT25020B
AT25040B

8707B–SEEPR–3/10

1. Absolute Maximum Ratings*

Operating Temperature	–40°C to + 125°C
Storage Temperature	–65°C to + 150°C
Voltage on Any Pin with Respect to Ground	–1.0V to + 7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram

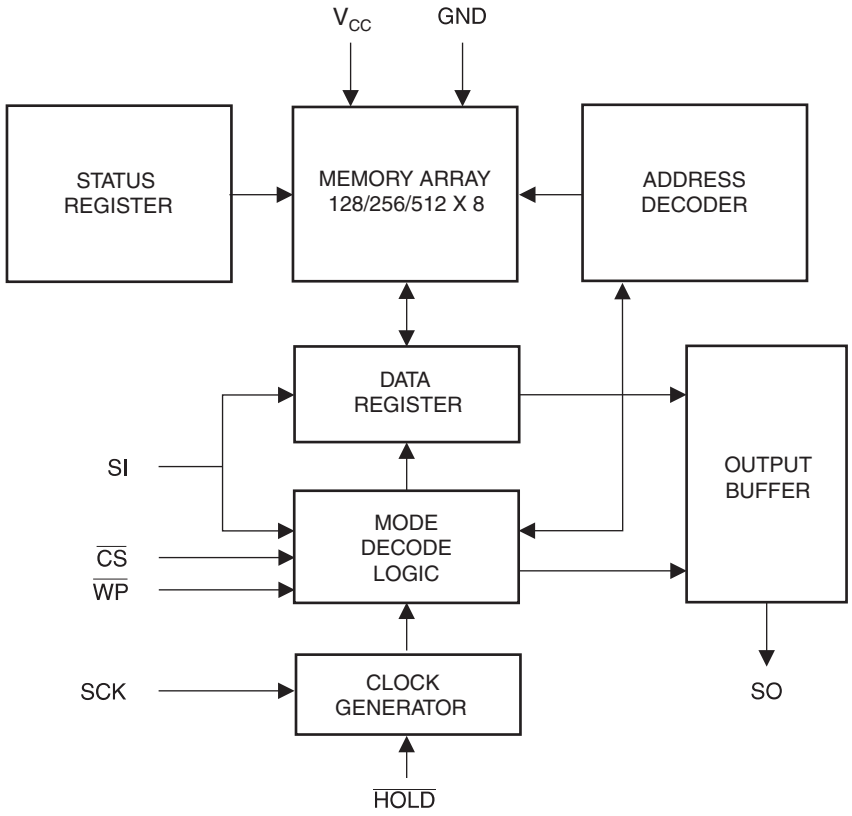


Table 1-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics[1]

Applicable over recommended operating range from: T_{AI} = –40·C to +85·C, V_{CC} = +1.8V to +5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 20 MHz, SO = Open, Read			8.5	10.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 10 MHz, SO = Open, Read, Write			4.5	5.0	mA
I_{CC3}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open, Read, Write			2.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			0.1	0.5	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V, $\overline{CS}$ = V_{CC}			0.2	1.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2.0	3.5	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–3.0			µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		–3.0		3.0	µA
V_{IL}[1]	Input Low-voltage			–0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High-voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low-voltage	3.6V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High-voltage		I_{OH} = –1.6 mA	V_{CC} – 0.8			V
V_{OL2}	Output Low-voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High-voltage		I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 1-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40 to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0	20 10 5	MHz
t_{RI}	Input Rise Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		2 2 2	µs
t_{FI}	Input Fall Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		2 2 2	µs
t_{WH}	SCK High Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	20 40 80		ns
t_{WL}	SCK Low Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	20 40 80		ns
t_{CS}	$\overline{CS}$ High Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	100 100 200		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	100 100 200		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	100 100 200		ns
t_{SU}	Data In Setup Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	20 40 80		ns
t_H	Data In Hold Time	4.5 – 5.5 2.5 - 5.5 1.8 - 5.5	20 40 80		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	20 40 80		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	20 40 80		ns
t_V	Output Valid	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0	20 40 80	ns
t_{HO}	Output Hold Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0		ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5	0 0 0	25 50 100	ns

Table 1-3. AC Characteristics (Continued)
Applicable over recommended operating range from T_{AI} = –40 to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
t_{HZ}	$\overline{Hold}$ to Output High Z	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		25 50 100	ns
t_{DIS}	Output Disable Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		25 50 100	ns
t_{WC}	Write Cycle Time	4.5 – 5.5 2.5 – 5.5 1.8 – 5.5		5 5 5	ms
Endurance[1]	5.0V, 25·C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

2. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the serial clock pin (SCK) is always an input, the AT25010B/020B/040B always operates as a slave.

TRANSMITTER/RECEIVER: The AT25010B/020B/040B has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed. The op-code also contains address bit A8 in both the read and write instructions.

INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25010B/020B/040B, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

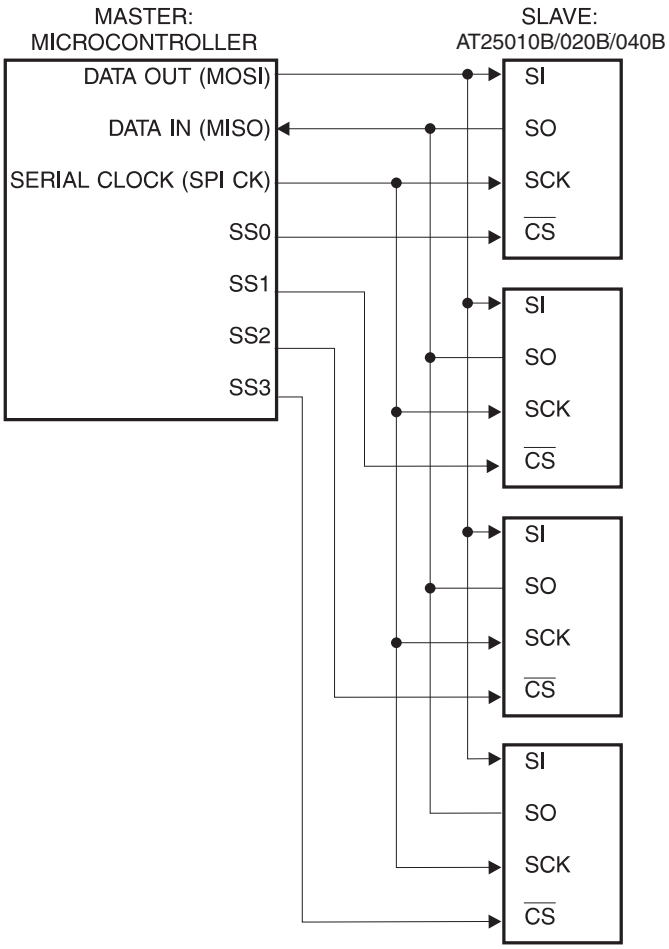
CHIP SELECT: The AT25010B/020B/040B is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the SO pin will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25010B/020B/040B. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low, all write operations are inhibited.

$\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the AT25010B/020B/040B. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

Figure 2-1. SPI Serial Interface



3. Functional Description

The AT25010B/020B/040B is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25010B/020B/040B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Figure 3-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{CS}$ transition.

Table 3-1. Instruction Set for the AT25010B/020B/040B

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: "A" represents MSB address bit A8.

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction. The $\overline{WP}$ pin must be held high during a WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The read/busy and write enable status of the device can be determined by the RDSR instruction. Similarly, the block write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 3-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 3-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = "0" ($\overline{RDY}$) indicates the device is ready. Bit 0 = "1" indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = "0" indicates the device *is not* write enabled. Bit 1 = "1" indicates the device is write enabled.
Bit 2 (BP0)	See Table 3-4.
Bit 3 (BP1)	See Table 3-4.
Bits 4–7 are "0"s when device is not in an internal write cycle.	
Bits 0–7 are "1"s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25010B/020B/040B is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in Table 3-4.

Bits BP1 and BP0 are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC}, RDSR).

Table 3-4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected		
	BP1	BP0	AT25010B	AT25020B	AT25040B
0	0	0	None	None	None
1 (1/4)	0	1	60–7F	C0–FF	180–1FF
2 (1/2)	1	0	40–7F	80–FF	100–1FF
3 (All)	1	1	00–7F	00–FF	000–1FF

READ SEQUENCE (READ): Reading the AT25010B/020B/040B via the SO pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the read op-code (including A8) is transmitted via the SI line followed by the byte address to be read (A7–A0). Upon completion, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous read cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25010B/020B/040B, the Write Protect pin ($\overline{WP}$) must be held high and two separate instructions must be executed. First, the device *must be write enabled* via the WREN instruction. Then a Write (WRITE) instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code (including A8) is transmitted via the SI line followed by the byte address (A7–A0) and the data (D7–D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The ready/busy status of the device can be determined by initiating a Read Status Register (RDSR) instruction. If Bit 0 = “1”, the write cycle is still in progress. If Bit 0 = “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

The AT25010B/020B/040B is capable of an 8-byte page write operation. After each byte of data is received, the three low-order address bits are internally incremented by one; the six high-order bits of the address will remain constant. If more than 8 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25010B/020B/040B is automatically returned to the write disable state at the completion of a write cycle.

Note: If the $\overline{WP}$ pin is brought low or if the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new CS falling edge is required to reinitiate the serial communication.

4. Timing Diagrams

Figure 4-1. Synchronous Data Timing (for Mode 0)

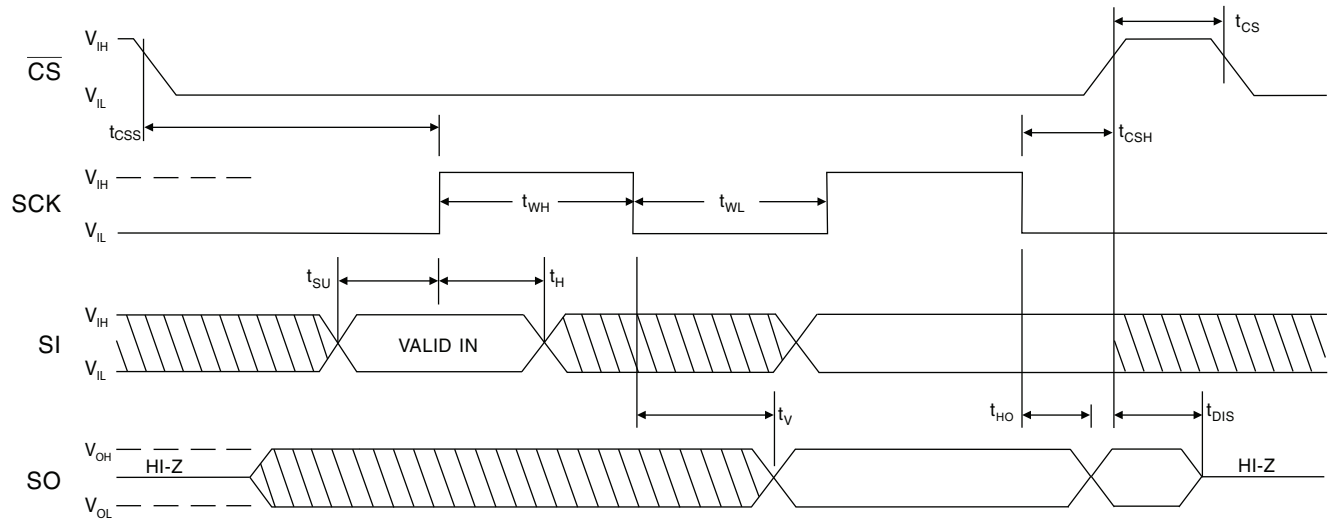


Figure 4-2. WREN Timing

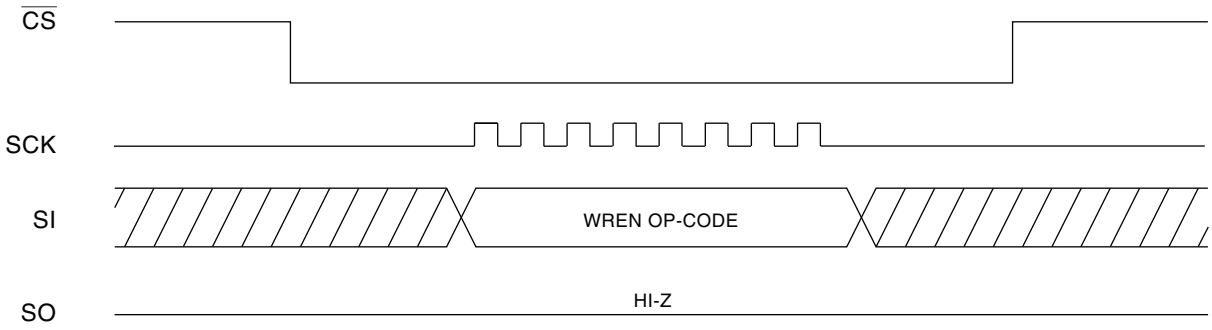


Figure 4-3. WRDI Timing

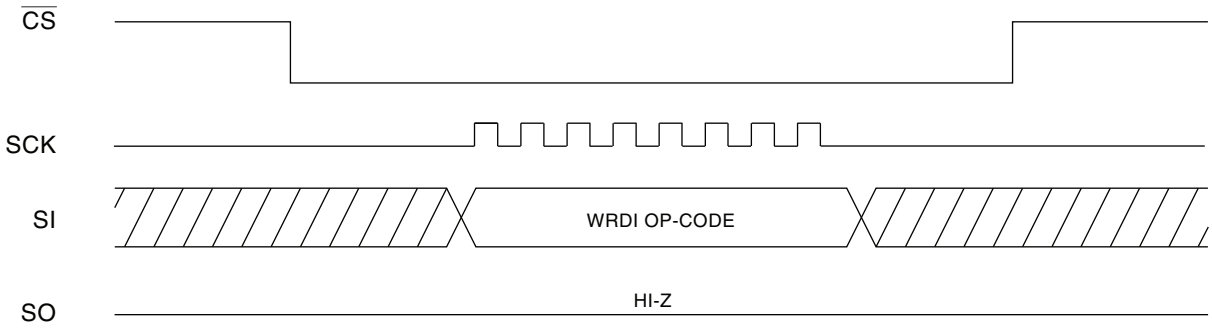


Figure 4-4. RDSR Timing

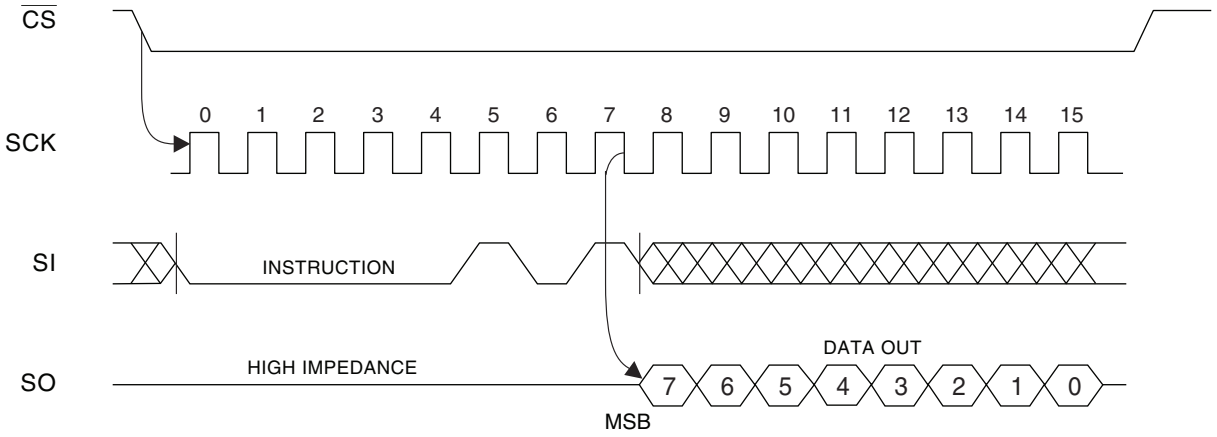


Figure 4-5. WRSR Timing

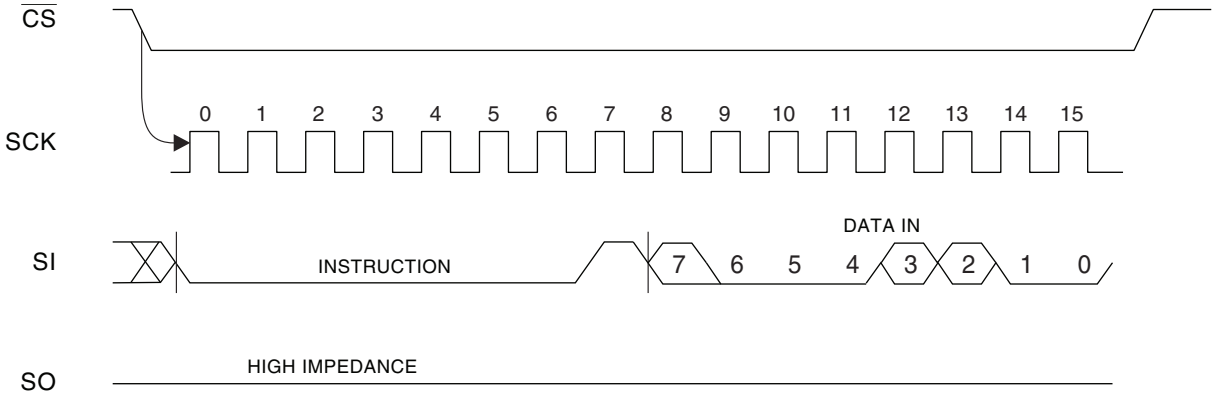


Figure 4-6. READ Timing

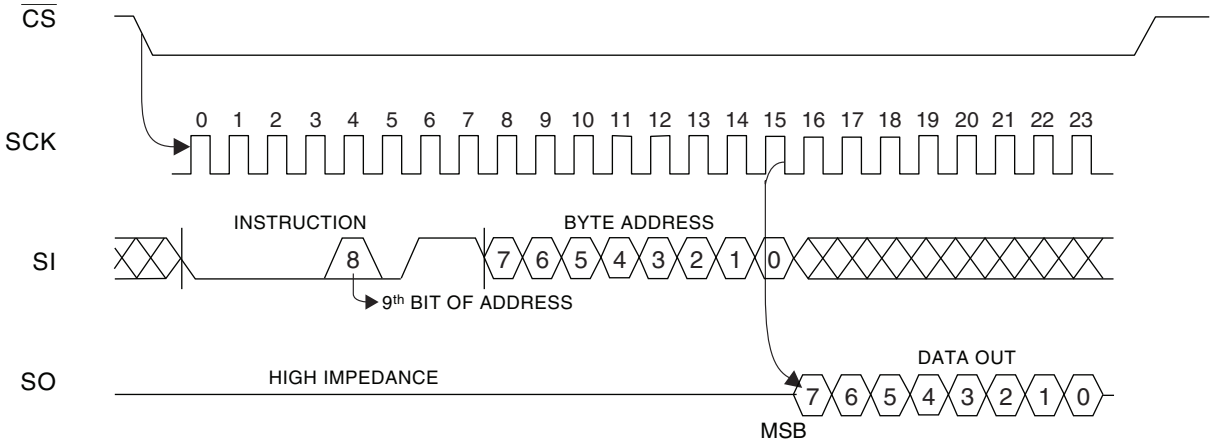


Figure 4-7. WRITE Timing

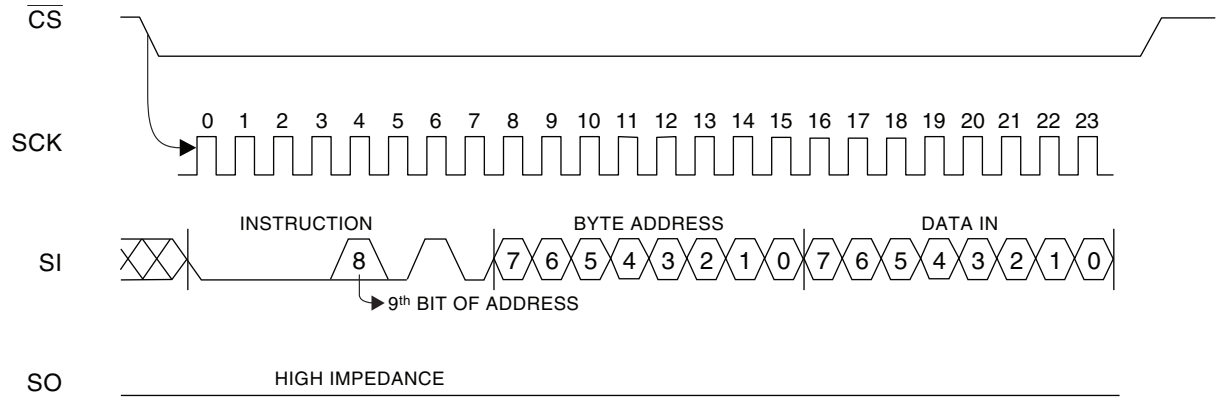
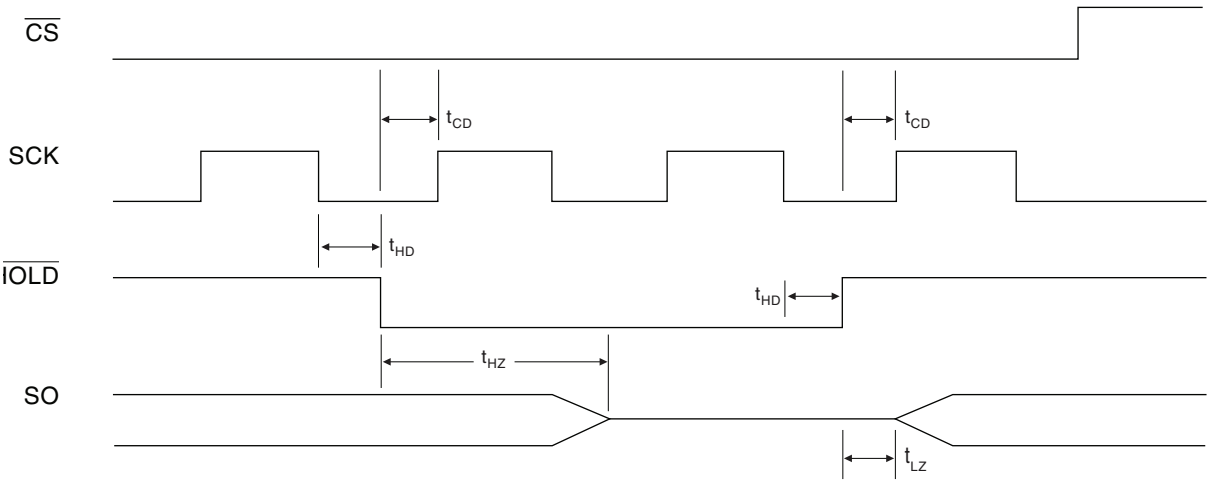
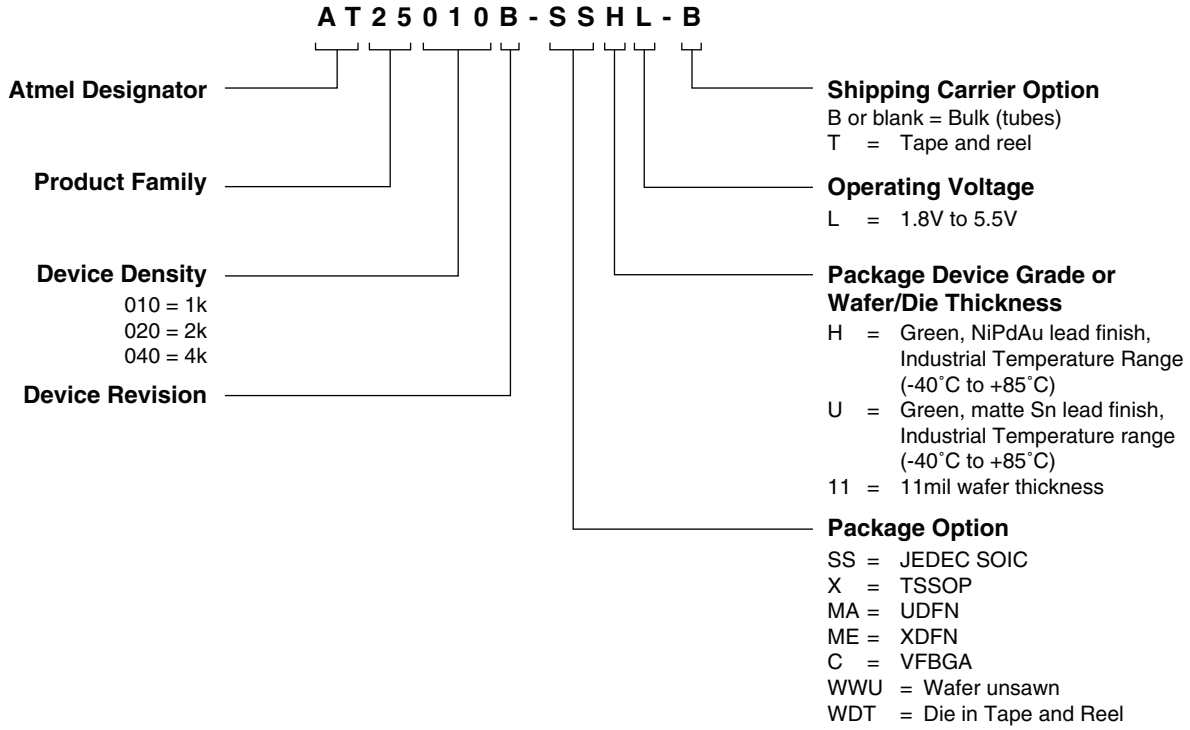


Figure 4-8. $\overline{\text{HOLD}}$ Timing

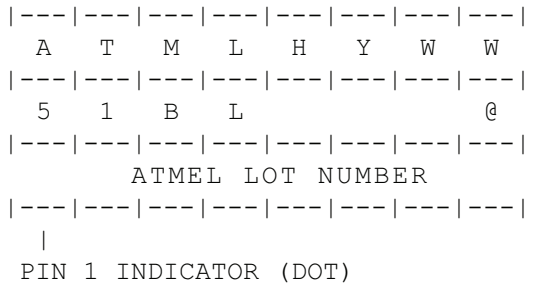


5. Ordering Code Detail



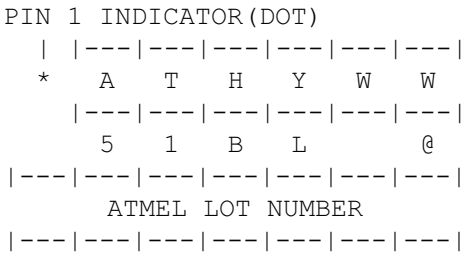
6. Part Markings

AT25010B-SSHL



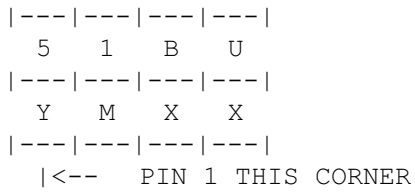
LINE 1: ATML=ATMEL H=MATERIAL SET/GRADE YWW=DATE CODE
LINE 2: 51B=AT25010B, L=1.8 to 5.5v, @=COUNTRY of ORIGIN
LINE 3: ATMEL LOT NUMBER

AT25010B-XHL



LINE 1: AT=ATMEL H=MATERIAL SET/GRADE YWW=DATE CODE
LINE 2: 51B=AT25010B, L=1.8 to 5.5v, @=COUNTRY of ORIGIN
LINE 3: ATMEL LOT NUMBER

AT25010B-CUL



LINE 1: 51B=AT25010B, U=MATERIAL SET/GRADE
LINE 2: YM=DATE CODE, XX=TRACE CODE

AT25010B-MAHL

```
|---|---|---|
  5   1   B
|---|---|---|
  H   L   @
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
PIN 1 INDICATOR (DOT)
```

LINE 1: 51B=AT25010B
LINE 2: H=MATERIAL SET/GRADE, L=1.8 to 5.5V, @=COUNTRY OF ORIGIN
LINE 3: Y=DATE CODE, XX=TRACE CODE

AT25010B-MEHL

```
|---|---|---|
  5   1   B
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
 PIN 1 INDICATOR (DOT)
```

LINE 1: 51B=AT25010B
LINE 2: Y=DATE CODE, XX=TRACE CODE

AT25020B-SSHL

```
|---|---|---|---|---|---|---|---|
  A   T   M   L   H   Y   W   W
|---|---|---|---|---|---|---|---|
  5   2   B       L           @
|---|---|---|---|---|---|---|---|
        ATMEL LOT NUMBER
|---|---|---|---|---|---|---|---|
  |
 PIN 1 INDICATOR (DOT)
```

LINE 1: ATML=ATMEL H=MATERIAL SET/GRADE YWW=DATE CODE
LINE 2: 52B=AT25020B, L=1.8 to 5.5v, @=COUNTRY of ORIGIN
LINE 3: ATMEL LOT NUMBER

AT25020B-XHL

```
PIN 1 INDICATOR (DOT)
  | |---|---|---|---|---|---|
  *   A   T   H   Y   W   W
    |---|---|---|---|---|---|
      5   2   B   L       @
|---|---|---|---|---|---|---|
     ATMEL LOT NUMBER
|---|---|---|---|---|---|---|

LINE 1:  AT=ATMEL H=MATERIAL SET/GRADE YWW=DATE CODE
LINE 2:  52B=AT25020B, L=1.8 to 5.5v, @=COUNTRY of ORIGIN
LINE 3:  ATMEL LOT NUMBER
```

AT25020B-CUL

```
|---|---|---|---|
  5   2   B   U
|---|---|---|---|
  Y   M   X   X
|---|---|---|---|
  |<--   PIN 1 THIS CORNER

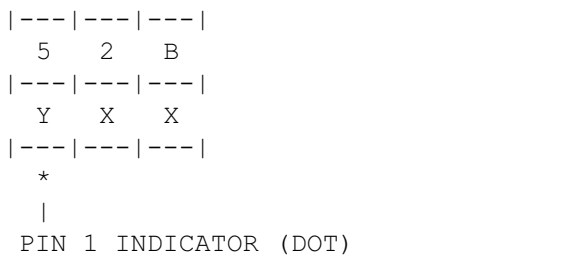
LINE 1:  52B=AT25020B, U=MATERIAL SET/GRADE
LINE 2:  YM=DATE CODE, XX=TRACE CODE
```

AT25020B-MAHL

```
|---|---|---|
  5   2   B
|---|---|---|
  H   L   @
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
 PIN 1 INDICATOR (DOT)

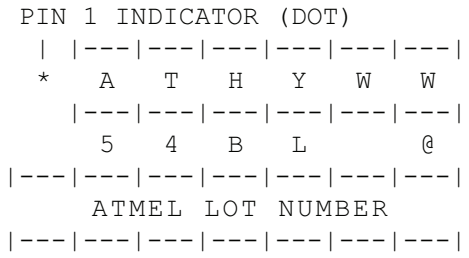
LINE 1:  52B=AT25020B
LINE 2:  H=MATERIAL SET/GRADE, L=1.8 to 5.5V, @=COUNTRY OF ORIGIN
LINE 3:  Y=DATE CODE, XX=TRACE CODE
```

AT25020B-MEHL



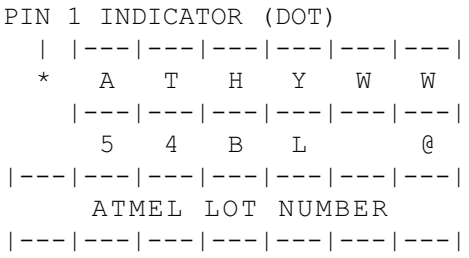
LINE 1: 52B=AT25020B
LINE 2: Y=DATE CODE, XX=TRACE CODE

AT25040B-SSHL



LINE 1: AT=ATMEL H=MATERIAL SET/GRADE YWW=DATE CODE
LINE 2: 54B=AT25040B, L=1.8 to 5.5v, @=COUNTRY of ORIGIN
LINE 3: ATMEL LOT NUMBER

AT25040B-XHL



LINE 1: AT=ATMEL H=MATERIAL SET/GRADE YWW=DATE CODE
LINE 2: 54B=AT25040B, L=1.8 to 5.5v, @=COUNTRY of ORIGIN
LINE 3: ATMEL LOT NUMBER

AT25040B-CUL

```
|---|---|---|---|
  5   4   B   U
|---|---|---|---|
  Y   M   X   X
|---|---|---|---|
  |<--   PIN 1 THIS CORNER

LINE 1:  54B=AT25040B, U=MATERIAL SET/GRADE
LINE 2:  YM=DATE CODE, XX=TRACE CODE
```

AT25040B-MAHL

```
|---|---|---|
  5   4   B
|---|---|---|
  H   L   @
|---|---|---|
  Y   X   X
|---|---|---|
  *
  PIN 1 INDICATOR (DOT)

LINE 1:  54B=AT25040B
LINE 2:  H=MATERIAL SET/GRADE, L=1.8 to 5.5V, @=COUNTRY OF ORIGIN
LINE 2:  Y=DATE CODE, XX=TRACE CODE
```

AT25040B-MEHL

```
|---|---|---|
  5   4   B
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
  PIN 1 INDICATOR (DOT)

LINE 1:  54B=AT25040B
LINE 2:  Y=DATE CODE, XX=TRACE CODE
```

7. Ordering Codes

AT25010B Ordering Information[1]

Ordering Code	Voltage	Package	Operation Range
AT25010B-SSHL-B[1] (NiPdAu Lead Finish)	1.8V to 5.5V	8S1	Lead-free/Halogen-free/ Industrial Temperature (–40 to 85°C)
AT25010B-SSHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8S1	
AT25010B-XHL-B[1] (NiPdAu Lead Finish)	1.8V to 5.5V	8A2	
AT25010B-XHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8A2	
AT25010B-MAHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8MA2	
AT25010B-MEHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8ME1	
AT25010B-CUL-T[2] (SnAgCu Ball Finish)	1.8V to 5.5V	8U3-1	
AT25010B-WWU11L[3]	1.8V to 5.5V	Die Sale	Industrial Temperature (–40 to 85°C)

Note: 1. Bulk delivery in tubes (SOIC and TSSOP 100/tube).
2. Tape and reel delivery (SOIC 4k/reel. TSSOP, UDFN, XDFN and VFBGA 5k/reel).
3. Contact Atmel Sales for Wafer sales.

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8MA2	8-lead, 2.00mm x 3.00mm Body, 0.50 mm Pitch, Dual No Lead Package (UDFN)
8ME1	8-lead (1.80x2.20mm body) Extra Thin DFN (XDFN)
8U3-1	8-ball die Ball Grid Array (VFBGA)

AT25020B Ordering Information[1]

Ordering Code	Voltage	Package	Operation Range
AT25020B-SSHL-B[1] (NiPdAu Lead Finish)	1.8V to 5.5V	8S1	Lead-free/Halogen-free/ Industrial Temperature (–40 to 85°C)
AT25020B-SSHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8S1	
AT25020B-XHL-B[1] (NiPdAu Lead Finish)	1.8V to 5.5V	8A2	
AT25020B-XHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8A2	
AT25020B-MAHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8MA2	
AT25020B-MEHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8ME1	
AT25020B-CUL-T[2] (SnAgCu Ball Finish)	1.8V to 5.5V	8U3-1	
AT25020B-WWU11L[3]	1.8V to 5.5V	Die Sale	Industrial Temperature (–40 to 85°C)

Note: 1. Bulk delivery in tubes (SOIC and TSSOP 100/tube).
2. Tape and reel delivery (SOIC 4k/reel. TSSOP, UDFN, XDFN and VFBGA 5k/reel).
3. Contact Atmel Sales for Wafer sales.

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8MA2	8-lead, 2.00mm x 3.00mm Body, 0.50 mm Pitch, Dual No Lead Package (UDFN)
8ME1	8-lead (1.80x2.20mm body) Extra Thin DFN (XDFN)
8U3-1	8-ball die Ball Grid Array (VFBGA)

AT25040B Ordering Information

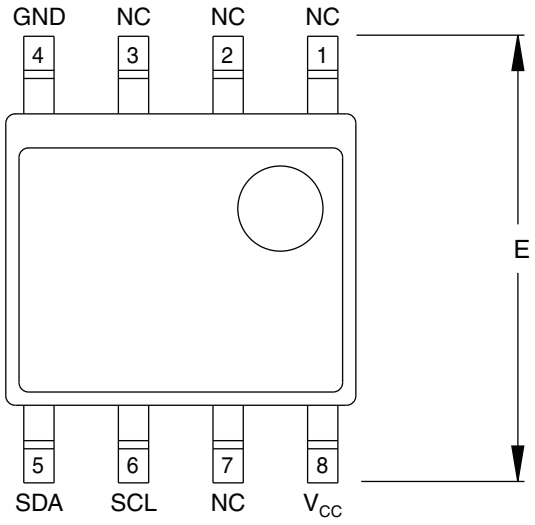
Ordering Code	Voltage	Package	Operation Range
AT25040B-SSHL-B[1] (NiPdAu Lead Finish)	1.8V to 5.5V	8S1	Lead-free/Halogen-free/ Industrial Temperature (–40 to 85°C)
AT25040B-SSHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8S1	
AT25040B-XHL-B[1] (NiPdAu Lead Finish)	1.8V to 5.5V	8A2	
AT25040B-XHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8A2	
AT25040B-MAHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8MA2	
AT25040B-MEHL-T[2] (NiPdAu Lead Finish)	1.8V to 5.5V	8ME1	
AT25040B-CUL-T[2] (SnAgCu Ball Finish)	1.8V to 5.5V	8U3-1	
AT25040B-WWU11L[3]	1.8V to 5.5V	Die Sale	Industrial Temperature (–40 to 85°C)

Note: 1. Bulk delivery in tubes (SOIC and TSSOP 100/tube).
2. Tape and reel delivery (SOIC 4k/reel. TSSOP, UDFN, XDFN and VFBGA 5k/reel).
3. Contact Atmel Sales for Wafer sales.

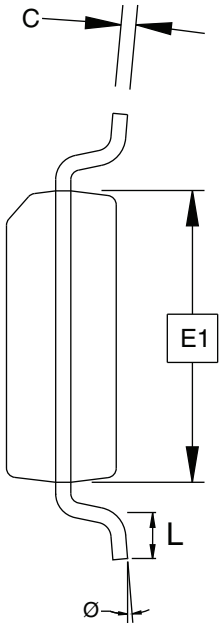
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8MA2	8-lead, 2.00mm x 3.00mm Body, 0.50 mm Pitch, Dual No Lead Package (UDFN)
8ME1	8-lead, 1.80mm x 2.20mm Body, Extra Thin DFN (XDFN)
8U3-1	8-ball die Ball Grid Array (VFBGA)

8. Packaging Information

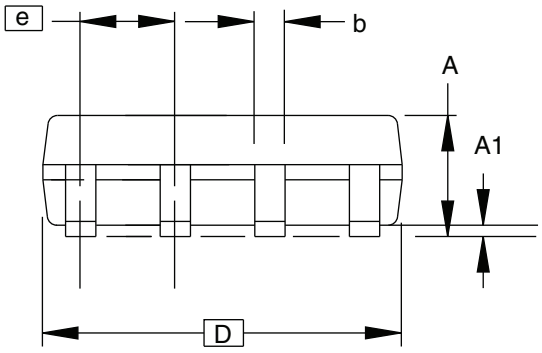
8S1 – JEDEC SOIC



Top View



End View



Side View

Notes: 1. These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

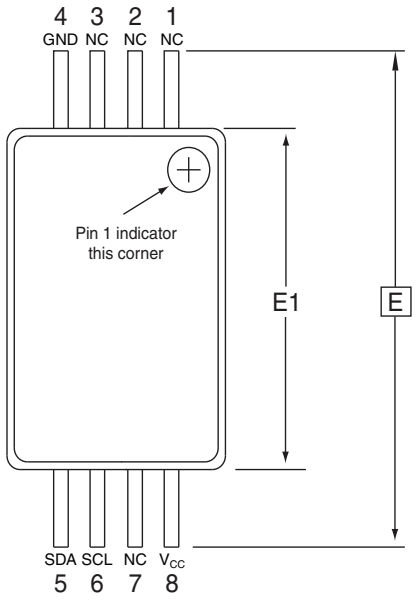
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

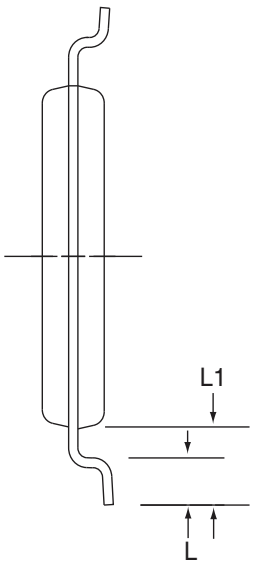
12/11/09

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8S1,** 8-lead, (0.150" Wide Body), Plastic Gull Wing Outline (JEDEC SOIC)	SWB	8S1	E

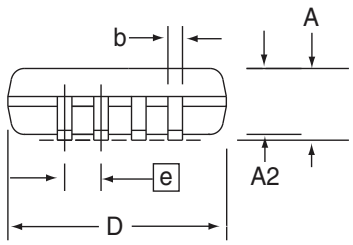
8A2 – TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

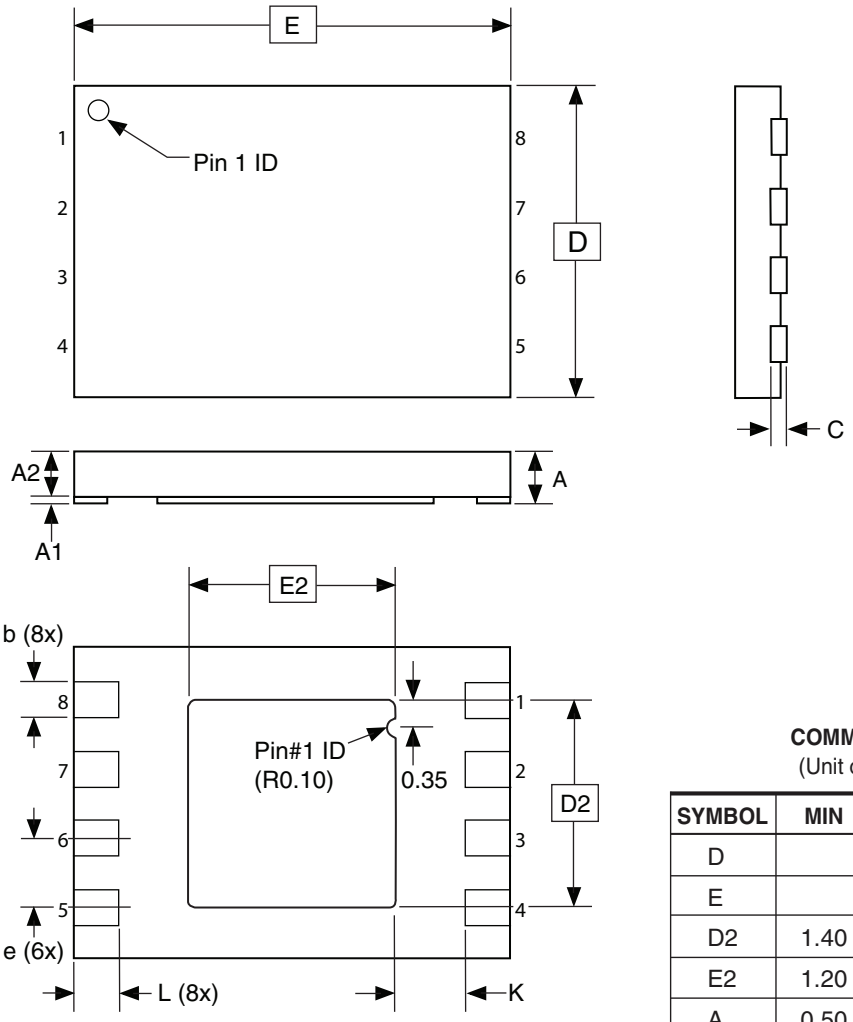
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	13.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 RE3		

12/11/09

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8A2,** 8-lead, 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8A2	D

8MA2 – UDFN



Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229 for proper dimensions, tolerances, datums, etc.
2. The terminal #1 ID is a laser-marked feature.
3. Dimensions b applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

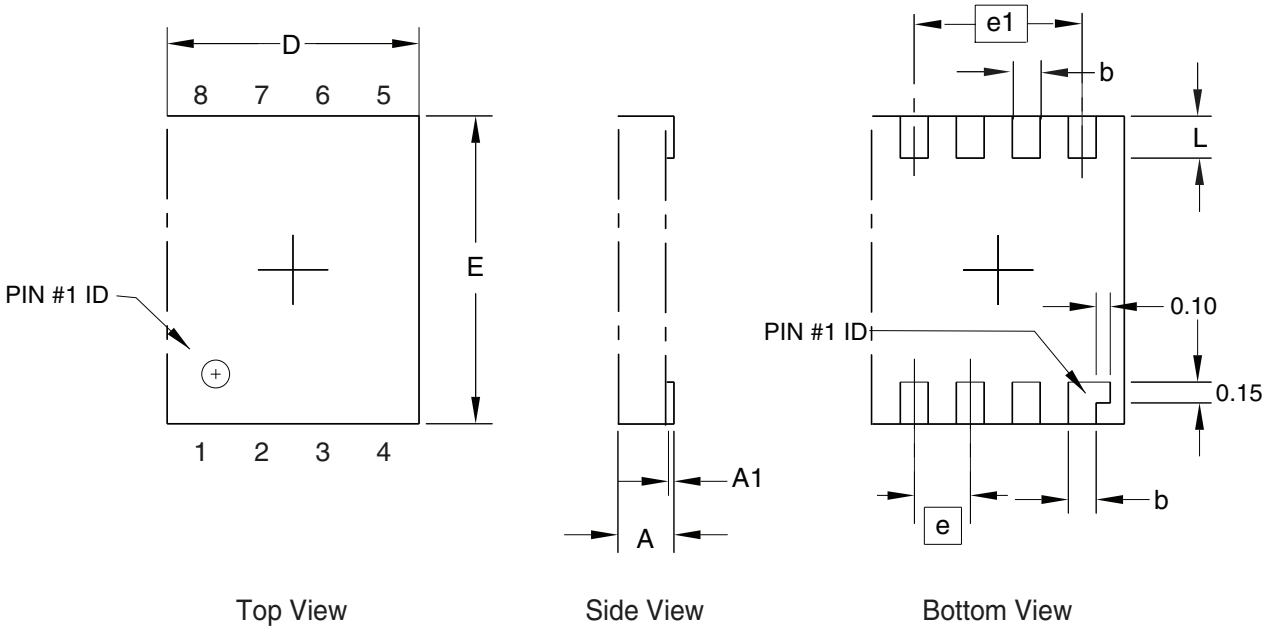
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	1.20	1.30	1.40	
A	0.50	0.55	0.60	
A1	0.00	0.02	0.05	
A2	–	–	0.55	
C		0.152 REF		
L	0.30	0.35	0.40	
e		0.50 BSC		
b	0.18	0.25	0.30	3
K	0.20	–	–	

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8MA2**, 8-pad, 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YNZ	8MA2	A

8ME1 – XDFN



Top View Side View Bottom View

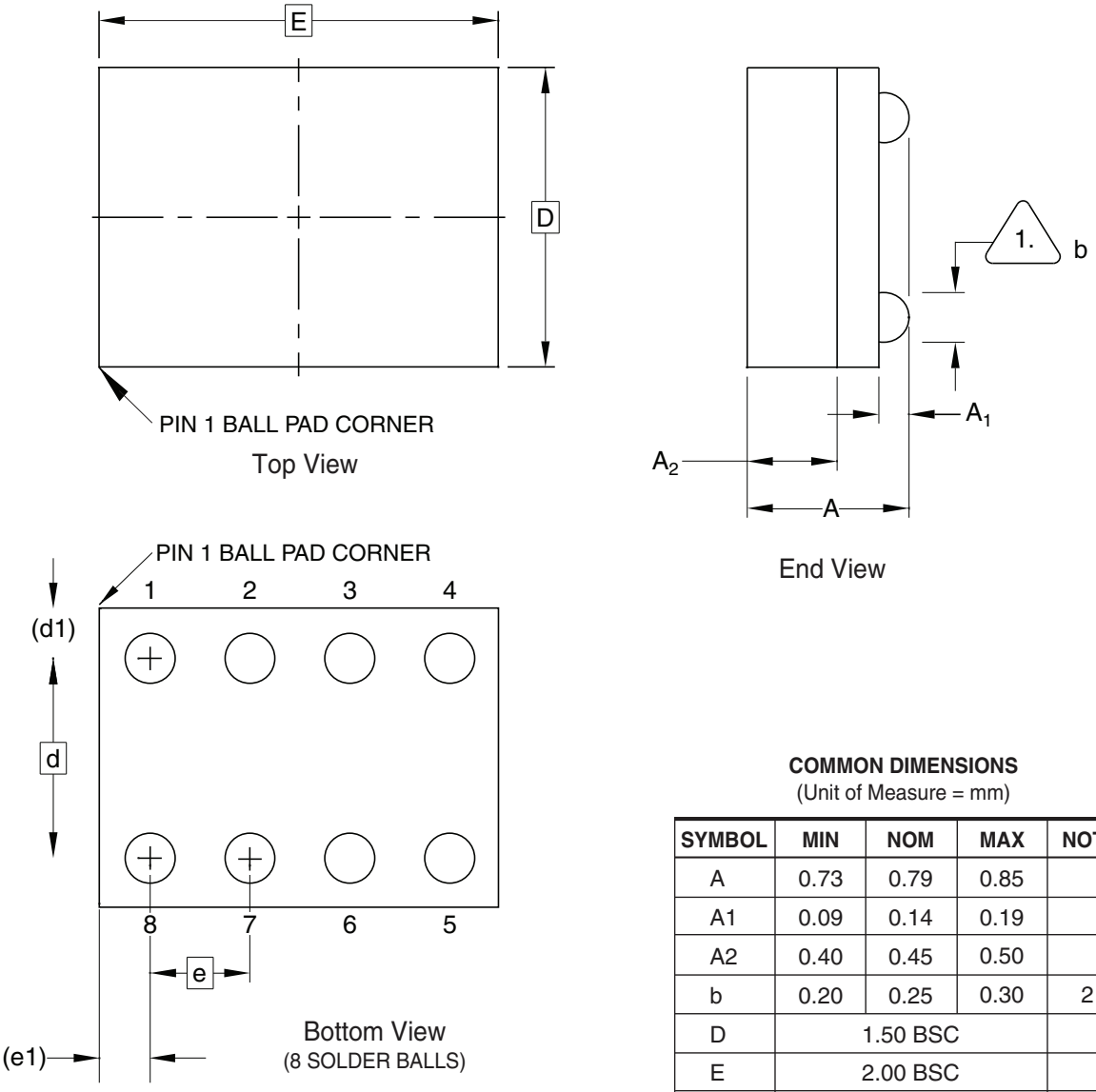
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e	0.40 TYP			
e1	1.20 REF			
L	0.26	0.30	0.35	

8/3/09

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8ME1,** 8-lead (1.80 x 2.20 mm Body) Extra Thin DFN (XDFN)	DTP	8ME1	A

8U3-1 – VFBGA



Notes:
1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.00 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

9/19/07

Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **8U3-1,** 8-ball, 1.50 x 2.00 mm Body, 0.50 mm pitch, VFBGA Package (dBGA2)	**DRAWING NO.** PO8U3-1	**REV.** C

9. Revision History

Doc. Rev.	Date	Comments
8707B	10/2010	Remove Preliminary
8707B	3/2010	Replace 8Y6 with 8MA2
8707A	2/2010	Initial document release

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