ASM3P2274A

4x Multiplier EMI Reduction IC

ON Semiconductor®

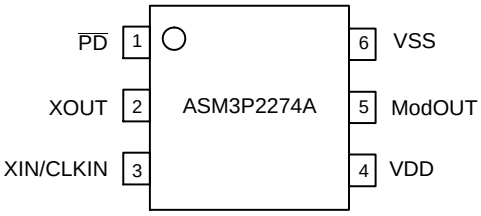
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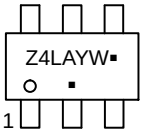
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TSOP−6
CASE 318G

PIN CONNECTION



MARKING DIAGRAM



Z4L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

Product Description

The ASM3P2274 is a versatile Spread Spectrum Frequency Modulator designed specifically for a wide range of clock frequencies. It provides a 4x Spread Spectrum Modulated output from an input clock source.

The ASM3P2274A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The ASM3P2274A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding that are traditionally required to pass EMI regulations.

The ASM3P2274A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

The ASM3P2274A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation.’

Features

- Generates a 4x EMI Optimized Clock Signal at the Output
- Integrated Loop Filter Components
- Operates with a 2.5/3.3 V Supply
- CMOS Design
- Input Frequency Range:
  - 12 MHz to 30 MHz for 2.5 V
  - 12 MHz to 30 MHz for 3.3 V
- Frequency Deviation: −1.5% (Typ) @ 66 MHz Output Frequency
- Available in TSOP−6 Package
- This Device is Pb-Free and is RoHS Compliant

Applications

The ASM3P2274A is targeted towards all portable devices like MP3 players, MFP, LCD Panel Module and digital still cameras.

Table 1. KEY SPECIFICATIONS

Description	Specification
Supply Voltages	V_{DD} = 2.5/3.3 V
Cycle-to-Cycle Jitter	±360 ps (Typ)
Output Duty Cycle	45/55%
Modulation Rate Equation	F_{IN}/640
Frequency Deviation	−1.5% (Typ) @ 66 MHz Output

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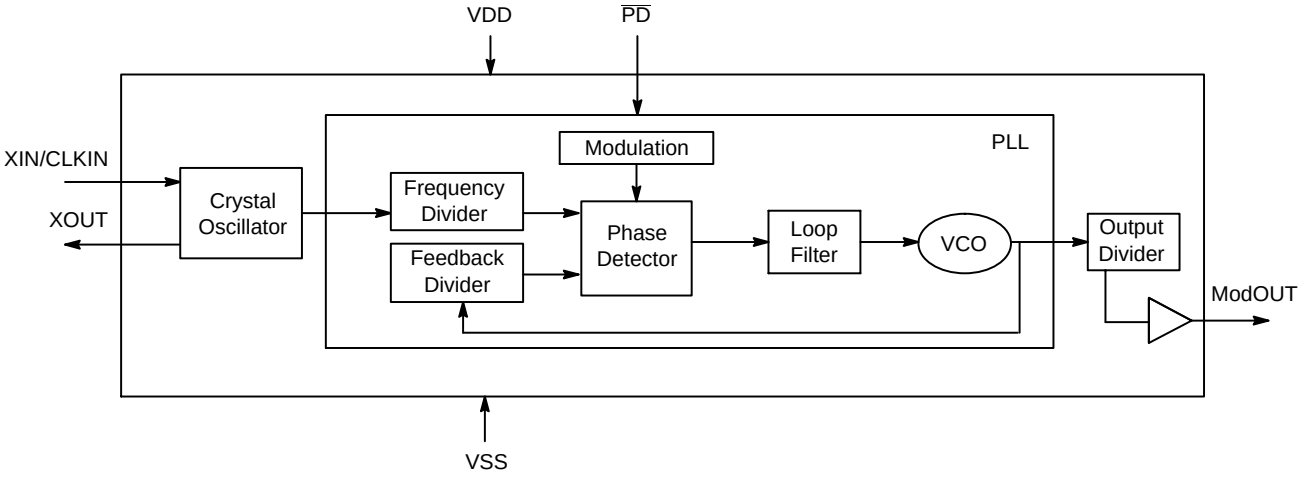


Figure 1. Block Diagram

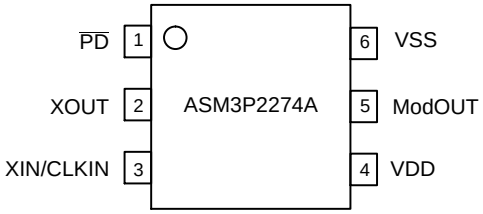


Figure 2. Pin Configuration

Table 2. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	$\overline{PD}$	I	Power-Down Control Pin. Pull Low to Enable Power-Down Mode. Connect to VDD if Not Used
2	XOUT	O	Crystal Connection. If Using an External Reference, this Pin Must be Left Unconnected
3	XIN/CLKIN	I	Crystal Connection or External Reference Frequency Input. This Pin has Dual Functions. It can be Connected either to an External Crystal or an External Reference Clock
4	VDD	P	Power Supply for the Entire Chip
5	ModOUT	O	Spread Spectrum Clock Output (4x Output)
6	VSS	P	Ground Connection

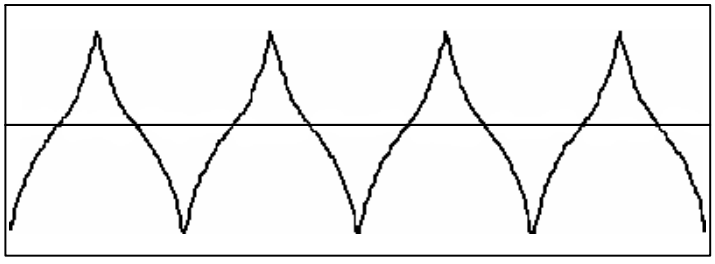


Figure 3. Modulation Profile

Table 3. SPECIFICATIONS

Description	Specification
Input Frequency Range for 2.5 V Supply for 3.3 V Supply	 12 MHz < CLKIN < 30 MHz 12 MHz < CLKIN < 30 MHz
Modulation Equation	$F_{IN}/640$
Frequency Deviation	−1.5% (Typ) @ 66 MHz Output

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any Pin with Respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage Temperature	−65 to +125	°C
T_S	Maximum Soldering Temperature (10 s)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (as per JEDEC STD22−A114−B)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	2.375	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance	−	15	pF
C_{IN}	Input Capacitance	−	7	pF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. DC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	V_{SS} − 0.3	−	0.8	V
V_{IH}	Input High Voltage	2.0	−	V_{DD} + 0.3	V
I_{IL}	Input Low Current	−	−	−35	μA
I_{IH}	Input High Current	−	−	35	μA
I_{XOL}	X_{OUT} Output Low Current (@ 0.5 V, V_{DD} = 2.5 V)	−	3	−	mA
I_{XOH}	X_{OUT} Output High Current (@ 1.8 V, V_{DD} = 2.5 V)	−	3	−	mA
V_{OL}	Output Low Voltage (V_{DD} = 2.5 V, I_{OL} = 8 mA)	−	−	0.6	V
V_{OH}	Output High Voltage (V_{DD} = 2.5 V, I_{OH} = 8 mA)	1.8	−	−	V
I_{DD}	Static Supply Current (Note 1)	−	−	2	μA
I_{CC}	Dynamic Supply Current (2.5 V, 66 MHz and No Load)		3.0		mA
V_{DD}	Operating Voltage	2.375	2.5	2.625	V
t_{ON}	Power-Up Time (First Locked Cycle after Power-Up) (Note 2)	−	−	5	ms
Z_{OUT}	Output Impedance	−	50	−	Ω

1. XIN/CLKIN pin and $\overline{PD}$ pin are pulled low.
2. VDD and XIN/CLKIN input are stable, $\overline{PD}$ pin is made high from low.

Table 7. AC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input Frequency	12	−	30	MHz
ModOUT	Output Frequency	48	−	120	MHz
f_D	Frequency Deviation Output Frequency = 48 MHz Output Frequency = 120 MHz	 − −	 −1.6 −1.4	 − −	%
t_{LH}*	Output Rise Time (Measured at 0.7 V to 1.7 V)	0.5	2.0	2.3	ns
t_{HL}*	Output Fall Time (Measured at 1.7 V to 0.7 V)	0.4	1.0	1.2	ns
t_{JC}	Jitter (Cycle-to-Cycle)	−	±360	−	ps
t_D	Output Duty Cycle	40	50	60	%

* t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

Table 8. DC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	V_{SS} − 0.3	−	0.8	V
V_{IH}	Input High Voltage	2.0	−	V_{DD} + 0.3	V
I_{IL}	Input Low Current	−	−	−35	μA
I_{IH}	Input High Current	−	−	35	μA
I_{XOL}	X_{OUT} Output Low Current (@ 0.4 V, V_{DD} = 3.3 V)	−	3	−	mA
I_{XOH}	X_{OUT} Output High Current (@ 2.5 V, V_{DD} = 3.3 V)	−	3	−	mA
V_{OL}	Output Low Voltage (V_{DD} = 3.3 V, I_{OL} = 8 mA)	−	−	0.4	V
V_{OH}	Output High Voltage (V_{DD} = 3.3 V, I_{OH} = 8 mA)	2.5	−	−	V
I_{DD}	Static Supply Current (Note 1)	−	−	2	μA
I_{CC}	Dynamic Supply Current (3.3 V, 66 MHz and No Load)		4.0		mA
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
t_{ON}	Power-Up Time (First Locked Cycle after Power-Up) (Note 2)	−	−	5	ms
Z_{OUT}	Output Impedance	−	45	−	Ω

1. XIN/CLKIN pin and $\overline{PD}$ pin are pulled low.
2. VDD and XIN/CLKIN input are stable, $\overline{PD}$ pin is made high from low.

Table 9. AC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

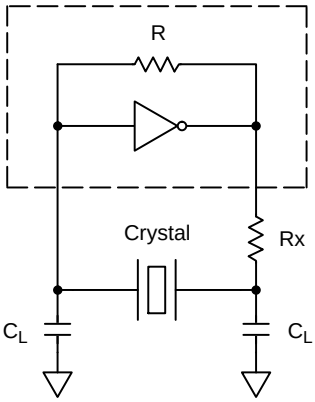
Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input Frequency	12	−	30	MHz
ModOUT	Output Frequency	48	−	120	MHz
f_D	Frequency Deviation Output Frequency = 48 MHz Output Frequency = 120 MHz	 − −	 −1.6 −1.4	 − −	%
t_{LH}*	Output Rise Time (Measured at 0.8 V to 2.0 V)	0.4	1.3	1.6	ns
t_{HL}*	Output Fall Time (Measured at 2.0 V to 0.8 V)	0.4	0.8	1.1	ns
t_{JC}	Jitter (Cycle-to-Cycle)	−	±360	−	ps
t_D	Output Duty Cycle	40	50	60	%

* t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

Table 10. TYPICAL CRYSTAL SPECIFICATIONS

Fundamental AT Cut Parallel Resonant Crystal	Rating
Nominal Frequency	14.31818 MHz
Frequency Tolerance	±50 ppm or Better at 25°C
Operating Temperature Range	−25 to +85°C
Storage Temperature	−40 to +85°C
Load Capacitance (C_P)	18 pF
Shunt Capacitance	7 pF Maximum
ESR	25 Ω

NOTE: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.



$C_L = 2 \cdot (C_P - C_S)$
Where: C_L = Load Capacitance of Crystal
C_S = Stray Capacitance due to C_{IN}, PCB, Trace, etc.

Figure 4. Typical Crystal Interface Circuit

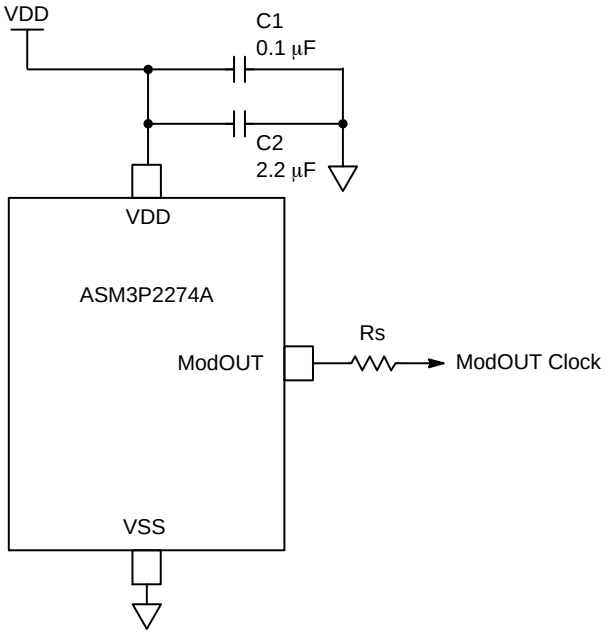


Figure 5. Typical Application Schematic

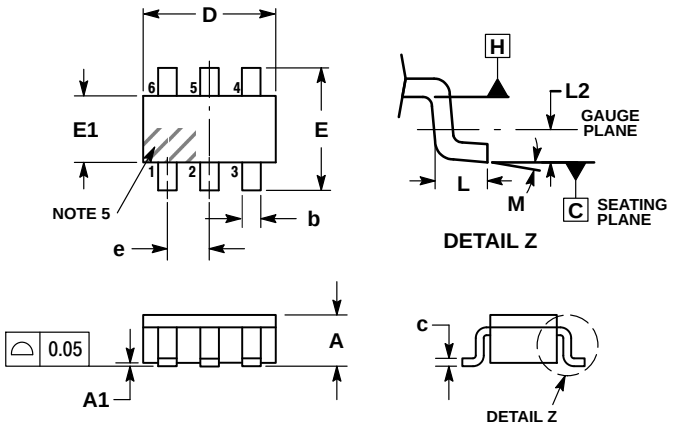
Table 11. ORDERING INFORMATION

Part Number	Marking	Package	Temperature	Shipping†
ASM3P2274AF-06OR	Z4L	TSOP−6 (Pb-Free)	0 to 70°C	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

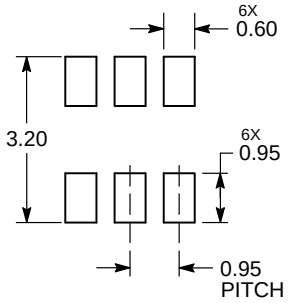
TSOP−6
CASE 318G−02
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2		0.25 BSC	
M	0°	–	10°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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