LCD Panel EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 15dB EMI reduction.
- Generates a 1X low EMI spread spectrum clock of the input frequency.
- Input frequency range: 25MHz to 210MHz.
- Internal loop filter minimizes external components and board space.
- Center spread.
- 4 spread frequency deviation selections: ± 0.13% to ± 1.24%.
- Low inherent Cycle-to-cycle jitter.
- 3.3V Operating Voltage.
- TTL or CMOS compatible inputs and outputs.
- Low power CMOS design.
- Supports notebook VGA and other LCD timing controller applications.
- Products are available for Industrial temperature range.
- Available in 8-pin SOIC and TSSOP Packages.

Product Description

The ASM3P2182A is a versatile spread spectrum frequency modulator designed specifically for a wide range of input clock frequencies from 25MHz to 210MHz. *(Refer Input Frequency and Modulation Rate Table)*. The ASM3P2182A can generate an EMI reduced clock from an OSC or a system generated clock. The ASM3P2182A offers a Center Spread clock and with a percentage deviation from ± 0.13% or ± 1.24%.

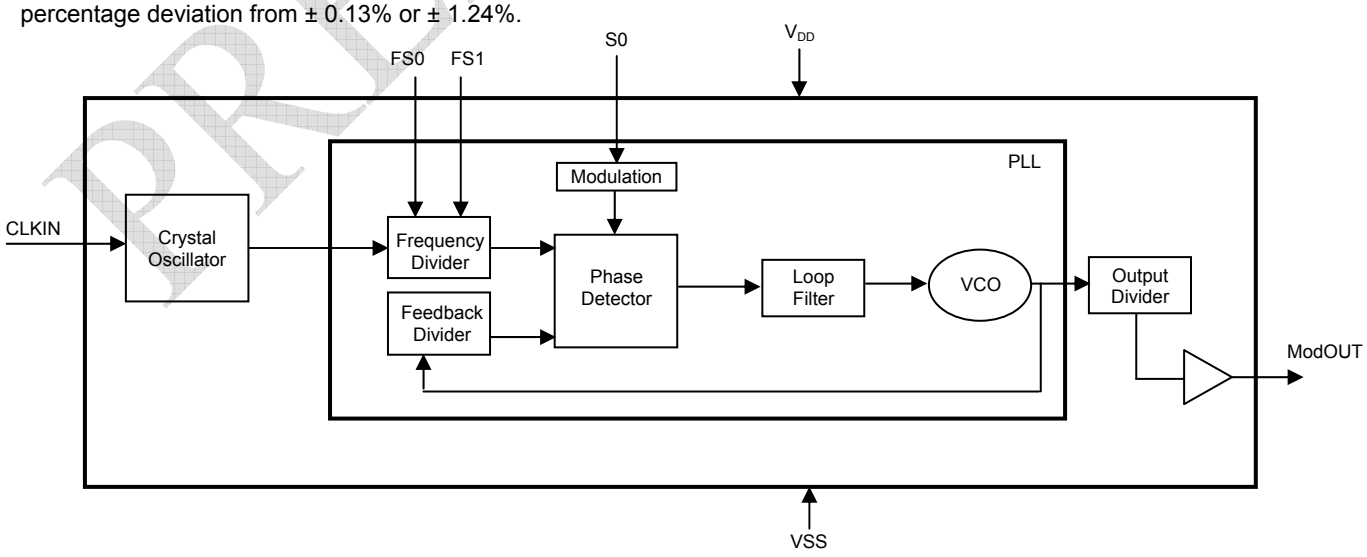
The ASM3P2182A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The ASM3P2182A allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The ASM3P2182A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The ASM3P2182A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

Applications

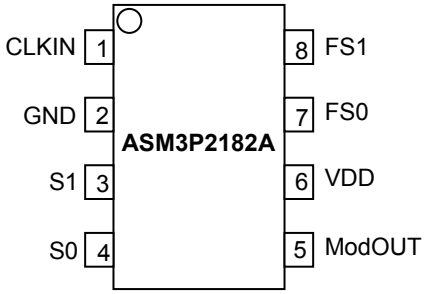
The ASM3P2182A is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high-speed digital applications such as PC peripheral devices, consumer electronics, and embedded controller systems.



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Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN	I	Connect to externally generated clock signal.
2	GND	P	Ground to entire chip.
3	S1	I	Spread range select. Digital logic input used to select frequency deviation (Refer *Spread Deviation Table*). This pin has an internal pull-up resistor.
4	S0	I	Spread range select. Digital logic input used to select frequency deviation (Refer *Spread Deviation Table*). This pin has an internal pull-up resistor.
5	ModOUT	O	Spread spectrum low EMI output.
6	VDD	P	Power supply for the entire chip (3.3V).
7	FS0	I	Frequency range select. Digital logic input used to select frequency range (*Refer Input Frequency and Modulation Rate Table*). This pin has an internal pull-up resistor.
8	FS1	I	Frequency range select. Digital logic input used to select frequency range (*Refer Input Frequency and Modulation Rate Table*). This pin has an internal pull-up resistor.

Input Frequency and Modulation Rate table

FS1 (pin 8)	FS0 (pin 7)	Frequency Range
0	0	25MHz to 50MHz
0	1	50MHz to 103MHz
1	0	75MHz to 150MHz
1	1	160MHz to 210MHz

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Spread Deviation Selection table

S1	S0	Spreading Range (± %)								
		25 MHz	40 MHz	65 MHz	81* MHz	81** MHz	108 MHz	120 MHz	162 MHz	200 MHz
0	0	0.28	0.19	0.15	0.12	0.18	0.15	0.1	0.1	0.06
0	1	0.8	0.3	0.3	0.2	0.5	0.3	0.19	0.3	0.1
1	0	1.2	0.54	0.45	0.4	0.8	0.6	0.36	1.0	0.6
1	1	2.1	1.0	1.1	0.9	1.4	1.1	0.75	1.9	1.2

*Frequency Range- 50MHz to 103MHz
** Frequency Range- 75MHz to 150MHz

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage pin with respect to Ground	-0.5 to +4.6	V
V_{IN}	Input Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V
V_{OUT}	Output Voltage pin with respect to Ground	VSS-0.5 to VDD+0.5	V
T_{STG}	Storage temperature	-55 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage(As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VDD	Operating Voltage	2.7	3.3	3.7	V
T_A	Operating Temperature (Ambient Temperature)	0		+70	°C
C_L	Load Capacitance			15	pF
C_{IN}	Input Capacitance		5		pF

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DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND – 0.3		0.8	V
V_{IH}	Input high voltage	2.0		V_{DD} + 0.3	V
I_{IL}	Input low current			-35	µA
I_{IH}	Input high current			35	µA
V_{OL}	Output low voltage (V_{DD} = 3.3V, I_{OL} = 20mA)			0.4	V
V_{OH}	Output high voltage (V_{DD} = 3.3V, I_{OH} = 20mA)	2.5			V
I_{CC}	Dynamic supply current Normal mode (3.3V and 10pF loading)	8.46	12	17.78	mA
I_{DD}	Static supply current Standby mode*		0.6		mA
V_{DD}	Operating voltage	2.7	3.3	3.7	V
t_{ON}	Power up time (first locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock out impedance		50		Ω

* CLKIN pin is pulled low

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input frequency	25		210	MHz
ModOUT	Output frequency	25		210	MHz
t_{LH}*	Output rise time (measured at 0.8V to 2.0V)	1.2	1.32	1.4	nS
t_{HL}*	Output fall time (measured at 2.0V to 0.8V)	0.8	0.9	1.0	nS
t_{JC}	Jitter (cycle to cycle)			360	pS
T_D	Output duty cycle	45	50	55	%

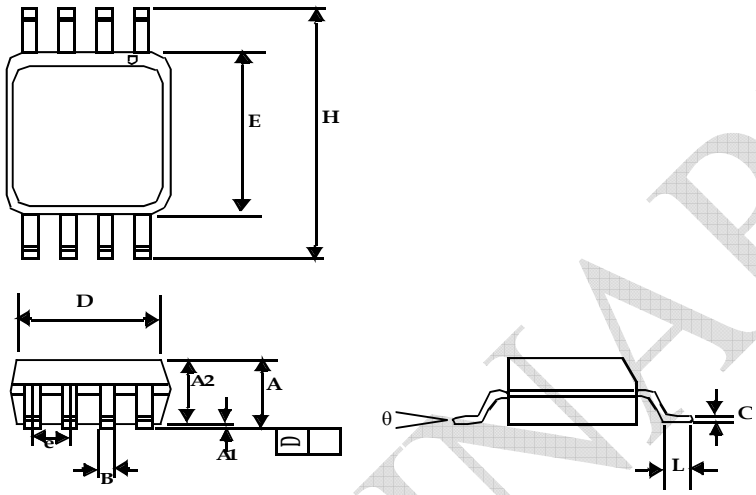
*t_{LH} and t_{HL} are measured into a capacitive load of 15pF

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Package Information

8-lead (150-mil) SOIC Package

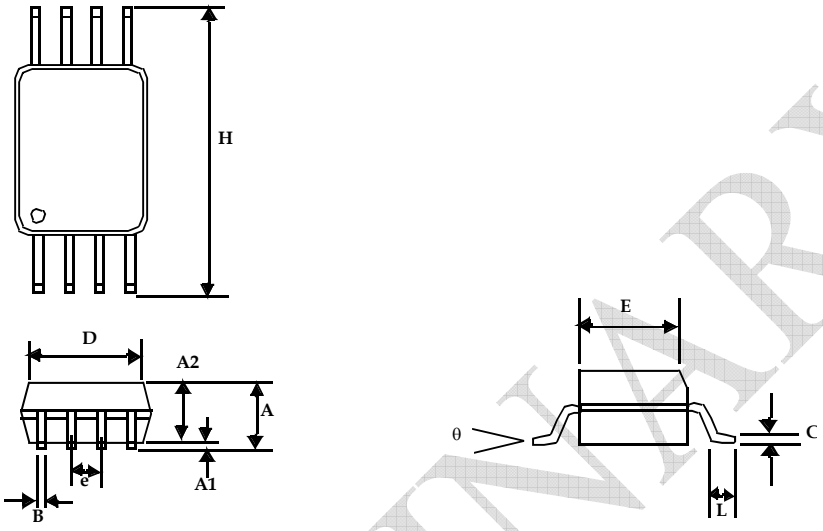


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

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8-lead Thin Shrunk Small Outline Package (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

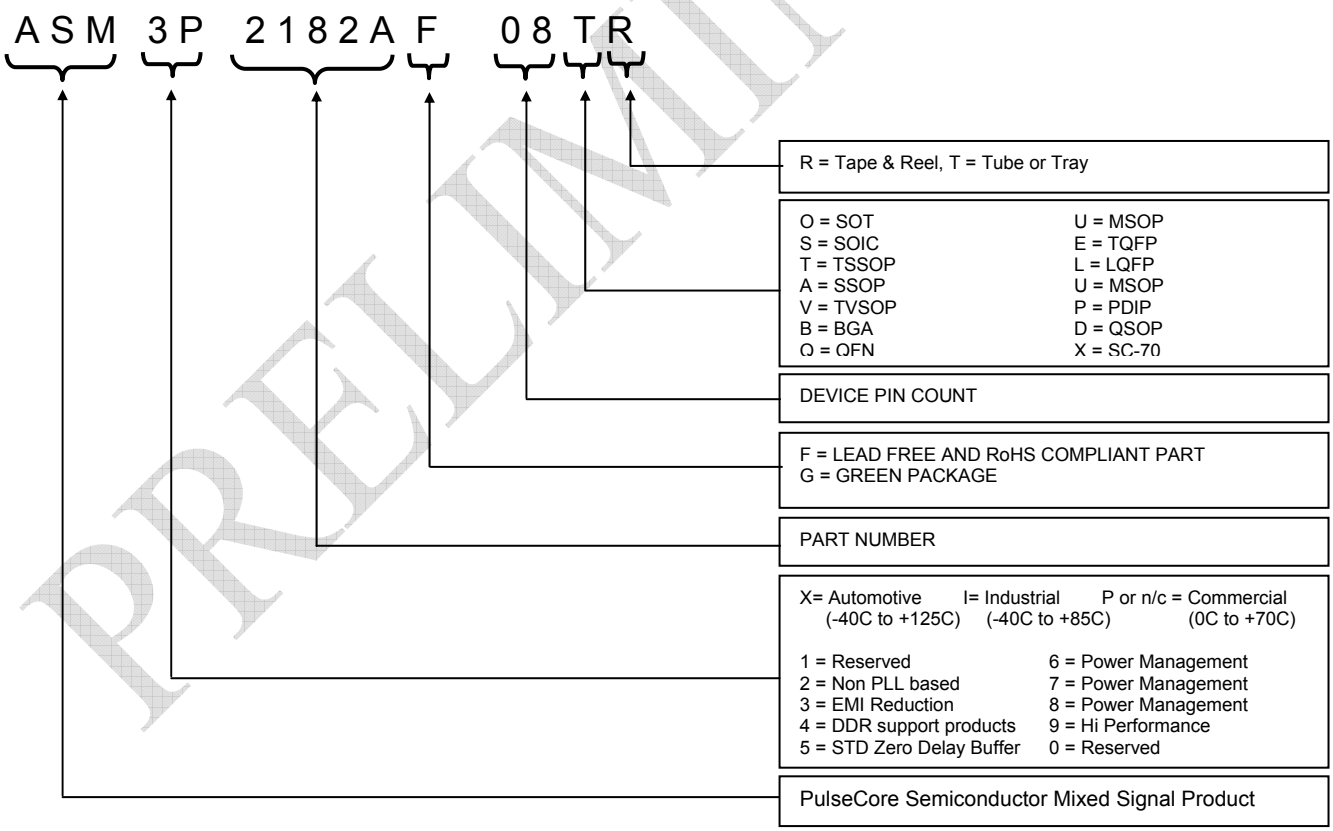
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Ordering Information

Part Number	Marking	Package	Temperature
ASM3P2182AF-08TT	3P2182AF	8-Pin TSSOP, TUBE, Pb Free	Commercial
ASM3P2182AF-08TR	3P2182AF	8-Pin TSSOP, TAPE & REEL, Pb Free	Commercial
ASM3P2182AF-08ST	3P2182AF	8-Pin SOIC, TUBE, Pb Free	Commercial
ASM3P2182AF-08SR	3P2182AF	8-Pin SOIC, TAPE & REEL, Pb Free	Commercial
ASM3P2182A-08TT	3P2182A	8-Pin TSSOP, TUBE	Commercial
ASM3P2182A-08TR	3P2182A	8-Pin TSSOP, TAPE & REEL	Commercial
ASM3P2182A-08ST	3P2182A	8-Pin SOIC, TUBE	Commercial
ASM3P2182A-08SR	3P2182A	8-Pin SOIC, TAPE & REEL	Commercial
ASM3P2182AG-08TT	3P2182AG	8-Pin TSSOP, TUBE, Green	Commercial
ASM3P2182AG-08TR	3P2182AG	8-Pin TSSOP, TAPE & REEL, Green	Commercial
ASM3P2182AG-08ST	3P2182AG	8-Pin SOIC, TUBE, Green	Commercial
ASM3P2182AG-08SR	3P2182AG	8-Pin SOIC, TAPE & REEL, Green	Commercial

Device Ordering Information



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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