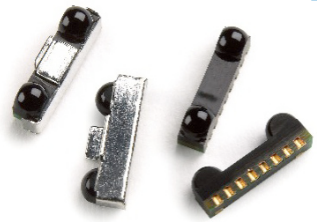
# ASDL-3023

IrDA® Data Compliant Low Power 4Mbit/s with Remote Control Infrared Transceiver

## Data Sheet



### Description

The ASDL-3023 is a new generation low profile high speed enhanced infrared (IR) transceiver module that provides the capability of (1) interface between logic and IR signals for through-air, serial, half-duplex IR data link, and (2) IR remote control transmission for universal remote control applications. The ASDL-3023 can be used for IrDA as well as remote control application without the need of any additional external components for multiplexing.

The ASDL-3023 is fully compliant to IrDA® Physical Layer specification version 1.4 low power from 9.6 kbit/s to 4.0 Mbit/s (FIR) and IEC825 Class 1 eye safety standards.

The ASDL-3023 can be shutdown completely to achieve very low power consumption. In the shutdown mode, the PIN diode will be inactive and thus producing very little photocurrent even under very bright ambient light. It is also designed to interface to input/output logic circuits as low as 1.5V. These features are ideal for battery operated mobile devices such as PDAs and mobile phones that require low power consumption.

### Applications

Mobile data communication and universal remote control

- Mobile Phones
- PDAs
- Digital Still Camera
- Printer
- Handy Terminal
- Industrial and Medical Instrument

### Application Support Information

The Application Engineering Group is available to assist you with the application design associated with ASDL-3023 infrared transceiver module. You can contact them through your local sales representatives for additional details.

### Features

#### General Features

- Operating temperature from -25° C ~ 85°C
  - Critical parameters are guaranteed over temperature and supply voltage
- Vcc Supply 2.4 to 3.6 V
- Interface to Various Super I/O and Controller Devices - Input/Output Interface Voltage of 1.5 V
- Miniature Package (Miniature Package (shielded))
  Height : 1.75 mm (Height : 1.95 mm)
  Width : 7.5 mm (Width : 8.0 mm)
  Depth : 2.75 mm (Depth : 3.00 mm)
- Moisture Level 3
- Power Saving using 3 ILED range (SIR, MIR/FIR, RC mode)
- LED stuck high protection
- High EMI Performance
- High ESD Performance
- Designed to Accommodate Light Loss with Cosmetic Windows
- IEC 825-Class 1 Eye Safe

#### IrDA® Features

- Fully Compliant to IrDA 1.4 Physical Layer Low Power Specifications from 9.6 kbit/s to 4.0 Mb/s
  - Link distance up to 30cm (minimum)
- Complete shutdown
- Low Power Consumption
  - Low shutdown current
  - Low idle current

#### Remote Control Features

- Wide angle and high radiant intensity
- Spectrally suited to remote control transmission function
- Minimum peak wavelength of 880nm
- 2 RC Transmission Mode
  - Single TXD (Programmable Mode)
  - Dual TXD (Direct)

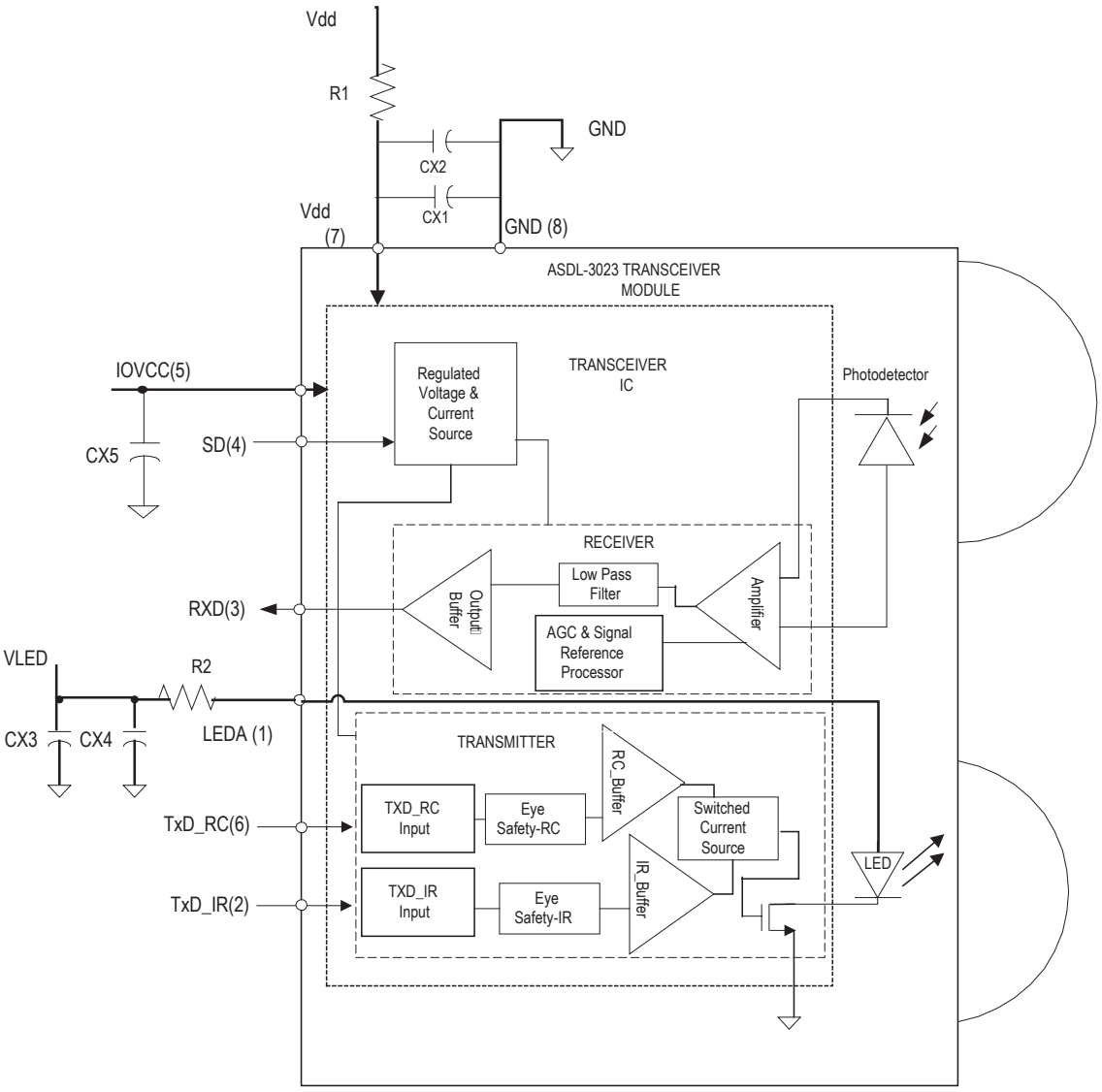



**Figure 1a. Functional Block Diagram of ASDL-3023**

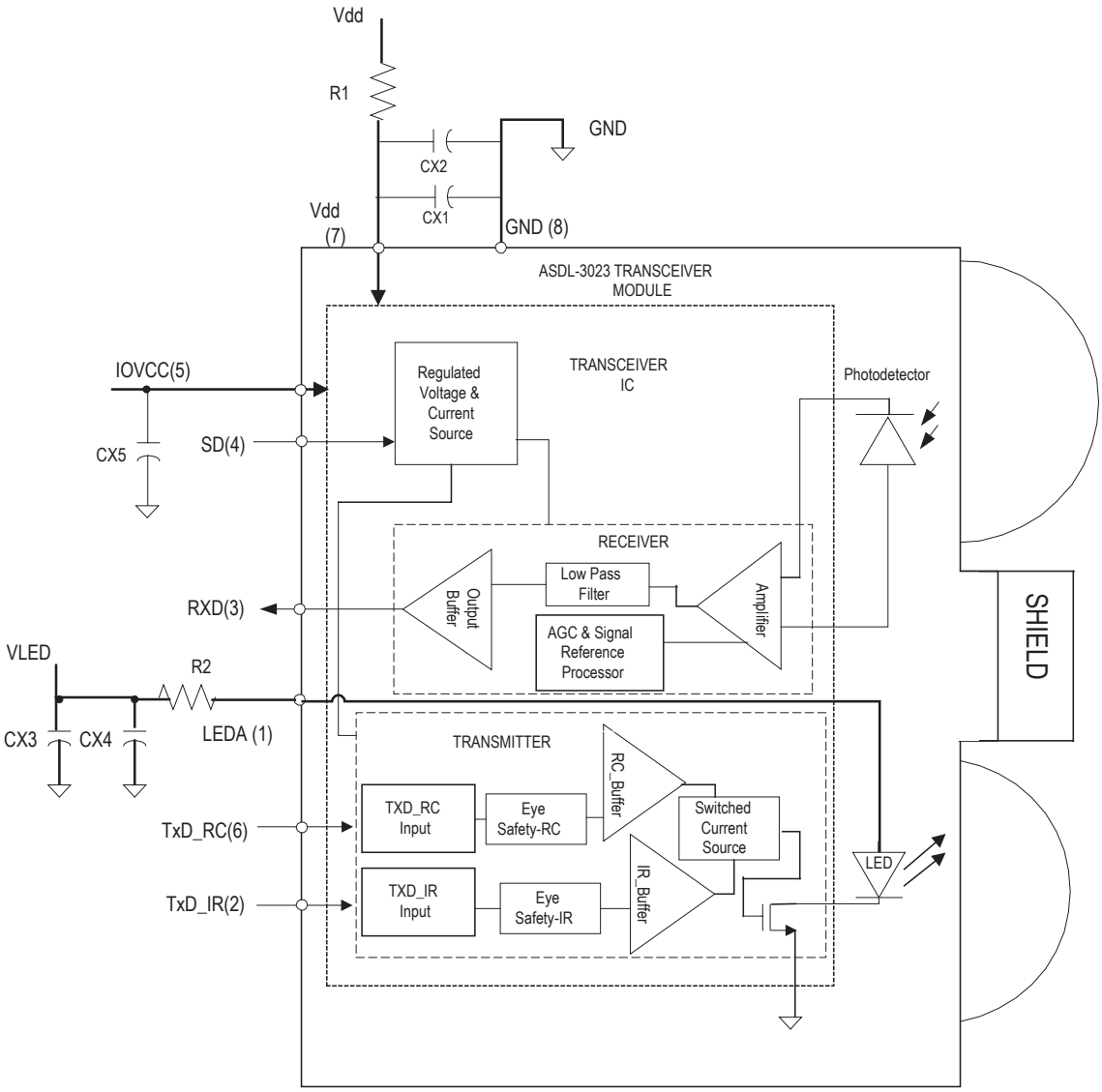



**Figure 1b. Functional Block Diagram of ASDL-3023-S21**

## Order Information

| Part Number | Packaging Type | Package | Quantity |
|---|---|---|---|
| ASDL-3023-021 | Tape and Reel | Front Option | 2500 |
| ASDL-3023-008 | Tape and Reel | Top Option | 2500 |
| ASDL-3023–S21 (Shielded) | Tape and Reel | Front Option | 2500 |

## Marking Information

The unit is marked with 'XYWLL' on the shield

Y = year

W = work week

LL = lot number

## ASDL-3023-021, ASDL-3023-008 and ASDL-3023-S21

### Pinout, Rear View

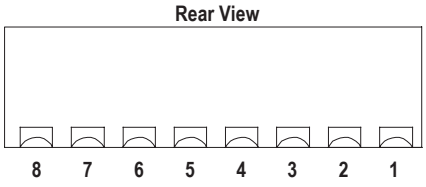



**Figure 2a. Pin out for ASDL-3023-021 and ASDL-3023-008,**

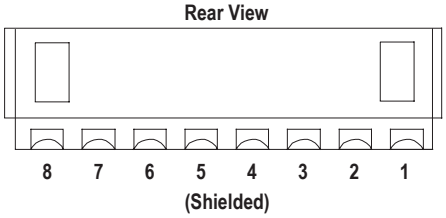



**Figure 2b. Pin out for ASDL-3023-S21**

### I/O Pins Configuration Table

| Pin | Symbol | Description | I/O Type | Notes |
|---|---|---|---|---|
| 1 | LEDA | LED Anode | | Note 1 |
| 2 | TxD_IR | IrDA transmitter data input. | Input. Active High | Note 2 |
| 3 | RxD | IrDA receive data | Output. Active Low | Note 3 |
| 4 | SD | Shutdown | Input. Active High | Note 4 |
| 5 | IOVCC | Input/Output ASIC voltage | | Note 5 |
| 6 | TxD_RC | RC transmitter data input. | Input. Active High | Note 6 |
| 7 | VCC | Supply Voltage | | Note 7 |
| 8 | GND | Ground | | Note 8 |

Notes:
1. Tied through external resistor, R2, to Vled. Refer to the table below for recommended series resistor value.
2. This pin is used to transmit serial data when SD pin is low. If held high for longer than 50 μs, the LED is turned off. Do NOT float this pin.
3. This pin is capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. The pin is in tri-state when the transceiver is in shutdown mode
4. Complete shutdown of IC and PIN diode. The pin is used for setting IR receiver bandwidth, range of IR LED current and RC drive programming mode. Refer to section on "Bandwidth Selection Timing" and "Remote Control Drive Modes" for more information. Do NOT float this pin. ***
5. Connect to ASIC logic controller supply voltage or Vcc. The voltage at this pin should be equal to or less than Vcc.
6. Logic high turns on the RC LED. If held high longer than 50 μs, the RC LED is turned off. Do NOT float the pin.
7. (i) Regulated, 2.4V to 3.6V
   (ii) This pin recommended to turn on before other pin.
8. Connect to system ground.

## Recommended Application Circuit Components

| Component | Recommended Value | Note |
|---|---|---|
| R1 | 4.7Ω,±5%, 0.25 watt for Vcc ≤ 3.0V | |
| R2 | 2.7Ω, for 2.4 ≤ VLED ≤ 2.7V;<br>3.3Ω, for 2.7 <VLED ≤ 3.0V<br>3.9Ω, for 3.0 <VLED ≤ 3.3V<br>4.7Ω, for 3.3 <VLED ≤ 3.6V<br>5.6Ω, for 3.6 <VLED ≤ 4.2V<br>10Ω, for 4.2 <VLED ≤ 5V | |
| CX1, CX3, CX5 | 100 nF, ± 20%, X7R Ceramic | 1 |
| CX2, CX4 | 4.7μF, ± 20%, Tantalum | 1 |

Notes: CX1, CX2, CX3 & CX4 must be placed within 0.7cm of ASDL-3023 to obtain optimum noise immunity

## Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ± 50°C/W.

| Parameter | Symbol | Min. | Max. | Units | Conditions | Ref |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | -40 | +100 | °C | | |
| Operating Temperature | $T_A$ | -25 | +85 | °C | | |
| LED Anode Voltage | $V_{LEDA}$ | -0.3 | 6.5 | V | | |
| Supply Voltage | $V_{CC}$ | -0.3 | 6 | V | | |
| Input Voltage : TXD, SD/Mode | $V_I$ | -0.3 | 5.5 | V | | |
| Output Voltage : RXD | $V_O$ | -0.3 | 5.5 | V | | |
| Peak IR LED Current | $I_{IRLED\ (PK)}$ | | 200 | mA | ≤ 25% duty cycle, ≤ 90 μs pulse width | Fig 3 |
| Peak RC LED Current | $I_{RCLED(PK)}$ | | 300 | mA | ≤ 10% duty cycle, ≤ 90 μs pulse width | Fig 4 |

***CAUTION: THE CMOS INHERENT TO THE DESIGN OF THIS COMPONENT INCREASES THE COMPONENT'S SUSCEPTIBILITY TO DAMAGE FROM ELECTROSTATIC DISCHARGE (ESD). IT IS ADVISED THAT NORMAL STATIC PRECAUTIONS BE TAKEN IN HANDLING AND ASSEMBLY OF THIS COMPONENT TO PREVENT DAMAGE AND/OR DEGRADATION WHICH MAY BE INDUCED BY ESD***

## Recommended Operating Conditions

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| Operating Temperature | | $T_A$ | -25 | | +85 | °C | |
| Supply Voltage | | $V_{CC}$ | 2.4 | | 3.6 | V | |
| Input/Output Voltage | | $IOV_{CC}$ | 1.5 | | 3.6 | V | |
| Logic Input Voltage for TXD, SD/Mode | Logic High | $V_{IH}$ | IOVcc-0.5 | | IOVcc | V | |
| | Logic Low | $V_{IL}$ | 0 | | 0.4 | V | |
| Receiver Input Irradiance | Logic High | $EI_H$ | 0.0090 | | 500 | $mW/cm^2$ | For in-band signals ≤ 115.2kbit/s [3] |
| | | | 0.0225 | | 500 | | 0.576 Mbit/s ≤ in-band signals ≤ 4.0 Mbit/s [3] |
| | Logic Low | $EI_L$ | | | 0.3 | $\mu W/cm^2$ | For in-band signals [3] |
| IR LED (Logic High) Current Pulse Amplitude – SIR Mode | | $I_{LEDA}$ | | 65 | | mA | |
| IR LED (Logic High) Current Pulse Amplitude – MIR/FIR Mode | | $I_{LEDA}$ | | 150 | | mA | |
| RC LED (Logic High) Current Pulse Amplitude | | $I_{LEDA}$ | | 250 | | mA | |
| Receiver Data Rate | | | 0.0096 | | 4.0 | Mbit/s | |
| Ambient Light | | | | | | | See IrDA Serial Infrared Physical Layer Link Specification, Appendix A for ambient levels |

Note :

3. An in-band optical signal is a pulse/sequence where the peak wavelength, $\lambda p$, is defined as $850 \le \lambda p \le 900$ nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification v1.4.

## Electrical and Optical Specifications

Specifications (Min. & Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C, Vcc set to 3.0V and IOVcc set to 1.5V unless otherwise noted.

### Receiver

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| Viewing Angle | | $2\theta_{1/2}$ | 30 | | | ° | |
| Peak Sensitivity Wavelength | | $\lambda_P$ | | 875 | | nm | |
| RxD_IrDA Output Voltage | Logic High | $V_{OH}$ | IOVcc – 0.5 | | IOVCC | V | $I_{OH}$ = -200 μA, EI ≤ 0.3 μW/cm$^2$ |
| | Logic Low | $V_{OL}$ | 0 | | 0.4 | V | |
| RxD_IrDA Pulse Width (SIR) [4, 5] | | $t_{RPW(SIR)}$ | 1 | | 4 | μs | $\theta_{1/2}$ ≤ 15°, $C_L$=9pF |
| RxD_IrDA Pulse Width (MIR) [4, 6] | | $t_{RPW(MIR)}$ | 100 | | 500 | ns | $\theta_{1/2}$ ≤ 15°, $C_L$=9pF |
| RxD_IrDA Pulse Width (Single) (FIR) [4, 7] | | $t_{RPW(FIR)}$ | 80 | | 175 | ns | $\theta_{1/2}$ ≤ 15°, $C_L$=9pF |
| RxD_IrDA Pulse Width (Double) (FIR) [4, 7] | | $t_{RPW(FIR)}$ | 200 | | 290 | ns | $\theta_{1/2}$ ≤ 15°, $C_L$=9pF |
| RxD_IrDA Rise & Fall Times | | $t_r$, $t_f$ | | 60 | | ns | $C_L$=9pF |
| Receiver Latency Time [8] | | $t_L$ | | | 100 | μs | EI = 9.0 μW/cm$^2$ |
| Receiver Wake Up Time [9] | | $t_{RW}$ | | | 200 | μs | EI = 10 mW/cm$^2$ |

### Infrared (IR) Transmitter

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| IR Radiant Intensity (SIR Mode) | | $I_{EH}$ | 4 | 20 | | mW/sr | IR_$I_{LEDA}$ = 65mA, $\theta_{1/2}$ ≤ 15°, TxD_IR ≥ $V_{IH}$, $T_A$ = 25°C |
| IR Radiant Intensity (MIR/FIR Mode) | | $I_{EH}$ | 10 | 50 | | mW/sr | IR_$I_{LEDA}$ = 150mA, $\theta_{1/2}$ ≤ 15°, TxD_IR ≥ $V_{IH}$, $T_A$ = 25°C |
| IR Viewing Angle | | $2\theta_{1/2}$ | 30 | | 60 | ° | |
| IR Peak Wavelength | | $\lambda_P$ | 850 | 885 | 900 | nm | |
| TxD_IrDA Logic Levels | High | $V_{IH}$ | IOVcc-0.5 | | IOVCC | V | |
| | Low | $V_{IL}$ | 0 | | 0.5 | V | |
| TxD_IrDA Input Current | High | $I_H$ | | 0.02 | | μA | $V_I$ ≥ $V_{IH}$ |
| | Low | $I_L$ | | -0.02 | | μA | 0 ≤ $V_I$ ≤ $V_{IL}$ |
| Wake Up Time [10] | | $t_{TW}$ | | 180 | | ns | |
| Maximum Optical Pulse Width [11] | | $t_{PW(Max)}$ | | 25 | 120 | μs | |
| TXD Pulse Width (SIR) | | $t_{PW(SIR)}$ | | 1.6 | | μs | $t_{PW}$(TXD_IR)=1.6μs at 115.2 kbit/s |
| TXD Pulse Width (MIR) | | $t_{PW(MIR)}$ | | 217 | | ns | $t_{PW}$(TXD_IR)=217ns at 1.152 Mbit/s |
| TXD Pulse Width (FIR) | | $t_{PW(FIR)}$ | | 125 | | ns | $t_{PW}$(TXD_IR)=125ns at 4.0 Mbit/s |
| TxD Rise & Fall Times (Optical) | | $t_r$, $t_f$ | | | 600 | ns | $t_{PW}$(TXD_IR)=1.6μs at 115.2 kbit/s |
| | | | | | 40 | ns | $t_{PW}$(TXD_IR)=125ns at 4.0 Mbit/s |
| IR LED Anode On-State Voltage (SIR Mode) | | $V_{ON}$ (IR_LEDA) | | 2.2 | | V | IR_$I_{LEDA}$=65mA, IR VLED = 3.6V, R = 4.7Ω, VI(TxD) ≥ VIH |
| IR LED Anode On-State Voltage (MIR/FIR Mode) | | $V_{ON}$ (IR_LEDA) | | 2.1 | | V | IR_$I_{LEDA}$=150mA, IR VLED = 3.6V, R = 4.7Ω, VI(TxD_IR) ≥ VIH |

## Remote Control (RC) Transmitter

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| RC Radiant Intensity | | $I_{EH}$ | | 80 | | mW/sr | RC_$I_{LEDA}$ = 250mA, $\theta_{1/2} \le 15°$, TxD_RC ≥ $V_{IH}$, $T_A$ = 25 °C |
| RC Viewing Angle | | $2\theta_{1/2}$ | 30 | | 60 | ° | |
| RC Peak Wavelength | | $\lambda_P$ | 880 | 885 | 900 | nm | |
| TxD_RC Logic Levels | High | $V_{IH}$ | IOVcc-0.5 | | IOVCC | V | |
| | Low | $V_{IL}$ | 0 | | 0.5 | V | |
| TxD_RC Input Current | High | $I_H$ | | 0.02 | 1 | µA | $V_I \ge V_{IH}$ |
| | Low | $I_L$ | | -0.02 | 1 | µA | $0 \le V_I \le V_{IL}$ |
| RC LED Anode On-State Voltage | | $V_{ON}$ (RC_LEDA) | | 2 | | V | RC_$I_{LEDA}$=250mA, RC VLED = 3.6V, R = 4.7Ω, $V_{I(TxD_RC)} \ge V_{IH}$ |

## Transceiver

| Parameters | | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| Input Current | High | $I_H$ | | 0.01 | 1 | µA | VI ≥ VIH |
| | Low | $I_L$ | -1 | -0.02 | 1 | µA | 0 ≤ VI ≤ VIL |
| Supply Current | Shutdown | $I_{CC1}$ | | | 1 | µA | VSD ≥ $IOV_{CC}$-0.5, TA=25°C |
| | Idle (Standby) | $I_{CC2}$ | | 2.0 | 2.9 | mA | $V_{I(TxD)} \le V_{IL}$, EI=0 |
| | Active | $I_{CC3}$ | | 3.5 | | mA | $V_{I(TxD)} \ge V_{IL}$, EI=10mW/cm$^2$ |

Note:
[4] An in-band optical signal is a pulse/sequence where the peak wavelength, $\lambda_P$, is defined as 850 nm ≤ $\lambda_P$ ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification version 1.4.
[5] For in-band signals 115.2 kbit/s where 9 µW/cm2 ≤ EI ≤ 500 mW/cm2.
[6] For in-band signals 1.152 Mbit/s where 22 µW/cm2 ≤ EI ≤ 500 mW/cm2.
[7] For in-band signals 4 Mbit/s where 22 µW/cm2 ≤ EI ≤ 500 mW/cm2.
[8] Latency is defined as the time from the last TxD_IrDA light output pulse until the receiver has recovered full sensitivity.
[9] Receiver Wake Up Time is measured from Vcc power ON to valid RxD_IrDA output.
[10] Transmitter Wake Up Time is measured from Vcc power ON to valid light output in response to a TxD_IrDA pulse.
[11] The Max Optical PW is defined as the maximum time which the IR LED will turn on, this, is to prevent the long Turn On time for the IR LED.

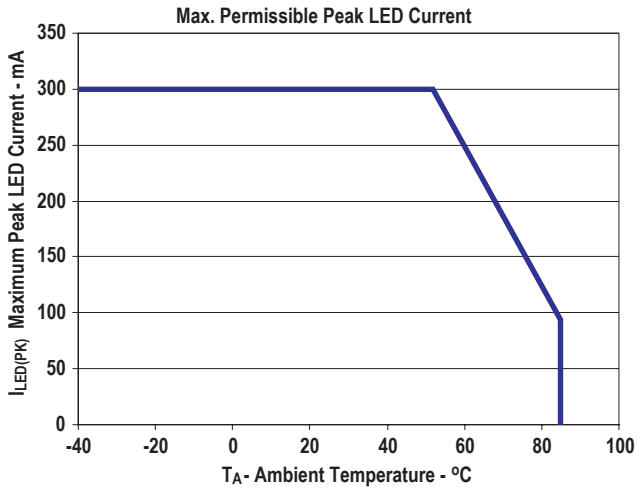



**Figure 3. Maximum Peak IR LED current vs. ambient temperature. Derated based on TJMAX = 100°C.**

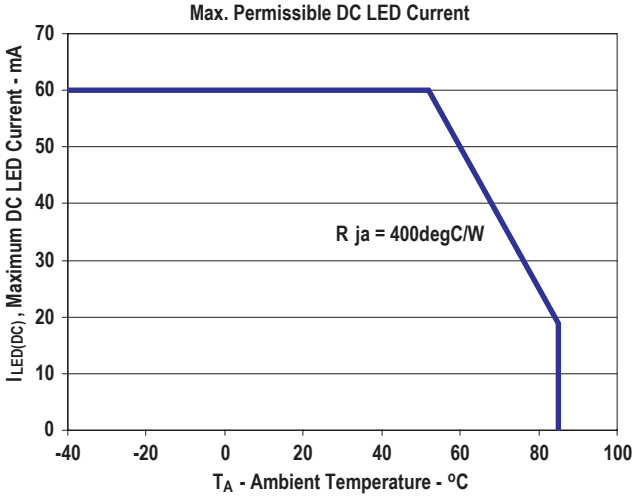



**Figure 4. Maximum Peak RC LED current vs. ambient temperature. Derated based on TJMAX = 100°C.**

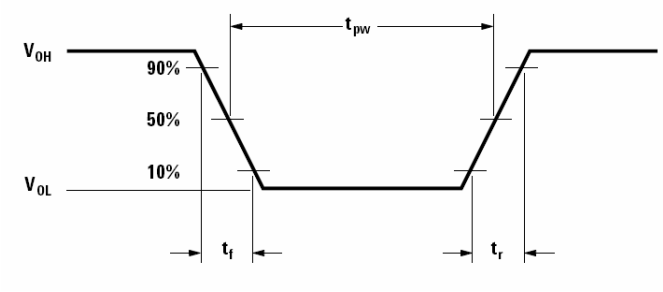



Figure 5a. Timing Waveform - RXD Output Waveform

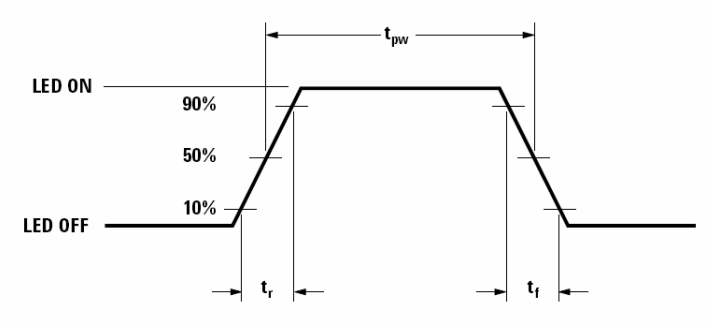



Figure 5b. Timing Waveform - LED Optical Waveform

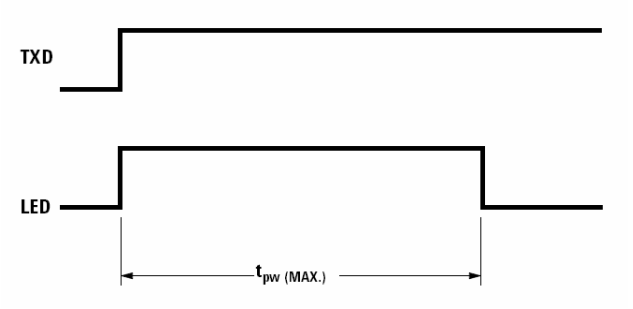



Figure 5c. Timing Waveform – TXD "Stuck-on" Protection Waveform

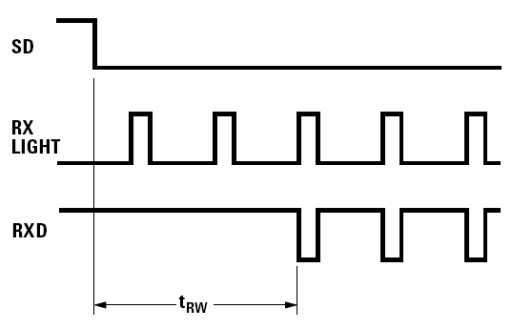



Figure 5d. Timing Waveform – Receiver Wakeup Time Waveform

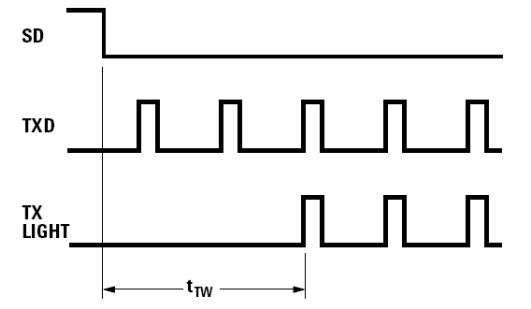
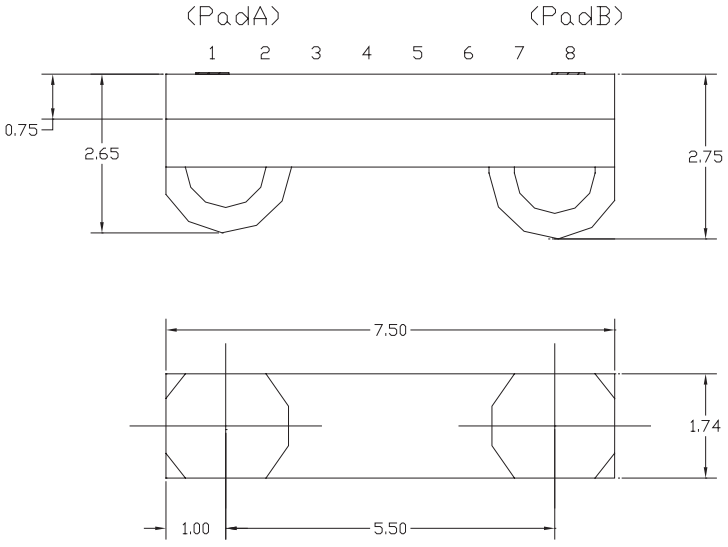



Figure 5e. Timing Waveform – TXD Wakeup Time Waveform

## Package Dimension: ASDL-3023-021 (Shieldless, Front) and ASDL-3023-008 (Shieldless, Top)

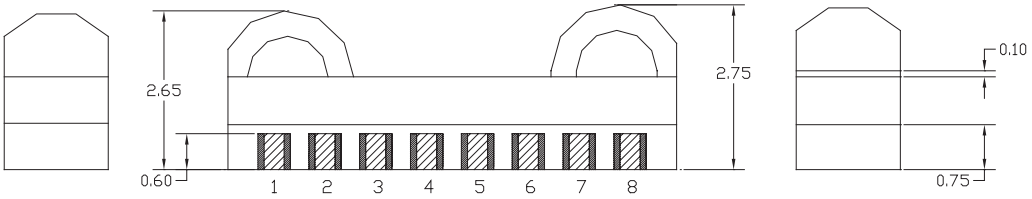


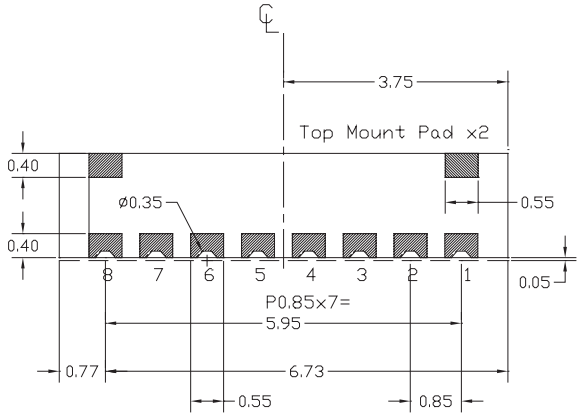

PIN ASSIGNMENT:

1=LEDA
2=TXD_IR
3=RXD
4=SD
5=I□VCC
6=TXD_RC
7=VDD
8=GND

Note:
Top Mount Enable Mount Pad x2 at location opposite Pin 1 and Pin 8.

Unit: mm.
Tolerance: =+/-0.2mm.

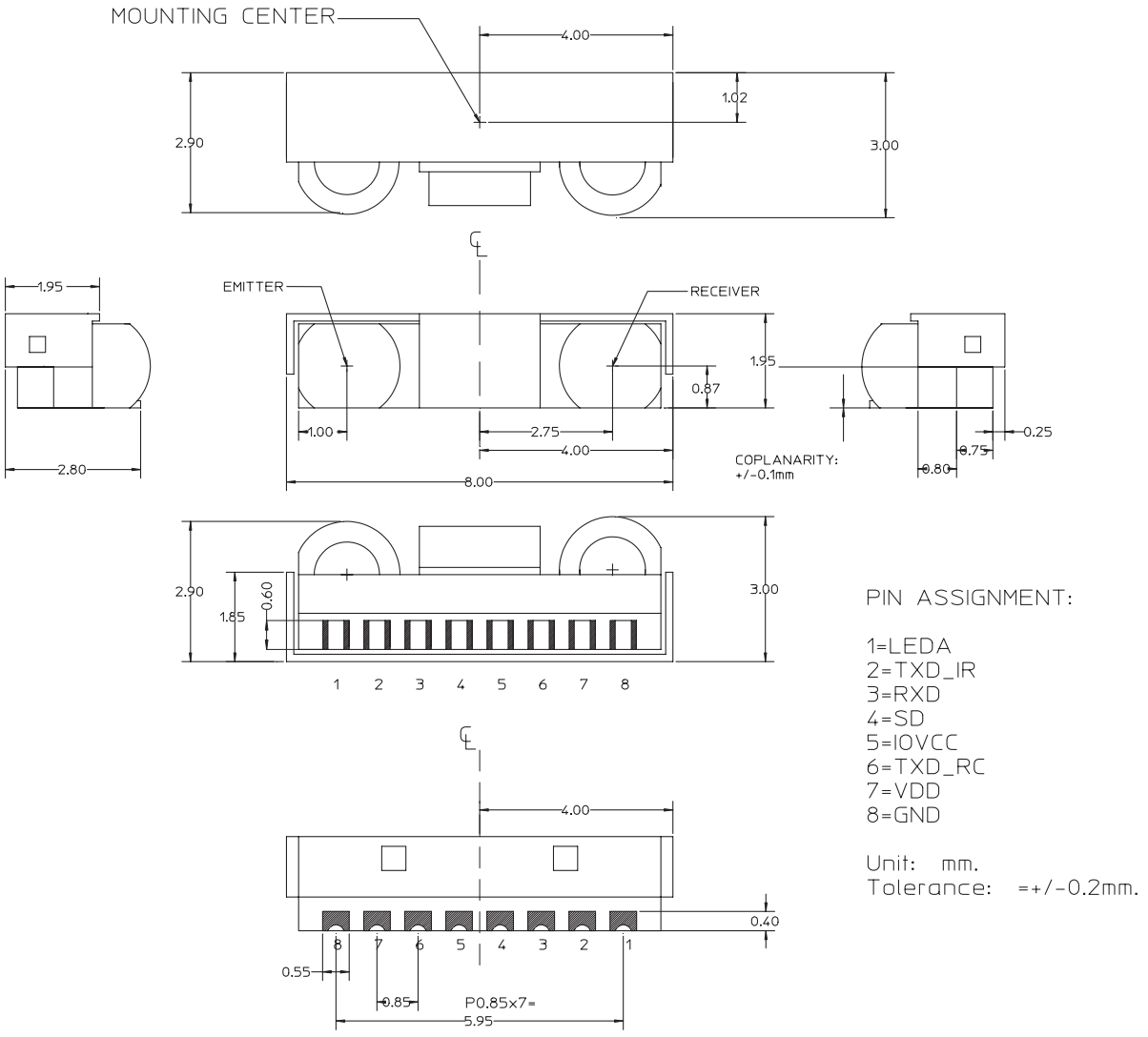



Remarks:

1) Top Mount Enable Pads (x2) opposite site of castellation holes.
2) These pads are not plated throught vias, but only surface pads.
3) Pad A: □pposite of Pin1; isolated.
Pad B: □pposite of Pin8,interconnected to Pin8/Gnd.

## Package Dimension: ASDL-3023-S21 (Shielded, Front)



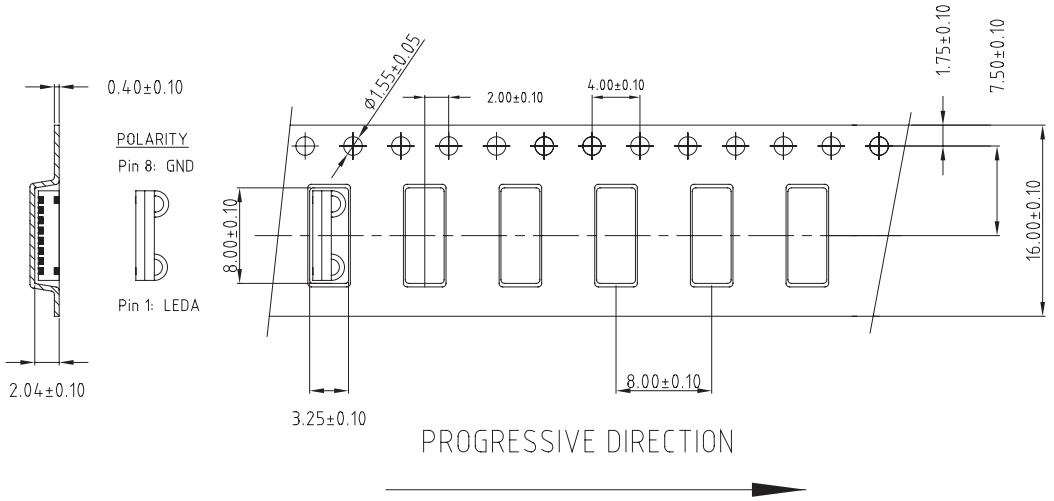

PIN ASSIGNMENT:

1=LEDA
2=TXD_IR
3=RXD
4=SD
5=IOVCC
6=TXD_RC
7=VDD
8=GND

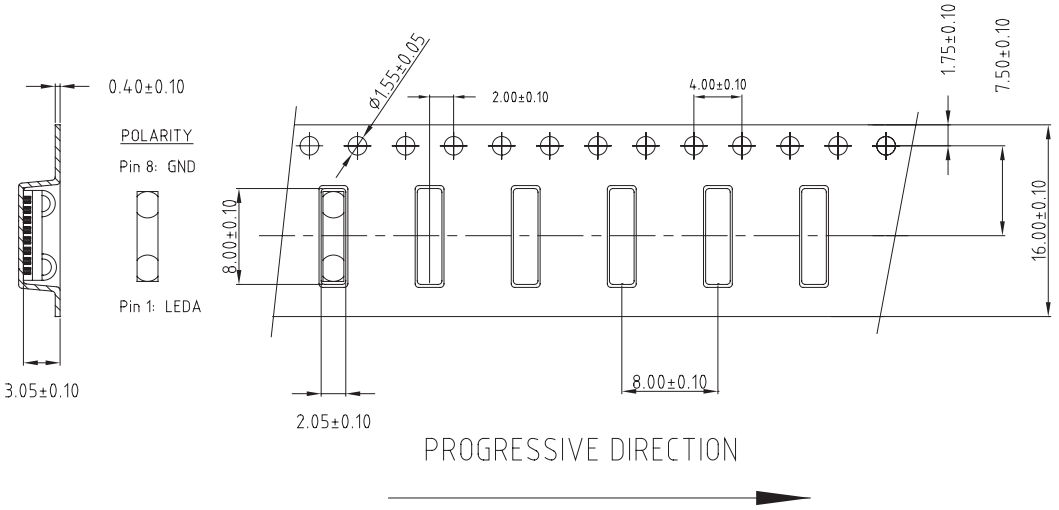
Unit: mm.
Tolerance: =+/-0.2mm.

## Tape & Reel Dimensions

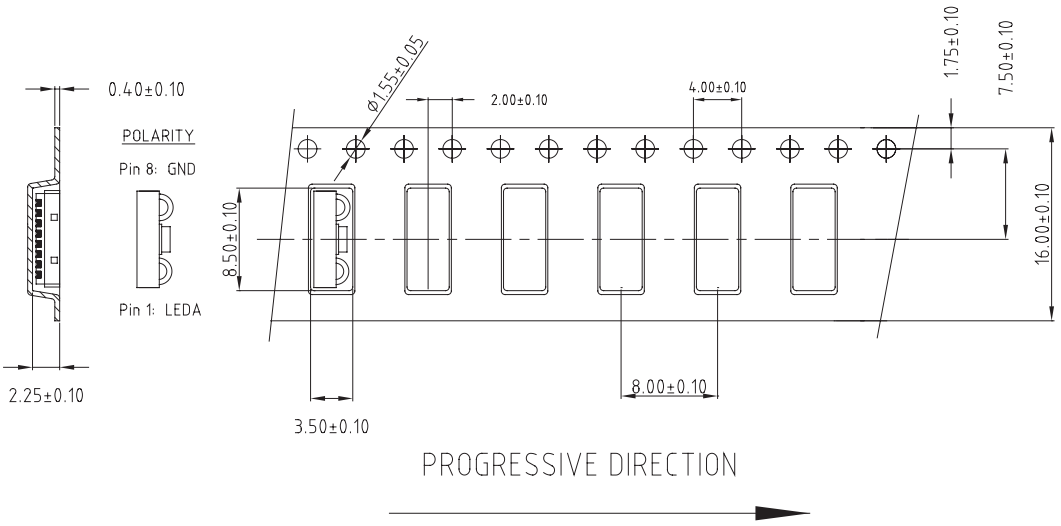
ASDL-3023-021 (Shieldless, Front)

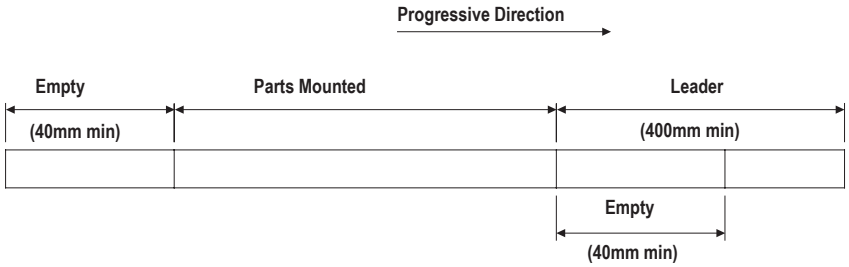



ASDL-3023-008 (Shieldless, Top)

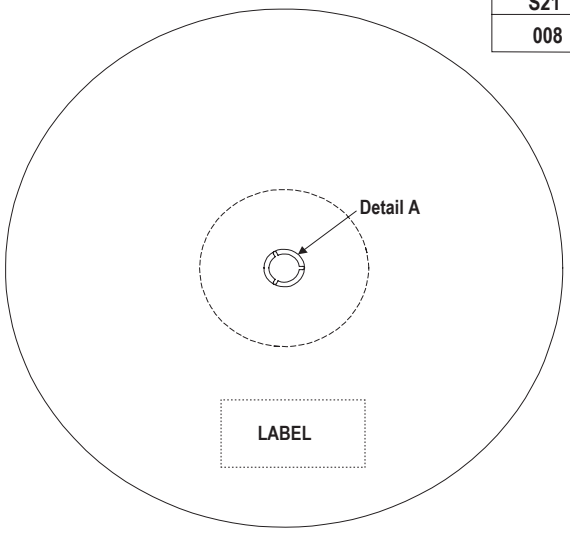


ASDL-3023-S21 (Shielded, Front)

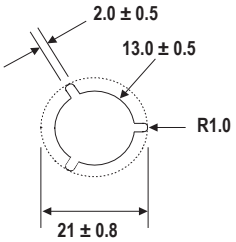


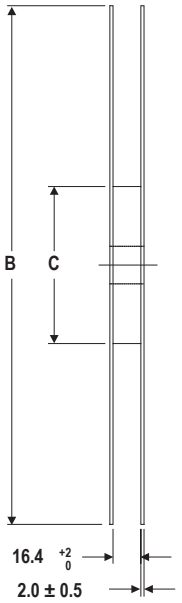

| Option # | "B" | "C" | Quantity |
|---|---|---|---|
| 021 | 330 | 80 | 2500 |
| S21 | 330 | 80 | 2500 |
| 008 | 330 | 80 | 2500 |




Unit: mm




Detail A



## ASDL-3023 Moisture Proof Packaging

All ASDL-3023 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 3.

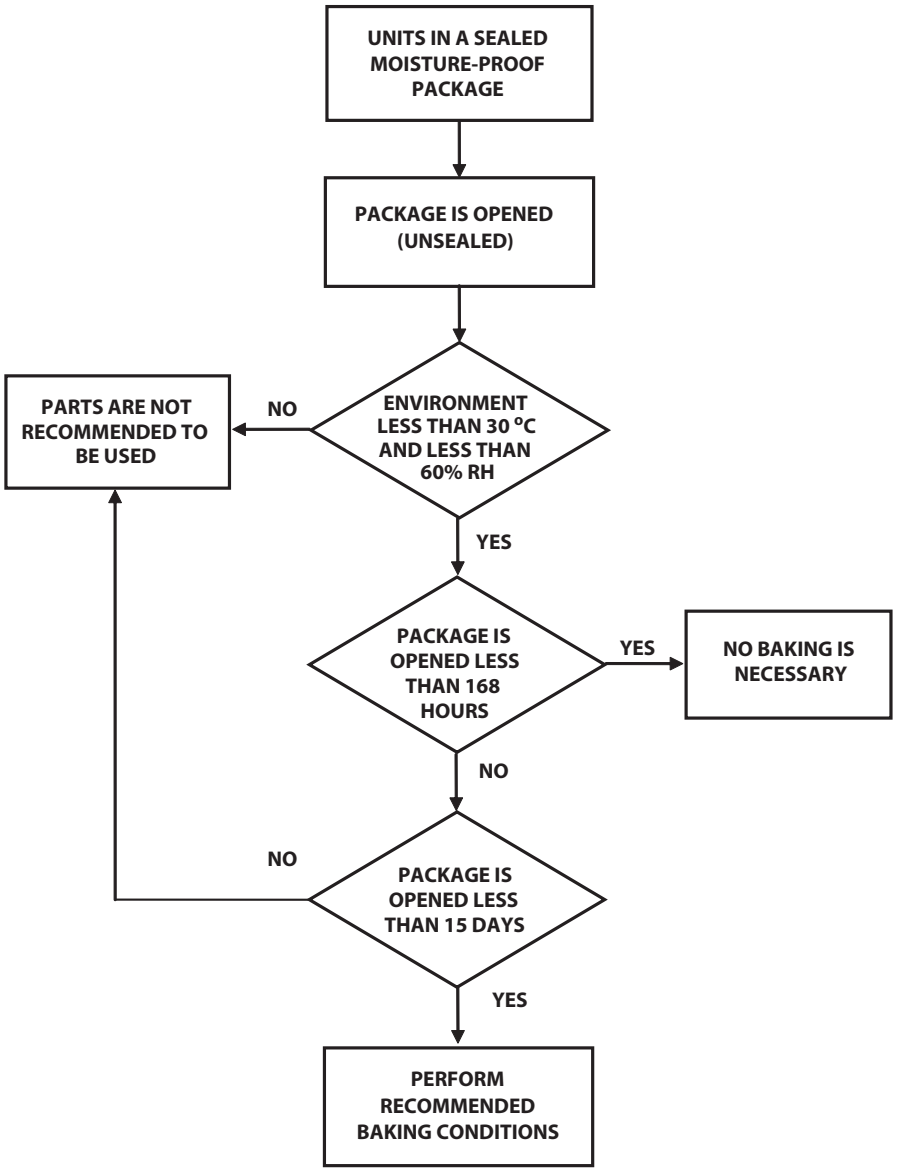



**Figure 6. Baking Conditions Chart**

### Recommended Storage Conditions

| | |
|---|---|
| Storage Temperature | 10°C to 30°C |
| Relative Humidity | below 60% RH |

### Time from unsealing to soldering

After removal from the bag, the parts should be soldered within 7 days if stored at the recommended storage conditions. When MBB (Moisture Barrier Bag) is opened and the parts are exposed to the recommended storage conditions more than 7 days but less than 15 days the parts must be baked before reflow to prevent damage to the parts.

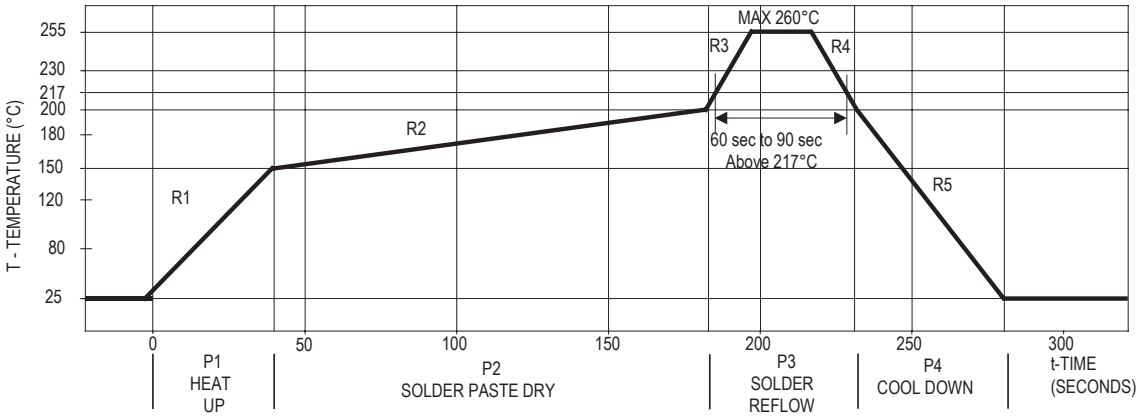
Note: To use the parts that exposed for more than 15 days is not recommended.

### Baking Conditions

| Package | Temp | Time |
|---|---|---|
| In reels | 60 °C | ≥ 48hours |
| In bulk | 100 °C | ≥ 4hours |

Baking should only be done once.

## Recommended Reflow Profile




| Process Zone | Symbol | ΔT | Maximum ΔT/Δtime or Duration |
|---|---|---|---|
| Heat Up | P1, R1 | 25°C to 150°C | 3°C/s |
| Solder Paste Dry | P2, R2 | 150°C to 200°C | 100s to 180s |
| Solder Reflow | P3, R3<br>P3, R4 | 200°C to 260°C<br>260°C to 200°C | 3°C/s<br>-6°C/s |
| Cool Down | P4, R5 | 200°C to 25°C | -6°C/s |
| Time maintained above liquidus point , 217°C | | > 217°C | 60s to 90s |
| Peak Temperature | | 260°C | - |
| Time within 5°C of actual Peak Temperature | | - | 20s to 40s |
| Time 25°C to Peak Temperature | | 25°C to 260°C | 8mins |

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

**In process zone P1**, the PC board and ASDL-3023 pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and ASDL-3023 pins.

**Process zone P2** should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

**Process zone P3** is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 90 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

**Process zone P4** is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and ASDL-3023 pins to change dimensions evenly, putting minimal stresses on the ASDL-3023.

It is recommended to perform reflow soldering no more than twice.

## Appendix A: ASDL-3023 SMT Assembly Application Note

## Solder Pad, Mask and Metal Stencil

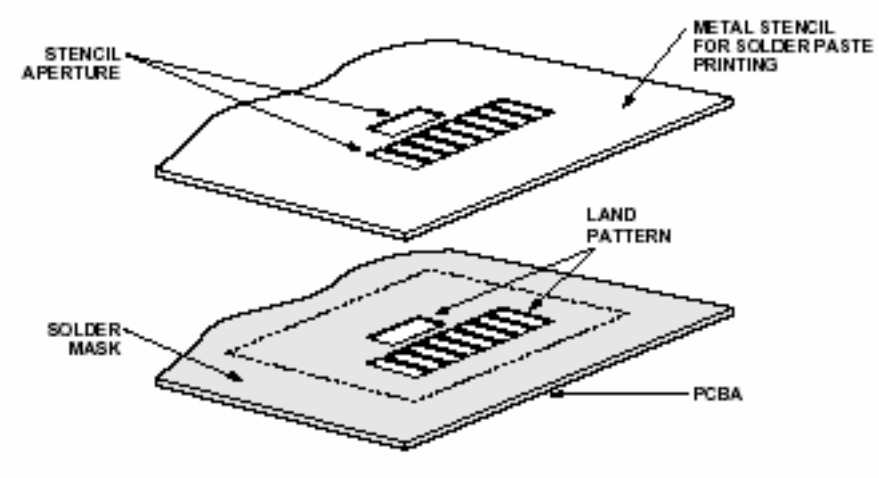
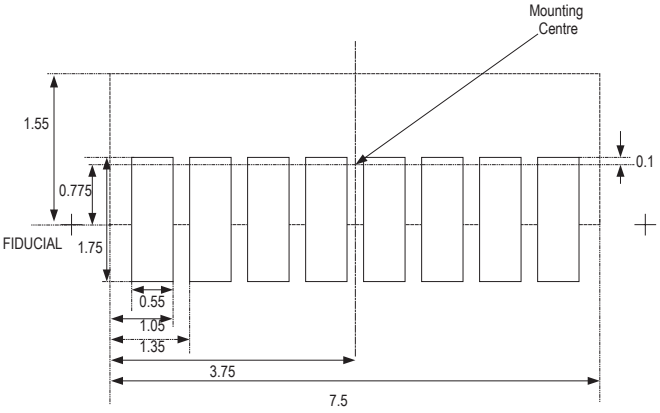



**Figure A1. Stencil and PCBA**

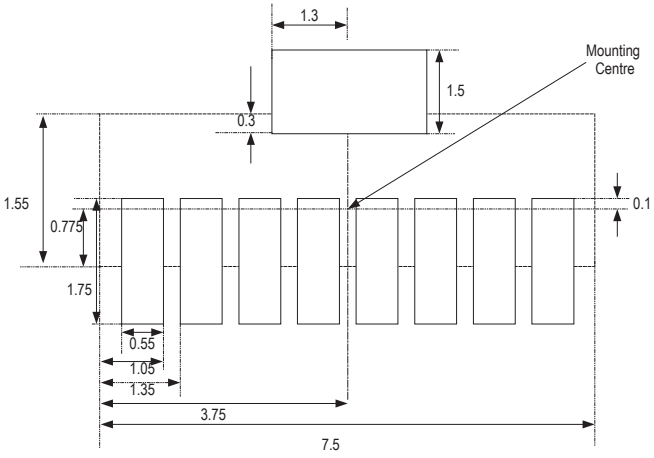
## Recommended land pattern for ASDL-3023-021




UNIT: mm

**Figure A2a. Recommended land pattern, ASDL-3023-021**

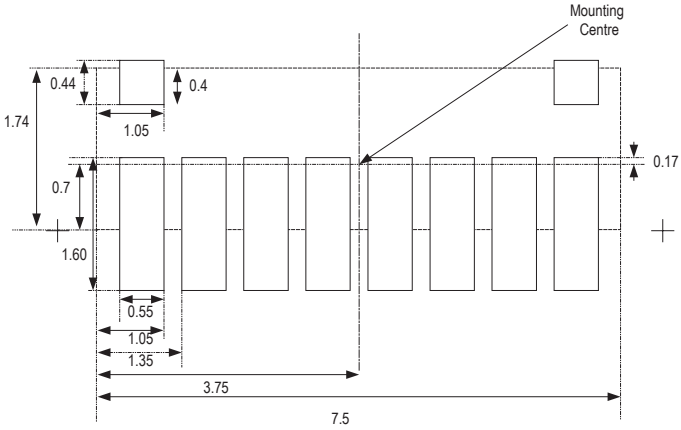
## Recommended land pattern for ASDL-3023- S21




UNIT: mm

**Figure A2b. Recommended land pattern, ASDL-3023-S21**

## Recommended land pattern for ASDL-3023- 008




UNIT: mm

**Figure A2c. Recommended land pattern, ASDL-3023-008**

## Recommended Metal solder Stencil Aperture

It is recommended that only a 0.11 mm (0.004 inch) or a 0.127 mm (0.005 inch) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the Table 1 below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used. Aperture opening for shield pad is 2.6 mm x 1.5 mm(for ASDL-3023-S1) as per land pattern. Compared to 0.127mm stencil thickness 0.11mm stencil thickness has longer length in land pattern. It is extended outwardly from transceiver to capture more solder paste volume.

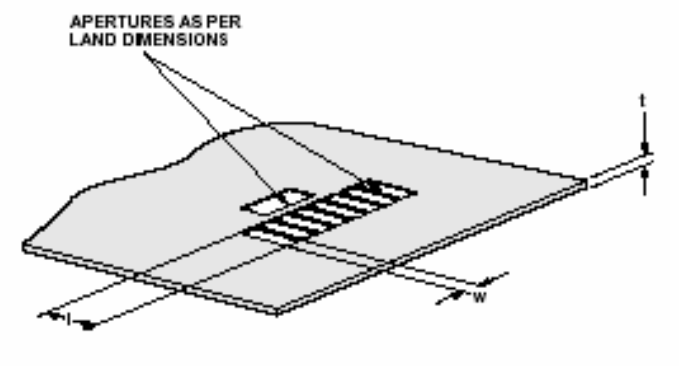



**Figure A3. Solder stencil aperture**

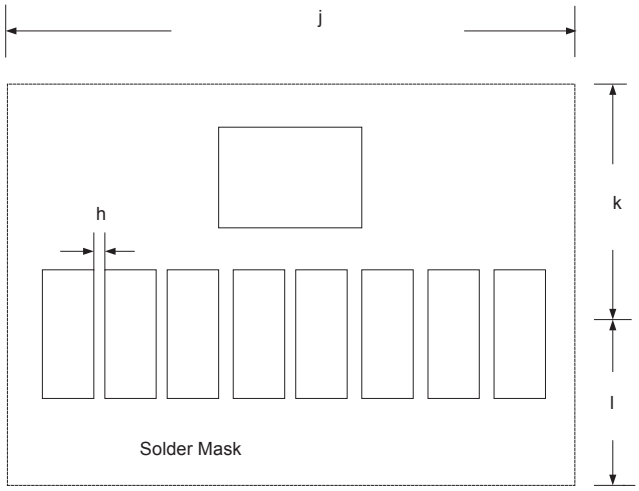
**Table 1.**

| Stencil thickness, t(mm) | Aperture size(mm) | |
|---|---|---|
| | Length,l | Width,w |
| 0.127mm | 1.75+/-0.05 | 0.55+/-0.05 |
| 0.11mm | 2.4+/-0.05 | 0.55+/-0.05 |

## Adjacent Land Keepout and Solder Mask Areas

Adjacent land keepout is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area. The minimum solder resist strip width required to avoid solder bridging adjacent pads is 0.2mm.It is recommended that two fiducially crosses be placed at mid length of the pads for unit alignment.

Note: Wet/Liquid Photo-imaginable solder resist/mask is recommended

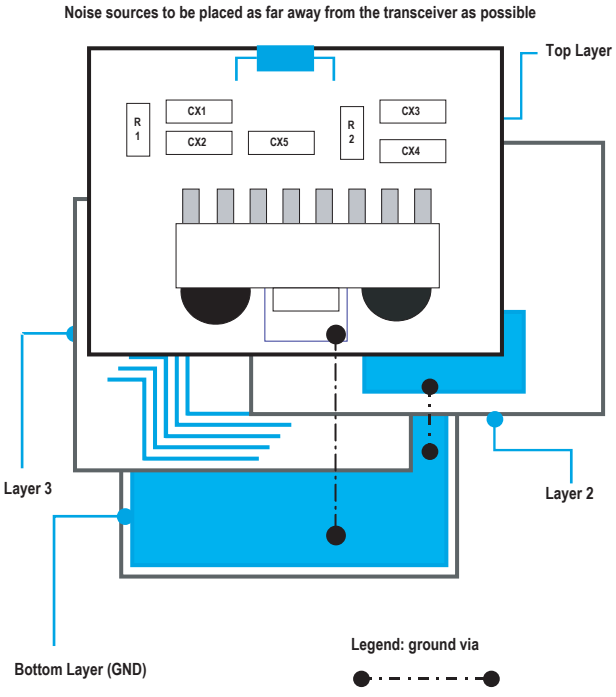



| Dimension | mm |
|---|---|
| h | 0.2 |
| l | 3.0 |
| k | 3.85 |
| j | 10.1 |

## Appendix B: PCB Layout Suggestion

The effects of EMI and power supply noise can potentially reduce the sensitivity of the receiver, resulting in reduced link distance. The PCB layout played an important role to obtain a good PSRR and EM immunity resulting in good electrical performance. Things to note:

1. The ground plane should be continuous under the part, but should not extend under the shield trace.
2. The shield trace is a wide, low inductance trace back to the system ground. CX1, CX2, CX3, CX4 and CX5 are optional supply filter capacitors; they may be left out if a clean power supply is used.
3. VLED can be connected to either unfiltered or unregulated power supply. The bypass capacitors should be connection before the current limiting resistor R2 respectively. In a noisy environment, including capacitor CX3and CX4 can enhance supply rejection. CX3 that is generally a ceramic capacitor of low inductance providing a wide frequency response while CX4 is tantalum capacitor of big volume and fast frequency response. The use of a tantalum capacitor is more critical on the VLED line, which carries a high current.
4. VCC pin can be connected to either unfiltered or unregulated power supply. The Resistor, R1 together with the capacitors, CX 1and CX2 acts as the low pass filter.
5. IOVCC is connected to the ASIC voltage supply or the VCC supply. The capacitor, CX5 acts as the bypass capacitor.

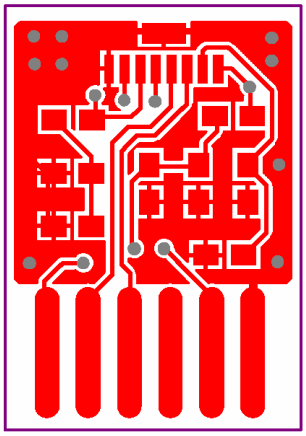



6. Preferably a multi-layered board should be used to provide sufficient ground plane. Use the layer underneath and near the transceiver module as Vcc, and sandwich that layer between ground connected board layers. The diagram below demonstrate an example of a 4 layer board :

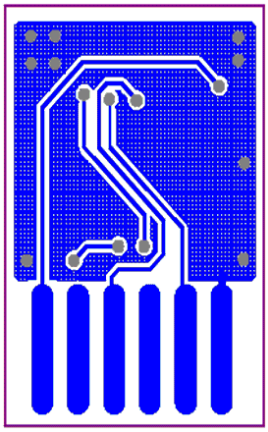
- Top Layer: Connect the metal shield and module ground pin to bottom ground layer;

  Place the bypass capacitors within 0.5cm from the VCC and ground pin of the module.
- Layer 2: Critical ground plane zone. 3 cm in all direction around the module. Connect to a clean, noiseless ground node (eg bottom layer).
- Layer 3: Keep data bus away from critical ground plane zone.
- Bottom layer: Ground layer. Ground noise <75 mVp-p. Should be separated from ground used by noisy sources.

The area underneath the module at the second layer, and 3cm in all direction around the module is defined as the critical ground plane zone. The ground plane should be maximized in this zone. Refer to application note AN1114 or the Avago Technologies IrDA Data Link Design Guide for details. The layout below is based on a 2-layer PCB.



Top Layer



Bottom Layer

## Appendix C: General Application Guide for the ASDL-3023 infrared IrDA Compliant 4 Mb/s Transceiver.

### Description

The ASDL-3023, a wide-voltage operating range infrared transceiver is a low-cost and small form factor device that is designed to address the mobile computing market such as PDAs, as well as small embedded mobile products such as digital cameras and cellular phones. It is spectrally suited to universal remote control transmission function at 940 nm typically. It is fully compliant to IrDA 1.4 low power specification

up 4Mb/s and support most remote control codes The design of ASDL-3023 also includes the following unique features :

- Spectrally suited to universal remote control transmission function at 940nm typically;
- Low passive component count;
- Shutdown mode for low power consumption requirement;
- Direct interface with I/O logic circuit.

### Selection of Resistor R2

Resistor R2 should be selected to provide the appropriate peak pulse IR and RC LED current respectively at different ranges of Vcc as shown on page 3 under "Recommended Application circuit components".

### Interface to the Recommended I/O chip

The ASDL-3023's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required. Data rate from 9.6kb/s to 4Mb/s is available at RXD pin. The TXD_RC, pin6 together with LEDA, pin1 is used to selected the remote control transmit mode. Alternatively, the TXD_IR, pin2 together with LEDA, pin1 is used for infrared transmit selection.

Following shows the hardware reference design with ASDL-3023

*Detail configuration of ASDL-3023 with the controller chip is shown in Figure 3.

The use of the infrared techniques for data communication has increase rapidly lately and almost all mobile application processors have built in the IR port. This does away with the external Endec and simplifies the interfacing to a direct connection between the processor and the transceiver. The next section discusses interfacing configuration with a general processor.

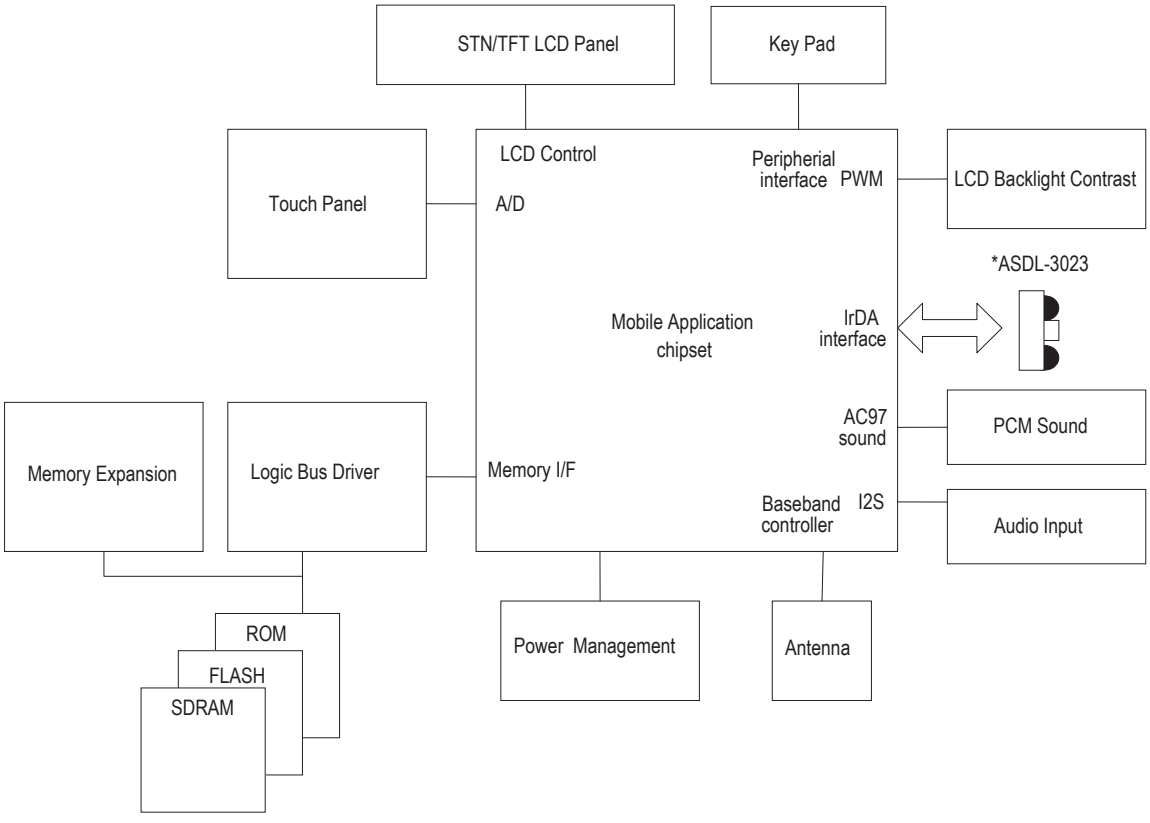



**Figure 2. Mobile Application Platform**

## General mobile application processor

The transceiver is directly interface with the microprocessor provided its support infrared communication commonly known as Infrared Communications Port (ICP). The ICP supports both SIR data rates up to 115.2kps and sometimes FIR data with data rates up to 4Mbps. The remote control commands can be sent one of the available General Purpose IO pins or the UART block with IrDA functionality. It should be should be observed that although both IrDA data transmission and Remote control transmission is possible simultaneously by the hardware, hence the software is required to resolve this issue to prevent the mixing and corruption of data while being transmitted over the free air. The above Figure 3 illustrates a reference interfacing to implement both IR and RC functionality with ASDL-3023.

## Remote Control Operation

The ASDL-3023 is spectrally suited to universal remote control transmission function at 940nm typically. Remote control applications are not governed by any standards, owing to which there are numerous remote codes in market. Each of those standards results in receiver modules with different sensitivities, depending on the carries frequencies and responsively to the incident light wavelength. Remote control carrier frequencies are in the range of 30KHz to 60KHz (for details of some the frequently used carrier frequencies, please refer to AN1314). Some common carrier frequencies and the corresponding SA-1110 UART frequency and baud rate divisor are shown in Table 3.

**Table 3.**

| Remote Control Carrier Frequency (KHz) | SA-1110 UART Frequency (KHz) | Baud Rate Divisor |
|---|---|---|
| 30 | 28.8 | 8 |
| 32,33 | 32.9 | 7 |
| 36,36.7,38,39.2,40 | 38.4 | 6 |
| 56 | 57.6 | 4 |

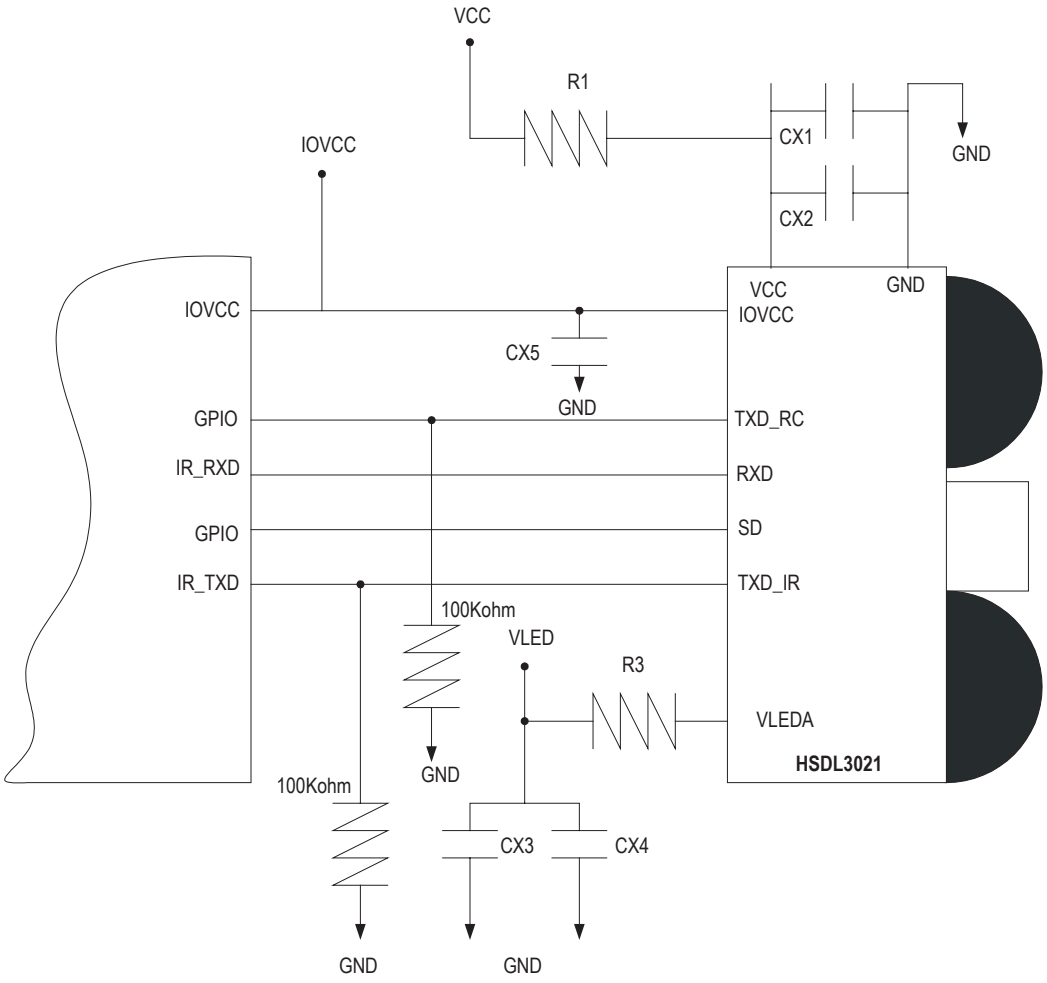
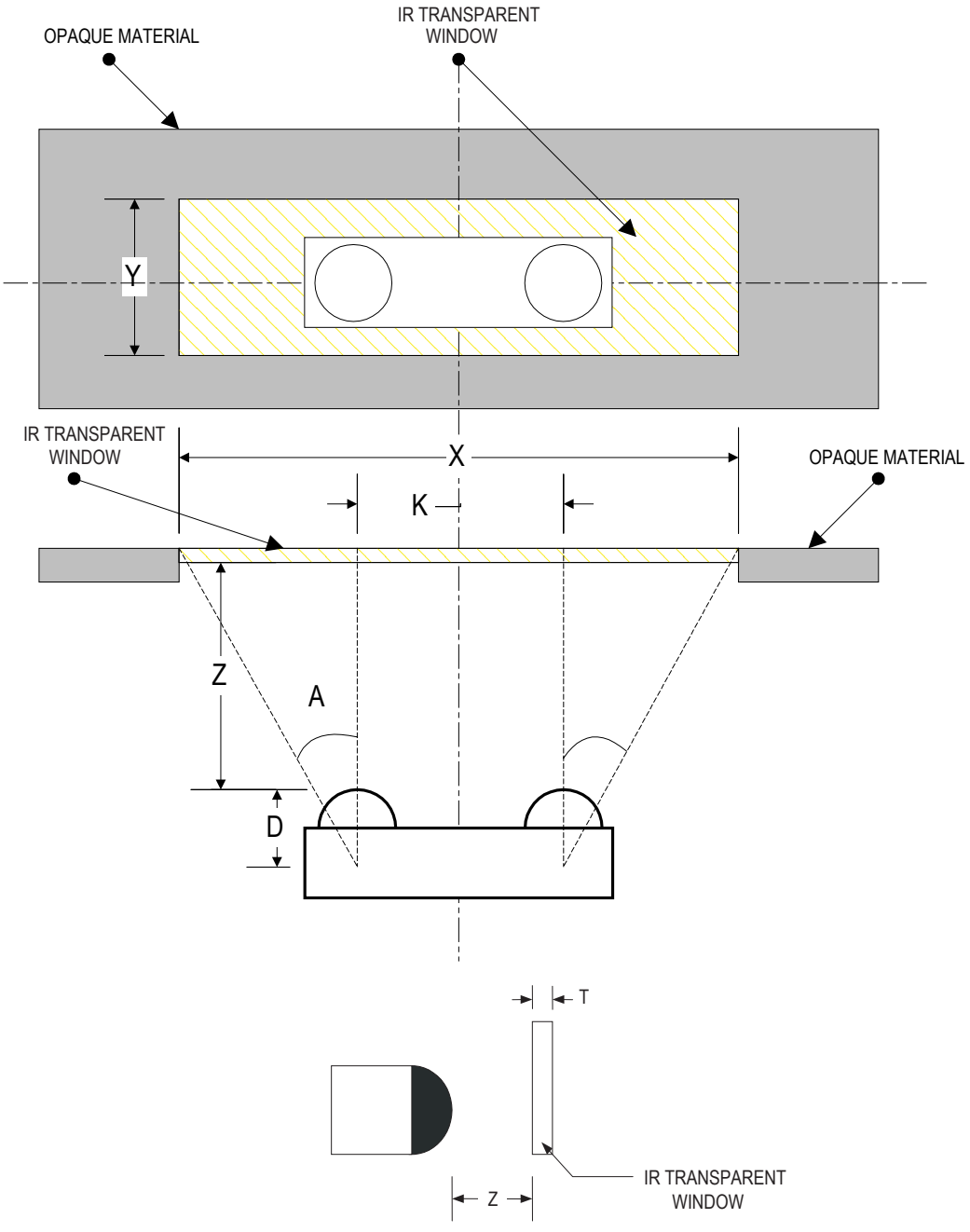



**Figure 3. ASDL-3023 configuration with general mobile architecture processor**

## Appendix E: Window Design for ASDL-3023

### Optical Port Dimensions for ASDL-3023

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30° and the maximum size corresponds to a cone angle of 60°.



In the figure above, X is the width of the window, Y is the height of the window and Z is the distance from the ASDL-3023 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 5.5mm. The equations for computing the window dimensions are as follows:

X = K + 2*(Z+D)*tanA

Y = 2*(Z+D)*tanA

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable,

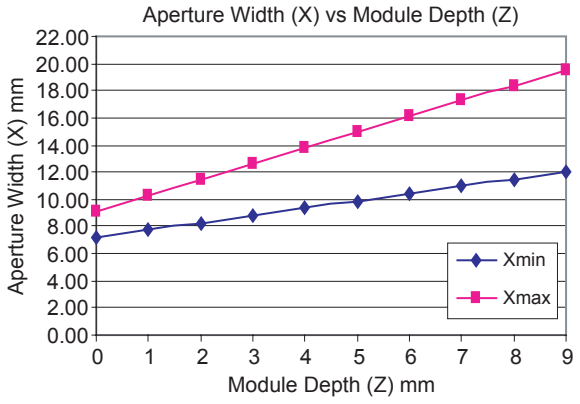
W1 = 0.33*T,

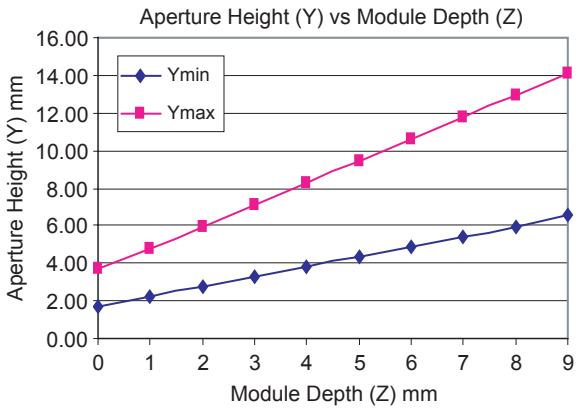
W2 = 0.66*T,

where T is the window thickness and the refractive index of the window material is 1.586.

The depth of the LED image inside the ASDL-3023, D, is 3.17mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 15° and the maximum is 30°. The equations result in the following tables and graphs. The graphs are plotted assuming that the thickness of the window is negligible.

| Module Depth (Z) mm | Aperture Width (X, mm) | | Aperture height (Y, mm) | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| 0 | 7.20 + W1 | 9.16 + W2 | 1.70 + W1 | 3.66 + W2 |
| 1 | 7.73 + W1 | 10.32 + W2 | 2.23 + W1 | 4.82 + W2 |
| 2 | 8.27 + W1 | 11.47 + W2 | 2.77 + W1 | 5.97 + W2 |
| 3 | 8.81 + W1 | 12.62 + W2 | 3.31 + W1 | 7.12 + W2 |
| 4 | 9.34 + W1 | 13.78 + W2 | 3.84 + W1 | 8.28 + W2 |
| 5 | 9.88 + W1 | 14.93 + W2 | 4.38 + W1 | 9.43 + W2 |
| 6 | 10.41 + W1 | 16.09 + W2 | 4.91 + W1 | 10.59 + W2 |
| 7 | 10.95 + W1 | 17.24 + W2 | 5.45 + W1 | 11.74 + W2 |
| 8 | 11.49 + W1 | 18.40 + W2 | 5.99 + W1 | 12.90 + W2 |
| 9 | 12.02 + W1 | 19.55 + W2 | 6.52 + W1 | 14.05 + W2 |




It is recommended that the tolerance for assembly be considered as well. The recommended minimum window size which will take into account of the assembly tolerance is defined as:

Xmin + assembly tolerance = Xmin + 2*(assembly tolerance) (Dimensions are in mm)

Ymin + assembly tolerance = Ymin + 2*(assembly tolerance) (Dimensions are in mm)

## Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10% or less for best optical performance. Light loss should be measured at 875 nm. The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics.

## Recommended Plastic Materials:

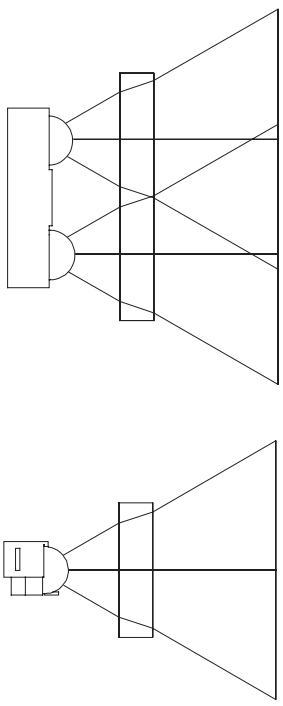
| Material # | Light Transmission | Haze | Refractive Index |
|---|---|---|---|
| Lexan 141 | 88% | 1% | 1.586 |
| Lexan 920A | 85% | 1% | 1.586 |
| Lexan 940A | 85% | 1% | 1.586 |

Note: 920A and 940A are more flame retardant than 141.

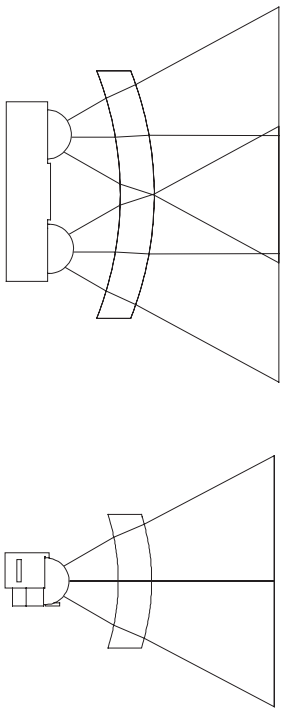
Recommended Dye: Violet #21051
(IR transmissant above 625mm)

## Shape of the Window

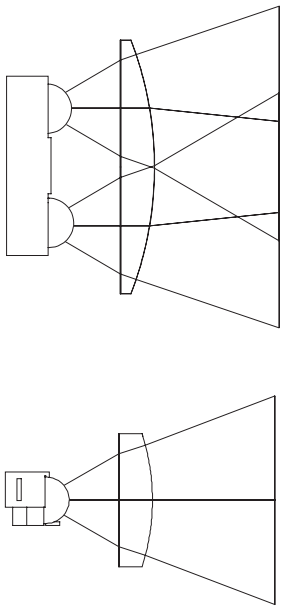
From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode. If the window must be curved for mechanical or industrial design reasons, place the same curve on the backside of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve. The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.



**Flat Window, (First Choice)**



**Curved Front and Back, (Second Choice)**



**Curved Front, Flat Back, (Do not use)**

## Appendix F: General Application Guide for the ASDL-3023

### Remote Control Drive Modes

The ASDL-3023 can operate in the single-TxD programmable mode or the two-TxD direct transmission mode.

### Single-TxD Programmable Mode

In the single-TxD programmable mode, only one input pin (TxD_IR input pin) is used to drive the LED in both IrDA mode as well as Remote Control mode of operation. This mode can be used when the external controller uses only one transmit pin for both IrDA as well RC mode of operation.

transceiver is in default mode (IrDA-SIR) when powered up. The user needs to apply the following programming sequence to both the TxD_IR and SD inputs to enable the transceiver to operate in either the IrDA or remote control mode.

### Two-TxD Direct Transmission Mode

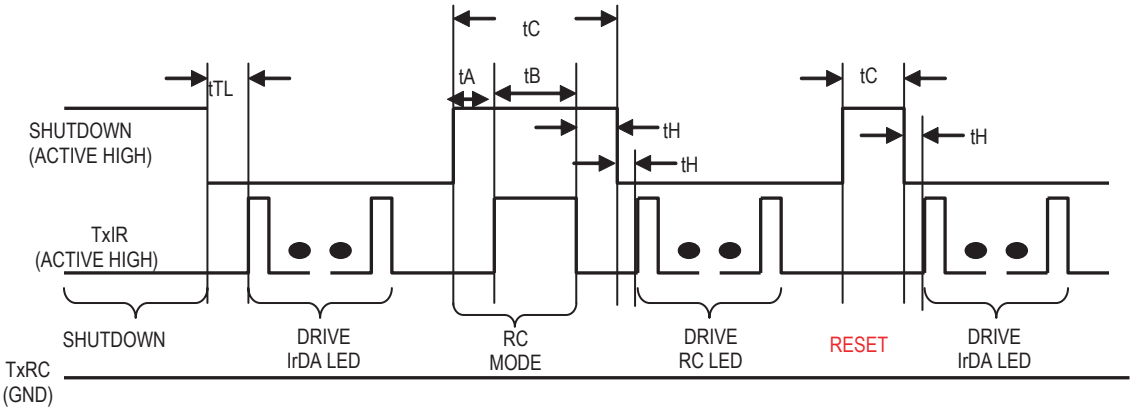
In the two-TxD direct transmission mode, the LED can be driven separately for IrDA and RC mode of operation through the TxD_IR and TxD_RC pins respectively. This mode can be used when the external controller utilizes separate transmit pins for IrDA and RC operation modes, thereby eliminating the need for external multiplexing.

Please refer to the Transceiver I/O truth table for more detail.

Transceiver Control I/O Truth Table for Two-TxD Direct Transmission Mode

| SD | TxIR | TxRC | LED | Remarks |
|---|---|---|---|---|
| 0 | 0 | 0 | OFF | IR Rx enabled. Idle mode |
| 0 | 0 | 1 | ON | Remote control operation |
| 0 | 1 | 0 | ON | IrDA Tx operation |
| 0 | 1 | 1 | - | Not recommended (Both Transmitters off) |
| 1 | 0 | 0 | OFF | Shutdown mode* |

* The shutdown condition will set the transceiver to the default mode (IrDA-SIR)




### Mode Programming Timing Table

The following timings describe input constraints required using the active serial interface for mode programming with pins SD, TxIR, and TxRC:

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Shutdown input pulse width, at pin SD | $t_{SDPW}$ | 30 | - | ∞ | µs | Will activate complete shutdown |
| SD mode setup time | $t_A$ | 200 | - | - | Ns | Setup for mode programming |
| TxIR pulse width for RC mode | $t_B$ | 200 | - | - | Ns | RC drive enabled with pin TxIR |
| SD programming pulse width Note: ( tA + tB ) < tC < tSDPW | $t_C$ | - | - | 5.0 | µs | Pulse width mode programming |
| TxIR setup time for SIR or MIR/FIR mode | $t_S$ | 50 | - | - | Ns | Setup time for IrDA bandwidth selection |
| TxIR or SD hold time to latch SIR, MIR/FIR or RC mode | $t_H$ | 50 | - | - | Ns | Hold time for IrDA or RC modes |

## Bandwidth Selection Timing

The power on state should be the IrDA SIR mode. The data transfer rate must be set by a programming sequence using the TxD_IR and SD inputs as described below.

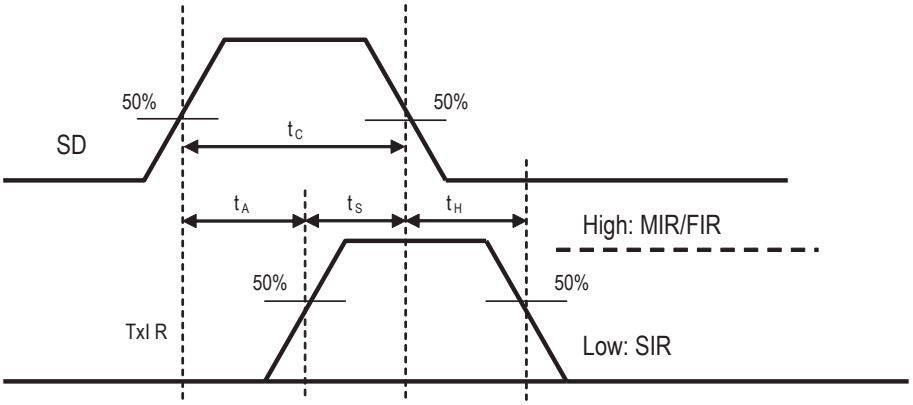
Note: SD should not exceed the maximum, $t_C \leq 5\mu s$, to prevent shutdown.

### Setting to the High Bandwidth MIR/FIR Mode (0.576Mbits/s to 4Mbits/s)

1. Set SD input to logic "HIGH". Wait $t_A \geq 200ns$
2. Set TxD_IR input to logic "HIGH". Wait $t_S \geq 50ns$.
3. Set SD to logic "LOW" (this negative edge latches state of TxD_IR, which determines speed setting).
4. After waiting $t_H \geq 50ns$ TxD_IR can be set to logic "LOW". TxD_IR is now re-enabled as normal IrDA transmit input for the High Bandwidth MIR/FIR mode.

### Setting to the LOW Bandwidth SIR Mode (2.4kbits/s to 115.2kbits/s)

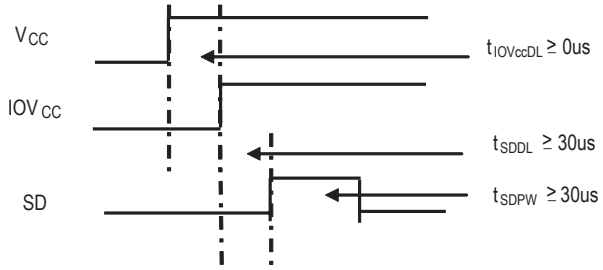
1. Set SD input to logic "HIGH".
2. Set TxIR input to logic "LOW". Wait $t_S \geq 50ns$.
3. Set SD to logic "LOW" (this negative edge latches state of TxIR, which determines speed setting).
4. TxIR must be held for $t_S \geq 50ns$. TxIR is now re-enabled as normal IrDA transmit input for the Low Bandwidth SIR mode.



## Power-Up Sequencing

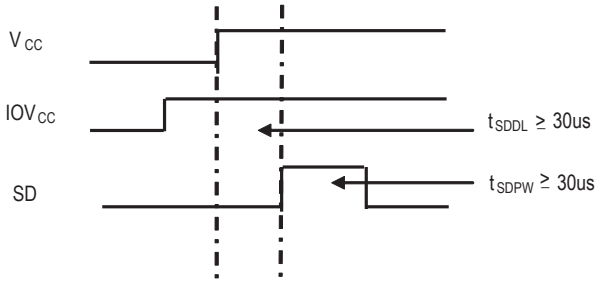
To have a proper operation for ASDL-3023, the following power-up sequencing must be followed.

(a) It's strongly recommended that Vcc must come prior to IOVcc.

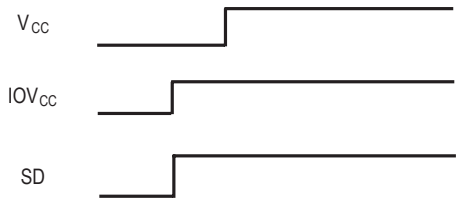



(b) It is not recommended to turn on IOVcc before Vcc while SD is low.

However, for application that IOVcc come prior to Vcc while SD is low, SD pin has to set high to assure proper functionality.




(c) Setting IOVcc high before Vcc while SD is high is forbidden.




Note:

$t_{IOVccDL}$ : IOVcc delay time

$t_{SDDL}$ : SD delay time

$t_{SDPW}$ : Shutdown Input Pulse Width



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