16Mb, 512Kx32 CMOS 5.0V, High Speed Static RAM Integrated Plastic Encapsulated Microcircuit

FEATURES

- Integrated Real-Time Memory Array Solution
  - No latency or refresh fycles
  - Parallel Read/Write Interface
  - User Configurable via multiple enables
- Random Access Memory Array
  - Fast Access Times: 12, 15, 20, and 25ns
  - TTL Compatible I/O
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 JEDEC M0-47AE
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
  - Single +5V (±5%) Supply Operation

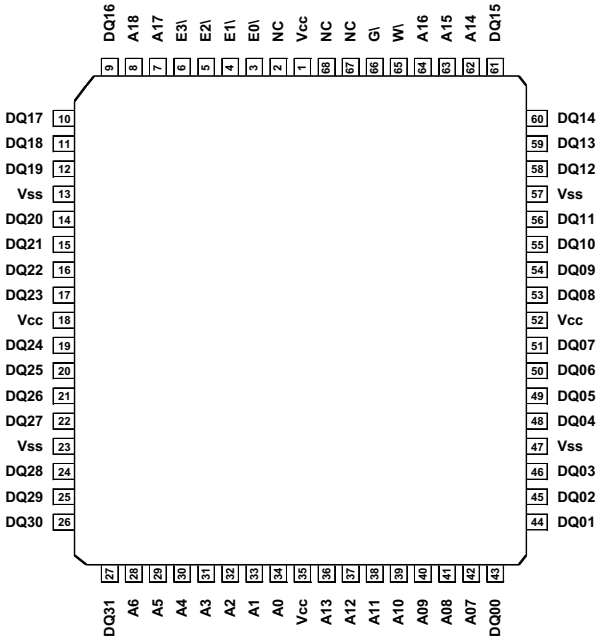
DESCRIPTION

The AS8S512K32 is a high speed, 5V, 16Mb SRAM. The device is available with access times of 12, 15, 20 and 25ns creating a zero wait state/latency, real-time memory solution. The high speed, 5v supply voltage and control lines,make the device ideal for all your real-time computer memory requirements.

The device can be configured as a 512K x 32 and used to create a single chip external data /program memory array solution or via use of the individual chip enable lines, be reconfigured as a 1M x 16 or 2M x 8.

The device provides a 50+% space savings when compared to four 512K x 8, 36 pin SOJs. In addition the AS8S512K32 has only a 20pF load on the Addr. lines vs. ~30pF for four plastic SOJs.

PIN CONFIGURATIONS AND BLOCK DIAGRAM

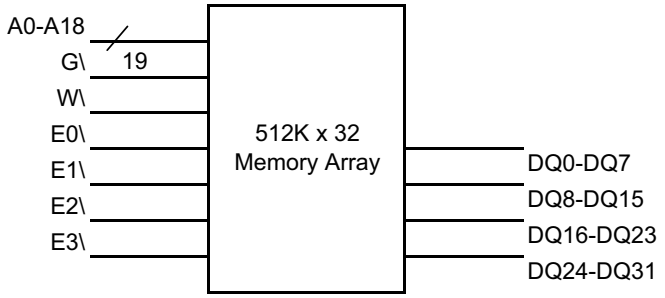


PIN NAMES

A0 - A18	Address Inputs
E0\ - E3\	Chip Enables
W\	Write Enables
G\	Output Enable
DQ0 - DQ31	Common Data Input/Output
Vcc	Power (+5V ± 10%)
Vss	Ground
NC	No Connection

BYTE CONTROL TABLE

Chip Enable	Byte Control
E0\	DQ0-7
E1\	DQ8-15
E2\	DQ16-23
E3\	DQ24-31



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss	-0.5V to 7.0V
Operating Temperature t_A (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	5.0 Watts
Output Current	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those in di cated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.75	5	5.25	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	---	Vcc+0.5V	V
Input Low Voltage	V_{IL}	-0.3	---	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 2

Note: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL=5pF

FIG. 2

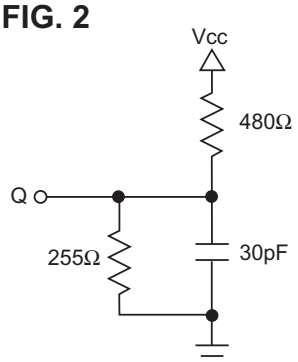
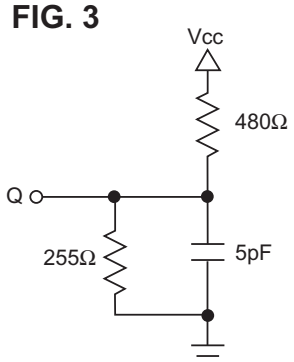


FIG. 3



DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max		Units
				12/15	20/25	ns
Operating Power Supply Current	I_{CC1}	W#=V_{IL}, $I_{I/O}$=0mA, Min Cycle		350	300	mA
Standby (TTL) Power Supply Current	I_{CC2}	E#≥V_{IH}, V_{IN}≤V_{IL} or V_{IN}≥V_{IH}, f=0MHz		120	125	mA
Full Standby Power Supply Current CMOS	I_{CC3}	E#≥V_{CC}-0.2V V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V		20	20	mA
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}		±5		µA
Output Leakage Current	I_{LO}	$V_{I/O}$=0V to V_{CC}		±5		µA
Ouput High Voltage	V_{OH}	I_{OH}=-4.0mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		0.4		V

TRUTH TABLE

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	HIGH Z	I_{CC2}
					I_{CC3}
H	L	H	Output Deselect	HIGH Z	I_{CC1}
L	L	H	Read	D_{OUT}	I_{CC1}
X	L	L	Write	D_{IN}	I_{CC1}

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	CI	20	pF
Data Lines	CD/Q	7	pF
Write & Output Enable Line	W#, G#	20	pF
Chip Enable Line	E0#, E3#	7	pF

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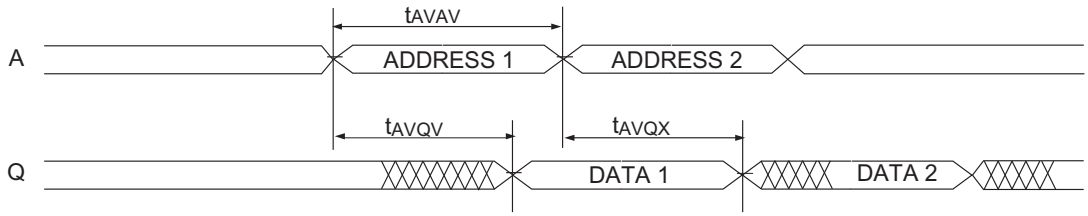
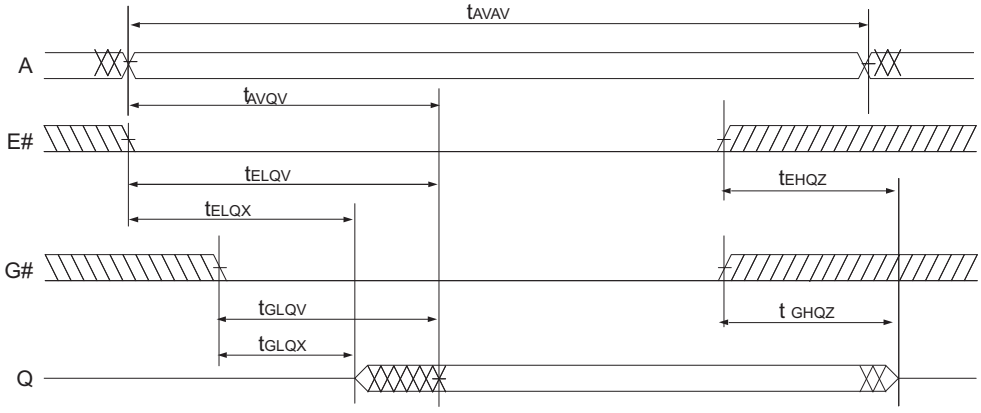
AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		12ns		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AVQV}	t_{AA}		12		15		20		25	ns
Chip Enable Access	t_{ELQV}	t_{ACS}		12		15		20		25	ns
Chip Enable to Output in Low Z	t_{ELQX}	t_{CLZ}	3		3		3		3		ns
Chip Disable to Output in High Z	t_{EHQZ}	t_{CHZ}		6		7		9		9	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		6		7		9		9	ns
Output Enable to Output in Low Z	t_{GLQX}	t_{OLZ}	0		0		0		0		ns
Output Enable to Output in High Z	t_{GHQZ}	t_{OHZ}		6		7		9		9	ns

READ CYCLE 1 - W\ HIGH, G\, E\ LOW



READ CYCLE 2 - W\ HIGH



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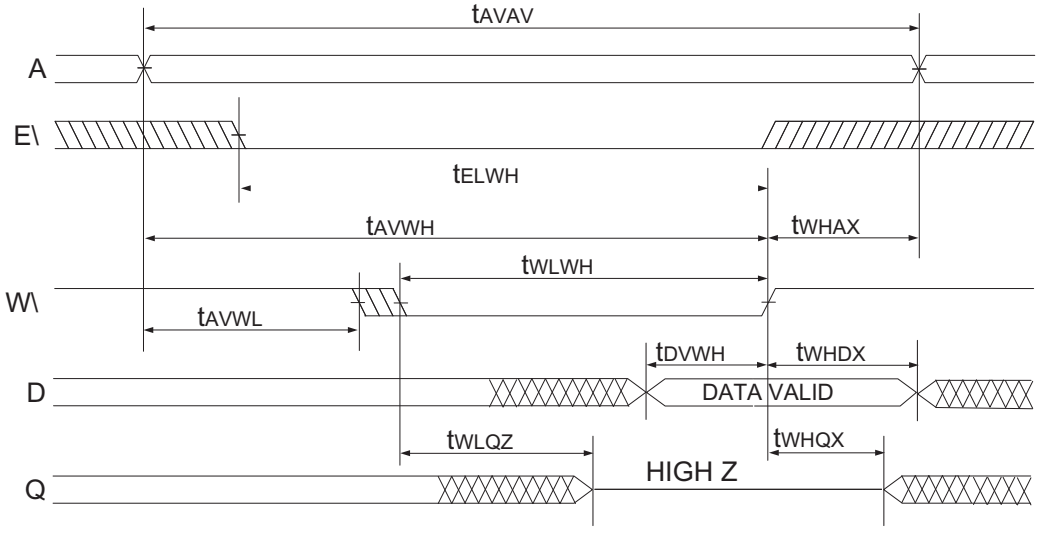
AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		12ns		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	12		15		20		25		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	8		10		11		12		ns
	t_{ELEH}	t_{CW}	8		10		11		12		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	8		10		11		12		ns
	t_{AVEH}	t_{AW}	8		10		11		12		ns
Write Pulse Width	t_{WLWH}	t_{WP}	8		10		11		12		ns
	t_{ELEH}	t_{WP}	10		12		13		14		
Write Recovery Time	t_{WHAZ}	t_{WR}	0		0		0		0		ns
	t_{EHAZ}	t_{WR}	0		0		0		0		
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		ns
	t_{EHDZ}	t_{DH}	0		0		0		0		
Write to Output in High Z	t_{WLQZ}	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time	t_{DVWH}	t_{DW}	6		7		8		9		ns
	t_{DVEH}	t_{DW}	6		7		8		9		
Output Active from End of Write	t_{WHQX}	t_{WLZ}	3		3		3		3		

WRITE CYCLE 1 - W\ CONTROLLED



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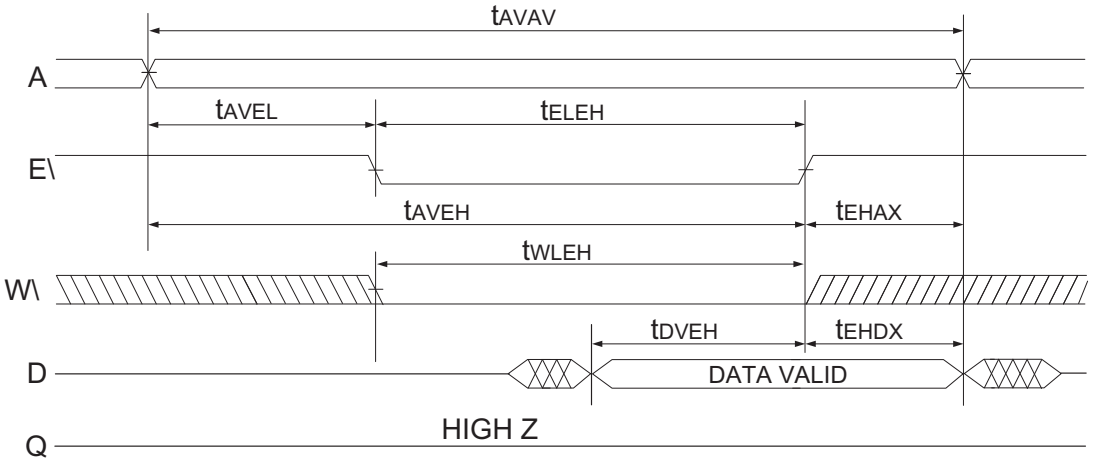
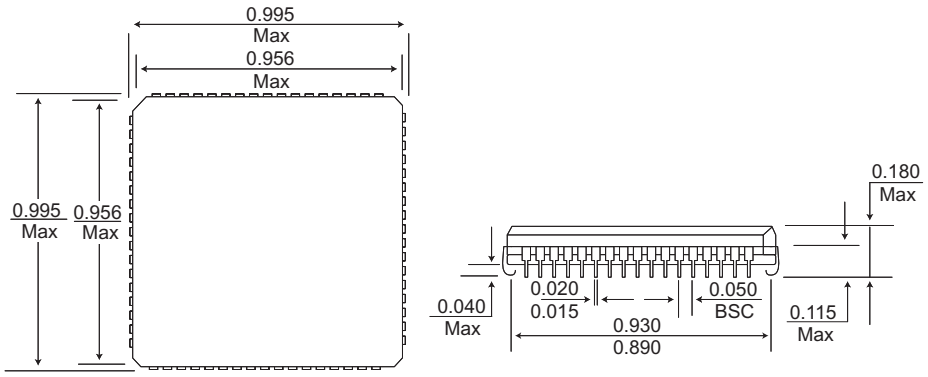
WRITE CYCLE 2 - E\ CONTROLLED



PACKAGE DRAWING

Package No. 99
68 Lead PLCC
JEDEC MO-47AE



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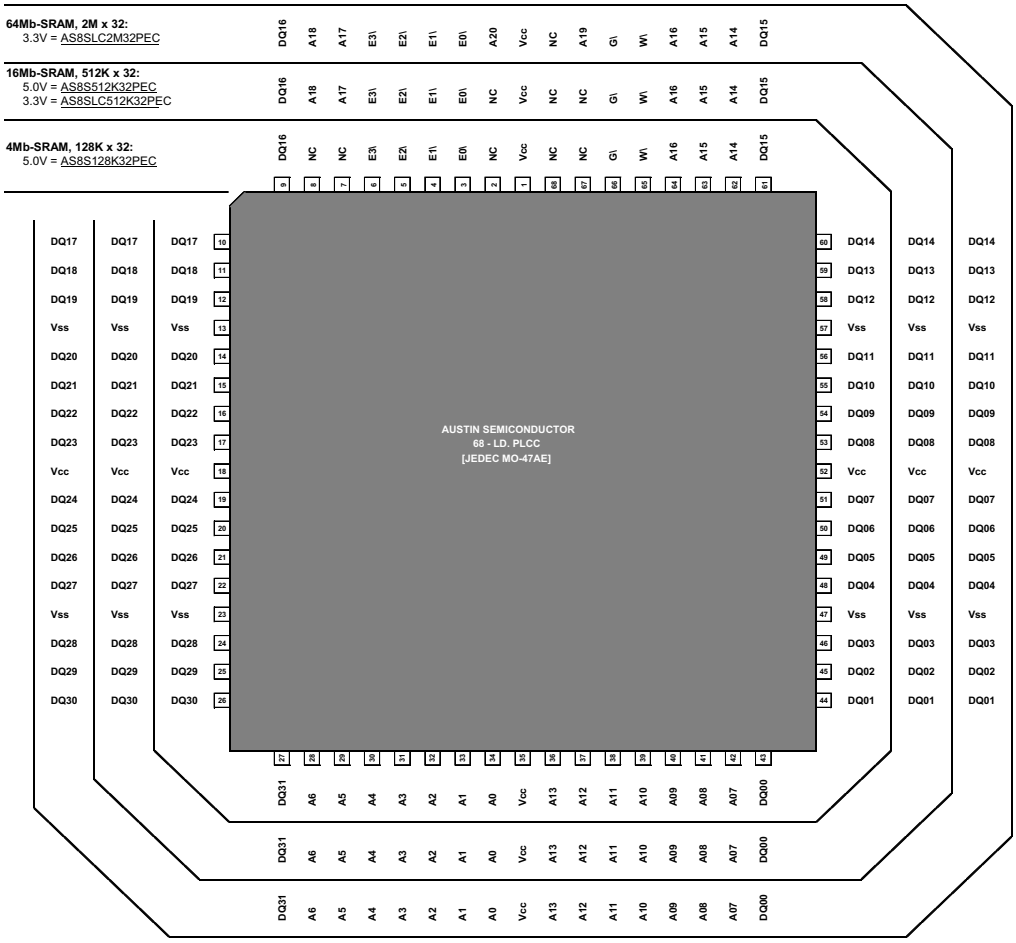
ORDERING INFORMATION

Part Number	Access Speed	Device Grade	Availability
AS8S512K32PEC-MS	NA	Mechanical Sample	SEPTEMBER 2006
AS8S512K32PEC-ES	NA	Engineering Sample	OCTOBER 2006
AS8S512K32PEC-12/IT	12ns	INDUSTRIAL	NOVEMBER 2006
AS8S512K32PEC-15/IT	15ns	INDUSTRIAL	NOVEMBER 2006
AS8S512K32PEC-20/IT	20ns	INDUSTRIAL	NOVEMBER 2006
AS8S512K32PEC-25/IT	25ns	INDUSTRIAL	NOVEMBER 2006
AS8S512K32PEC-12/ET	12ns	ENHANCED	NOVEMBER 2006
AS8S512K32PEC-15/ET	15ns	ENHANCED	NOVEMBER 2006
AS8S512K32PEC-20/ET	20ns	ENHANCED	NOVEMBER 2006
AS8S512K32PEC-25/ET	25ns	ENHANCED	NOVEMBER 2006
AS8S512K32PEC-12/XT	12ns	MIL-TEMP	**CF**
AS8S512K32PEC-15/XT	15ns	MIL-TEMP	NOVEMBER 2006
AS8S512K32PEC-20/XT	20ns	MIL-TEMP	NOVEMBER 2006
AS8S512K32PEC-25/XT	25ns	MIL-TEMP	NOVEMBER 2006

FAMILY PIN MATRIX



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DOCUMENT TITLE

16Mb, 512K x 32, SRAM, 5.0V, 0.990”sq. - 68 LD. PLCC, Multi-Chip Package [iPEM]

REVISION HISTORY

Rev #	History	Release Date	Status
0.0	Initial Release	September 2005	Advance
0.1	Updated Order Chart	January 2009	Advance