high performance needs great design.

Datasheet: AS8650B High-efficient Power Management Device with High-speed CAN Interface

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AS8650B

High-efficient Power Management Device with High-speed CAN Interface

1 General Description

The AS8650B is a companion IC which combines power management functions and a fully conforming high-speed CAN Transceiver in one high performance analog device for automotive applications. The AS8650B is powered by the battery, provides 4 output voltage levels of which 3 outputs in the range of 1.8V to 3.3V with a maximum current consumption up to 120mA at the LDO voltage regulator outputs. An integrated DCDC converter with a very high efficiency for the 5V output supplies the 3 voltage regulators and ensures a voltage stability of ±2.5%. The combination of DCDC converter with low-drop-out voltage regulators makes the AS8650B suitable for all Automotive Control Units where power efficiency is a must.

The AS8650B provides a high-speed CAN interface up to 1Mbps communication rate conforming to ISO 11898-5. The AS8650B provides wake-up via remote wake-up at CAN bus lines and a local wake pin. The watchdog unit provides three different timing functions: start-up, window- and timeout watchdog; configurable via the SPI and I²C interface.

Voltage monitoring is implemented for the battery supply, DCDC output and the 3 LDO regulator outputs. Undervoltage will be signalled on the INTN pin to the microcontroller. All diagnostics and status flags can be accessed with the SPI interface.

The product is available in a 36-pin QFN (6x6x0.9) package.

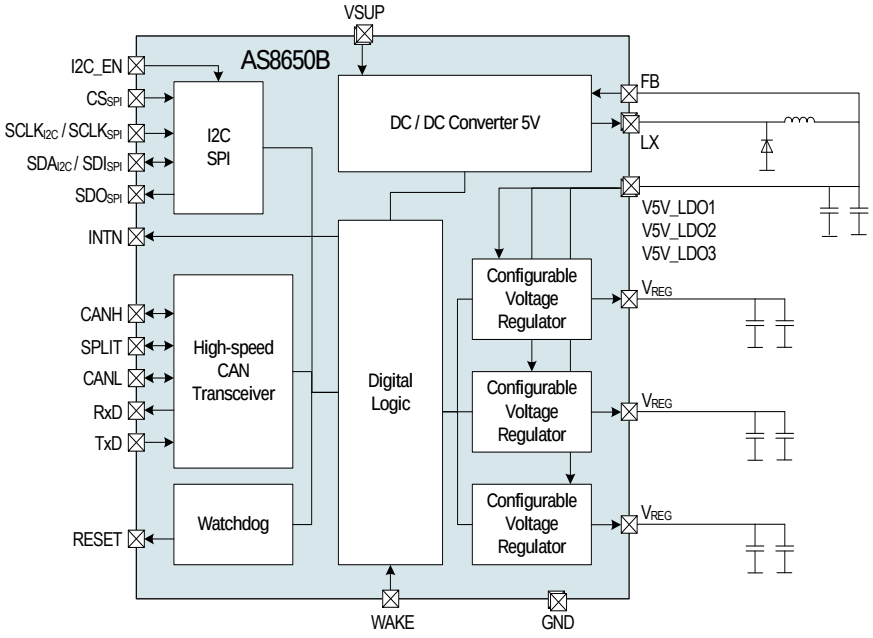
2 Key Features

- DCDC converter for 5V output with very high efficiency
- Three voltage regulators providing 3.3V, 2.8V and 1.8V with accuracy better than 2.5% (Two are adjustable through factory settings).
- High-speed CAN interface (ISO 11898-5) with remote wake-up
- Comprehensive voltage monitoring
- Configurable watchdog functions for start-up, operation, and standby
- Automatic thermal shutdown protection
- Excellent EMC performance with outstanding switching technology for the DCDC converter
- Ambient temperature range from -40°C to +105°C in maximum load conditions
- Lead-free 36-pin QFN (6x6x0.9) package

3 Applications

The AS8650B provides high efficient and flexible power supply together with state-of-the-art high-speed CAN Interface for automotive control units.The device is pin compatible with AS8550 (LIN interface) in order to change from CAN to LIN easy.

Figure 1. AS8650B Block Diagram



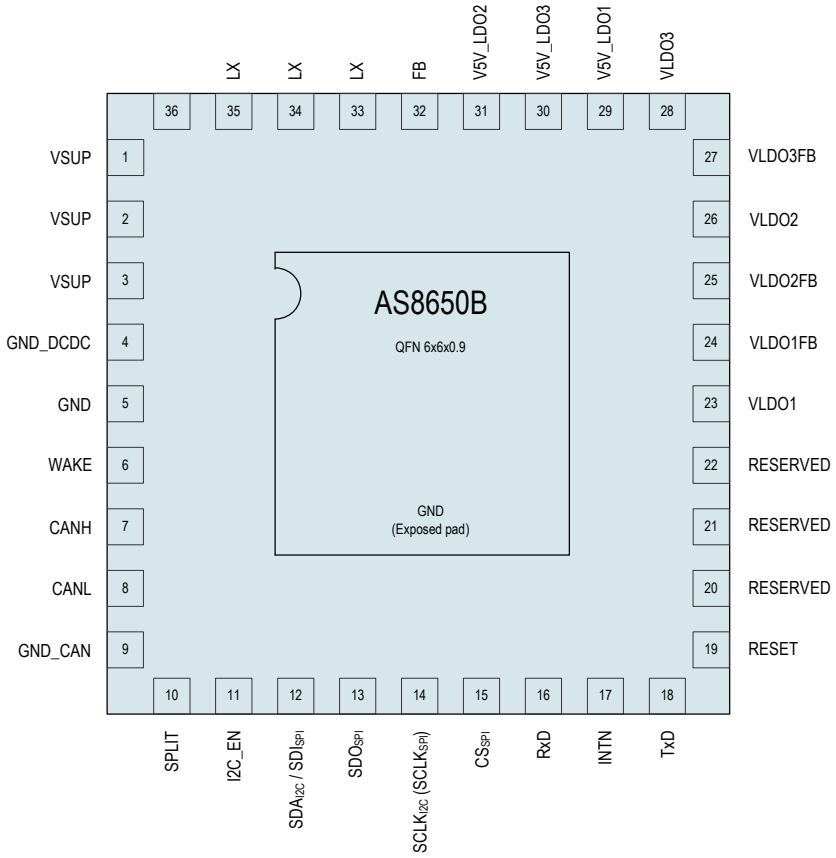
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4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin	Pin Name	Pin Type	Description
1, 2, 3	VSUP	Power Supply Input	Power Supply
4	GND_DCDC		
5	GND		
6	WAKE	Analog Input / Output high-voltage	Local wake request (high-voltage input)
7	CANH		High level CAN bus line
8	CANL		Low level CAN bus line
9	GND_CAN	Power Supply Input	Power supply
10	SPLIT	Analog Input / Output high-voltage	Common-mode stabilization output

Table 1. Pin Descriptions

Pin	Pin Name	Pin Type	Description
11	I2C_EN	Digital Input	I²C/SPI select signal (High = I²C, Low = SPI)
12	SDA_{I2C} / SDI_{SPI}	Digital Input/Output / Digital Input	Unidirectional for SPI, Bidirectional for I²C
13	SDO_{SPI}	Digital Output	SPI data out
14	$SCLK_{I2C}$ / $SCLK_{SPI}$	Digital Input	Serial clock (Multiplexed for I²C and SPI) unidirectional
15	CS_{SPI}	Digital input with pull-up	SPI chip select
16	RxD	Digital output with pull-up	CAN Transceiver receive signal
17	INTN	Digital Output	Active low interrupt to µC. Generated if status / diagnostic is updated.
18	TxD	Digital input with pull-up	CAN Transceiver transmit signal
19	RESET	Digital Output	Digital Output referenced to VLDO1, active low
20	Reserved	Pin with Digital / Analog Input / Open-Drain-Output	Reserved
21		Analog Input / Output	
22			
23	VLDO1	Power Supply Input	Regulated voltage output
24	VLDO1FB	Pin with Digital / Analog Input / Open-Drain-Output	Regulated voltage feedback
25	VLDO2FB	Pin with Digital / Analog Input / Open-Drain-Output	Regulated voltage feedback
26	VLDO2	Power Supply Input	Regulated voltage output
27	VLDO3FB	Pin with Digital / Analog Input / Open-Drain-Output	Regulated voltage feedback
28	VLDO3	Power Supply Input	Regulated voltage output
29	V5V_LDO1		Step-down converter 5V output, supply for LDO1
30	V5V_LDO3		Step-down converter 5V output, supply for LDO3
31	V5V_LDO2		Step-down converter 5V output, supply for LDO2
32	FB (DCDC)	Analog Input	DCDC output voltage feedback
33, 34, 35	LX (DCDC)	Power Supply Input	DCDC output
0	GND		Exposed pad (GND)

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings[1]

Parameter	Min	Max	Units	Notes
Electrical Parameters				
Voltage at positive supply pin (V_{VSUP})	-0.3	40	V	
Voltage at pin V5V_LDO1, V5V_LDO2, V5V_LDO3, VLDO1, VLDO2, VLDO3, FB, VLDO1FB, VLDO2FB, VLDO3FB	-0.3	7	V	
Voltage at pin CANH, CANL, SPLIT	-40	+40	V	
Voltage at pin LX, WAKE	-0.3	V_{VSUP} + 0.3	V	
Voltage at pin RESET, INTN, RxD, TxD, CS, SCLK, SDO, SDA/SDI, I2C_EN	-0.3	4.5	V	
Input Supply slew-rate (V_{sup_slew})		1	V/µs	Input power supply ramp rate
Electrostatic Discharge				
Electrostatic discharge voltage AEC-Q100-002 human body model standard (ESD)	±2		kV	All pins except VSUP, GND, CANH, CANL, WAKE, SPLIT
	±4			VSUP, GND, WAKE, SPLIT
	±8			CANH, CANL
Latch-Up Immunity	-100	+100	mA	AEC-Q100-004
Continuous Power Dissipation				
Maximum power dissipation (P_{tot})		1.2	W	
Temperature Ranges and Storage Conditions				
Junction temperature (T_J)		170	°C	
Storage temperature (T_{stg})	-55	+150	°C	
Thermal resistance MLF package (R_{thj_36})		30	°C/W	SEMI G42-88
Package body temperature (T_{BODY})		260	°C	*The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

1. All voltages mentioned above are referred with respect to ground reference voltage V_{GND}.

6 Electrical Characteristics

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions						
V_{SUP}	Positive supply voltage	Normal operating condition	6		18	V
GND	Ground	In reference to all the voltages	0			V
T_{AMB}	Ambient temperature	Junction temperature (T_J) ≤ 150ºC (at full-load)	-40		105	ºC
I_{supp}	Supply current, Normal mode	VSUP = 6V, LDOs at full load, DCDC load = 390mA, CAN dominant		425		mA
		VSUP = 18V, LDOs at full load, DCDC load = 390mA, CAN dominant, not production tested.		150		
		VSUP = 16V, LDOs at full load, CAN dominant		170		
CS						
Vt-	Negative-Going Threshold	VLDO1 = 3.3V	1.12		1.52	V
Vt+	Positive-Going Threshold		1.77		2.23	V
I_{iil_cs}	Pull up current	In CS pad, Pulled up to VLDO1	-60		-15	µA
SDO						
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage	VSUP ≥ 6V			0.4	V
I_O	Output drive current				4	mA
SDA / SDI						
V_{IH}	High level input voltage		0.7* VLDO1			V
V_{IL}	Low level input voltage				0.3* VLDO1	V
V_{OL}	Low level output voltage				0.4	V
SCLK						
V_{IH}	High level input voltage	Open-drain, external 500Ω pull-up	0.7* VLDO1			V
V_{IL}	Low level input voltage				0.3* VLDO1	V
RESET, INTN						
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage	VSUP ≥ 6V			0.4	V
I_O	Output drive current				4	mA
TxD						
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_O	Output drive current	VSUP ≥ 6V			1	mA
I_{iil}	Pull-up current	TxD pulled up to VLDO1 with control RxD pulled up to VLDO1	-60		-15	µA

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RxD						
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output drive current	VSUP ≥ 6V			1	mA
I_{lil}	Pull-up current	TxD pulled up to VLDO1 with control RxD pulled up to VLDO1	-60		-15	µA

6.1 Electrical System Specification

-40°C < T_J < 150°C

Table 4. Electrical System Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IDDnom	Current consumption Normal mode	No load, VSUP = 12V, CAN recessive		3.5	6	mA
IDDrecv	Current consumption Receive-only mode	No load, VSUP = 12V, CAN recessive		1	2	mA
IDDstby	Current consumption Standby mode	No load, VSUP = 12V		135	270	µA
IDDsleep	Current consumption Sleep mode	No load, VSUP = 12V		75	150	µA

6.2 DCDC Converter

-40°C < T_J < 150°C; all voltages are with respect to ground, normal operating mode, unless otherwise mentioned.

Table 5. DCDC Converter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSUP	Battery Voltage Range		6	12	18	V
V5V	Output Voltage	For inductor 22µH and capacitor 100µF	4.75	5	5.25	V
I_{LXS}	LX current limit		0.8	1	1.25	A
I_{V5V}	DCDC output current				500	mA
R_{ON}	LX switch on-resistance	(bondwire resistance included)		0.8	1	Ω
V_{FB}	Reference Voltage for FB		4.75	5	5.25	V
Lireg_dc	Line regulation	Step from V_{IN} = 6V to V_{IN}2 = 18V, I_{LOAD} = 100mA Lireg = 100*(V_{OUT}1-V_{OUT}2) / [V_{OUT}2*(V_{IN}1-V_{IN}2)]	-0.1		+0.1	% / V
Loreg_dc	Load regulation	I_{LOAD} step from 90mA to 10mA VSUP = 12V Loreg = 100*(V_90mA-V_10mA) / V_90mA	-0.9		+0.9	%
LX_ind	Output inductor		10		22	µH
V5V_cer1	Output ceramic capacitor 1		10		100	µF
V5V_esr1	ESR of ceramic capacitor 1		0		0.05	Ω
V5V_cer2	Output ceramic capacitor 2	X7R type	100		220	nF
V5V_esr2	ESR of ceramic capacitor 2				0.01	Ω
Csup	Input capacitor (ceramic)	For EMC suppression	22		100	µF
Csup_esr					1	Ω

6.3 Low Drop Out Regulators

-40°C < Tj < 150°C; all voltages are with respect to ground, normal operating mode, unless otherwise mentioned. The LDO block is a linear voltage regulator, which provides a regulated (band-gap stabilized) output voltage from the DCDC converter output voltage (V5V).

Table 6. VLDO1 Block Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V5V	Input Voltage Range		4.75	5	5.25	V
$I_{OUTLDO1}$	Output current	Guaranteed by design. Not production tested.	0		100	mA
VLDO1	Output Voltage Range		3.217	3.3	3.383	V
ICC_SH	Output Short Circuit Current	Normal mode			300	mA
dVLDO1	Line Regulation	ΔVLDO1 / ΔV5V (static) for the input range, I_{LOAD} = 100mA	-8		8	mV/V
LOREG_NM	Load Regulation	ΔVLDO1 (for 100mA > I_{LOAD} > 1mA), V5V = 5V	-0.15		+0.15	mV/mA
CL2	Output Capacitor (Ceramic)	X7R type	2		5	µF
ESR2			0.02		0.1	Ω
CL1		X7R type	100		220	nF
ESR1					0.01	Ω

Table 7. VLDO2[1] Block Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V5V	Input Voltage Range		4.75	5	5.25	V
IOUTLDO2	Output current	Guaranteed by design. Not production tested.	0		120	mA
VLDO2	Output Voltage Range	V_{OUT} (typ) depends on the trim code as in OTP register mapping. Default code gives 2.8V	0.975* V_{OUT}	V_{OUT}	1.025* V_{OUT}	V
ICC_SH	Output Short Circuit Current	Normal mode			300	mA
dVLDO2	Line Regulation	ΔVLDO2 / ΔV5V (static) for the input range, I_{LOAD} = 100mA	-8		8	mV/V
LOREG_NM	Load Regulation	ΔVLDO2 (for 120mA > I_{LOAD} > 1mA)	-0.15		+0.15	mV/mA
CL2	Output Capacitor (Ceramic)	X7R type	2		5	µF
ESR2			0.02		0.1	Ω
CL1		X7R type	100		220	nF
ESR1					0.01	Ω

1. Factory setting: V_{OUT} = 2.8V.

Table 8. VLDO3[1] Block Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V5V	Input Voltage Range		4.75	5	5.25	V
$I_{OUTLDO3}$	Output current	Guaranteed by design. Not production tested.	0		100	mA
VLDO3	Output Voltage Range	VOUT (typ) depends on the trim code as in OTP register mapping. Default code gives 1.8V	0.975* VOUT	VOUT	1.025* VOUT	V
ICC_SH	Output Short Circuit Current	Normal mode			300	mA
dVLDO3	Line Regulation	ΔVLDO3 / ΔV5V (static) for the input range, ILOAD = 100mA	-8		8	mV/V
LOREG_NM	Load Regulation	ΔVLDO3 (for 100mA > ILOAD > 1mA)	-0.15		+0.15	mV/mA
CL2	Output Capacitor (Ceramic)	X7R type	2		5	µF
ESR2			0.02		0.1	Ω
CL1		X7R type	100		220	nF
ESR1					0.01	Ω

1. Factory setting: VOUT = 1.8V.

6.4 CAN Transceiver

6V < VSUP < 18V; -40°C < Tj < 150°C; all voltages are with respect to ground; 4.75V < V5V_LDO1 < 5.25V; RL=60Ω.

Table 9. DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver						
CANH_dom	Dominant output voltage	V_TxD = 0V	3		4.25	V
CANL_dom			0.5		1.75	V
VO_dom_m	Matching dominant output voltage V5V_LDO1-V_CANH-V_CANL		-0.1		0.15	V
VO_diff	Differential output voltage V_CANH-V_CANL	45Ω < RL < 60Ω, V_TxD = 0V (dominant)	1.5		3	V
		No load; V_TxD = VLDO1 (recessive)	-50		50	mV
VO_rec	Recessive output voltage V_CANH, V_CANL	V_TxD = VLDO1; No bus load, Normal mode	2		3	V
		No bus load, Standby mode	-0.1		0.1	V
IO_short	Short circuit output current	V_TxD = 0V, V_CANH = 0V	-160		-50	mA
		V_TxD = 0V, V_CANL = 40V	+50		+160	mA
IO_rec	Recessive output current	-27V < V_CAN < 40V	-2.5		+2.5	mA
Receiver						
V_RxD_th	Differential receiver threshold voltage	-12V < V_CANH < 12V -12V < V_CANL < 12V Receive-only mode (CAN receiver)	0.5		0.9	V
		-12V < V_CANH < 12V -12V < V_CANL < 12V Standby mode (low-power receiver)	0.4		1.15	V

Table 9. DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_RxD_hys	Differential receiver hysteresis voltage	-12V < V_CANH < 12V -12V < V_CANL < 12V Receive-only mode (CAN receiver)	20		130	mV
I_RxD_LEAK	Input leakage current	V5V_LDO1 = 0V; V_CANH = V_CANL = 5V	100		250	µA
R_IN_cm	Common mode input resistance	Tested in Receive-only mode	15		35	kΩ
R_IN_cm_m	Common mode input resistance matching	V_CANH = V_CANL (Tested in Receive-only mode)	-3		+3	%
R_IN_diff	Differential input resistance	Tested in Receive-only mode	25		75	kΩ
VO_SPLIT	Output voltage on **SPLIT** pin	Normal mode -500µA < I_SPLIT < 500µA	0.3* V5V_LDO1		0.7* V5V_LDO1	V
IL_SPLIT	Leakage current on **SPLIT** pin	Standby mode 0V < V_SPLIT < 35V (Not production tested)	-5		+5	µA
		Standby mode -22V < V_SPLIT < 0 (Not production tested)	-1		+1	mA

Table 10. AC Electrical Characteristics

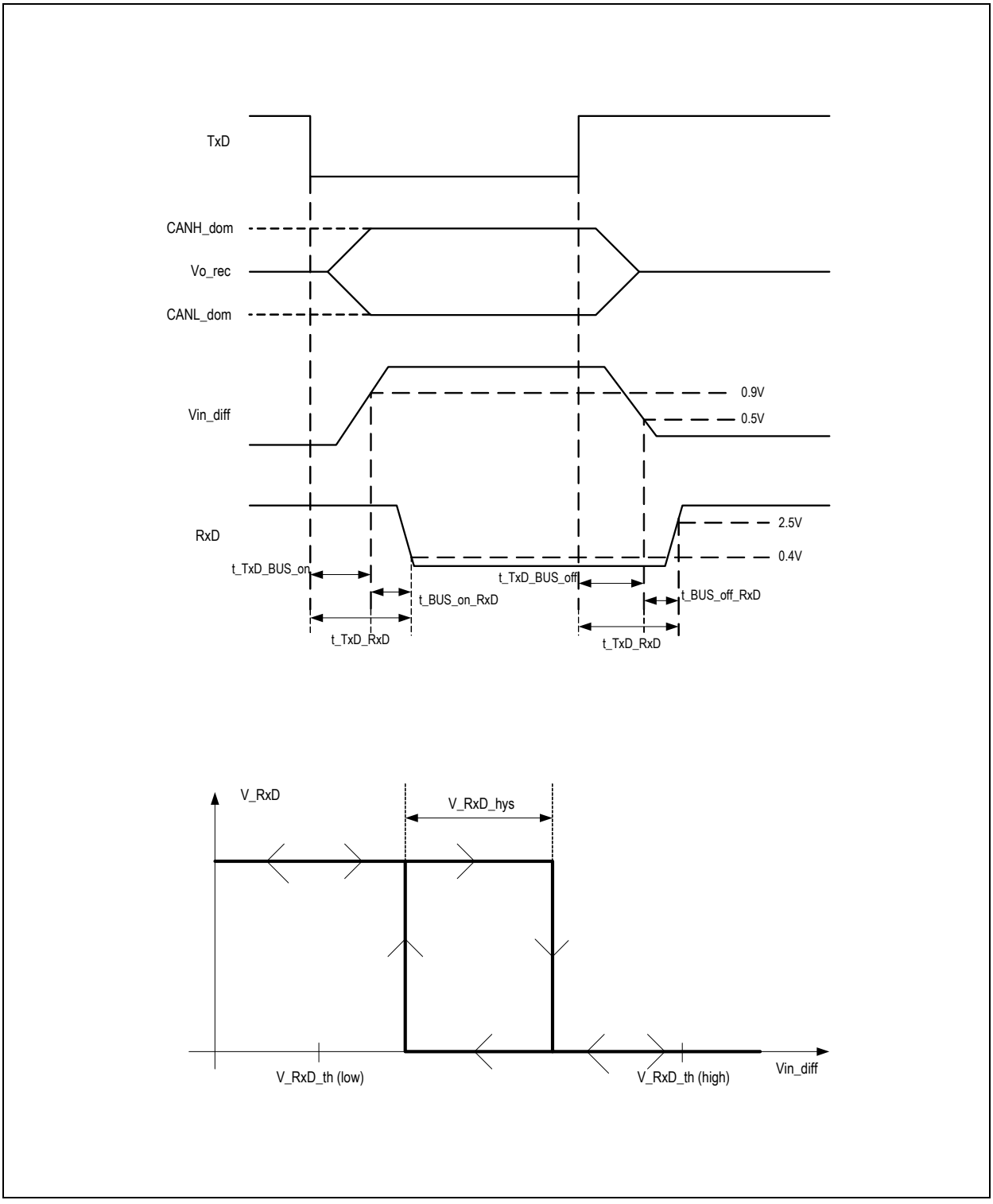
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_TxD_BUS_on	Delay TxD to bus dominant		10		110	ns
t_TxD_BUS_off	Delay TxD to bus recessive		10		140	ns
t_BUS_on_RxD	Delay bus dominant to RxD		15		115	ns
t_BUS_off_RxD	Delay bus recessive to RxD		20		160	ns
t_TxD_RxD	Propagation Delay TxD to RxD		40		255	ns
WAKE UP via BUS						
t_BUS_WR	Dominant time for wake-up detection via bus		0.75		5	µs
BUS Diagnostic						
t_OC_CANH	Time to detect over current CANH	V_TxD = 0V, V_CANH = 0V (Not production tested)	60			µs
t_LC_CANH	Time to detect low current CANH	V_TxD = 0V, V_CANH = 40V (Not production tested)	60			µs
t_OC_CANL	Time to detect over current CANL	V_TxD = 0V, V_CANL = 40V (Not production tested)	60			µs
t_LC_CANL	Time to detect low current CANL	V_TxD = 0V, V_CANL = 0V (Not production tested)	60			µs

Table 11. Temperature Limiter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{jshut}	Shut down temperature	Junction temperature when IC shuts down	150	170	185	ºC
T_{jrecv}	Recovery temperature	Junction temperature below which state machine returns from shutdown / warning	125	140	155	ºC
T_{jwarn}	Over-temperature warning flag set	Junction temperature beyond which the warning flag is set	140	157	175	ºC

6.4.1 Timing Diagrams

Figure 3. Timing Diagram and Hysteresis of CAN Receiver



6.5 Undervoltage Detection

Table 12. Undervoltage Detection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSUP_POR	VSUP Power on Reset threshold on	Rising edge of VSUP	5.09	5.5	5.91	V
VSUP_RESET	VSUP Power on Reset threshold off	(Master Reset for Device)	4.49	4.85	5.21	V
VSUP_POKTH	VSUP undervoltage threshold off	VSUP rising edge (Brown out reset threshold)	4.95	5.35	5.75	V
VSUP_UVTH	VSUP undervoltage threshold on (CAN bus in recessive state)	VSUP falling edge (Brown out reset threshold)	4.625	5.0	5.375	V
V5V_POKTH	V5V undervoltage threshold off	Rising edge of V5V	4.16	4.5	4.84	V
V5V_UVTH	V5V undervoltage threshold on	Falling edge of V5V	3.8	4.1	4.4	V
VLDO_POKTH	LDO undervoltage threshold off (VLDO1, VLDO2 and VLDO3)	Percent value is with respect to LDO output. Rising edge of LDO	87	89	91	%
VLDO_UVTH	LDO undervoltage threshold on (VLDO1, VLDO2 and VLDO3)	Percent value is with respect to LDO output. Falling edge of LDO	78	80	82	%
t_{rr}	Spike filter on VLDO1	To remove disturbance	2	4	8	µs
t_{Res}	Reset delay time		4	8	12	ms

6.6 Digital Timing Specification

SPI Protocol.

Table 13. SPI Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
BR_{SPI}	Bit rate				1	Mbps
T_{SCLKH}	Clock high time		500			ns
T_{SCLKL}	Clock low time		500			ns
Write Operation Parameters						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		10			ns
T_{CSH}	CS hold time		40			ns
Read Operation Parameters						
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus			80	ns
Timing Parameters for SCLK Polarity Identification						
t_{CPS}	Clock setup time (CLK polarity)	Setup time of SCLK with respect to CS falling edge	20			ns
t_{CPHD}	Clock hold time (CLK polarity)	Hold time of SCLK with respect to CS falling edge	20			ns

I²C Protocol. Electrical characteristics of SDA & SCLK bus lines for F/S mode

Table 14. I²C Electrical Parameters

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
V_{IL}	Low level input voltage: VLDO1related input levels		0.3V*LDO1		0.3V*LDO1	V
V_{IH}	High level input voltage: VLDO1-related input levels	0.7V*LDO1		0.7V*LDO1		V
V_{hys}	Hysteresis of Schmitt trigger input	n/a	n/a	0.05V*LDO1		V
V_{OL1}	Low level output voltage (open drain or open collector) at 3mA sink current		0.4		0.4	V
t_{of}	Output fall time from VIHmin to VILmax with a bus capacitance from 10pF to 400pF		250 (see Footnote 2)	20 + 0.1Cb (see Footnote 1)	250 (see Footnote 2)	ns (lab tested only)
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	n/a	n/a		50	ns
I_i	Input current of each I/O pin with an input voltage between 0.1VLDO1 and 0.9VLDO1 maximum	-10	10	-10 (see Footnote 3)	10 (see Footnote 3)	µA
C_i	Capacitance for each I/O pin		10		10	pF (guaranteed by design)

1. Cb = capacitance of one bus line in pF.
2. The maximum t_f for the SDA and SCLK bus lines quoted in Table 15 (300ns) is longer than the specified maximum t_{of} for the output stages (250ns). This allows for any series protection resistors to be connected between the SDA/SCLK pins and the SDA/SCLK bus lines without exceeding the maximum specified t_f.
3. I/O pins of Fast-mode devices must not obstruct the SDA and SCLK lines if VLDO1 is switched off.

Characteristics of the SDA and SCLK Bus Lines for F/S Mode I²C Bus.

Table 15. I²C Timing Parameters

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max (see Footnote 1)	
f_{SCLK}	SCLK clock frequency	0	100	0	400	kHz
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4	-	0.6	-	µs
t_{LOW}	Low period of the SCLK clock	4.7	-	1.3	-	µs
t_{HIGH}	High period of the SCLK clock	4.0	-	0.6	-	µs
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
t_{SU_DAT}	Data set-up time	250	-	100 (see Footnote 2)	-	ns
t_{HD_DAT}	Data hold-time	0 (see Footnote 5)	3450 (see Footnote 3)	0 (see Footnote 5)	900 (see Footnote 3)	ns
t_r	Rise time of SDA and SCLK signals	-	1000	20+ $0.1C_b$ (see Footnote 4)	300	ns
t_f	Fall time of SDA and SCLK signals	-	300	20+ $0.1C_b$ (see Footnote 4)	300	ns
t_{SU_STO}	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
V_{nL}	Noise margin at the Low level for each connected device (including hysteresis)	0.1V*LDO1	-	0.1V*LDO1	-	
V_{nH}	Noise margin at the High level for each connected device (including hysteresis)	0.2V*LDO1	-	0.2V*LDO1	-	

1. All values referred to V_{IHmin} and V_{Ilmax} levels (see Table 14).
2. A fast mode I²C bus device can be used in Standard mode I²C bus system, but the requirement $t_{SU_DAT} \geq 250ns$ must then be met. This will automatically be the case if the device do not stretch the low period of the SCLK signal. If such a device does stretch the low period of the SCLK signal, it must output the next data bit to the SDA line t_{rmax}. $T_{SU_DAT} = 1000 + 250 = 1250ns$ (according to standard mode I²C bus specification) before the SCLK line released.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCLK signal.
4. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 14 allowed.
5. This device internally provides a hold time of at least 300ns for the SDA signal to bridge the undefined region of the falling edge of the SCLK.

6.6.1 System Specification and Timings

Table 16. System Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Mode Transition Related Timing						
T_{POST}	Power-up to Standby mode	Reset time included, Start-up watchdog not included			70	ms
T_{STNO}	Standby to Normal mode				10	ms
T_{SLST}	Sleep to Standby mode	Reset time included			50	ms
Wake-up Timing						
Tdom(wake)	Minimum dominant pulse for CAN wake-up detection (remote wake)		5			µs
Trec(wake)	Minimum recessive pulse for CAN wake-up detection (remote wake)		5			µs
TL_wake	Time between edge on WAKE pin to local wake detection			32		µs
TLW_filter	Time between edge on WAKE pin to WAKE_LOCAL signal (Filter on WAKE pin)		0.75		5	µs
TR_wake	Remote wake detection time from the valid pattern detection			24		µs
TINTN	INTN pin high time		7			µs
V_LWUTH	Local WAKE threshold input		2		4	V
Local Failure Related Timing						
TTxDC(dom)	TxD dominant timeout period		600	1000	1400	µs
TBUSC(dom)	BUS dominant clamping timeout period		600	1000	1400	µs
Watchdog Timing & Timeouts						
TWD(init)	Start-up Watchdog timeout (initialization time)			300		ms
Twd_trig	Window watchdog Trigger window	Twwd_period is defined in WWD register	0.375	0.5	0.625	Twwd_period

7 Detailed Description

The AS8650B consists of the following components on chip:

- DCDC converter with 5V outputs that supplies the three LDO voltage regulators and the CAN Transceiver
- Three voltage regulators with output voltages 3.3V, 2.8V and 1.8V and output accuracy up to 2.5%
- High-speed CAN bus Transceiver according to ISO 11898-5
- Integrated RESET unit with a power-on-reset delay and a programmable watchdog time

7.1 Operating Modes and States

The AS8650B provides four main operating modes Normal, Receive-only, Standby, and Sleep. In Normal mode, the CAN Transceiver can be disabled in case of over-temperature condition. The detailed transition table for each mode is shown in the subsequent pages.

7.1.1 Normal Mode

In Normal mode DCDC converter, the three voltage regulators, BUS Transceiver, and Window Watchdog are turned on with full functionality. All the LDO regulators are capable of delivering maximum load current possible as per their respective ratings. The BUS Transceiver is capable of sending the TxD data from the microcontroller to the CANH at the maximum rate.

7.1.2 Receive-Only Mode

In this mode, the CAN transmitter is disabled. The CAN receiver, the three voltage regulators, and over-temperature monitor circuit are enabled.

7.1.3 Standby Mode

This is the mode after power up. The Standby mode is a functional low-power mode where the CAN Transceiver is disabled. The bus wake-up (low power receiver) circuit, LDO1, and over-temperature monitor circuit are enabled. Both LDO2 and LDO3 can be enabled or disabled (default state) using the host command. The AS8650B can enter Normal mode, Sleep mode or Receive-only mode through host command.

7.1.4 Sleep Mode

Sleep mode is the current saving mode that is entered by host command or by over-temperature condition. The DCDC converter, the three voltage regulators, CAN Transceiver, the reset, and window watchdog unit are all switched off. The bus wake-up (low power receiver) circuit, oscillator, and over-temperature monitor circuit are active. The bus is in recessive state (high). The only wake-up possible is through remote wake-up (through the bus lines) or local wake up (through the WAKE pin) as described in the WAKE specification. In the case of entering Sleep mode due to over-temperature condition ($T > T_{jshut}$), the device can come out of Sleep only after the temperature falls back below the return temperature T_{jrecv} and any one of the wake up events mentioned above.

7.2 Power Management Strategy

The detailed block diagram and the power management strategy are shown in Figure 4.

Internal Regulator. This module is powered externally by the VSUP. All the critical modules that needs to be kept always on, work on this supply. Some of the important modules among them are Over-temperature monitor, Local Wake block, Internal Power-on Reset module, Internal Oscillator, complete mode-control unit, Undervoltage comparators of three external LDOs.

DCDC Converter. This is the main supply regulator for all the internal blocks. A step-down hysteretic buck converter is used to generate 5V output from VSUP. This 5V output is then used to generate all the three LDOs. This high-efficiency step-down DCDC converter contains the following features:

- Current limited operation
- Thermal shutdown

LDO1. This is the main I/O supply. This is generated internally from the 5V DCDC converter output and gives a regulated 3.3V output to power-up the external micro-controller. All the I/Os that interface with the microcontroller work on this supply.

LDO2. This regulator is generated internally from the 5V DCDC converter output and gives a regulated 2.8V output. The voltage level can be changed through factory settings.

LDO3. This regulator is generated internally from the 5V DCDC converter output and gives a regulated 1.8V output. The voltage level can be changed through factory settings.

Figure 4. Power Management Strategy

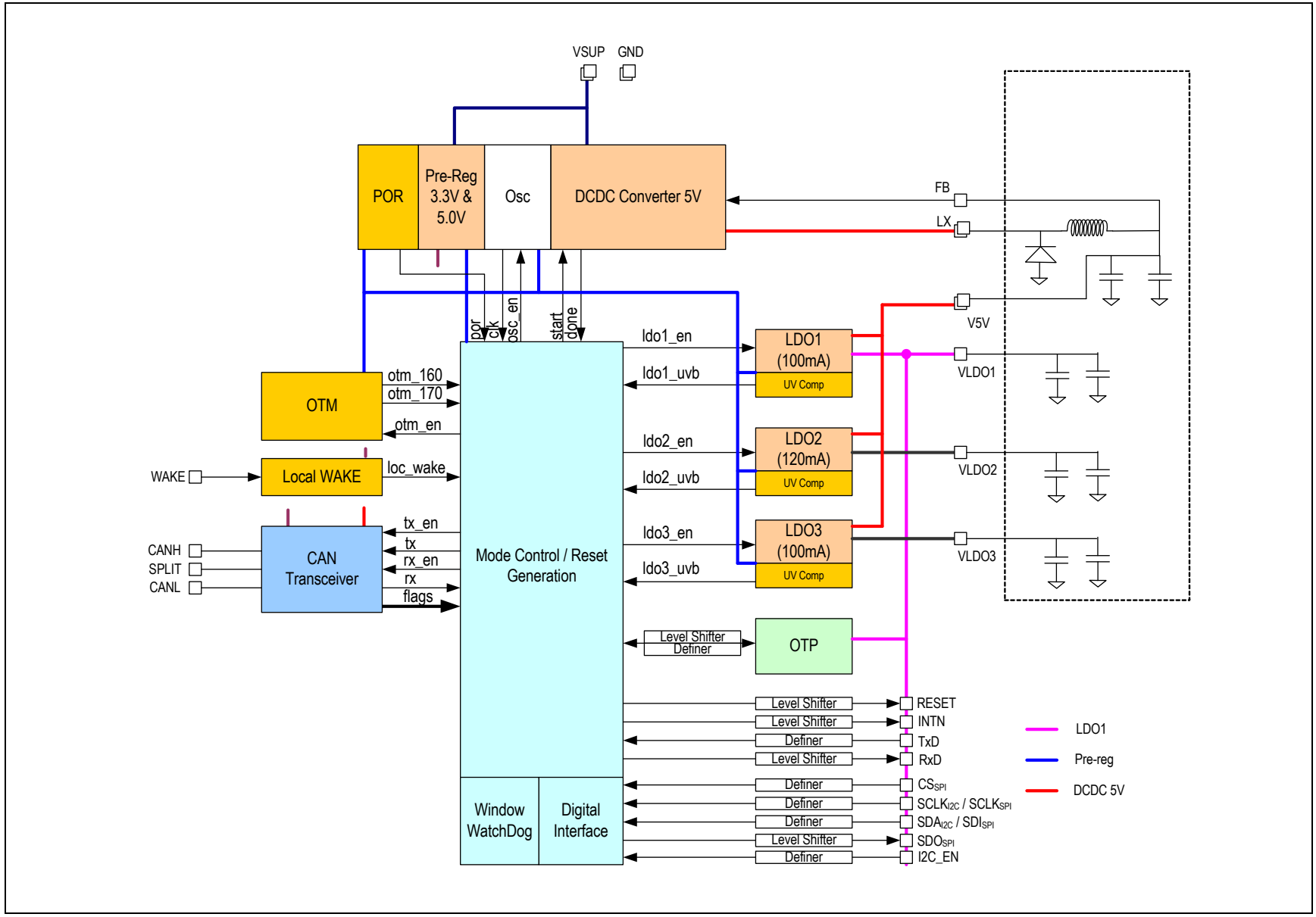


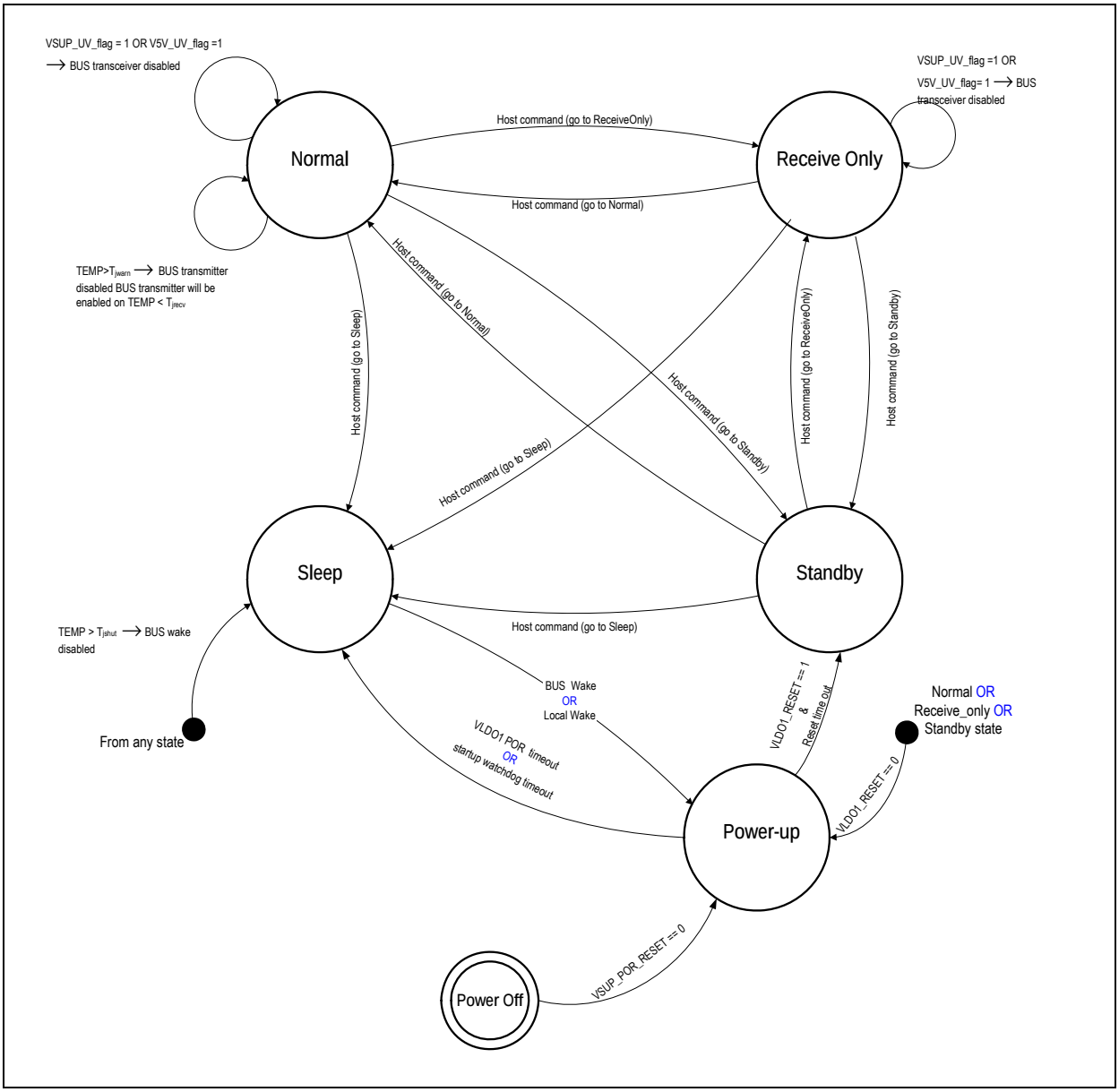
Table 17. Power Management Strategy for AS8650B

Control States	Power-up	Normal	Rx Only	Standby	Sleep
Analog Blocks					
DCDC Converter	ON	ON	ON	ON	OFF [1]
Oscillator	ON	ON	ON	ON	ON
Internal Regulator	ON	ON	ON	ON	ON
OTM	ON	ON	ON	ON	ON
LDO1	ON	ON	ON	ON	OFF
LDO2	OFF	ON [2]	ON [2]	OFF [1]	OFF
LDO3	OFF	ON [2]	ON [2]	OFF [1]	OFF
CAN Tx	OFF	ON	OFF	OFF	OFF
CAN Rx	OFF	ON	ON	OFF	OFF
Low Power Rx	OFF	OFF	OFF	ON	ON
LOCAL WAKE	OFF	OFF	OFF	ON	ON
SPLIT Generation	OFF	ON	ON	ON	ON
Digital Blocks					
WWD	OFF	ON	ON	ON	OFF
Digital Interface	OFF	ON	ON	ON	OFF

1. Can be turned ON using Device Configuration Register
2. Can be turned OFF using Device Configuration Register

7.3 State Diagram

Figure 5. State Machine Model



7.4 Initialization Sequence

The DCDC converter is switched 'ON'. Subsequently, on receiving power-good (PG) signal from the DCDC converter, the LDO1 regulator is switched 'ON'. During the initialization sequence, the VLDO1 is set to 2.5V if VLDO1 > VLDO1_POKTH threshold. VLDO1_RESET is released to 'high'. Then, active-low PORN_2_OTP is generated.

Initially the rising edge of PORN_2_OTP loads contents into the OTP latch. Next the LOAD_OTP_IN_PREREG signal loads the content of OTP latch into the pre-regulator domain register. Once the VLDO1_POKTH threshold is reached, the reset timeout timer also starts.

The RESET signal expires after Reset timeout period T_{Res}. After the RESET signal is 'high', the startup watchdog is launched. If the microcontroller generates a trigger within the startup window, then the device enters into Standby mode.

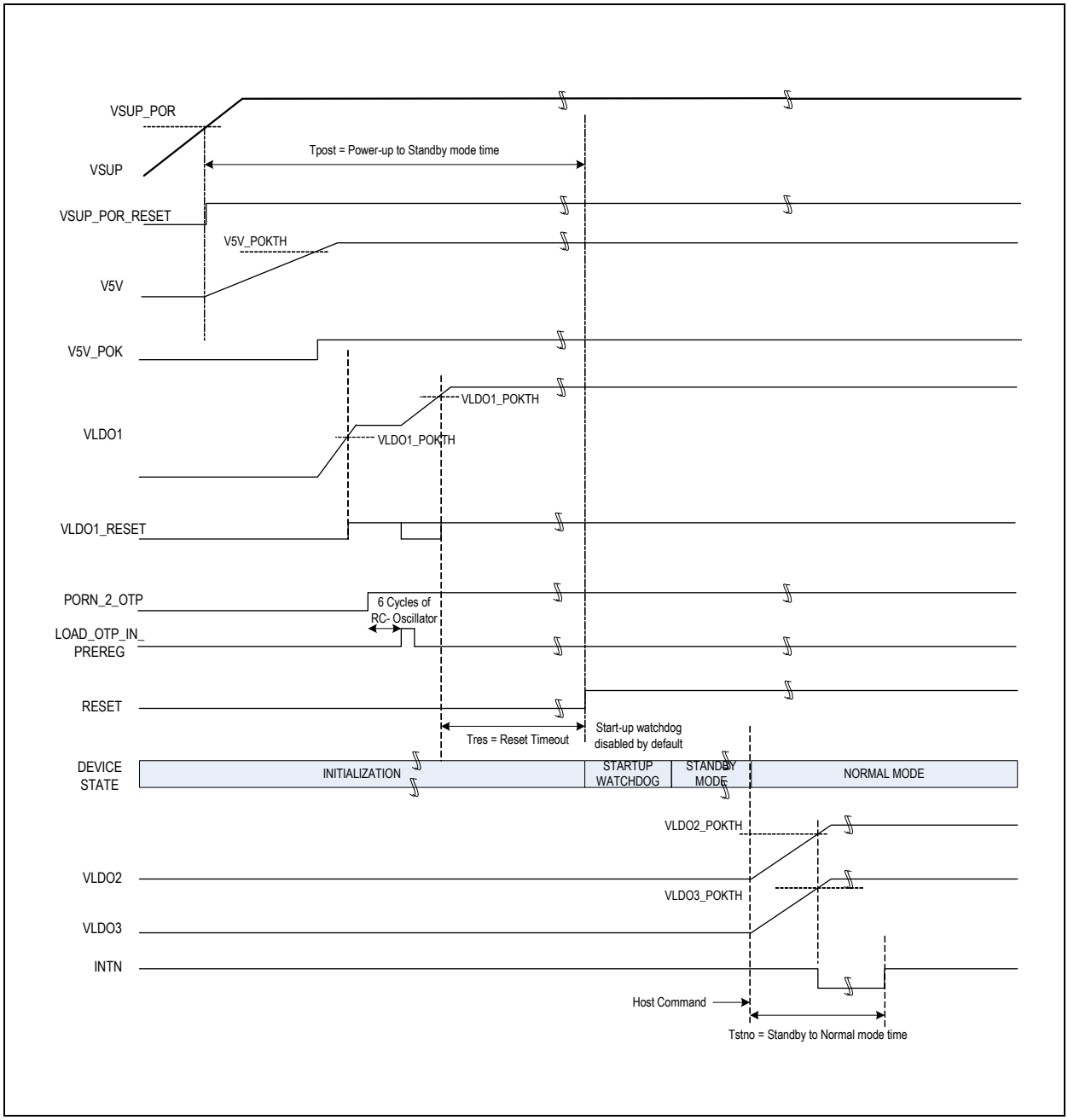
If the microcontroller fails to generate the trigger, then the RESET signal is generated and the Reset timeout will start.

If the microcontroller fails to generate the startup watchdog trigger for 3 consecutive times, then the device enters into Sleep mode. On receiving Normal mode command from the microcontroller, the LDO2 and LDO3 regulators are activated. By the time VLDO2 and VLDO3 reach their respective power-ok (POK) threshold values, an interrupt signal is generated. The AS8650B supports very slow VSUP ramp up of 0.5V/min.

The power initialization sequence diagram is shown in Figure 6.

- After activating the power supply on VSUP pin, the VSUP_POR_RESET flag becomes inactive (high) while the voltage exceeds the VSUP_POR threshold.
- The DCDC output voltage V5V exceeds the V5V_POKTH thresholds after the DCDC settling time and the first voltage regulator (LDO1) will be activated with the V5V_POK set.
- If the voltage output at LDO1 (set to 2.5V on power-up) reaches the VLDO1_POKTH threshold, the PORN_2_OTP flag is set and OTP register setting for the LDO1 is read. Consequently the output voltage will be regulated to the actual OTP settings.
- The initialization phase of the device is terminated after the preset output voltage level threshold is exceeded and the reset timeout is expired.
- After entering Standby mode the host controller can switch the device in any operation mode through the I²C or SPI interface.

Figure 6. Initialization Sequence



7.5 DCDC Converter

The high-efficiency, high-voltage, hysteretic step-down DCDC converter, operates in asynchronous mode and delivers 500mA of output load to drive the three internal LDOs and the CAN Transceiver. The low-power architecture extends hold-up time in battery-backed and critical applications where maximum up-time over a wide input supply voltage range is needed, while still providing for high efficiencies of up to 90% during peak current demands.

7.6 Voltage Regulator LDO1

The stability of the voltage output is below ±2.5% over the full input range and temperature for load current up to 100mA at 3.3V. Power Input to this LDO is the V5V_LDO1 pin. This LDO is activated in Normal, Receive-only or Standby mode. It is switched OFF in Sleep mode.

7.7 Voltage Regulator LDO2

The stability of the voltage output is below ±2.5% over input range and temperature for load current up to 120mA at 2.8V. Power Input to this LDO is the V5V_LDO2 pin. LDO2 is activated in Normal and Receive-only mode. The output voltage level can be changed through factory settings. For further information, please contact *ams* regional sales person.

7.8 Voltage Regulator LDO3

The stability of the voltage output is below ±2.5% over input range and temperature for load current up to 100mA at 1.8V. Power Input to this LDO is the V5V_LDO3 pin. LDO3 is activated in Normal and Receive-only mode. The output voltage level can be changed through factory settings. For further information, please contact *ams* regional sales person.

7.9 Over-Temperature Monitor

In Normal mode, if the junction temperature reaches the over-temperature threshold T_{jwarn}, a warning flag is set in the diagnostic register which can be accessed via the I²C and the SPI interface and an interrupt is signalled on INTN pin. The CAN transmitter is disabled and the device remains in Normal mode. If the junction temperature falls below T_{jrecv}, the CAN transmitter is enabled. The warning flag is cleared in the diagnostic register and an interrupt is signalled at the INTN pin. If the junction temperature exceeds the over-temperature threshold T_{jshut}, the device enters Sleep mode irrespective of the current mode and bus wake receiver (Low power receiver) is disabled. As soon as the temperature falls below T_{jrecv} (thermal recovery), the device goes through the power-up sequencing while entering Power-up mode and enters Standby mode if the boundary conditions of the statemachine are fulfilled.

7.10 Undervoltage Reset

Undervoltage on VSUP (Brown out Indication). If VSUP voltage falls below VSUP_UVTH threshold, the VSUP_UV_flag is set and an interrupt at INTN is generated. In this case the device enters into the Standby mode. The LDO1 voltage regulator remains activated. Two scenarios are possible at this stage:

- VSUP is recovering: If VSUP exceeds the VSUP_POKTH threshold, the VSUP_POK_flag is set and the device remains in Standby mode.
- VSUP is still falling: In this case the device continues to stay in Standby mode. If voltage falls below VSUP_RESET threshold, then the device enters Power-Off and the logic is reset.

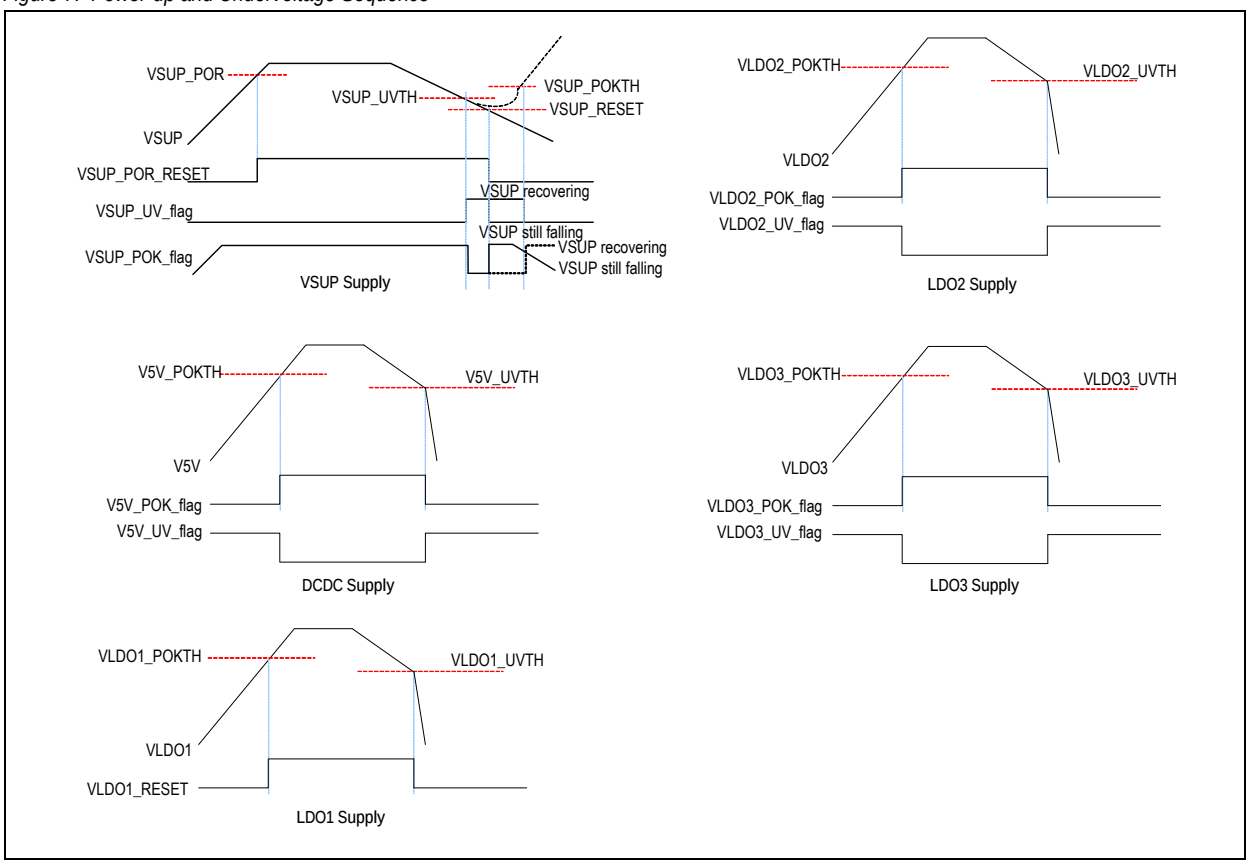
Undervoltage on V5V. If the V5V falls below V5V_UVTH threshold, the V5V_UV_flag is set. Once V5V returns to V5V_POKTH threshold value, V5V_POK_flag is set. In case a flag is set, an interrupt is generated at the INTN pin. If undervoltage on V5V occurs in Normal or Receive-only modes then CAN Transceiver is disabled and the device remains in its operation mode.

Undervoltage on LDO1. If the voltage level of LDO1 falls below the VLDO1_UVTH threshold value and device is not in Sleep mode, the device enters into power-up state while RESET signal is asserted and the voltage regulator is still active. Once the VLDO1_POKTH threshold is reached, RESET signal is de-asserted after reset timeout period and device enters into Standby mode.

Undervoltage on LDO2. If the voltage level of the LDO2 falls below the VLDO2_UVTH threshold value a VLDO2_UV_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin. Once VLDO2 returns to VLDO2_POKTH threshold value, VLDO2_POK_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin.

Undervoltage on LDO3. If the voltage level of the LDO3 falls below the VLDO3_UVTH threshold value a VLDO3_UV_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin. Once VLDO3 returns to VLDO3_POKTH threshold value, VLDO3_POK_flag is set. An indication is given to microcontroller by setting a bit in interrupt register and giving interrupt on INTN pin.

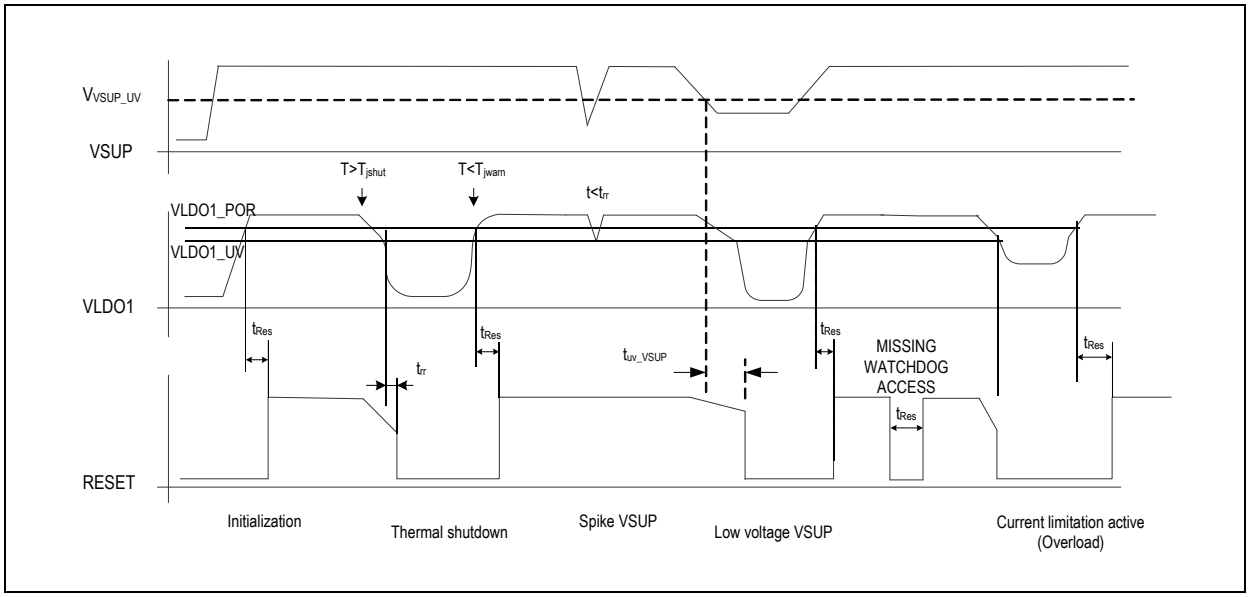
Figure 7. Power-up and Undervoltage Sequence



7.11 Reset Block

The reset block generates an external RESET signal to reset the microcontroller and all other external circuits. The reset functionality is explained in Figure 8. The reset block consists of a digital buffer at the output. The RESET signal is affected by VLDO1_RESET (during overload, reset on VLDO1) and watch dog output. All conditions which cause a drop of the VLDO1 voltage will be detected from the low voltage reset unit which in-turn generates a reset signal.

Figure 8. Reset Block Functional Waveform



7.12 CAN Transceiver

The AS8650B provides an advanced interface between the protocol controller and the physical bus in a Controller Area Network (CAN) node. This is intended for automotive high-speed CAN application (up to 1 Mbit/s), providing differential transmit capability to the bus and differential receive capability to the CAN controller. It is fully compatible to the ISO 11898-5 standard and offers excellent Electromagnetic Compatibility (EMC) performance. The CAN is a high-speed, low complexity protocol with improved EMI and EMC performance. The CAN is a serial communication protocol efficiently supporting the control of mechatronic nodes in a distributive automotive application. The basic blocks of the CAN Transceiver are described below:

7.12.1 BUS Driver

This driver has the basic functionality of relaying the data from the microcontroller on to the CAN bus. The data on the CAN needs to have a controlled slew to reduced EMI. A low side driver is used which has an inherent reverse polarity protection. It has a Short-Circuit current limitation.

7.12.2 Normal Receiver

It relays the data from the CAN bus to the microcontroller in Normal mode.

7.12.3 Low Power Receiver

It relays the data from the CAN bus to the microcontroller in low power mode state.

7.12.4 Operating Modes

The CAN Transceiver provides the following operating modes:

- NORMAL: Non low power mode
- RECEIVE-ONLY: Non low power mode
- STANDBY: Low power mode
- SLEEP: Low power mode

Normal Mode. In this mode the Transceiver is able to send and receive data signals on the bus. RxD reflects the bus data.

Receive-Only Mode. In this mode the Transceiver has the same behavior as in Normal mode but the transmitter is disabled.

Standby Mode or Sleep Mode. In this mode the Transceiver is not able to send and receive data signals from the bus, but the wake up detector is active. The power consumption is significantly reduced respect the non low power operation modes. The WAKE_REMOTE reflects the remote wake up detector output; WAKE_LOCAL reflects the input signal on WAKE pin.

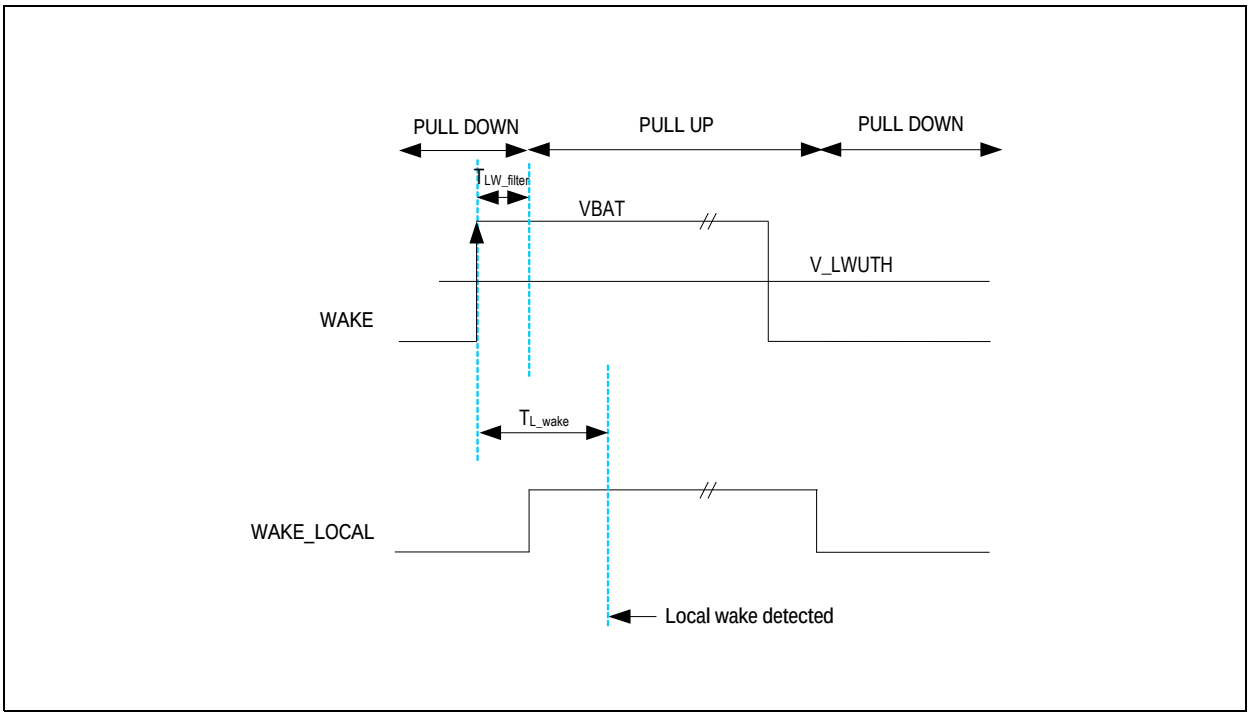
Table 18. Operating Modes

State	TxD	Transmitter	Normal Receiver	Low Power Receiver	Bust State
NORMAL	L	Enabled	Enabled	Disabled	Dominant
	H	Enabled	Enabled	Disabled	Recessive
REC ONLY	X	Disabled	Enabled	Disabled	(CANH, CANL are not driven)
STANDBY	X	Disabled	Disabled	Enabled	(CANH, CANL are not driven)
SLEEP	X	Disabled	Disabled	Enabled	(CANH, CANL are not driven)

7.12.5 Local Wake-up Event

The WAKE pin is pulled-down to ground using the internal resistor. In all low power modes, if the voltage on the WAKE pin rises above V_LWUTH for longer than T_{LW_filter}, WAKE_LOCAL rises up. For valid wake-up, the WAKE pin needs to be above V_LWUTH as shown in Figure 9. Valid WAKE is detected only at the positive edge of the WAKE pin.

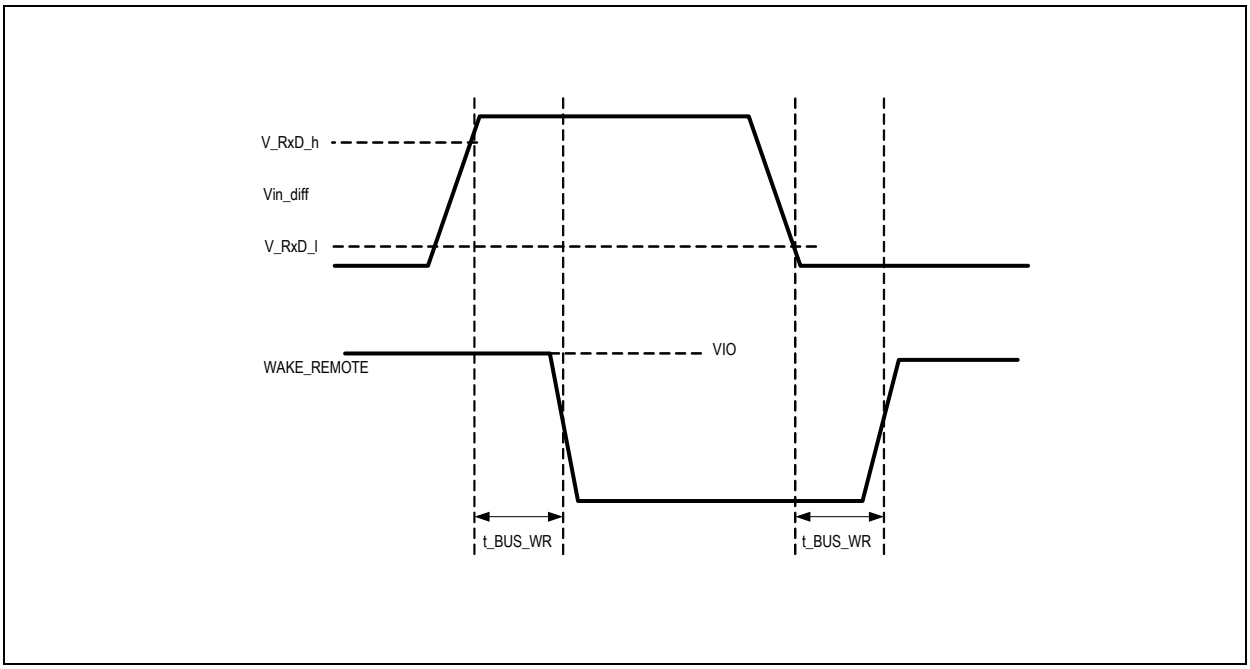
Figure 9. WAKE Input Pin Behavior



7.12.6 Remote Wake-up

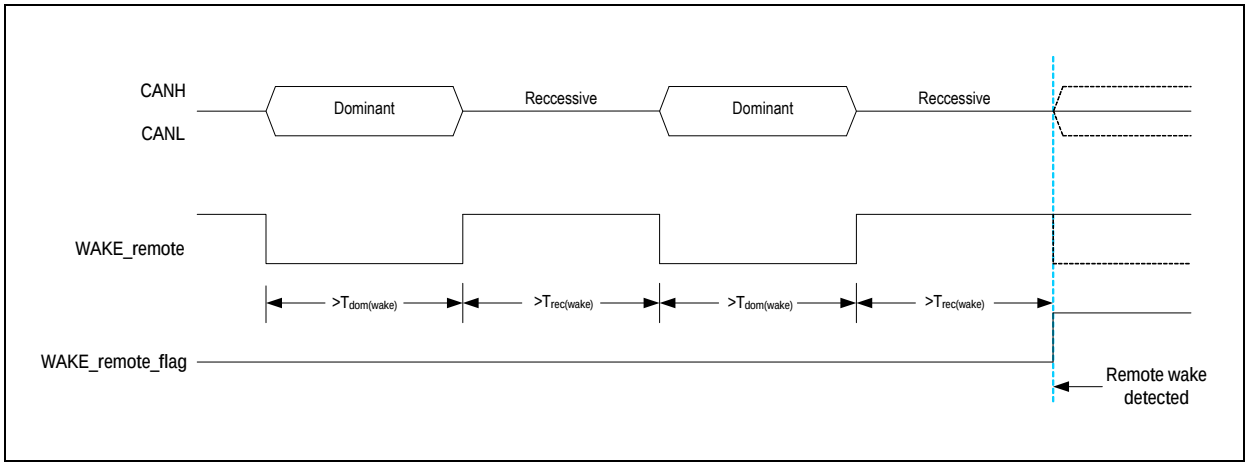
In all low power modes, if the differential voltage on the bus becomes recessive for longer than t_BUS_WR, WAKE_REMOTE rises up. If the differential voltage on the bus becomes dominant for longer than t_BUS_WR, WAKE_REMOTE falls down as shown in Figure 10.

Figure 10. Remote Wake-up Event



A remote wake request is detected after two dominant pulses with each pulse separated by a recessive pulse of at least $T_{rec\ (wake)}$. The remote wake detection circuit is active in Sleep and Standby modes. The wake message pattern is shown in Figure 11.

Figure 11. Wake Message Pattern



7.13 Internal Flags

The AS8650B supports internal flags to indicate the failures in the system. If any of these flag is set an interrupt is generated on INTN pin.

7.13.1 VSUP_UV_flag

This is a VSUP undervoltage flag. This flag is set when VSUP falls below the VSUP_UVTH threshold. When this flag is set the device enters into Standby mode and BUS Transceiver is switched off to save power. When VSUP recovers and raises above VSUP_POKTH threshold the VSUP_UV_flag is reset.

7.13.2 VSUP_POK_flag

This is a VSUP power ok flag. This indicates the VSUP recovery from undervoltage condition. When the VSUP rises above VSUP_POKTH threshold, this flag is set. This indicates the microcontroller that undervoltage condition on battery is cleared.

7.13.3 V5V_UV_flag

This is a V5V undervoltage flag. This flag is set when V5V falls below the V5V_UVTH threshold. When this flag is set the device enters into Standby mode and BUS Transceiver is switched off to save power. When V5V recovers and raises above V5V_POKTH threshold the V5V_UV_flag is reset.

7.13.4 V5V_POK_flag

This is a V5V power ok flag. This indicates the V5V recovery from undervoltage condition. When the V5V rises above V5V_POKTH threshold, this flag is set. This indicates the microcontroller that undervoltage condition on DCDC converter is cleared.

7.13.5 VLDO2_UV_flag

This is a VLDO2 undervoltage flag. This flag is set when VLDO2 falls below the VLDO2_UVTH threshold. When VLDO2 recovers and raises above VLDO2_POKTH threshold the VLDO2_UV_flag is reset.

7.13.6 VLDO2_POK_flag

This is a VLDO2 power ok flag. This indicates the VLDO2 recovery from undervoltage condition. When the VLDO2 rises above VLDO2_POKTH threshold this flag is set. This indicates the microcontroller that undervoltage condition on LDO2 is cleared.

7.13.7 VLDO3_UV_flag

This is a VLDO3 undervoltage flag. This flag is set when VLDO3 falls below the VLDO3_UVTH threshold. When VLDO3 recovers and raises above VLDO3_POKTH threshold the VLDO3_UV_flag is reset.

7.13.8 VLDO3_POK_flag

This is a VLDO3 power ok flag. This indicates the VLDO3 recovery from undervoltage condition. When the VLDO3 rises above VLDO3_POKTH threshold this flag is set. This indicates the microcontroller that undervoltage condition on LDO3 is cleared.

7.13.9 BUS Wake_up Flag

The BUS Wake_up flag is set when the device detects a remote wake-up (BUS message) request. The remote wake-up request is detected when pattern shown in Figure 11 is found on wake_remote port of low power receiver. This indicates the microcontroller about the Bus wake event.

7.13.10 Local Wake_up Flag

The Local Wake_up flag is set when the device detects a local wake-up request on WAKE pin. A local wake-up request is detected when a logic state change on pin **WAKE** as shown in Figure 9. This indicates the microcontroller about the local wake event.

7.13.11 OVT_Warning Flag

The OVT_Warning flag is set when temperature exceeds T_{jwarn}. This indicates the microcontroller about temperature exceeding warning levels.

7.13.12 OVT_Recover Flag

The OVT_Recover flag is set when temperature falls back below T_{jrecv}. This indicates the microcontroller about temperature falling back below recovery levels.

7.13.13 Bus Failure Flags

The bus failure flag is set if the CAN Transceiver detects a bus line short-circuit condition to VSUP, V5V_LDO1 or GND. Such possible conditions are indicated to microcontroller through these flags. All these flags are cleared on microcontroller read. If the fault condition still exist after microcontroller read, the particular flag is set again. The device still be working in the current state. The microcontroller takes appropriate action on reading of these flags.

CANH_short_GND. This flag indicates Over Current condition on pin CANH. For example short to ground on pin CANH. When the output current on pin **CANH** exceeds the threshold OC_CANH_th then the output OC_CANH switches on high level after a filter time t_OC_CANH.

CANH_short_VSUP. This flag indicates Low Current on pin CANH. For example open load or short to VSUP on pin CANH. When the output current on pin **CANH** falls below the threshold LC_CANH_th then the output LC_CANH switches on high level after a filter time t_LC_CANH.

CANL_short_VSUP. This flag indicates Over Current on pin CANL. For example short to VSUP on pin CANL. When the output current on pin **CANL** exceeds the threshold OC_CANL_th, then the output OC_CANL switches on high level after a filter time t_OC_CANL.

CANL_short_GND. This flag indicates Low Current on pin CANL. For example open load or short to ground on pin CANL. When the output current on pin **CANL** falls the threshold LC_CANL_th then the output LC_CANL switches on high level after a filter time t_LC_CANL.

7.13.14 Local Failure Flags

The AS8650B prevents the system from four kinds of local failures without disturbing the BUS network. The four failures are TxD dominant clamping, RxD recessive clamping, TxD & RxD short, and bus dominant clamping. All these failures are indicated to microcontroller through flags.

TxD_Dom_Clamp flag. A permanent Low-level on pin TxD (due to a hardware or software application failure) would drive the BUS into a permanent dominant state, blocking BUS network communication. If pin TxD remains at a Low level for longer than the TxD dominant timeout period $T_{TxDC(dom)}$, the device disables the transmitter of BUS Transceiver and TxD_Dom_Clamp flag is set. The device prevents such BUS network lock-up by disabling the transmitter of the transceiver. The device will not change the functional state. The transmitter remains disabled until the local failure persists. The flag is cleared with microcontroller read request.

TxD_RxD_Short flag. The TxD_RxD short circuit would result in a dead-lock situation clamping the bus dominant. For example the Transceiver receives a dominant signal, RxD outputs a dominant level. Because of the short circuit, TxD reflects a dominant signal, retaining the dominant bus state. As a result TxD and the bus are clamped continuously dominant. The resulting effect is the same as for the continuously clamped dominant TxD signal. The TxD dominant timeout interrupts the deadlock situation by disabling the transmitter and the TxD_RxD short condition is differentiated. The bus becomes recessive again and TxD will be recessive if it is not driven by microcontroller. However, the failure scenario may still exist and with the next dominant signal on the bus the described procedure will start again.

The device keeps the transmitter off after detection of TxD_RxD short fault and keeps updating this flag status. The microcontroller has to send 2 consecutive low pulses of duration 500ns with high period of 500ns in-between, in regular intervals to check short circuit recovery. This way a local TxD/RxD short circuit will not disturb the communication of the remaining bus system.

BUS_Dom_Clamp flag. In the case of a short circuit from BUS to GND, the circuit for the BUS receiver senses dominant signal continuously even if there is no dominant transmitting node. The result may be a permanently dominant clamped bus. The device detects and reports a Bus Dominant Clamping situation to microcontroller through BUS_Dom_Clamp flag. If the receiver detects a bus dominant phase of longer than the bus dominant time out $T_{BUSC(dom)}$ BUS_Dom_Clamp flag is set. The flag is cleared on microcontroller read.

7.14 Watchdog (WD)

The WD has the following three monitory timing functions:

- Start-up watchdog: Gives opportunity to microcontroller to initialize the system.
- Window watchdog: Detects too early or too late microcontroller software response (loops and hangs).
- Timeout watchdog: Detects too very long response from microcontroller.

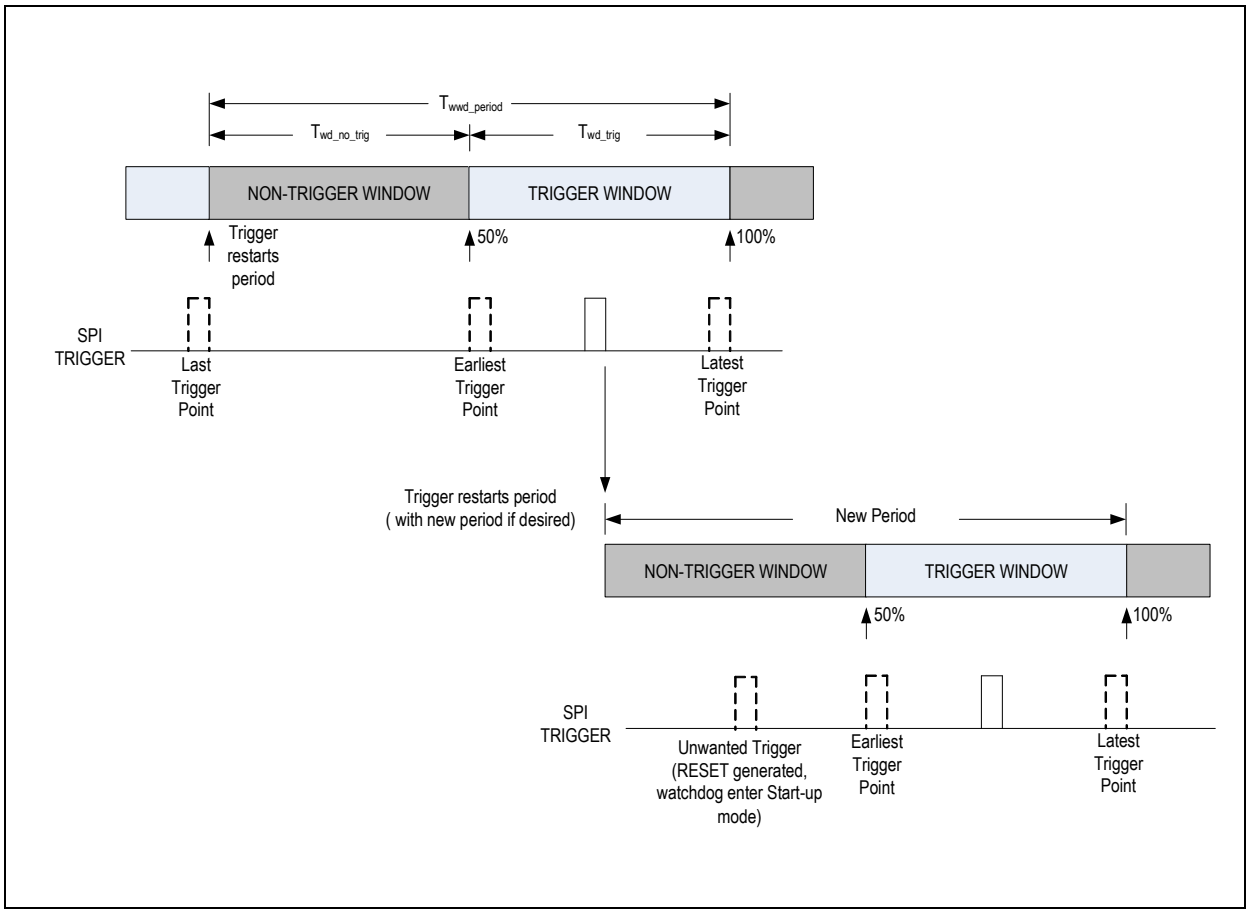
7.14.1 Start-up Watchdog Behavior

Following any reset event the watchdog is used to monitor the ECU start-up procedure. Once the reset is released the watchdog counter will start. In case the watchdog is not properly served (a trigger from microcontroller) within TWD(init), another reset is forced on RESET pin and the monitoring procedure is restarted. The watchdog will give three opportunities to microcontroller to initialize the system. In case the watchdog is not properly served for three times, then the system enters into Sleep mode.

7.14.2 Window Watchdog Behavior

Whenever the device enters Normal mode, the Window mode of the watchdog is activated. This ensures that the microcontroller operates within the required speed; a too fast as well as a too slow operation will be detected. Watchdog triggering using the Window watchdog is illustrated in Figure 12.

Figure 12. Window Watchdog Triggering

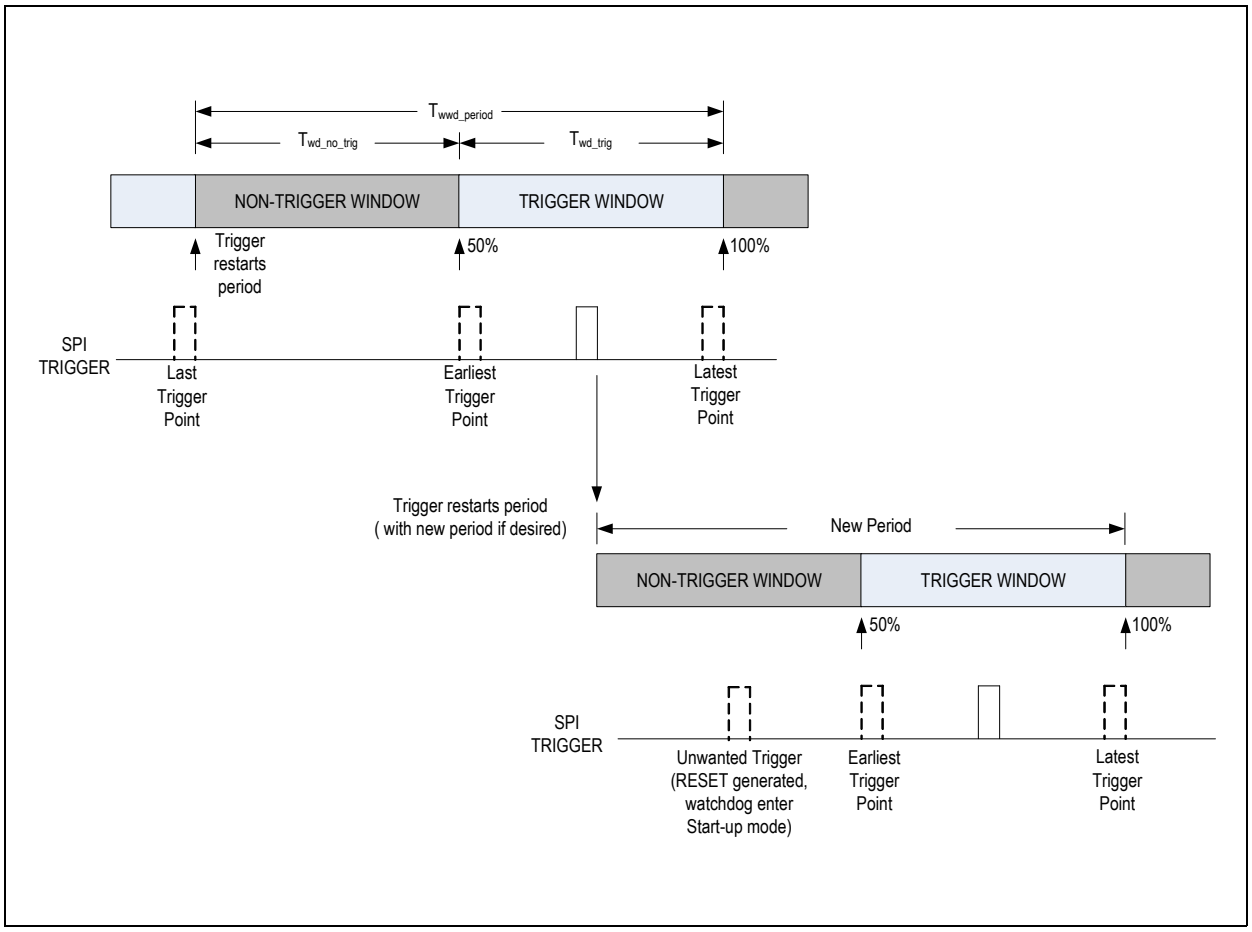


The AS8650B provides 8 different period timings. This timing can be changed through digital interface when desired. The period can be changed within any valid trigger window. Whenever the watchdog is triggered within the window time T_{wd_trig}, the timer will be reset to start a new period. The watchdog window is defined to be between 50% and 100% of the nominal programmed watchdog period. Any too early (trigger in non-trigger window) or too late watchdog trigger will result an immediate system reset on RESET pin and watchdog entering Start-up watchdog mode. During undervoltage condition on VLDO1 the watchdog timer is disabled.

7.14.3 Timeout Watchdog Behavior

Whenever the AS8650B operates in Standby mode, active watchdog operates in Timeout watchdog mode. The watchdog has to be triggered within the actual programmed period time $T_{wd_tout_period}$. The device provides 8 different possible periods for programming through digital interface. If the microcontroller fails to trigger the watchdog within trigger range then the system reset is generated on RESET pin and watchdog enters into Start-up watchdog mode. The timeout watchdog function is illustrated in Figure 13.

Figure 13. Timeout Watchdog Triggering

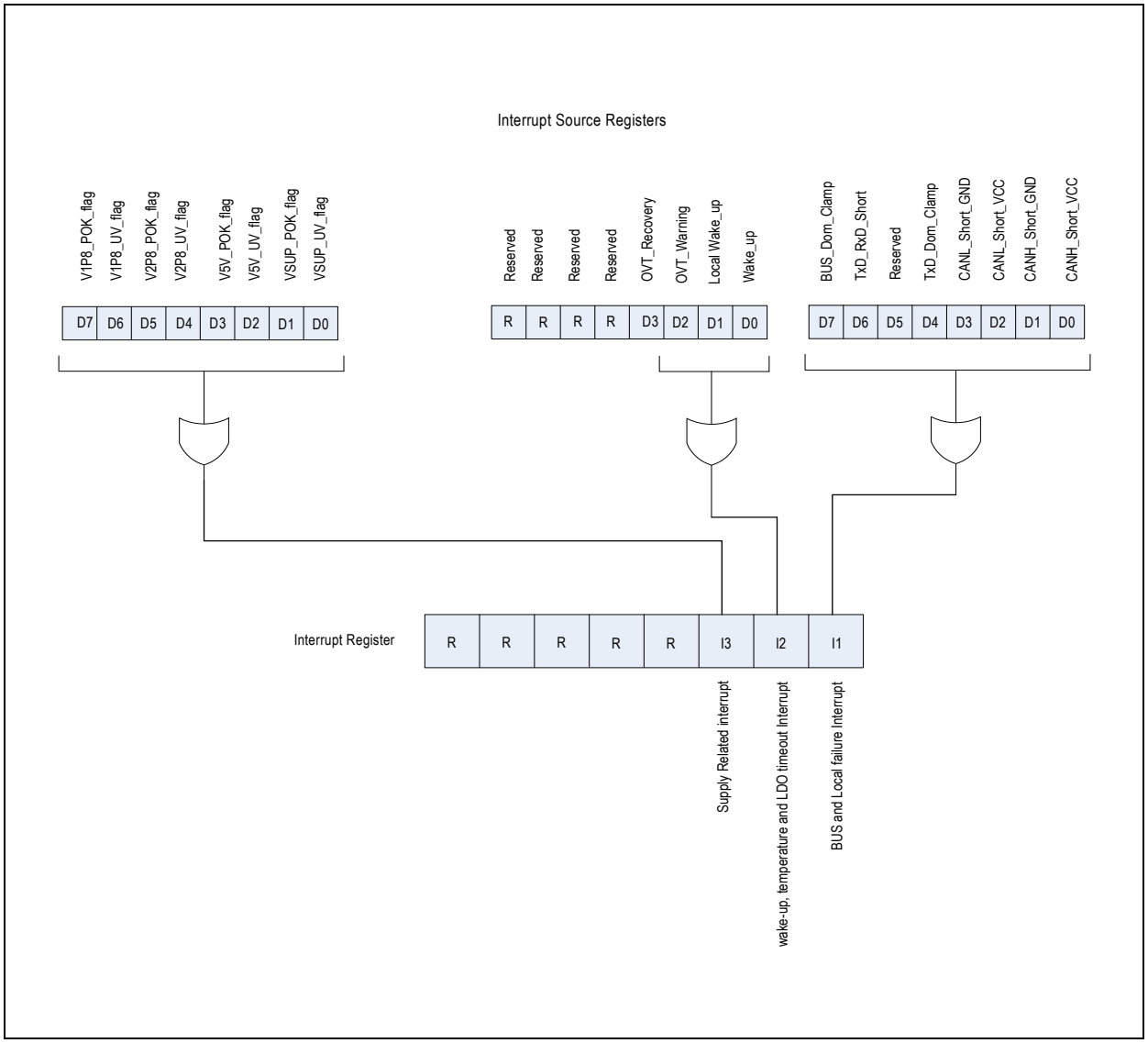


7.15 Interrupt Generation

The pin INTN is an interrupt output. The INTN is forced 'low' if one bit in the Interrupt register is set. The Interrupt register bits are cleared when the microcontroller clears the corresponding interrupt source register. The Interrupt register will also be cleared during a system reset (RESET LOW). As there are microcontrollers with level sensitive or edge sensitive interrupt port, pin INTN will be 'high' for at least TINTN after any of the interrupt source register is cleared. The Interrupt source register is cleared through write operation by overwriting '1' in to respective set bits position. Without further interrupts within TINTN pin INTN stays 'high', otherwise it will revert to 'low' again.

The Interrupt register indicates the cause of an interrupt event. There are two levels of interrupt registers. First level register indicates the source region of interrupt and the second level register indicates the exact source of interrupt. With this structured interrupt, the microcontroller can trace source of interrupt by two read operations instead of polling for source of interrupt and also interrupts can be prioritized by microcontroller. The interrupt register structure is given in Figure 14. The register is cleared through digital interface write operation and upon any reset event. The hardware ensures no interrupt event is lost in case there is a new interrupt forced while reading the register.

Figure 14. Interrupt Register Structure



7.16 Status Registers

The AS8650B has three Flag status registers and one RESET Reason Register. The Flag status registers indicate the current status of flags which are related to respective interrupt source registers. The Flag status registers are BUS Status Register, Temperature Status Register, and Supply Status Register. The microprocessor can read these registers any time to check the status of device. The function of each flag is listed in register space description in subsequent sections.

A RESET Reason register indicates the reasons for RESET generation. Once the RESET pin goes ‘low’, the reason of this reset event is stored in RESET Reason register. When RESET is released microprocessor can read this register to know the cause for last RESET signal. The RESET Reason register is cleared once microprocessor reads this register through read operation. The bits functionality of this register is explained in register space description table.

8 Application Information

Device Interfaces. There are two ways to communicate with AS8650B, one is 4 wires SPI and other is I²C. The selection between these two interfaces is through I2C_EN pin, as shown in Table 19. The pins CS, SCLK, SDI, and SDO are used for SPI interface. For I²C interface, SCLK is used as I²C Clock and SDA is used as I²C data line. Pins $SCLK_{I2C}$ / $SCLK_{SPI}$ and SDA_{I2C} / SDI_{SPI} are multiplexed for both SPI and I²C interface. Since **I2C_EN** is a digital input pin, it has to be connected either to VLDO1 or GND.

Note: **I2C_EN** should not be changed during a I²C/SPI Read/Write operation. Maximum switching delay between I²C and SPI is 8µs.

Table 19. Device Interface Selection

I2C_EN	Description
LOW	Interface is 4-wire SPI
HIGH	Interface is I²C

8.1 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller. The SPI is configured for half-duplex data transfer. The SPI provides access to configuration registers, control registers, and diagnostic registers. The modes of the AS8650B are changed by writing required code in to Mode Control Register through SPI. The SPI is also used to enter into test and OTP modes. This interface is only slave interface and only master can initiate SPI operation.

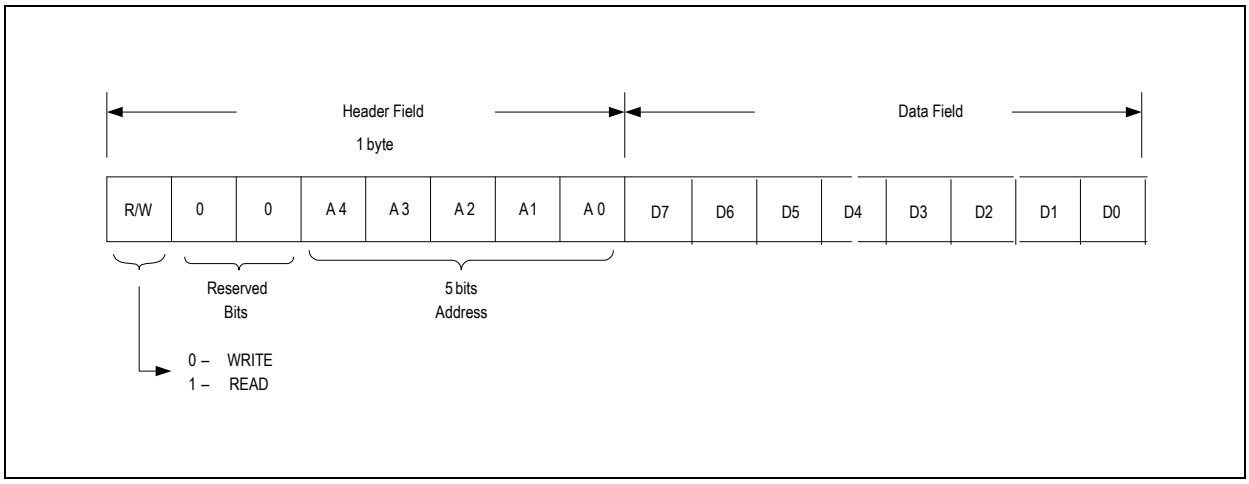
The SPI can work on both the clock polarities. The polarity of the clock depends on the value of SCLK at the falling edge of CS. At the falling edge of CS if SCLK is “1” then the SPI is positive edge triggered and if the SCLK is “0” then SPI is negative edge triggered logic (see Table 20).

Table 20. SPI Clock Polarity

CS	SCLK	Description
LOW	HIGH	Serial data is transferred at falling edge and sampled at rising edge of SCLK
LOW	LOW	Serial data is transferred at rising edge and sampled at falling edge of SCLK

The SPI protocol frame is divided in to two fields, the header field and the data field. The header field is 1 byte long containing a read/write command bit, 5 address bits and 2 reserved bits. The data field is of one data byte. The SPI frame format is shown in Figure 15. In the data phase MSB is sent first and LSB is sent last.

Figure 15. SPI Frame Format



8.1.1 SPI Write Operation

The SPI write operation begins with clock polarity selection at negative edge of CS, given in Table 20. Once the clock polarity is selected the SPI write command is given by providing '0' in R/W bit of the header field in first sampling edge at SDI pin. The 5 bits address of register to be written is provided at SDI pin in next five consecutive sampling edges of SCLK. The first 2 bits in header fields are reserved and set to '0'. The data to be written is followed by last bit of header field. With each sampling edge a bit is sampled starting from MSB to LSB. During complete SPI write operation the CS has to be 'low'. The SPI write operation ends with positive edge of CS. The wave form for SPI write operation with single data byte is shown in Figure 16 and Figure 17.

Figure 16. SPI Write Operation with Negative Clock Polarity and 1 Byte of Data Field

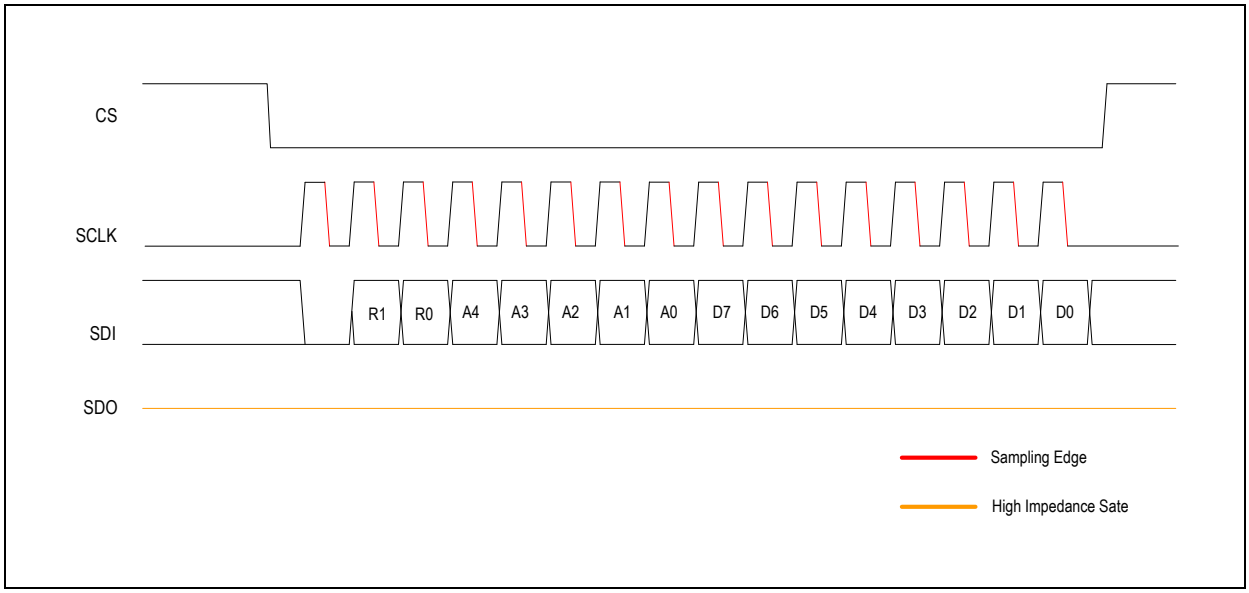
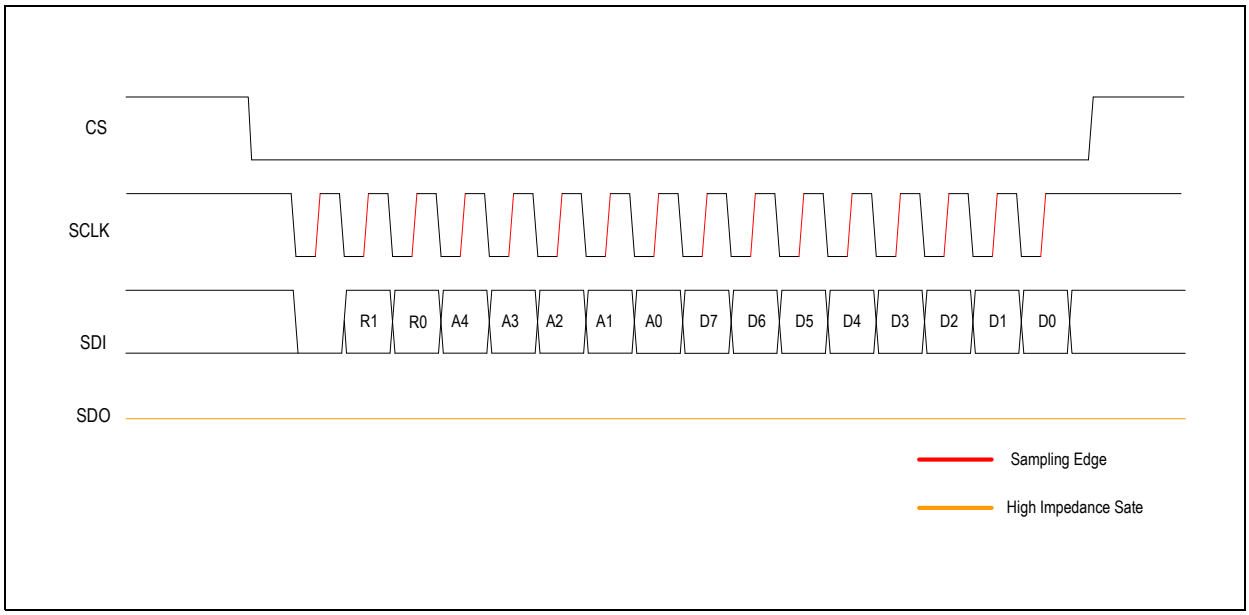


Figure 17. SPI Write Operation with Positive Clock Polarity and 1 Byte of Data Field



8.1.2 SPI Read Operation

The SPI read operation also begins with clock polarity selection at negative edge of CS, given in Table 20. Once the clock polarity is selected the SPI read command is given by providing '1' in R/W bit of the header field in first sampling edge at SDI pin. The 5 bits address of register to be read is provided at SDI pin in next five consecutive sampling edges of SCLK. The first 2 bits in header fields are reserved and set to '0'. The read data is followed by last bit of header field on SDO pin. With each sampling edge a bit can be read on SDO pin starting from MSB to LSB. During complete SPI read operation the CS has to be 'low'. The SPI read operation ends with positive edge of CS. The wave form for SPI read operation with single data byte is shown in Figure 18 and Figure 19.

Figure 18. SPI Read Operation with Negative Clock Polarity and 1 Byte of Data Field

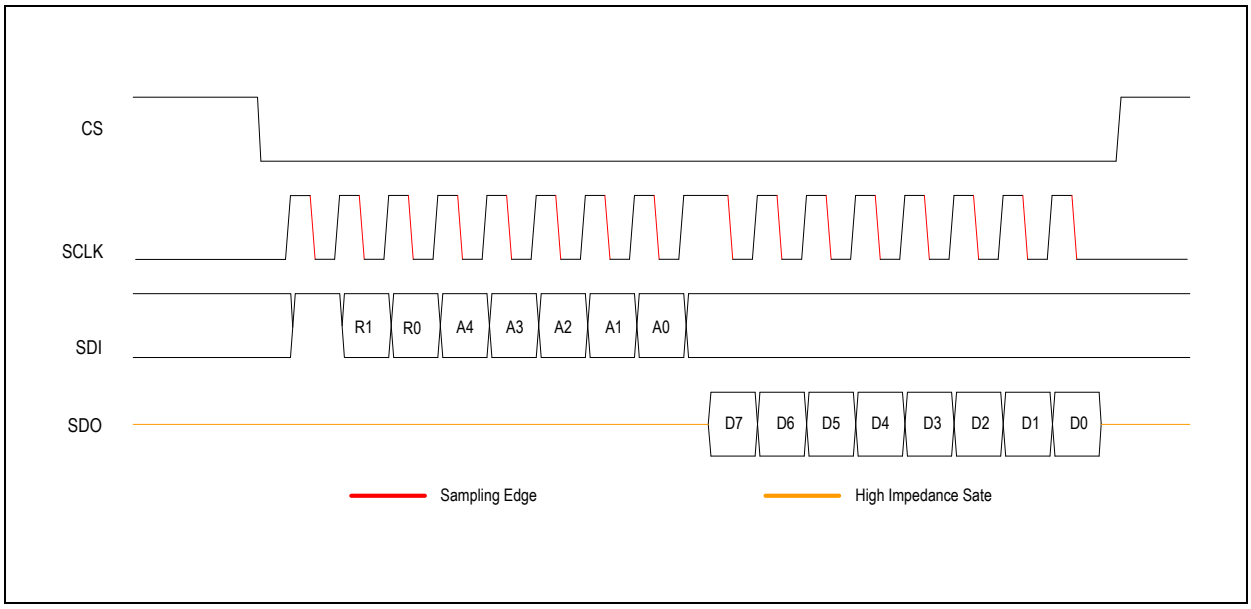
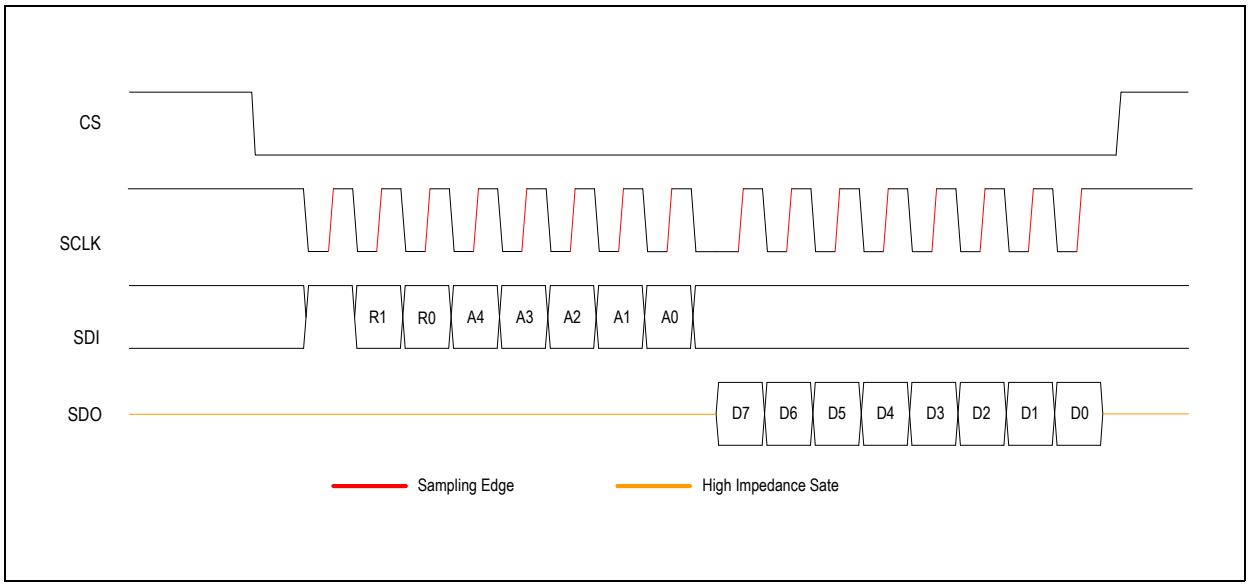


Figure 19. SPI Read Operation with Positive Clock Polarity and 1 Byte of Data Field



8.1.3 SPI Timing Diagram

Figure 20. Timing Diagram for SPI Write Operation

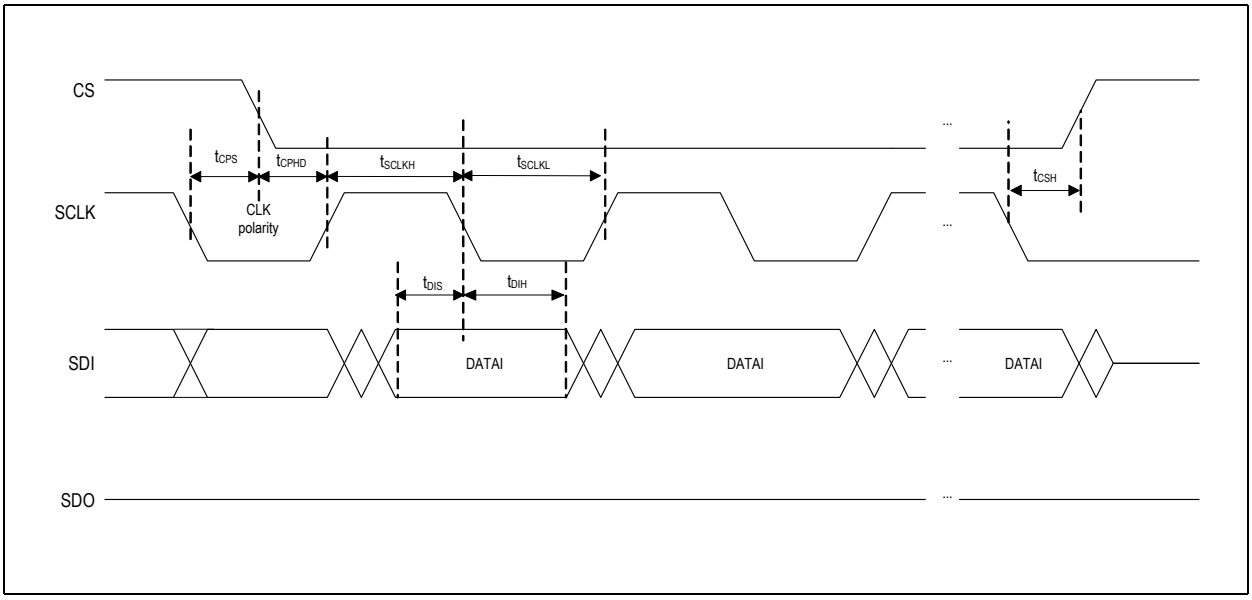
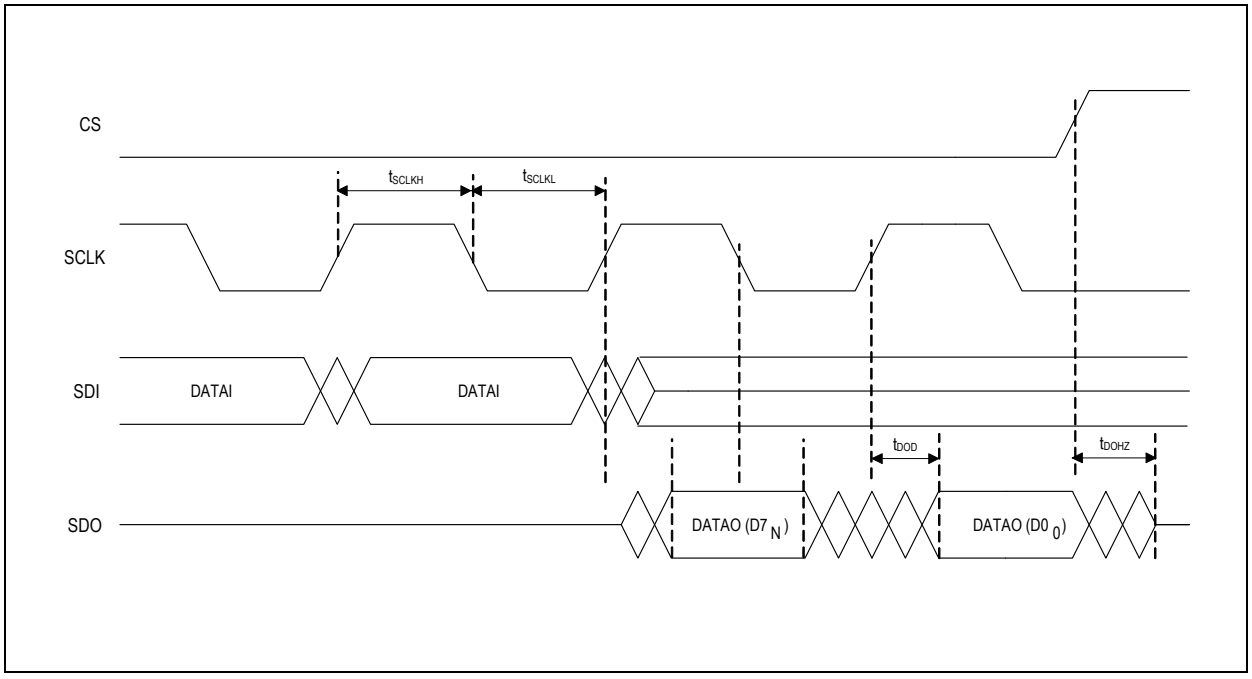


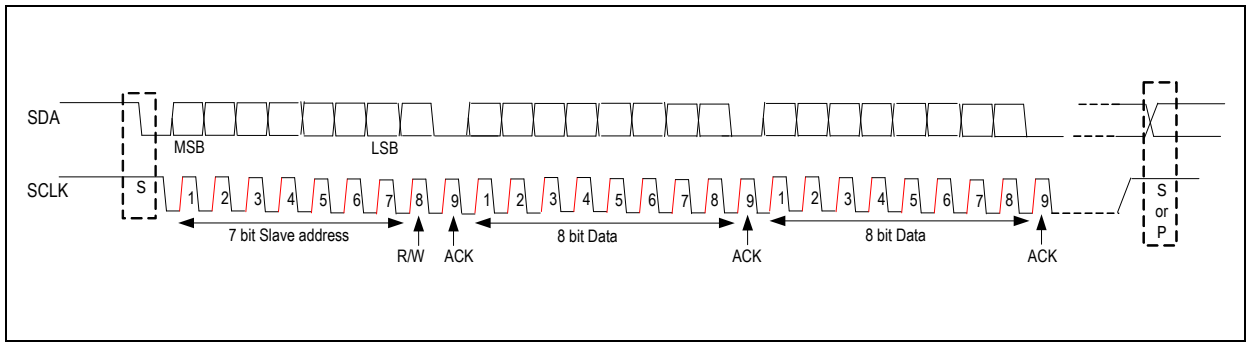
Figure 21. Timing Diagram for SPI Read Operation



8.2 Inter-Integrated Circuit (I²C) Interface

I²C is a bidirectional 2 line bus interface with a serial data line (SDA) and a serial clock line (SCLK) for inter IC control. This interface is only slave interface and only microcontroller can start and stop the I²C operation. The overview of I²C protocol is shown in Figure 22. A 'high' to 'low' transition on SDA line while SCLK is 'high' is the START (S) condition and a 'low' to 'high' transition on SDA line while SCLK is 'high' is the STOP (P) condition, as shown in Figure 22. The START and STOP conditions should always be generated by the microcontroller. After the START condition, microcontroller has to make sure that data on SDA line must be stable during the 'high' period of SCLK. The data should only change when SCLK line is 'low'. The Bus is busy after the START condition and it is free after the STOP condition. Any number of data bytes can be transmitted between START and STOP. Each byte is followed by an acknowledgement (which is the ninth bit). The data transmitter always receives an acknowledgement from the data receiver at end of each byte. The data transmitter releases the SDA bus at start of 'low' period of 8th clock pulse and data receiver acknowledges by pulling the SDA to 'low' during the 'low' period of the SCLK. The Data receiver releases the bus at start of 'low' period of 9th clock pulse of the SCLK and data transmitter gets the data bus.The AS8650B does not support general call address, START byte and high-speed mode.

Figure 22. I²C Bus Protocol



8.2.1 I²C Slave Address

The 7-bit slave address of the device is by default set to 0000000.
On request the slave address can be changed in the range from 0000000 to 1111110 through factory settings.

8.2.2 I²C Write Operation

After the START condition, microcontroller has to send, in the first byte, the 7-bit slave address and 0 into the R/W bit as shown in Figure 23. The microcontroller has to send the address of the register to be written in the second byte. The first 3 MSB bits are reserved and remaining 5 bits are used as address bits. The data is sent starting from MSB to LSB. The AS8650B sends acknowledgement on 9th clock pulse. In the next byte (3rd byte) microcontroller has to send the data to be written into addressed register. If it is a single write operation, after receiving the acknowledgment from AS8650B, microcontroller has to send START or STOP condition, as shown in Figure 23. In case of auto increment write operation, microcontroller should not generate START or STOP condition after the third byte. If microcontroller continuously writes then address pointer rolls back to the starting register address after reaching the last register address. Data bytes coming from the microcontroller are written at the consecutive address locations, starting from the address sent in first data byte. After each data byte, direction of the bus line changes and AS8650B acknowledges by pulling the SDA line 'low'. To terminate the write operation microcontroller has to generate STOP or repeated START condition. For details, see Figure 24.

Figure 23. I²C Write Operation

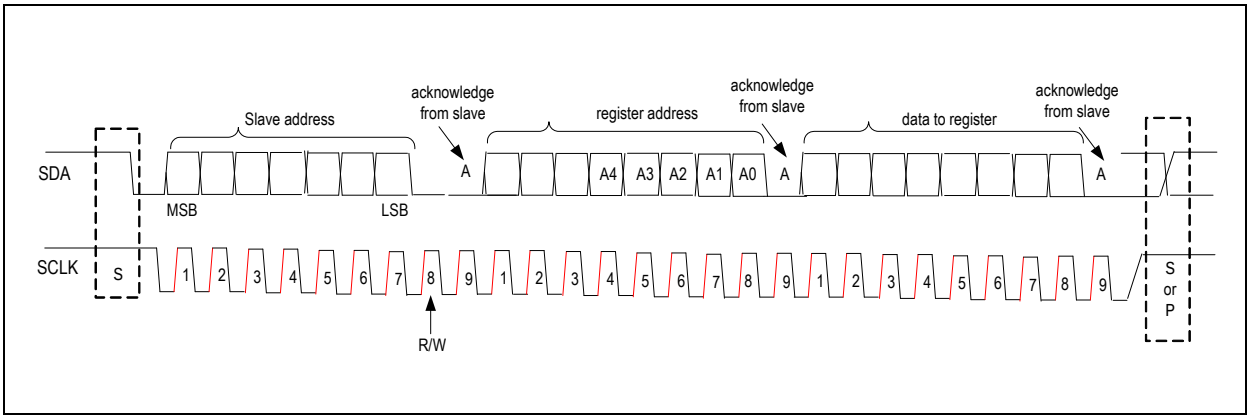
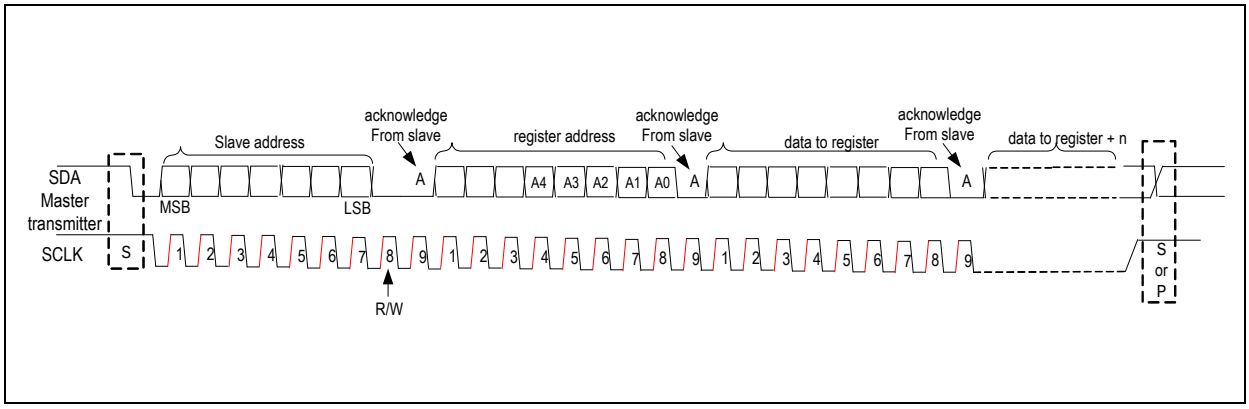


Figure 24. I²C Auto-increment Write Operation



8.2.3 I²C Read Operation

After the START condition, microcontroller has to send, in the first byte, the 7-bit slave address and 0 into the R/W bit as shown in Figure 25. The microcontroller has to send the address of the register to be written in the second byte. The first 3 MSB bits are reserved and remaining 5 bits are used as address bits. The data is sent starting from MSB to LSB. After receiving the acknowledgement on the 9th clock pulse, microcontroller has to send on the SDA line repeated START or STOP, as shown in Figure 25. If microcontroller sends STOP then microcontroller has to send START again. If microcontroller sends repeated START then there is no need to generate START again. The microcontroller again has to send the 7-bit slave address and writes '1' into the R/W bit (8th bit). Now AS8650B sends data of the corresponding addressed register in the next eight clock cycles. In case of single read, microcontroller does not acknowledge on the 9th clock pulse and generates START or STOP condition after the ninth clock pulse. If it is an auto increment read operation, microcontroller acknowledges on the 9th clock pulse and AS8650B sends data from the consecutive address locations, (see Figure 25). If microcontroller continuously reads then address pointer rolls back to the starting register address after reaching the last register address. In the data phase MSB is sent first and LSB is sent last. After each data byte, microcontroller has to send the acknowledgement. The microcontroller can terminate the auto read operation by not generating acknowledgement for the last byte that was sent by the AS8650B and generates STOP or repeated START condition after the 9th clock pulse.

Figure 25. I²C Read Operation

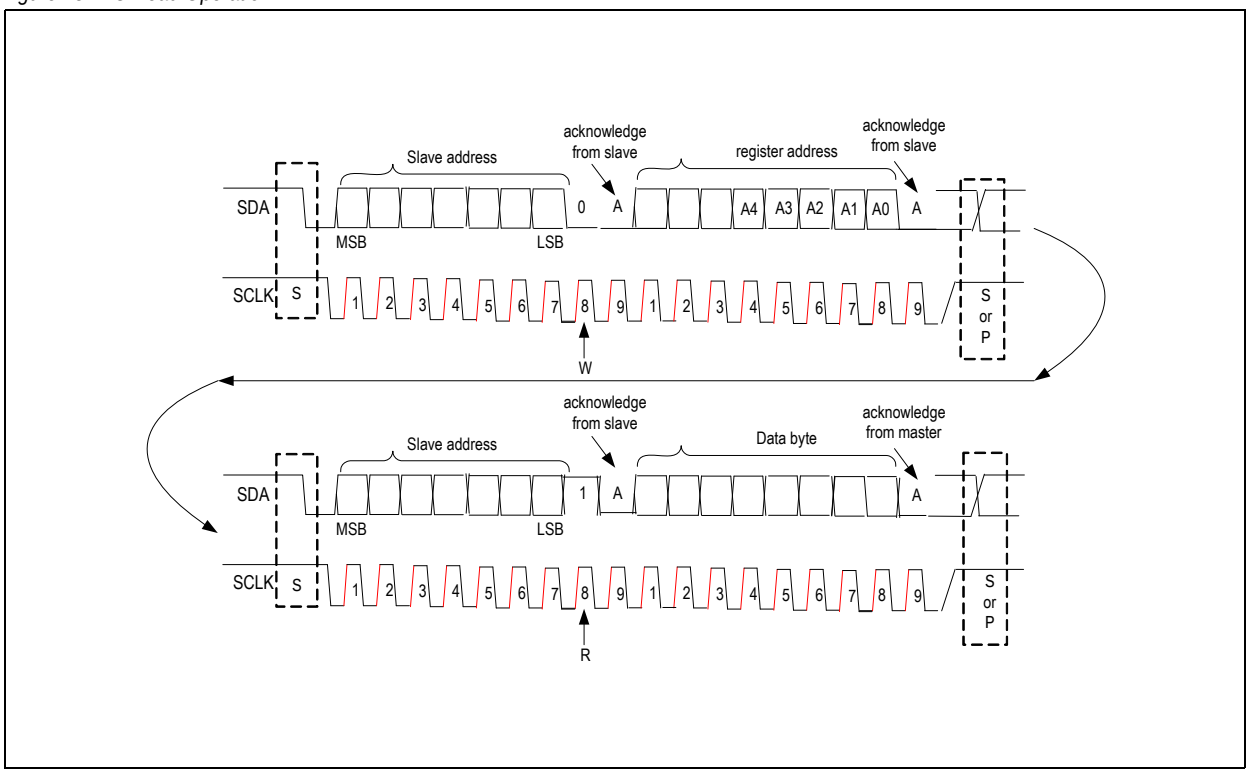


Figure 26. I²C Auto-increment Read Operation

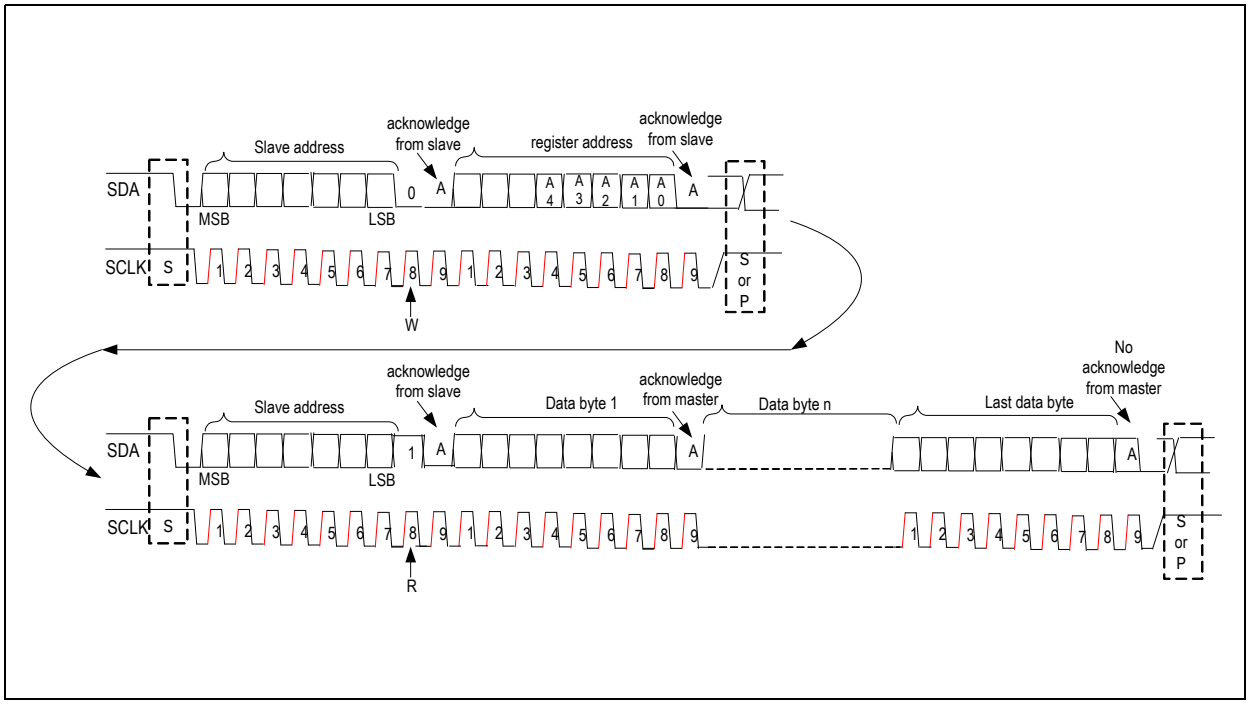
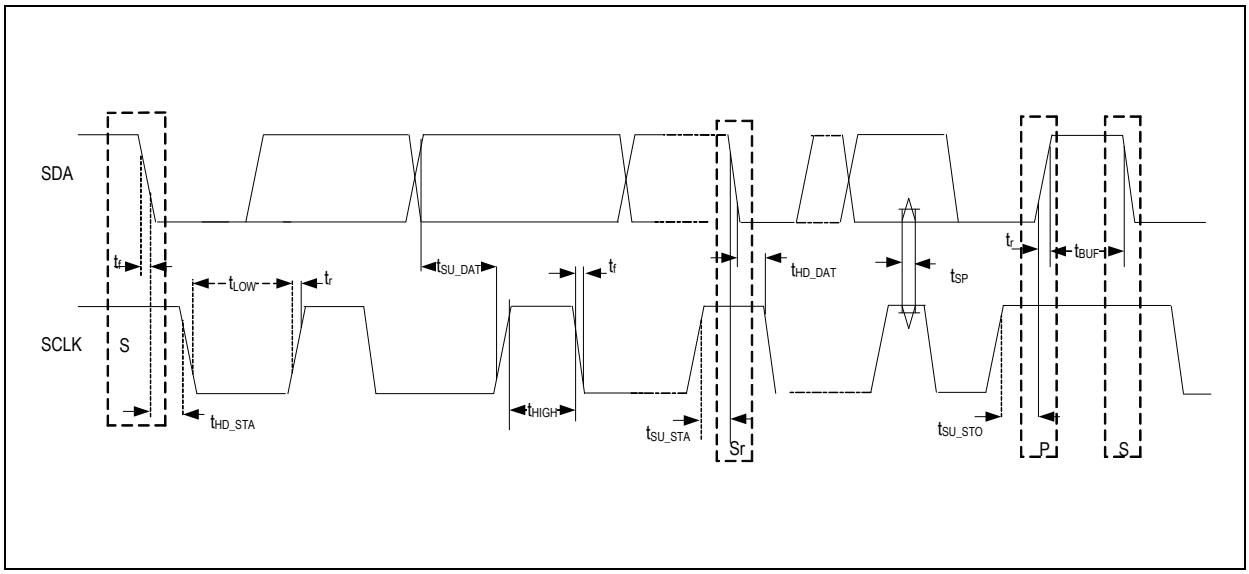


Figure 27. Definition of I²C Timing Parameters



8.3 Register Space

The AS8650B register space consists of configuration registers, control registers and diagnostic registers. All of these registers are accessible through SPI or I²C commands.

Table 21. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description	
0x00	Reserved				Reserved	
0x01	Reserved				Reserved	
0x02	WD Access Control Register	0000_0000 POR_VLDO1	D[7:0]	R/W	0101_1010	WD Configuration Register access Enabled
						Else WD Configuration Register access disabled
0x03	WD Configuration Register	0000_1001 POR_VSUP	D[7:6]	R/W	01	WD disabled
						Else WD enabled
			D[5:3]		Timeout Watchdog mode Window period Twd_tout_period. (Accuracy of the timings is ±25%)	
					000	80 ms
					001	160 ms
					010	320 ms
					011	480 ms
					100	800 ms
					101	1000 ms
					110	2000 ms
					111	4000 ms
			D[2:0]		Window Watchdog mode Window period Twwd_period (50% of above value is trigger window)	
					000	10 ms
					001	40 ms
					010	80 ms
					011	120 ms
					100	160 ms
					101	240 ms
					110	320 ms
					111	400 ms
0x04	WD Trigger Register	0000_0000 POR_VLDO1	D[7:1]	W	Reserved	
			D[0]		Watchdog trigger bit. The microcontroller set this bit within the required window of watchdog timer. After this internal counter is reset and this bit is cleared internally.	

Table 21. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description	
0x05	Device Configuration Register	0110_1101 POR_VSUP	D[7]	R/W	0	LDO3 disable in Standby mode
					1	LDO3 enable in Standby mode
			D[6]		0	LDO3 disable in Receive-only mode
					1	LDO3 enable in Receive-only mode
			D[5]		0	LDO3 disable in Normal mode
					1	LDO3 enable in Normal mode
			D[4]		0	LDO2 disable in Standby mode
					1	LDO2 enable in Standby mode
			D[3]		0	LDO2 disable in Receive-only mode
					1	LDO2 enable in Receive-only mode
			D[2]		0	LDO2 disable in Normal mode
					1	LDO2 enable in Normal mode
			D[1]		0	DCDC disable in Sleep mode
					1	DCDC enable in Sleep mode
0x06	Mode Control Register	0000_0000 POR_VSUP	D[7:6]	R/W	Reserved	
			D[5:4]		Device state (Read-only values)	
					0	Device in Standby mode
					1	Device in Normal mode
					10	Device in Receive-only mode
			D[3:2]		Reserved	
			D[1:0]		00	Standby mode
					01	Normal mode
					10	Receive-only mode
					11	Sleep mode
0x07	Interrupt Register	0000_0000 POR_VSUP	D[7:3]	R	Reserved	
			D[2]		0	No Interrupt
					1	Supply Related Interrupt. The source of interrupt is known by reading Interrupt Source Register 3
			D[1]		0	No Interrupt
					1	Wake-up & temperature Related Interrupt. The source of interrupt is known by reading Interrupt Source Register 2
			D[0]		0	No Interrupt
					1	BUS & Local Failure Related Interrupt. The source of interrupt is known by reading Interrupt Source Register 1

Table 21. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description	
0x08	Interrupt Source Register 1	0000_0000 POR_VSUP	D[7]	R/W	0	No Interrupt
					1	Interrupt due to BUS clamped to dominant
			D[6]		0	No Interrupt
					1	Interrupt due to short TxD & RxD pins
			D[5]		Reserved	
			D[4]		0	No Interrupt
					1	Interrupt due to TxD pin clamped to Dominant
			D[3]		0	No Interrupt
					1	Interrupt due to CANL pin shorted to VCC
			D[2]		0	No Interrupt
					1	Interrupt due to CANL pin shorted to GND
			D[1]		0	No Interrupt
					1	Interrupt due to CANH pin shorted to GND
			D[0]		0	No Interrupt
					1	Interrupt due to CANH pin shorted to VCC
0x09	Interrupt Source Register 2	0000_0000 POR_VSUP	D[7:4]		Reserved	
			D[3]		0	No Interrupt
					1	Interrupt due to junction temperature falling back below T_{jrecv}
			D[2]		0	No Interrupt
					1	Interrupt due to junction temperature exceeding T_{jwarn}
			D[1]		0	No Interrupt
					1	Interrupt due to Local Wake up event on WAKE pin
			D[0]		0	No Interrupt
					1	Interrupt due to Wake up by BUS message (remote wake)

Table 21. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description	
0x0A	Interrupt Source Register 3	0000_0000 POR_VSUP	D[7]	R/W	0	No Interrupt
					1	Interrupt due to VLDO3_POK_flag set
			D[6]		0	No Interrupt
					1	Interrupt due to VLDO3_UV_flag set
			D[5]		0	No Interrupt
					1	Interrupt due to VLDO2_POK_flag set
			D[4]		0	No Interrupt
					1	Interrupt due to VLDO2_UV_flag set
			D[3]		0	No Interrupt
					1	Interrupt due to V5V_POK_flag set
			D[2]		0	No Interrupt
					1	Interrupt due to V5V_UV_flag set
			D[1]		0	No Interrupt
					1	Interrupt due to VSUP_POK_flag set
			D[0]		0	No Interrupt
					1	Interrupt due to VSUP_UV_flag set
0x0B	Reserved	0000_0000 POR_VSUP	D[7:0]		Reserved	
0x0C	BUS Status Register	0000_0000 POR_VSUP	D[7]	R	BUS clamped to dominant	
			D[6]		TxD & RxD pins short	
			D[4]		TxD pin clamped to Dominant	
			D[3]		CANL pin shorted to VCC	
			D[2]		CANL pin shorted to GND	
			D[1]		CANH pin shorted to GND	
			D[0]		CANH pin shorted to VCC	
0x0D	Temperature Status Register	0000_0000 POR_VSUP	D[7:2]	R	Reserved	
			D[1]		OTM 140 Recovery flag	
			D[0]		OTM 160 Warning flag	
0x0E	Supply Status Register	1010_1010 POR_VSUP	D[7]	R	VLDO3_POK_flag	
			D[6]		VLDO3_UV_flag	
			D[5]		VLDO2_POK_flag	
			D[4]		VLDO2_UV_flag	
			D[3]		V5V_POK_flag	
			D[2]		V5V_UV_flag	
			D[1]		VSUP_POK_flag	
			D[0]		VSUP_UV_flag	

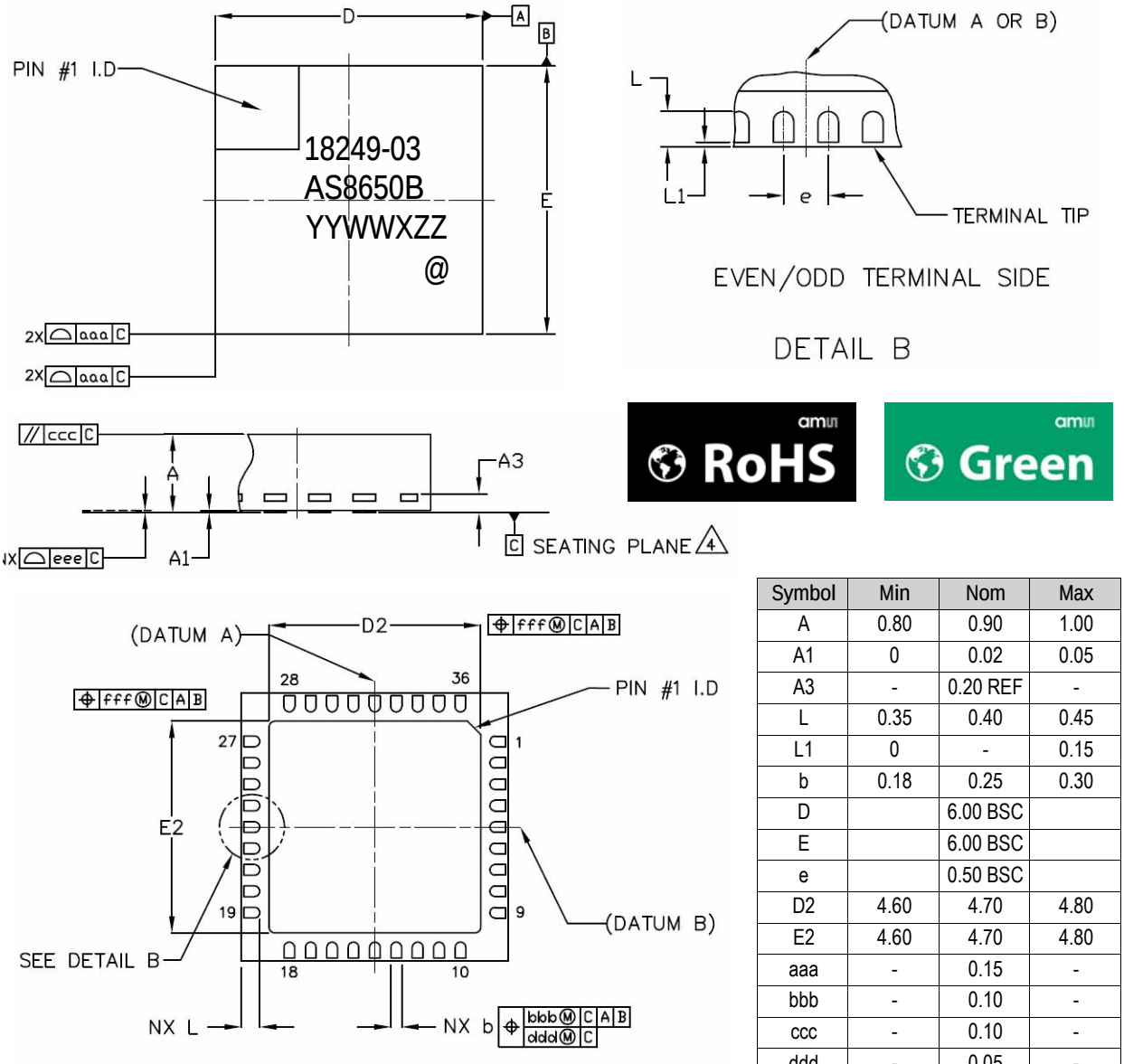
Table 21. Configuration Registers

Addr	Register Name	POR Value	Bit	Type	Description
0x0F	RESET Reason Register	0000_0000 POR_VSUP		R	These bits are cleared on microcontroller read
			D[7]		Reserved
			D[6]		Sleep mode exit by Local Wake up on WAKE pin
			D[5]		Sleep mode exit by Remote wake
			D[4]		Window Watchdog failure
			D[3]		Timeout Watchdog failure
			D[2]		Start-up Watchdog failure
			D[1]		Undervoltage on VLDO1
			D[0]		OTM Shutdown flag
0x10	Backup Register	0000_0000 POR_VSUP	D[7:0]	R/W	OTP_BITS[32:25] / MCU Backup Data
0x11			D[7:0]		OTP_BITS[40:33] / MCU Backup Data
0x12			D[7:0]		OTP_BITS[48:41] / MCU Backup Data
0x13			D[7:0]		OTP_BITS[56:49] / MCU Backup Data
0x14			D[7:0]		{1'b0, OTP_BITS[63:57]} / MCU Backup Data
0x15			D[7:0]		{2'd0, Slave address[6:1]}/MCU Backup Data
0x16			D[7:0]		10bit_slave_address[3:0]/MCU Backup Data
0x17			D[7:0]		MCU Backup Data

9 Package Drawings and Markings

The device is available in a 36-pin QFN (6x6x0.9) package.

Figure 28. Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.20 REF	-
L	0.35	0.40	0.45
L1	0	-	0.15
b	0.18	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
D2	4.60	4.70	4.80
E2	4.60	4.70	4.80
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N	36		

Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.

Marking Description:

YY	WW	X	ZZ	@
Last two digits of the current year	Manufacturing Week	Assembly plant identifier	Assembly traceability code	Sublot identifier

Revision History

Revision	Date	Owner	Description
1.0	28 Mar, 2012	hgl	Initial release for AS8650B
1.1	Jan 11, 2013		Updated Ordering Information

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 22.

Table 22. Ordering Information[1]

Ordering Code	Marking	Description	Delivery Form	Package
AS8650B-ZQFP-01	AS8650B	AS8650B Power Management device with high-speed CAN Interface (standard configuration)	Tape & Reel in Dry Pack (1 reel = 4000 units)	36-pin QFN (6x6x0.9)
AS8650B-ZQFM-01	AS8650B		Tape & Reel in Dry Pack (1 reel = 1000 units)	36-pin QFN (6x6x0.9)

1. The AS8650B provides various configuration options during production. For more information, please contact our sales office.

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