austriamicrosystems AG

is now

ams AG

The technical content of this austriamicrosystems datasheet is still valid.

Contact information:

Headquarters:
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

AS8220A

FlexRay™ Basis Transceiver

Objective Data Sheet

1 General Description

This objective data sheet describes the intended functionality of the AS8220A bus transceiver. As long the device is not fully qualified, the parameters are not characterized in the means that parameters may change or can be updated during final product qualification and characterization. This document shows the objective of the AS8220A and this document is subjected to change without notice.

The AS8220A is a high-speed automotive transceiver for fault tolerant and high speed applications, operating as the bi-directional interface between a generic communication controller and the twisted pair copper wires. The device enables two-way communication with the microcontroller with full mode handling, including the low-power modes.

The transmission rates up to 10Mbps as well as the implemented Bus Guardian interface enables this transceiver the usage in fault tolerant and hard real-time applications in the stringent automotive environment. An extended diagnostic interface, offers advanced bus-failure detection capabilities with the intelligent combination of bus-current measurement and logical comparators.

A thermal sensor circuit with an integral shutdown mechanism prevents damage to the device in extreme temperature conditions. The symmetrical transient control for the high- and low-side driver for both the bus-minus and bus-plus line allows an ideal balance of communications over different network topologies, with excellent EMC performance. The product is available in SSOP14 package.

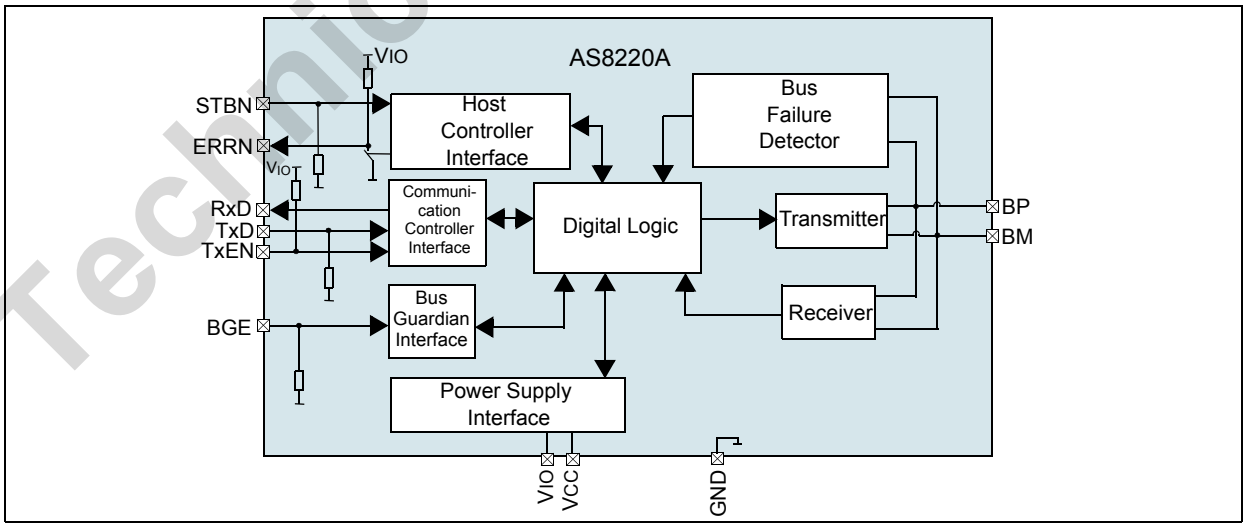
2 Key Features

- Data transfer up to 10 Mbps
- Compliant with FlexRay Electrical Physical Layer Specification V2.1 Rev. B
- Excellent EMC performances. High common mode range insure excellent EMI
- Enable pin for an optional bus guardian
- Automatic thermal shutdown protection
- Low standby current
- Supports 2.5, 3, 3.3, 5 V micro controllers and automatically adapts to interface levels
- Protection against damage due to short circuit conditions on the bus (positive and negative battery voltage)
- Operating temperature range -40ºC to +125ºC

3 Applications

The device is ideal for high speed automotive bus systems, backbone bus and gateways, X-by-wire systems, redundant bus systems, bus topologies with Active Stars, and safety critical applications. Designed for FlexRay, where the basic features are demanded.

Figure 1. Block Diagram



Technical content still valid
ams AG

Contents

1 General Description 1
2 Key Features 1
3 Applications 1
4 Pin Assignments 4
4.1 Pin Descriptions 4
5 Absolute Maximum Ratings 5
6 Electrical Characteristics 6
7 Typical Operating Characteristics 11
8 Detailed Description 12
8.1 Block Description 12
8.2 Events 12
8.3 Operating Modes 12
8.3.1 NORMAL mode 13
8.3.2 STANDBY mode 13
8.4 Non Operating Mode 13
8.4.1 Power Off 13
8.5 Undervoltage Events 13
8.5.1 Undervoltage VIO 13
8.5.2 Undervoltage VCC 13
8.6 Power On/Off Events 14
8.7 System Description 14
8.8 Fail Silent Behavior 15
8.8.1 State transitions due to under voltage detection 15
8.8.2 State transitions due to voltage recovery detection 15
8.9 Mode Transitions 15
8.9.1 ERRN Signalling 16
8.10 Loss of ground 16
8.11 Error Flags Description 16
8.11.1 Bus error 16
8.11.2 Low current on BP high side driver 16
8.11.3 Low current on BP low side driver 16
8.11.4 Low current on BM high side driver 16
8.11.5 Low current on BM low side driver 16
8.11.6 High current on BP high side driver 16
8.11.7 High current on BP low side driver 16
8.11.8 High current on BM high side driver 17
8.11.9 High current on BM low side driver 17
8.11.10 BP open line 17
8.11.11 BM open line 17
8.11.12 BP short circuit to VCC 17
8.11.13 BP short circuit to GND 17
8.11.14 BM short circuit toVCC 17
8.11.15 BM short circuit to GND 17
8.11.16 Short circuit between BP and BM 17
8.11.17 Over temperature 17

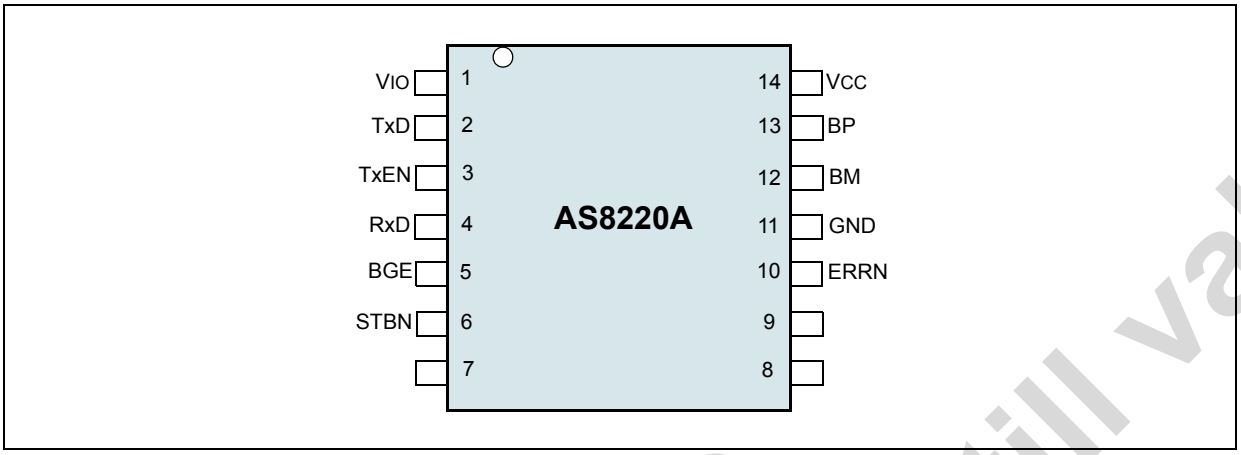
Technical content still valid
ams AG

8.11.18 TxEN_BGE timeout 17
8.11.19 Error flag 17
8.12 Status Flags Description 17
8.12.1 Power on flag 17
8.13 Transmitter 18
8.14 Receiver 20
8.14.1 Bus activity and idle detection (only in NORMAL mode) 20
8.14.2 Bus data detection (NORMAL mode) 20
8.14.3 Receiver test signal 22
8.14.4 Transceiver Timing 23
8.15 Test Circuits 24
9 Appendix 25
10 Package Drawings and Markings 31
11 Ordering Information 32

ams AG
Technical content still valid

4 Pin Assignments

Figure 2. Pin Assignments SSOP14 Package



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
VIO	1	I/O supply voltage
TxD	2	Transmit data input
TxEN	3	Transmitter enable input
RxD	4	Receive data output
BGE	5	Bus guardian enable input
STBN	6	Standby input
ERRN	10	Error diagnosis output
GND	11	Ground
BM	12	Bus line Minus
BP	13	Bus line Plus
VCC	14	Supply Voltage

Technical Content still valid
ams AG

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Supply Voltage (V_{CC})	-0.3	+7.0	V	
Supply Voltage (V_{IO})	-0.3	+7.0	V	
DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN	-0.3	V_{IO} + 0.3	V	$V_{IO} < V_{CC}$
DC Voltage at BP and BM	-40	+50	V	
Input current (latchup immunity)	-100	100	mA	According to JEDEC 78
Electrostatic discharge at bus lines BP and BM	-4	+4	kV	According to AEC-Q100-002
Electrostatic discharge	-2	+2	kV	According to AEC-Q100-002
Transient voltage on BP, BM	-200	+200	V	According to ISO7637 part3 test pulses a and b; class C; RL=45 W, CL= 100 pF; (see Figure 17 on page 24).
Total power dissipation (all supplies and outputs)		150	mW	
Storage temperature	-55	+150	ºC	
Junction temperature	-40	+150	ºC	
Package body temperature[1]		250	ºC	
Humidity non-condensing	5	85	%	

1. The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

Technical content still valid ams AG

6 Electrical Characteristics

T_{vj} = -40 to +150 ºC, V_{CC} = +4.75V to +5.25V, V_{IO} = +2.2 to V_{CC}, R_L= 45Ω, C_L= 100 pF unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage						
T_{amb}	Ambient temperature		-40		+125	ºC
V_{CC}-V_{IO}	Difference of supplies		-0.1		3.05	V
I_{CC}	V_{CC} current consumption	STANDBY Mode[1] V_{CC} = 0V to +5.25V	-5		30	µA
		NORMAL mode, driver enabled	0		45	mA
		NORMAL Mode, driver enabled, R_{BUS} = ∞Ω	0		15	mA
		NORMAL mode, driver disabled	0		10	mA
I_{IO}	V_{IO} current consumption	STANDBY mode[1] V_{IO} = 0V to +5.25V	-5		5	µA
		NORMAL Mode	0		1	mA
State Transitions						
t_{STBN_RxD}	Delay STBN high to RxD high with wake flag set		1		50	µs
$t_{STANDBY}$	go-to STANDBY hold time	INH1 low = 20% V_{BAT}	10		70	µs
Transmitter						
$V_{BUS_DIFF_D0}$	Differential bus voltage low in NORMAL mode (Data0)	$V_{BPdata0}$ - $V_{BMdata0}$; 40Ω < R_L < 55Ω	-2		-0.6	V
$V_{BUS_DIFF_D1}$	Differential bus voltage high in NORMAL mode (Data1)	$V_{BPdata1}$ - $V_{BMdata1}$; 40Ω < R_L < 55Ω	0.6		2	V
ΔV_{BUS_DIFF}	Matching between Data0 and Data1 differential bus voltage in NORMAL mode	$V_{BUS_DIFF_D0}$ - $V_{BUS_DIFF_D1}$ 40Ω < R_L < 55Ω	-200		200	mV
$V_{BUS_COM_D0}$	Common mode bus voltage in case of Data0 in NORMAL mode	$V_{BPdata0}$/2 + $V_{BMdata0}$/2 40Ω < R_L < 55Ω	0.4 * V_{CC}		0.6 * V_{CC}	V
$V_{BUS_COM_D1}$	Common mode bus voltage in case of Data1 in NORMAL mode	$V_{BPdata1}$/2 + $V_{BMdata1}$/2 40Ω < R_L < 55Ω	0.4 * V_{CC}		0.6 * V_{CC}	V
ΔV_{BUS_COM}	Matching between Data0 and Data1 common mode voltage	$V_{BUS_COM_D0}$ - $V_{BUS_COM_D1}$ 40Ω < R_L < 55Ω	-200		200	mV
$V_{BUS_DIFF_Idle}$	Absolute differential bus voltage in idle mode				30	mV
$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute max current when BP is shorted to BM	V_{BP}=V_{BM}			+100	mA
$IBP_{GNDShortMax}$	Absolute max current when BP is shorted to GND	V_{BP}= 0V			+100	mA
$IBM_{GNDShortMax}$	Absolute max current when BM is shorted to GND	V_{BM}= 0V			+100	mA

Technical content still valid ams AG

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$IBP_{-5VShortMax}$	Absolute max current when BP is shorted to -5 V	V_{BP}= -5V			+100	mA
$IBM_{-5VShortMax}$	Absolute max current when BM is shorted to -5 V	V_{BM}= -5V			+100	mA
$IBP_{27VShortMax}$	Absolute max current when BP is shorted to 27 V	V_{BP}= 27V			+100	mA
$IBM_{27VShortMax}$	Absolute max current when BM is shorted to 27 V	V_{BM}= 27V			+100	mA
$IBP_{48VShortMax}$	Absolute max current when BP is shorted to 48 V	V_{BP}= 48V			+100	mA
$IBM_{48VShortMax}$	Absolute max current when BM is shorted to 48 V	V_{BM}= 48V			+100	mA
t_{TxD_BUS01}	Delay time from TxD to BUS positive edge	t_{TxD_RISE} = 5ns			50	ns
t_{TxD_BUS10}	Delay time from TxD to BUS negative edge	t_{TxD_FALL} = 5ns			50	ns
$t_{TxD_MISMATCH}$	Delay time from TxD to BUS mismatch	t_{TxD_BUS10} - t_{TxD_BUS01}	-4		4	ns
t_{BUS10}	Fall time differential bus voltage	80% - 20% of V_{BUS}	3.75		18.75	ns
t_{BUS01}	Rise time differential bus voltage	20% - 80% of V_{BUS}	3.75		18.75	ns
$t_{TxEN_BUS_Idle_Active}$	Delay time from TxEN to bus active				50	ns
$t_{TxEN_BUS_Active_Idle}$	Delay time from TxEN to bus idle				50	ns
$t_{TxEN_MISMATCH}$	Delay time from TxEN to bus mismatch	$\lvert t_{TxEN_BUS_Idle_Active}$ - $t_{TxEN_BUS_Active_Idle} \rvert$			50	ns
$t_{BGE_BUS_Idle_Active}$	Delay time from BGE to bus active				50	ns
$t_{BGE_BUS_Active_Idle}$	Delay time from BGE to bus idle				50	ns
$t_{BUS_Idle_Active}$	Differential bus voltage transition time: idle to active				30	ns
$t_{BUS_Active_Idle}$	Differential bus voltage transition time: active to idle				30	ns
$t_{TxEN_timeout}$	TxEN timeout		0.64		3.07	ms
Receiver						
R_{BP}, R_{BM}	BP, BM input resistance	Idle mode; R_{BUS}=∞	10		40	KΩ
R_{DIFF}	BP, BM differential input resistance	Idle mode; R_{BUS}=∞	20		80	KΩ
V_{BPidle}, V_{BMidle}	Idle voltage in NORMAL mode on pin BP, BM	NORMAL mode; V_{TxEN} = V_{IO}	0.4* V_{CC}	0.5* V_{CC}	0.6* V_{CC}	V
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in STANDBY mode on pin BP, BM	STANDBY mode	-0.2	0	+0.2	V

Technical content still valid
ams AG

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{BPidle}	Absolute idle output current on pin BP	-40V < V_{BP} < 50V	0		7.5	mA
I_{BMidle}	Absolute idle output current on pin BM	-40V < V_{BM} < 50V	0		7.5	mA
I_{BPleak}, I_{BMleak}	Absolute leakage current, when not powered	V_{BP} = V_{BM} = 5V, V_{CC} = 0V, V_{BAT} = 0V; V_{IO} = 0V	0		+10	uA
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	NORMAL mode -10V < (V_{BP} , V_{BM}) < 15V	150	225	400	mV
$V_{BUSActiveLow}$	Activity detection differential input voltage low	NORMAL mode -10V < (V_{BP} , V_{BM})< 15V	-400	-225	-150	mV
V_{Data1}	Data1 detection differential input voltage	Pre-condition: activity already detected. NORMAL mode. -10V < (V_{BP} , V_{BM})< 15V	150	225	300	mV
V_{Data0}	Data0 detection differential input voltage	Pre-condition: activity already detected. NORMAL mode. -10V < (V_{BP} , V_{BM})< 15V	-300	-225	-150	mV
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	$2 \times (\lvert\lvert V_{Data0}\rvert - \lvert V_{Data1}\rvert\rvert) / (\lvert V_{Data0}\rvert + \lvert V_{Data1}\rvert)^2$			10	%
t_{BUS_RxD10}	Delay from BUS to RxD negative edge	C_{RxD} = 15 pF [3]			80	ns
t_{BUS_RxD01}	Delay from BUS to RxD positive edge	C_{RxD} = 15 pF [3]			80	ns
t_{BIT}	Bit time	C_{RxD} = 15 pF [3]	54			ns
t_{RxD_ASYM}	Delay time from BUS to RxD mismatch	C_{RXD}=15 pF; $\lvert t_{BUS_RxD10} - t_{BUS_RxD01}\rvert$ [3]			5	ns
t_{RxD_FALL}	Fall time RxD voltage	80% - 20% of V_{RxD}; C_{RxD}=15 pF [3]			5	ns
t_{RxD_RISE}	Rise time RxD voltage	20% - 80% of V_{RxD}; C_{RxD}=15 pF [3]			5	ns
$t_{BUSIdleDetection}$	Idle detection time	V_{BUS}: 400mV → 0V	50		200	ns
$t_{BUSActivitiyDetection}$	Activity detection time	V_{BUS}: 0V → 400mV	100		250	ns
$t_{BUSIdleReaction}$	Idle reaction time	V_{BUS}: 400mV → 0V	50		300	ns
$t_{BUSActivityReaction}$	Activity reaction time	V_{BUS}: 0V → 400mV	100		350	ns
Supply Voltage Monitor						
V_{CCTHH}	V_{CC} under-voltage recovery threshold		3.5		4.5	V
V_{CCTHL}	V_{CC} undervoltage detection threshold		2.5		3.5	V
V_{IOTHH}	V_{IO} undervoltage recovery threshold		1.25		2.0	V
V_{IOTHL}	V_{IO} undervoltage detection threshold		0.75		1.5	V

Technical content still valid ams AG

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{UV_DETECT}	Detection time for undervoltage at V_{BAT}, V_{CC}, V_{IO}		100		700	ms
t_{UV_REC}	Detection time for undervoltage recovery at V_{CC}, V_{IO}		0.7		5	ms
Bus Error Detection						
I_{THL}	Absolute bus current for low current detection	NORMAL mode, Transmitter enabled		5		mA
I_{THH}	Absolute bus current for high current detection	NORMAL mode, Transmitter enabled		40		mA
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	NORMAL mode, Transmitter enabled		225		mV
t_{BUS_ERROR}	Bus error detection time	NORMAL mode, Transmitter enabled		20		µs
Over Temperature						
OT_{TH}	Over temperature threshold		150		180	ºC
OT_{TL}	Over temperature hysteresis		10		20	ºC
Communication Controller Interface						
V_{TxDIH}	Threshold for detecting TxD as on logical high				0.7* V_{IO}	V
V_{TxDIL}	Threshold for detecting TxD as on logical low		0.3* V_{IO}			V
I_{TxDIH}	TxD high level input current		30		100	µA
I_{TxDIL}	TxD low level input current		-5		5	µA
V_{TxENIH}	Threshold for detecting TxEN as on logical high				0.7* V_{IO}	V
V_{TXENIL}	Threshold for detecting TxEN as on logical low		0.3* V_{IO}			V
I_{TxENIH}	TxEN high level input current		-5		5	µA
I_{TxENIL}	TxEN low level input current		-100		-30	µA
V_{RxDOH}	RxD high level output voltage	I_{RxD} = -4mA, V_{IO} = 5V	0.8* V_{IO}		1.0* V_{IO}	V
V_{RxDOL}	RxD low level output voltage	I_{RxD} = 4mA, V_{IO} = 5V	0		0.2* V_{IO}	V
Host Interface						
V_{STBNIH}	Threshold for detecting STBN as on logical high				0.7* V_{IO}	V
V_{STBNIL}	Threshold for detecting STBN as on logical low		0.3* V_{IO}			V
I_{STBNIH}	STBN high level input current		30		100	µA

Technical content still valid ams AG

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{STBNIL}	STBN low level input current		-5		5	µA
$t_{STBN_DEB_STBY}$	STBN de-bouncing time STANDBY mode		0.1		40	µs
$t_{STBN_DEB_NORM}$	STBN de-bouncing time NORMAL mode		0.1		2	µs
V_{ERRNOH}	ERRN high level output voltage	I_{ERRN} = -4mA, V_{IO} = 5V	0.8* V_{IO}		1.0* V_{IO}	V
V_{ERRNOL}	ERRN low level output voltage	I_{ERRN} = 4mA, V_{IO} = 5V	0		0.2* V_{IO}	V
Bus Guardian Interface						
V_{BGEIH}	Threshold for detecting BGE as on logical high				0.7* V_{IO}	V
V_{BGEIL}	Threshold for detecting BGE as on logical low		0.3* V_{IO}			V
I_{BGEIH}	BGE high level input current		30		100	µA
I_{BGEIL}	BGE low level input current		-5		5	µA

1. STBN, ERRN, TxD, RxD, TxEN, and BGE open
2. Test condition: $(V_{BP} + V_{BM}) / 2 = 2{,}5V \pm 5\%$
3. For test signal (see Figure 15)

ams AG
Technical content still valid

7 Typical Operating Characteristics

Figure 3.

Figure 4.

Figure 5.

Figure 6.

Figure 7.

Figure 8.

ams AG
Technical content still valid

8 Detailed Description

The AS8220A is a high-speed fault tolerant device operating as an interface between a generic controller and the copper wire physical bus. The AS8220A is designed to extend the application range for high speed and safety critical time triggered bus systems in an automotive environment. The drivers are short circuit protected against the positive and negative supply voltage to increase the robustness and reliability of automotive systems. The AS8220A operates at baudrates up to 10 Mbps to increase the bandwidth for automotive applications.

Block Description

The electrical AS8220A high-speed bus-system transceiver is the interface between a FlexRay™ network node module and the channel. The transceiver provides differential transmit and receive capability to the bus, allowing the node module bidirectional time multiplexed binary data stream transfer. Besides the transmit and receive function, the transceiver provides low power management, supply voltage monitoring (under voltage detection) as well as bus failure detection and represents a ESD-protection barrier between the bus and the ECU.

The AS8220A consists of 8 different functional blocks (see Figure 1):

Table 4. Functional Blocks

Functional Block	Short Description
Host Controller Interface (HCI)	Digital interface between the transceiver and the host controller (HC) The host interface comprises the read out handler, which delivers failure and status information via the ERRN pin to the host controller.
Communication Controller Interface (CCI)	Digital interface between the transceiver and the FlexRay communication controller (CC)
Bus Guarding Interface (BGI)	Digital interface between the transceiver and the FlexRay bus guardian (BG)
Power Supply Interface (PSI)	The power supply interface consists of an sub functional block, the voltage monitor (VM) and includes two analogue inhibit outputs for signalling the internal state of the transceiver
Internal Logic (IL)	The digital signals from the functional blocks of the device are fed into the internal logic where the forwarding of FlexRay messages from analogue side to digital interfaces and vice versa is done. The state machine is performed in this block and is dealing the error, wake and power-on flags.
Bus Failure Detector (BFD) Temperature Protection (TP)	The bus failure detector is directly connected to the bus pins, in order to detect several external failure conditions which may occur on the bus. The temperature protection turns off the output driver when reaching the specified internal temperature in order to protect the device.
Transmitter	The transmitter provides the bus signals as specified on the bus lines.
Receiver	The receiver captures FlexRay valid signals on the bus lines and provides received data streams to the internal logic

Events

Transitions in order to change between the operation modes are possible only when events are detected. The device supports two type of events, events on the host controller interface (STBN) and detection of undervoltage or supply voltage recovery. Whenever an event is recognized, a transition can be performed.

Operating Modes

The AS8220A provides the following operating modes:

- NORMAL: non low power mode
- STANDBY: low power mode

Technical content still valid
ams AG

NORMAL mode

In this mode the transceiver is able to send and receive data signals on the bus. TxEN and BGE control the state of the transmitter. RxD reflects the bus data and reflect the bus state. In this mode, the transmitter state can be selected as shown in the Table 5. In case the over-temperature flag is set the transmitter is disabled. The bus wires are terminated to VCC/2 via receiver input resistances.

Table 5. Transmitter State

BGE	TxEN	TxD	Transmitter state	Bus State
H	L	H	Enabled	Data1 (BP is driven high, BM is driven low)
H	L	L	Enabled	Data0 (BP is driven low, BM is driven High)
X	H	X	Disabled	Idle (BP and BM are not driven)
L	X	X	Disabled	Idle (BP and BM are not driven)

- If the differential bus voltage is higher than $V_{BUSActivehigh}$ or lower than $V_{BUSActivelow}$ for a time longer than $t_{BUSActivityDetection}$, then activity is detected on the bus (Bus = active), RxD is released.
- If, after the activity detection, the differential bus voltage is higher than V_{Data1}, RxD is high.
- If, after the activity detection, the differential bus voltage is lover than V_{Data0}, RxD is low.
- If the absolute differential bus voltage is lower than $V_{BUSActivehigh}$ and higher than $V_{BUSActivelow}$ for a time longer than $t_{BUSIdleDetection}$, then idle is detected on the bus (Bus=idle), RxD is switched to logical “high”

STANDBY mode

In this mode the transceiver is not able to send and receive data signals from the bus. The power consumption is significantly reduced respect the NORMAL mode. The bus wires are terminated to GND (bus state: Idle_LP).

Non Operating Mode

The AS8220A provides the following non operating mode:

Power Off

In this mode the transceiver is not able to operate. RxD is set to high and ERRN is set to low. The bus wires are not connected to GND (bus state: Idle_HZ).

Undervoltage Events

Undervoltage VIO

When VIO voltage falls below V_{IOTHL} for a time longer than t_{UV_DETECT} then the undervoltage VIO flag is set and it is reset when VIO exceeds the voltage threshold V_{IOTHH} for a time longer than t_{UV_REC}. The flag can be set or reset in all the operation modes. The flag is reset at power off.

Undervoltage VCC

When VCC voltage falls below V_{CCTHL} for a time longer than t_{UV_DETECT} then the undervoltage VCC flag is set and it is reset when VCC exceeds the voltage threshold V_{CCTHH} for a time longer than t_{UV_REC}. The flag can be set or reset in all the operation modes. The flag is reset at power off.

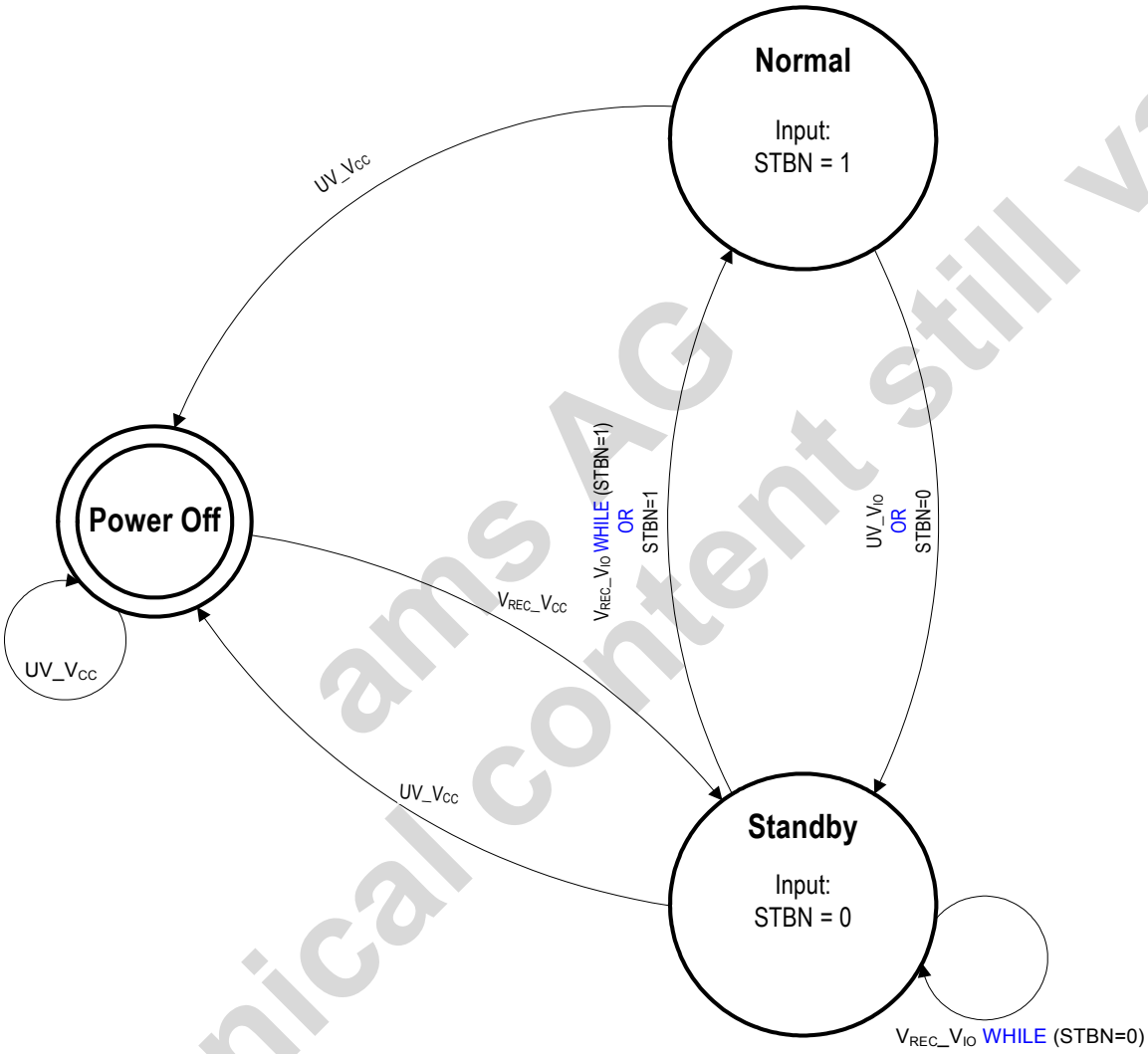
Technical content still valid ams AG

Power On/Off Events

- Starting from power off mode a power on event occurs in case undervoltage flag is reset.
- Starting from every operation mode a power off event occurs in case VCC undervoltage flag is set.

System Description

Figure 9. State Diagram



Note: In Table 7 the corresponding transition table is shown

Prefix of "WHILE" is always the event and suffix in brackets checks the flags or in case of STBN the input condition. For example: $V_{REC}_V_{BAT}$ WHILE (STBN=1)

After the event VIO supply voltage recovery is detected, the transition is performed if STBN is "high".

Legend:

UV_V_{IO}: Undervoltage event and/or flag for VIO supply voltage

UV_V_{CC}: Undervoltage event and/or flag for VCC supply voltage

$V_{REC}_V_{IO}$: Voltage recovery event and/or flag for VIO supply voltage

$V_{REC}_V_{CC}$: Voltage recovery event and/or flag for VCC supply voltage

ams AG
Technical content still valid

Fail Silent Behavior

In order to be fail silent, undervoltage detection on the two power supplies V_{IO} and V_{CC} is implemented

- V_{IO}**:** Supply voltage for I/O digital level adaptation
- V_{CC}**:** Supply voltage (+5V)

State transitions due to under voltage detection

- In case of V_{IO} undervoltage is detected, STANDBY mode will be entered regardless of the voltage present on pin STBN.
- In case V_{CC} undervoltage is present, the device will enter power off mode (bus state: Idle_HZ), regardless on supply voltage at V_{IO} and the voltage present on STBN.

State transitions due to voltage recovery detection

- Starting from the power off, the device enters STANDBY mode only in case VCC undervoltage flag is reset..
- When $V_{CC} \leq V_{CCTHL}$ the device is in power off state and the bus wires are not terminated (bus state: Idle_HZ).

Mode Transitions

In case all the undervoltage flags are reset the operation mode is selected by STBN according to Table 6.

Table 6. Pin Signalling and Operating modes

Inputs	Operation Mode	OutPut	
STBN		**RxD**	**RxEN**
H	NORMAL	L Bus = Data_0	L Bus = Active
		H Bus = Idle or Data_1	H Bus = Idle
L	STANDBY	H	H

Where: H = Digital level high
L = Digital level low
x = Do not care
Float = The analog output is not driven

Table 7. Transition Table

Supply Voltage Flag Event			Host Event	
Intial Mode	**V_{IO}**	**V_{CC}**	**STBN**	**Next Mode**
Normal	L	L	H→L	Standby
	L→H	L	X	
Standby	H→L	L	H	Normal
	L	L	L→H	
Power Off	X	H→L	X	Standby
Any	X	L→H	X	Power Off

ams AG
Technical content still valid

ERRN Signalling

The ERRN signalling is shown in Table 8.

Table 8. ERRN signalling

SUPPLY VOLTAGE FLAG EVENT V_{IO}		
	STBN	ERRN
L	H	not failure
L	L	H
L	X	L

Note: ERROR means the logic OR of the error flags

Loss of ground

In case the ground of the device is disconnected and the host pins are open, the bus lines are switched to Idle_HZ.

Error Flags Description

Bus error

The bus error flag is set when 2 consecutive rising edges on the TxD pin without any rising edge on the RxD pin are detected or when 2 consecutive falling edges on the TxD pin without any falling edge on the RxD pin are detected. This flag is reset when a rising edge on the TxD pin is followed by a rising edge on RxD pin before of the next TxD rising edge or when a falling edge on the TxD pin is followed by a falling edge on RxD pin before of the next TxD falling edge. This flag can be set or reset only in NORMAL mode when the transmitter is enabled. The flag is reset at power off.

Low current on BP high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

Low current on BP low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

Low current on BM high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

Low current on BM low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is lower than I_{THL} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

High current on BP high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

High current on BP low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BP pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

ams AG
Technical content still valid

High current on BM high side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data0 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

High current on BM low side driver

This flag can only be set/reset in NORMAL mode when the driver is enabled and during the transmission of a stable Data1 longer than t_{BUS_ERROR}. If the absolute value of the BM pin current is higher than I_{THH} after t_{BUS_ERROR} since the driver enable signal then the flag is set otherwise it is reset. The flag is reset at power off.

BP open line

This flag is the logical “AND” between: low current on BP high side and low current on BP low side.

BM open line

This flag is the logical “AND” between: low current on BM high side and low current on BM low side.

BP short circuit to V_{CC}

This flag is the logical “AND” between: low current on BP high side and high current on BP low side.

BP short circuit to GND

This flag is the logical “AND” between: high current on BP high side and low current on BP low side.

BM short circuit toV_{CC}

This flag is the logical “AND” between: low current on BM high side and high current on BM low side.

BM short circuit to GND

This flag is the logical “AND” between: high current on BM high side and low current on BM low side.

Short circuit between BP and BM

This flag can only be set or reset in NORMAL mode when the driver is enabled. After a time t_{BUS_ERROR} since TxD edge if the absolute value of the differential bus voltage is lower than V_{SHORT} then the flag is set otherwise it is reset. he flag is reset at power off.

Over temperature

This flag can only be set or reset in the non low power modes. The flag is set when the junction temperature exceeds OT_{TH} and it is reset when the junction temperature falls below OT_{TL}.

TxEN_BGE timeout

This flag can only be set in NORMAL mode when the driver is enabled (TxEN is low and BGE is high) for a time longer than t_{TxEN_max}. It is reset every transition on TxEN or BGE or if the device exits NORMAL mode. If the flag is set the driver is disabled.

Error flag

This flag is set if at least one error flag or if V_{IO} flag is set and it is reset if none of the previous flag is set.

Status Flags Description

Power on flag

The power on flag is set leaving the power off state and it is reset entering a low power mode after a non low power mode.

Technical content still valid
ams AG

Transmitter

The transmitter generates out of a digital input signal on TxD the FlexRay differential bus voltage. The transmitter is only active in NORMAL mode when BGE is on logical high and TxEN is on logical low.

Figure 10. Transmitter characteristics (TxD → BUS)

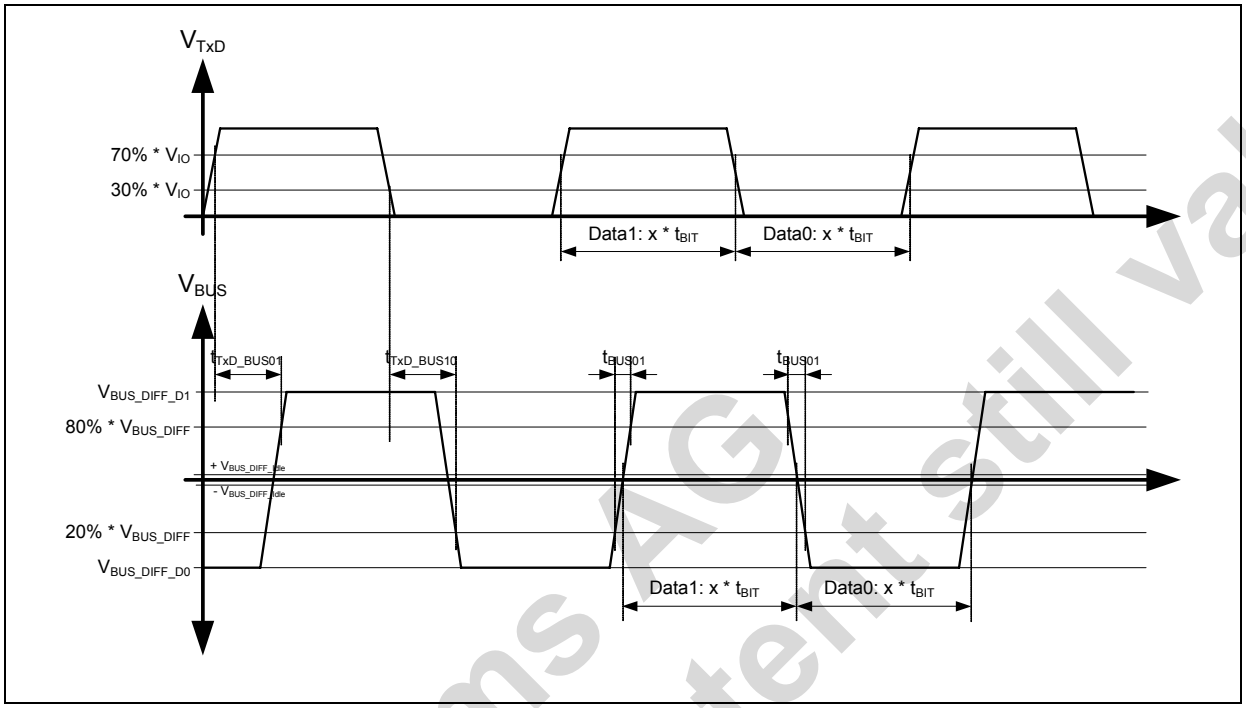
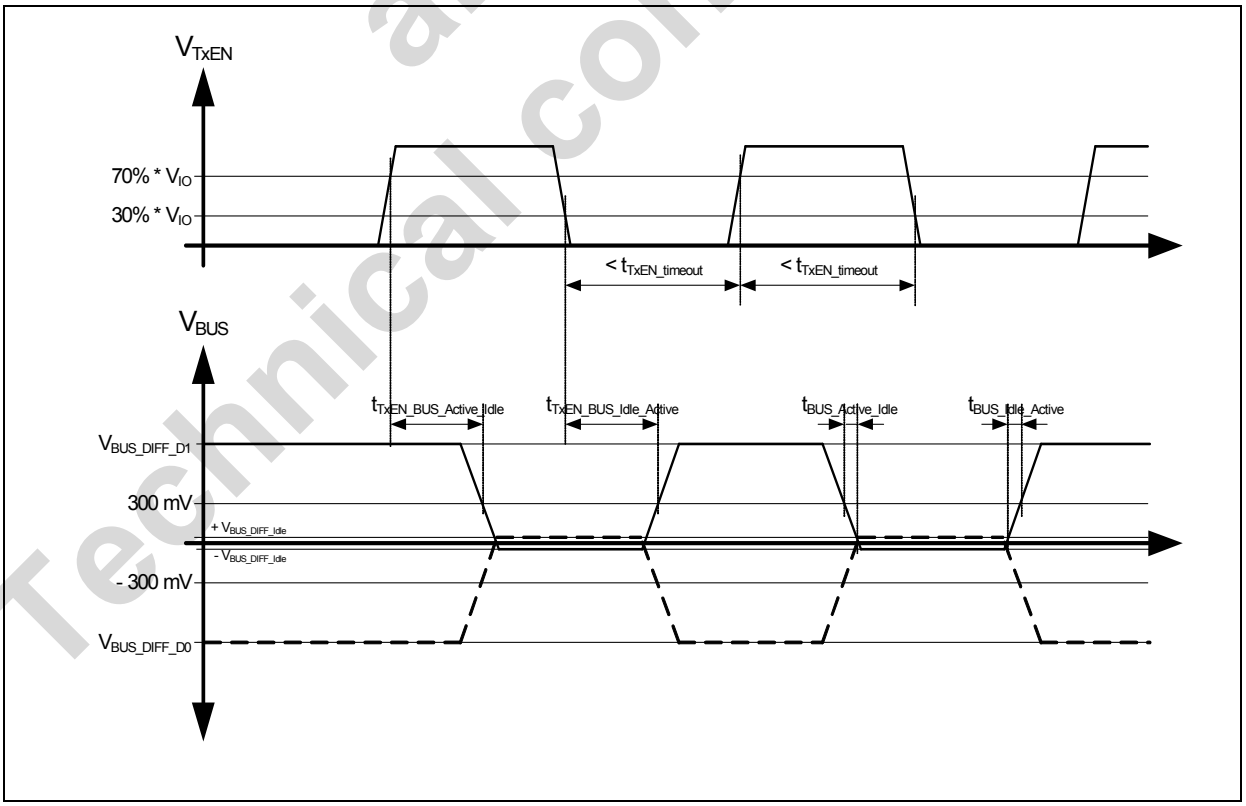
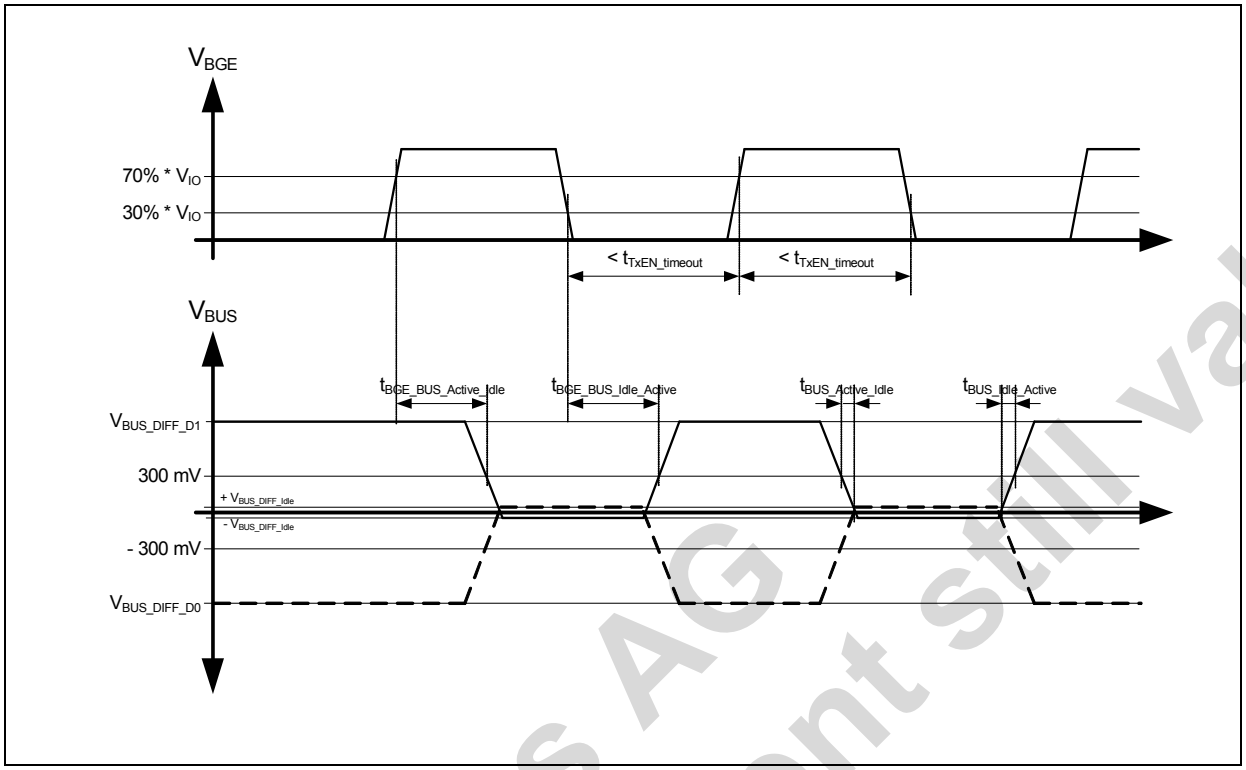


Figure 11. Transmitter characteristics (TxEN → BUS)



ams AG
Technical content still valid

Figure 12. Timing characteristics (BGE → BUS)



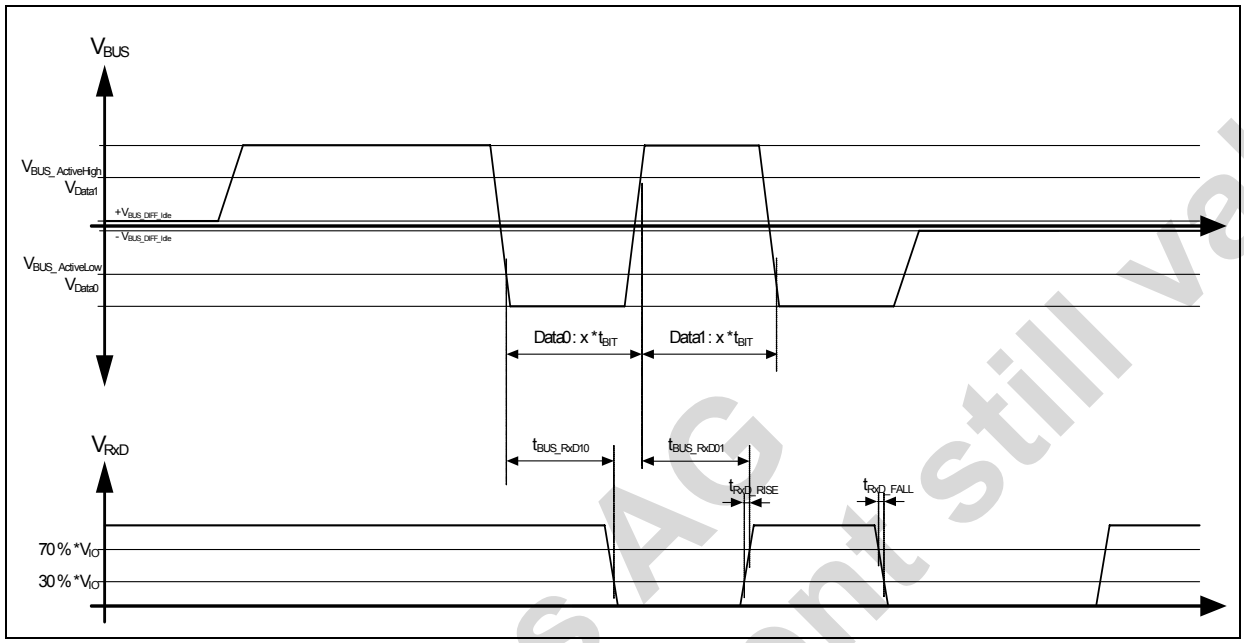
In NORMAL mode the transmitter drives on the bus Idle in case no data are transmitted. In STANDBY mode the transmitter drives Idle_LP (idle low power) on the bus pins. In POWER OFF mode the bus pins shows Idle_HZ (idle high impedance).

Technical content still valid
ams AG

Receiver

The receiver generates from the FlexRay differential bus voltage a digital signal on the RxD pin. RxD shows the data (Data0 and Data1). The receiver is only active in NORMAL mode.

Figure 13. Timing characteristics of the bus signals to RxD



Bus activity and idle detection (only in NORMAL mode)

If the absolute differential bus voltage is higher than $V_{BUSActiveLow}$ and less than $V_{BUSActiveHigh}$ for a time longer than $t_{BUSIdleDetection}$, bus Idle is detected, RxD is switched to logical high after a time $t_{BUSIdleReaction}$.

If the absolute differential bus voltage is higher than VBUSActiveHigh or lower than $V_{BUSActiveLow}$ for a time loner than $t_{BUSActivitiyDetection}$, bus Activity is detected, RxD is following the detected bus data states as indicated below with a time $t_{BUSActivityReaction}$.

Table 9. Logic table for receiver bus signal detection

Receiver Operation mode	Bus signals	RxD
NORMAL mode	Idle	H
	Data0	L
	Data1	H

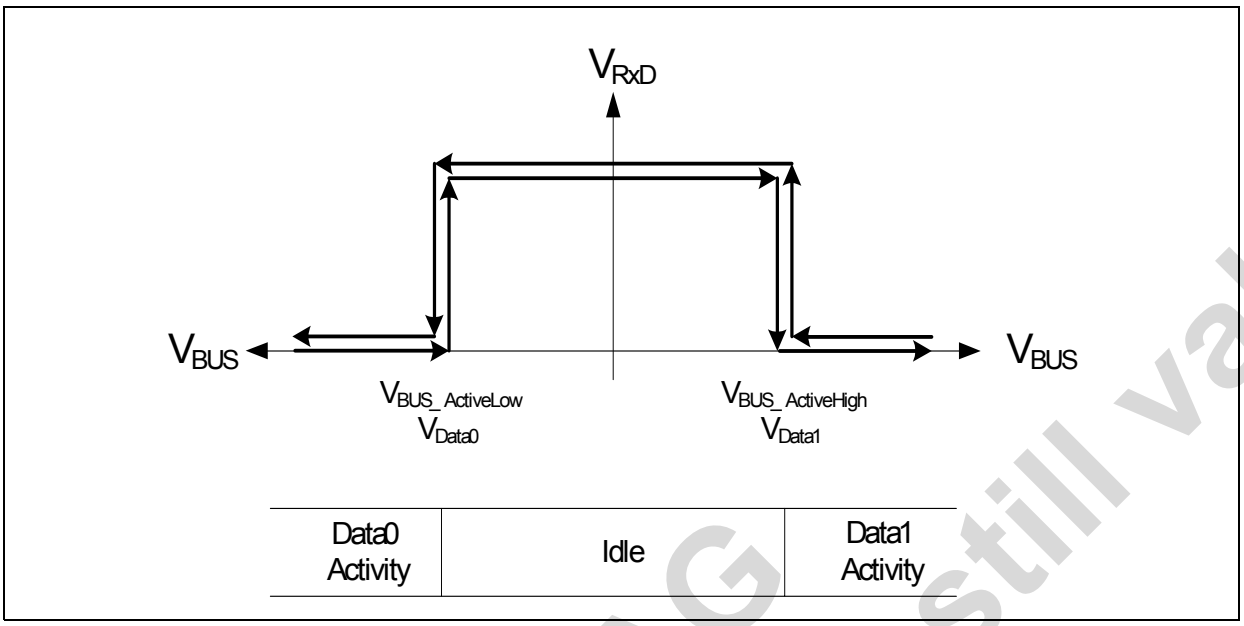
Bus data detection (NORMAL mode)

If, after the activity detection the differential bus voltage is higher than V_{Data1}, RxD will be high after a time t_{BUS_RxD01}.

If, after the activity detection the differential bus voltage is lower than V_{Data0}, RxD will be low after a time t_{BUS_RxD10}.

Technical content still valid
ams AG

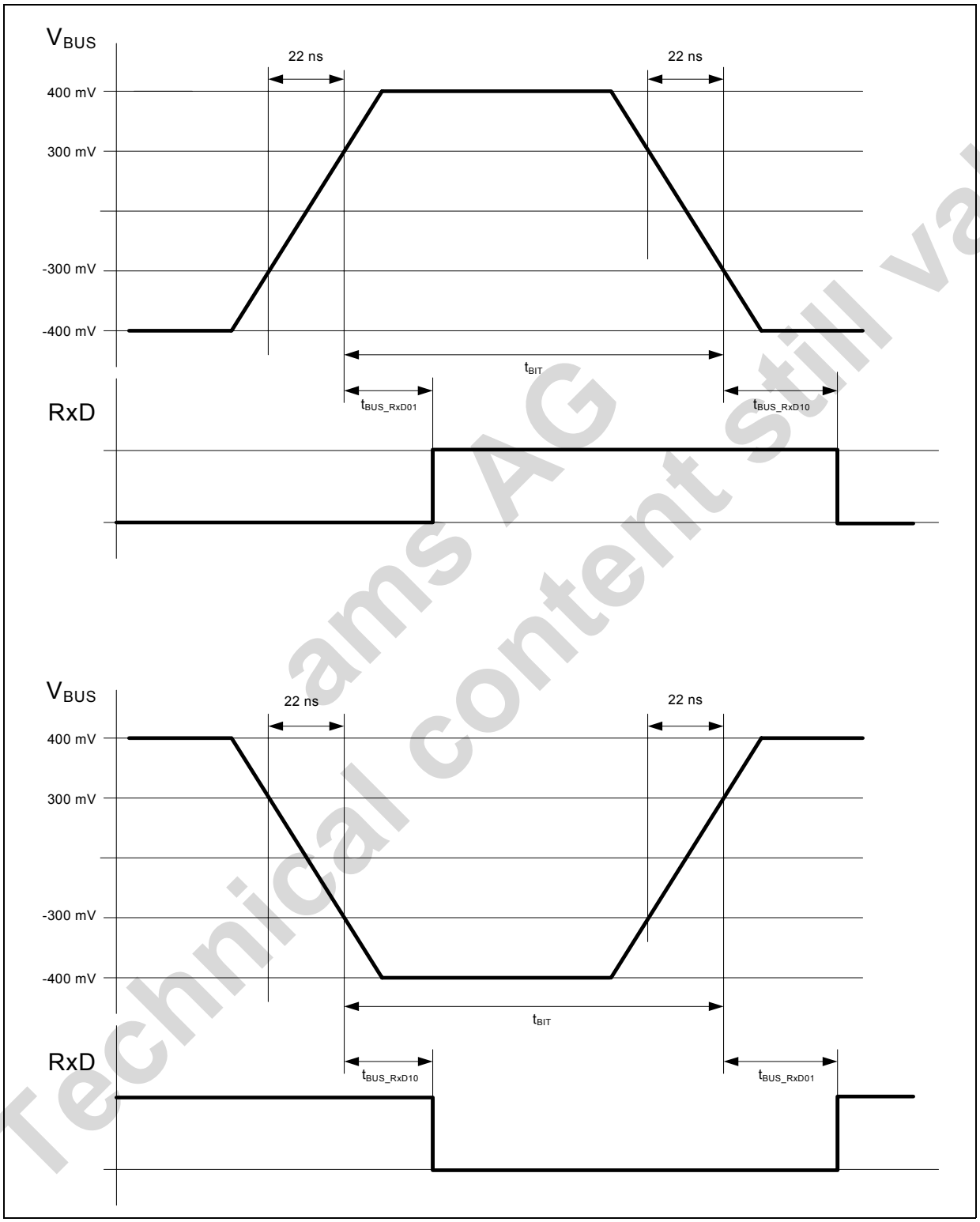
Figure 14. Receiver characteristics (BUS → RxD,)



ams AG
Technical content still valid

Receiver test signal

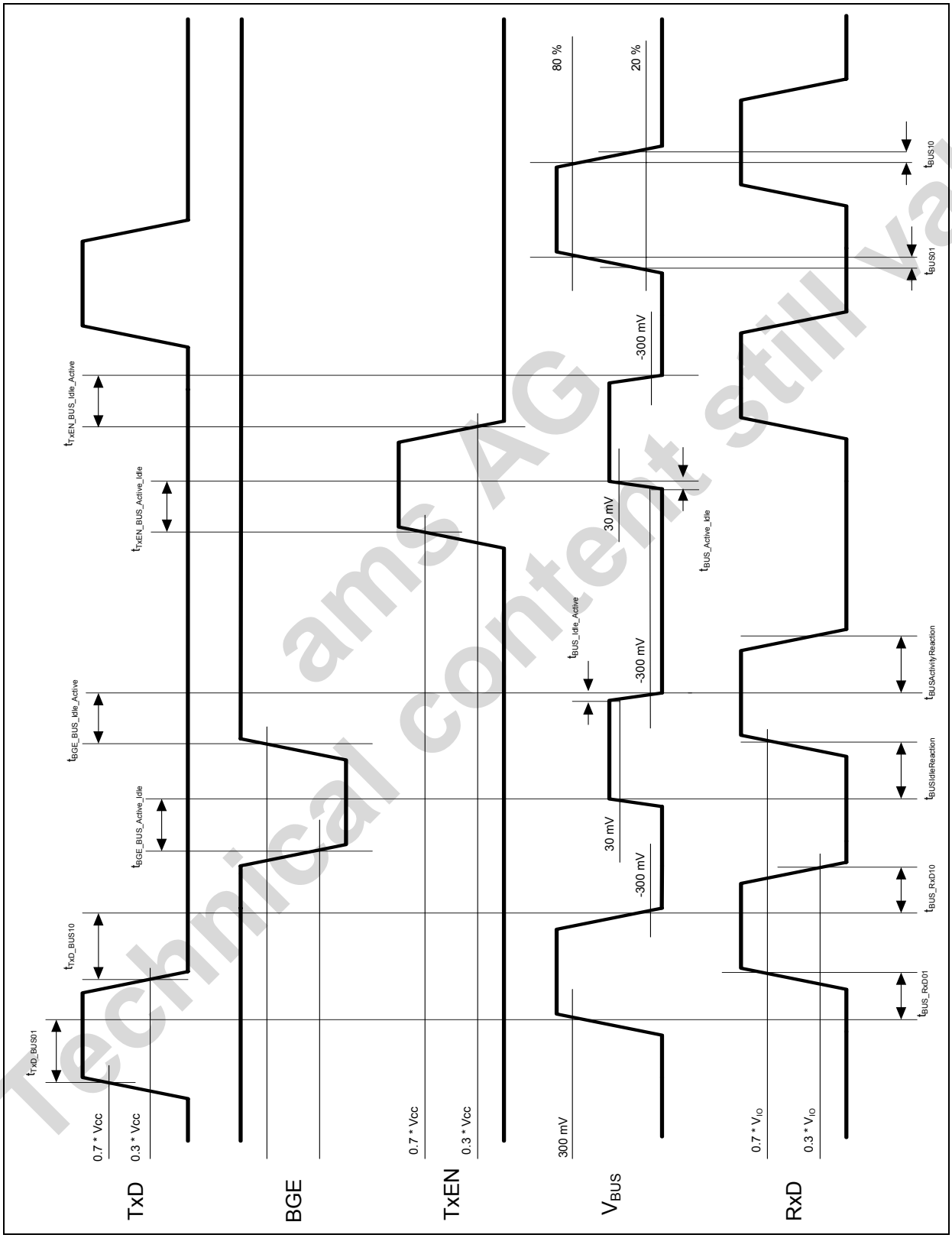
Figure 15. Receiver test signal



Technical content still valid ams AG

Transceiver Timing

Figure 16. Timing Diagram



Technical content still valid ams AG

Test Circuits

Figure 17. Test Circuit for Automotive Transients

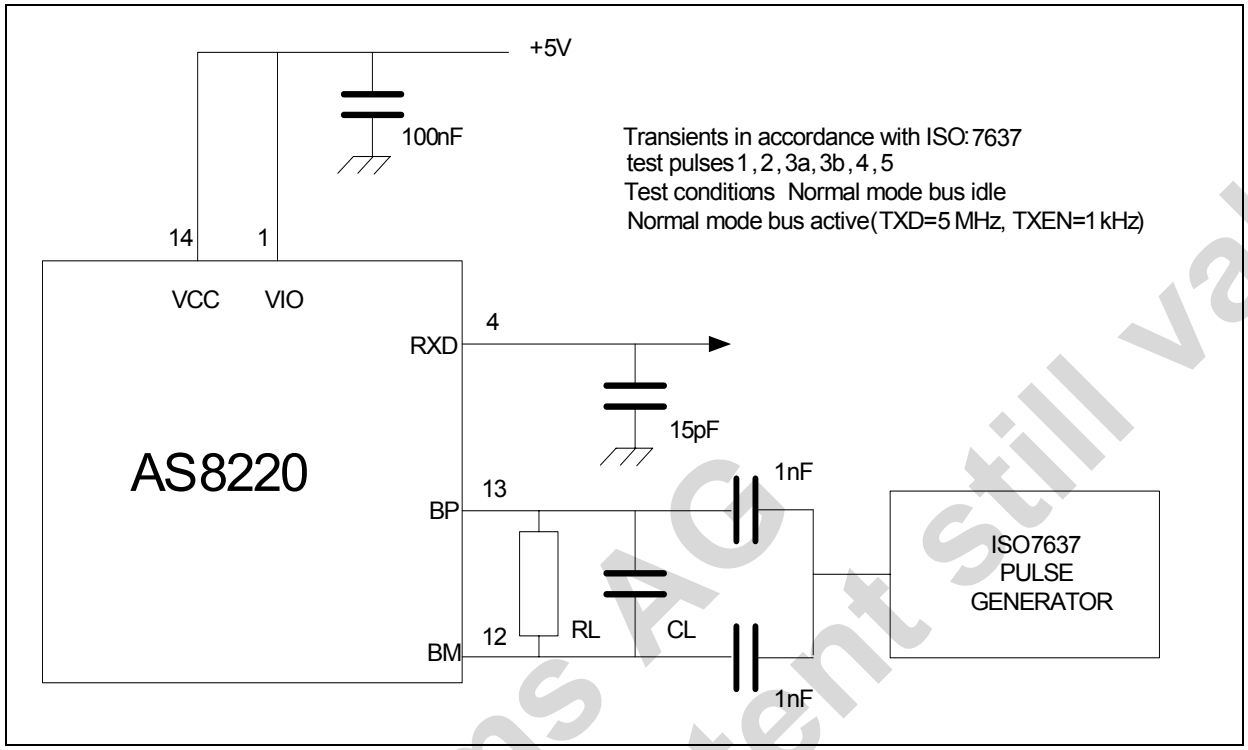
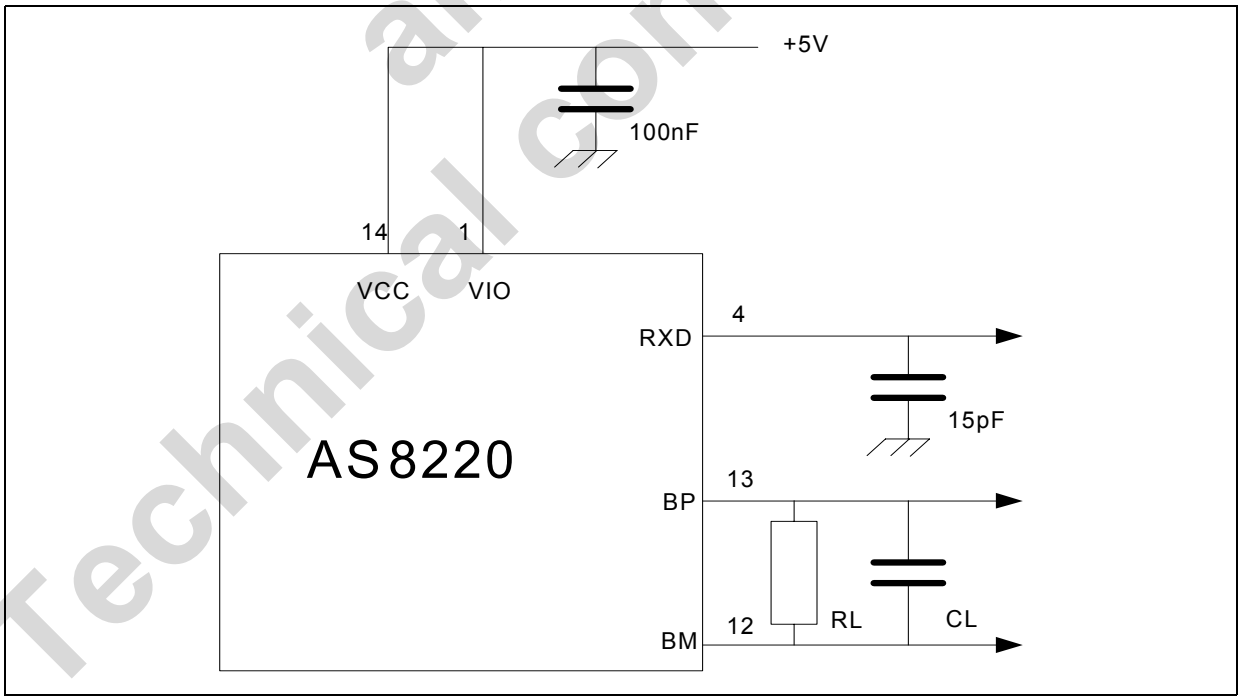


Figure 18. Test circuit for dynamic characteristics



Technical content still valid
ams AG

9 Appendix

The following table shows the comparison of conventions used in AS8220A datasheet and FlexRay Electrical Physical Layer Specification V2.1 Rev. B.

Table 10. Comparison table

AS8220A Datasheet		FlexRay Electrical Physical Layer Specification V2.1 RevB	
Symbol	**Parameter**	**Name**	**Description**
General Parameters			
-	Battery Supply Voltage (V_{BAT})	-	-
-	Supply Voltage (V_{CC})	-	-
-	Supply Voltage (V_{IO})	-	-
-	DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN	-	-
-	DC Voltage on pin WAKE, INH1, INH2	-	-
-	DC Voltage at BP and BM	-	-
-	Input current (latchup immunity)	-	-
-	Electrostatic discharge at bus lines BP, BM, V_{BAT}, WAKE	uESDExt	ESD protection on pins that lead to ECU external terminals
-	Electrostatic discharge	uESDint	ESD on all other pins
-	Transient voltage on BP, BM	-	-
-	Transient voltage on V_{BAT}	-	-
-	Total power dissipation (all supplies and outputs)	-	-
-	Storage temperature	-	-
-	Junction temperature	-	-
-	Package body temperature	-	-
-	Humidity non-condensing	-	-
Supply Voltage			
Tamb	Ambient temperature	T	Ambient temperature
V_{CC} - V_{IO}	Difference of supplies	-	-
I_{CC}	V_{CC} current consumption	-	-
I_{IO}	V_{IO} current consumption	-	-
State Transitions			
t_{STBN_RxD}	Delay STBN high to RxD high with wake flag set	-	-
$t_{STANDBY}$	go-to STANDBY hold time	-	-
Transmitter			
$V_{BUS_DIFF_D0}$	Differential bus voltage low in NORMAL mode (Data0)	-	-
$V_{BUS_DIFF_D1}$	Differential bus voltage high in NORMAL mode (Data1)	-	-

Technical content still valid
ams AG

Table 10. Comparison table

AS8220A Datasheet		FlexRay Electrical Physical Layer Specification V2.1 RevB	
Symbol	**Parameter**	**Name**	**Description**
V_{BUS_DIFF}	Matching between Data0 and Data1 differential bus voltage in NORMAL mode	-	-
$V_{BUS_COM_D0}$	Common mode bus voltage in case of Data0 in NORMAL mode	-	-
$V_{BUS_COM_D1}$	Common mode bus voltage in case of Data1 in NORMAL mode	-	-
V_{BUS_COM}	Matching between Data0 and Data1 common mode voltage	-	-
$V_{BUS_DIFF_Idle}$	Absolute differential bus voltage in idle mode	uBDTxidle	Absolute value of uBus, while Idle
$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute max current when BP is shorted to BM	$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute maximum output current when BP shorted to BM
$IBP_{GNDShortMax}$	Absolute max current when BP is shorted to GND	$IBP_{GNDShortMax}$	Absolute maximum output current when shorted to GND
$IBM_{GNDShortMax}$	Absolute max current when BM is shorted to GND	$IBM_{GNDShortMax}$	Absolute maximum output current when shorted to GND
$IBP_{-5VShortMax}$	Absolute max current when BP is shorted to -5 V	$IBP_{-5VShortMax}$	Absolute maximum output current when shorted to -5V
$IBM_{-5VShortMax}$	Absolute max current when BM is shorted to -5 V	$IBM_{-5VShortMax}$	A Absolute maximum output current when shorted to -5V
$IBP_{27VShortMax}$	Absolute max current when BP is shorted to 27 V	$IBP_{BAT27VShortMax}$	Absolute maximum output current when shorted to 27V
$IBM_{27VShortMax}$	Absolute max current when BM is shorted to 27 V	$IBM_{BAT27VShortMax}$	Absolute maximum output current when shorted to 27V
$IBP_{48VShortMax}$	Absolute max current when BP is shorted to 48 V	$IBP_{BAT48VShortMax}$	Absolute maximum output current when shorted to 48V
$IBM_{48VShortMax}$	Absolute max current when BM is shorted to 48 V	$IBM_{BAT48VShortMax}$	Absolute maximum output current when shorted to 48V
t_{TxD_BUS01}	Delay time from TxD to BUS positive edge	dBDTx10	Transmitter delay, negative edge
t_{TxD_BUS10}	Delay time from TxD to BUS negative edge	dBDTx01	Transmitter delay, positive edge
$t_{TxD_MISMATCH}$	Delay time from TxD to BUS mismatch	dTxAsym	Transmitter delay mismatch | dBDTx10 - dBDTx01 |
t_{BUS_10}	Fall time differential bus voltage	dBusTx10	Fall time differential bus voltage (80% → 20%)
t_{BUS_01}	Rise time differential bus voltage	dBusTx01	Rise time differential bus voltage (20% → 80%)

Technical content still valid
ams AG

Table 10. Comparison table

AS8220A Datasheet		FlexRay Electrical Physical Layer Specification V2.1 RevB	
Symbol	**Parameter**	**Name**	**Description**
$t_{TxEN_BUS_Idle_Active}$	Delay time from TxEN to bus active	dBDTxia	Propagation delay idle →active
$t_{TxEN_BUS_Active_Idle}$	Delay time from TxEN to bus idle	dBDTxai	Propagation delay active → idle
$t_{TxEN_MISMATCH}$	Delay time from TxEN to bus mismatch	dBDTxDM	| dBDTxia - dBDTxai |
$t_{BGE_BUS_Idle_Active}$	Delay time from BGE to bus active	dBDTxia	Propagation delay idle → active
$t_{BGE_BUS_Active_Idle}$	Delay time from BGE to bus idle	dBDTXai	Propagation delay active → idle
$t_{BUS_Idle_Active}$	Differential bus voltage transition time: idle to active	dBusTxia	Transition time idle → active
$t_{BUS_Active_Idle}$	Differential bus voltage transition time: active to idle	dBusTxai	Transition time active → idle
$t_{TxEN_timeout}$	TxEN timeout	-	-
Receiver			
R_{BP}, R_{BM}	BP, BM input resistance	RCM1, RCM2	Receiver common mode input resistance
R_{DIFF}	BP, BM differential input resistance	-	-
V_{BPidle}, V_{BMidle}	Idle voltage in NORMAL mode on pin BP,BM	uBias	Bus bias voltage during BD_Normal mode
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in NORMAL mode on pin BP, BM	uBias	Bus bias voltage during low power modes
I_{BPidle}	Absolute idle output current on pin BP	-	-
I_{BMidle}	Absolute idle output current on pin BM	-	-
I_{BPleak}, I_{BMleak}	Absolute leakage current, when not powered	iBPLeak, iBMLeak	Absolute leakage current, when not powered
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	uBusActiveHigh	Upper receiver threshold for detecting activity
$V_{BUSActiveLow}$	Activity detection differential input voltage low	uBusActiveLow	Lower receiver threshold for detecting activity
V_{Data1}	Data1 detection differential input voltage	uData1	Receiver threshold for detecting Data_1
V_{Data0}	Data0 detection differential input voltage	uData0	Receiver threshold for detecting Data_0
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	uData	Mismatch of receiver thresholds
t_{BUS_RxD10}	Delay from bus to RxD negative edge	dBDRx10	Receiver delay, negative edge
t_{BUS_RxD01}	Delay from bus to RxD positive edge	dBDRx01	Receiver delay, positive edge

Technical content still valid
ams AG

Table 10. Comparison table

AS8220A Datasheet		FlexRay Electrical Physical Layer Specification V2.1 RevB	
Symbol	**Parameter**	**Name**	**Description**
t_{BIT}	Bit time	-	-
t_{RxD_ASYM}	Delay time from bus to RxD mismatch	dRxAsym	Receiver delay mismatch | dBDRx10 – dBDRx01 |
$t_{BUSIdleDetection}$	Idle detection time	dIdleDetection	Filter-time for idle detection
$t_{BUSActivityDetection}$	Activity detection time	dActivityDetection	Filter-time for activity detection
$t_{BUSIdleReaction}$	Idle reaction time	dBDRxai	Idle reaction time
$t_{BUSActivityReaction}$	Activity reaction time	dBDRxia	Activity reaction time
Supply Voltage Monitor			
V_{CCTHH}	V_{CC} undervoltage recovery threshold	-	-
V_{CCTHL}	V_{CC} undervoltage detection threshold	uUVCC	Undervoltage detection threshold
V_{IOTHH}	V_{IO} undervoltage recovery threshold	-	-
V_{IOTHL}	V_{IO} undervoltage detection threshold	uUVIO	Undervoltage detection threshold
t_{UV_DETECT}	Detection time for undervoltage at V_{CC}, V_{IO}	dUVCC, dUVIO	Undervoltage reaction time
t_{UV_REC}	Detection time for undervoltage recovery at V_{CC}, V_{IO}	-	-
Bus Error Detection			
I_{THL}	Absolute bus current for low current detection	-	-
I_{THH}	Absolute bus current for high current detection	-	-
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	-	-
t_{BUS_ERROR}	Bus error detection time	-	Detection only required while actively transmitting a data frame, error indication to host latest when transmission stops.
Over Temperature			
OT_{TH}	Over temperature threshold	-	-
OT_{TL}	Over temperature hysteresis	-	-
Communication Controller Interface			
V_{TxDIH}	Threshold for detecting TxD as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high

Technical content still valid ams AG

Table 10. Comparison table

AS8220A Datasheet		FlexRay Electrical Physical Layer Specification V2.1 RevB	
Symbol	**Parameter**	**Name**	**Description**
V_{TxDIL}	Threshold for detecting TxD as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{TxDIH}	TxD high level input current	-	-
I_{TxDIL}	TxD low level input current	-	-
V_{TxENIH}	Threshold for detecting TxEN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{TXENIL}	Threshold for detecting TxEN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{TxENIH}	TxEN high level input current	-	-
I_{TxENIL}	TxEN low level input current	-	-
V_{RxDOH}	RxD high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{RxDOL}	RxD low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Host Interface			
V_{STBNIH}	Threshold for detecting STBN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{STBNIL}	Threshold for detecting STBN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{STBNIH}	STBN high level input current	-	-
I_{STBNIL}	STBN low level input current	-	-
$t_{STBN_DEB_LP}$	STBN de-bouncing time low power modes	-	-
$t_{STBN_DEB_NLP}$	STBN de-bouncing time non low power modes	-	-
V_{ERRNOH}	ERRN high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{ERRNOL}	ERRN low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Bus Guardian Interface			
V_{BGEIH}	Threshold for detecting BGE as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high

ams AG
Technical content still valid

Table 10. Comparison table

AS8220A Datasheet		FlexRay Electrical Physical Layer Specification V2.1 RevB	
Symbol	**Parameter**	**Name**	**Description**
V_{BGEIL}	Threshold for detecting BGE as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{BGEIH}	BGE high level input current	-	-
I_{BGEIL}	BGE low level input current	-	-

ams AG
Technical content still valid

10 Package Drawings and Markings

Figure 19. package Diagram

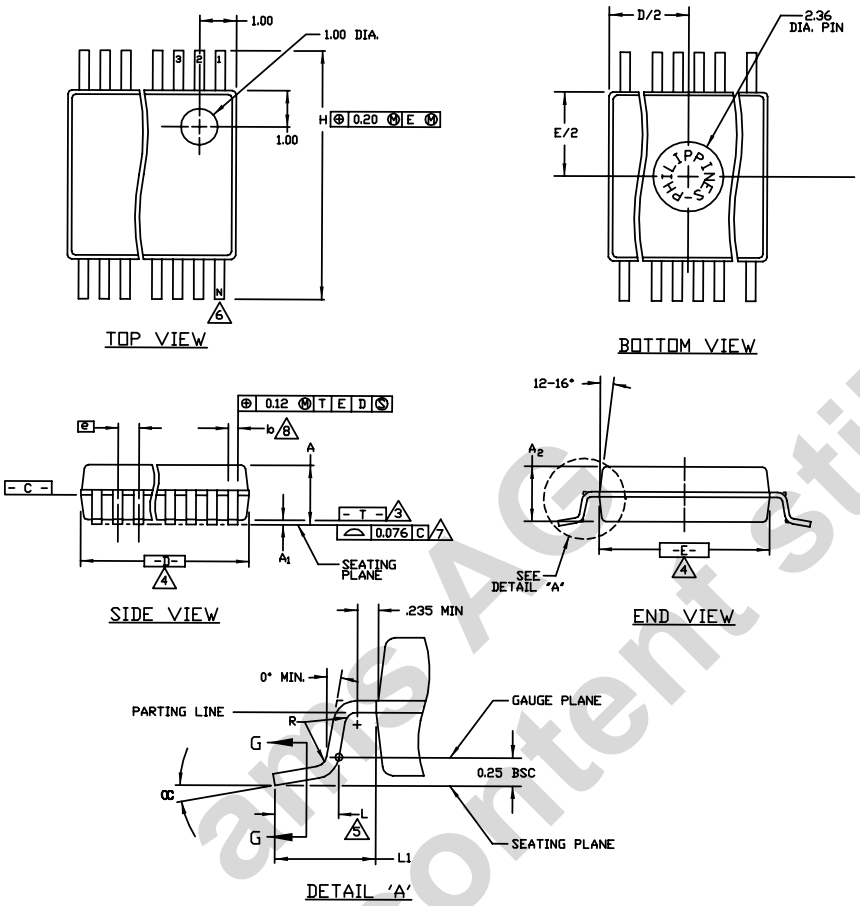


Table 11. package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	1.73	1.86	1.99	L	0.63	0.75	0.95
A1	0.05	0.13	0.21	L1		1.25 REF	
A2	1.68	1.73	1.78	N		See Variations	
b	0.25	-	0.38		0°	4°	8°
b1	0.25	0.30	0.33	R	0.09	0.15	
C	0.09	-	0.20	AA	6.07	6.20	6.33
C1	0.09	0.15	0.16	AB	6.07	6.20	6.33
D		See Variations		AC	7.07	7.20	7.33
E	5.20	5.30	5.38	AD	8.07	8.20	8.33
e		0.65 BSC		AE	10.07	10.20	10.33
H	7.65	7.80	7.90	AF	10.07	10.20	10.33

Note:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. N is the total number of terminals.

Technical content still valid
ams AG

11 Ordering Information

Table 12. Ordering Information

Type	Marking	Description	Delivery Form	Package

ams AG
Technical content still valid

Copyrights

Copyright © 1997-2008, austriamicrosystems AG, Schloss Premstaetten, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

ams AG
Technical content still valid

Contact Information

Headquarters
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact