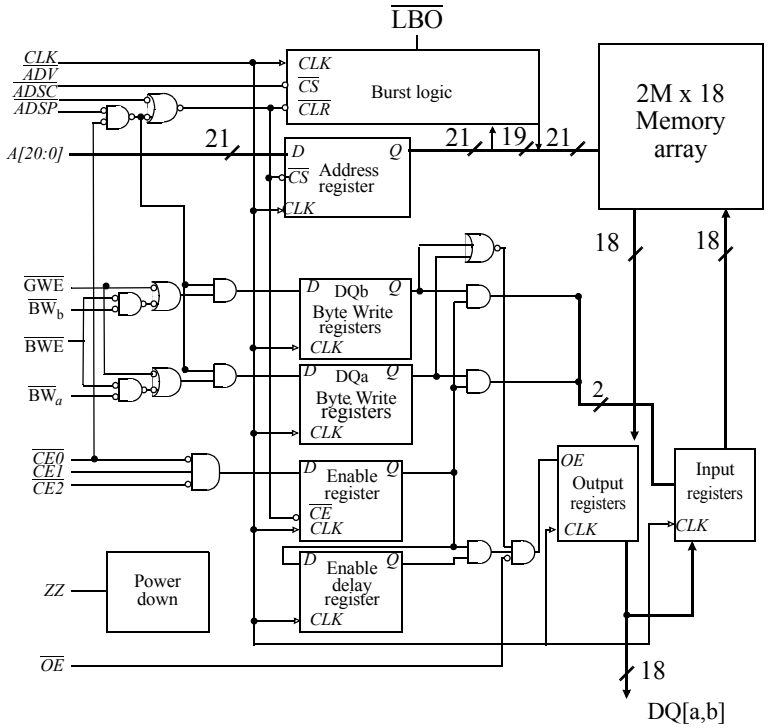
# 2.5V 2M × 18 pipelined burst synchronous SRAM

## Features

- Organization: 2,097,152 words × 18 bits
- Fast clock speeds to 200 MHz
- Fast clock to data access: 3.1/3.5/3.8 ns
- Fast $\overline{OE}$ access time: 3.1/3.5/3.8 ns
- Fully synchronous register-to-register operation
- Double-cycle deselect
- Asynchronous output enable control
- Available in 100-pin TQFP package
- Individual byte write and global write
- Multiple chip enables for easy expansion
- 2.5V core power supply
- Linear or interleaved burst control
- Snooze mode for reduced power-standby
- Common data inputs and data outputs

## Logic block diagram




## Selection guide

| | -200 | -166 | -133 | Units |
|---|---|---|---|---|
| Minimum cycle time | 5 | 6 | 7.5 | ns |
| Maximum clock frequency | 200 | 166 | 133 | MHz |
| Maximum pipelined clock access time | 3.1 | 3.5 | 3.8 | ns |
| Maximum operating current | 450 | 400 | 350 | mA |
| Maximum standby current | 170 | 150 | 140 | mA |
| Maximum CMOS standby current (DC) | 90 | 90 | 90 | mA |


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## 2.5V 32 Mb Synchronous SRAM products list[1,2]

| Org | Part Number | Mode | Speed |
|---|---|---|---|
| 2MX18 | AS7C252MPFS18A | PL-SCD | 200/166/133 MHz |
| 1MX32 | AS7C251MPFS32A | PL-SCD | 200/166/133 MHz |
| 1MX36 | AS7C251MPFS36A | PL-SCD | 200/166/133 MHz |
| 2MX18 | AS7C252MPFD18A | PL-DCD | 200/166/133 MHz |
| 1MX32 | AS7C251MPFD32A | PL-DCD | 200/166/133 MHz |
| 1MX36 | AS7C251MPFD36A | PL-DCD | 200/166/133 MHz |
| 2MX18 | AS7C252MFT18A | FT | 7.5/8.5/10 ns |
| 1MX32 | AS7C251MFT32A | FT | 7.5/8.5/10 ns |
| 1MX36 | AS7C251MFT36A | FT | 7.5/8.5/10 ns |
| 2MX18 | AS7C252MNTD18A | NTD-PL | 200/166/133 MHz |
| 1MX32 | AS7C251MNTD32A | NTD-PL | 200/166/133 MHz |
| 1MX36 | AS7C251MNTD36A | NTD-PL | 200/166/133 MHz |
| 2MX18 | AS7C252MNTF18A | NTD-FT | 7.5/8.5/10 ns |
| 1MX32 | AS7C251MNTF32A | NTD-FT | 7.5/8.5/10 ns |
| 1MX36 | AS7C251MNTF36A | NTD-FT | 7.5/8.5/10 ns |

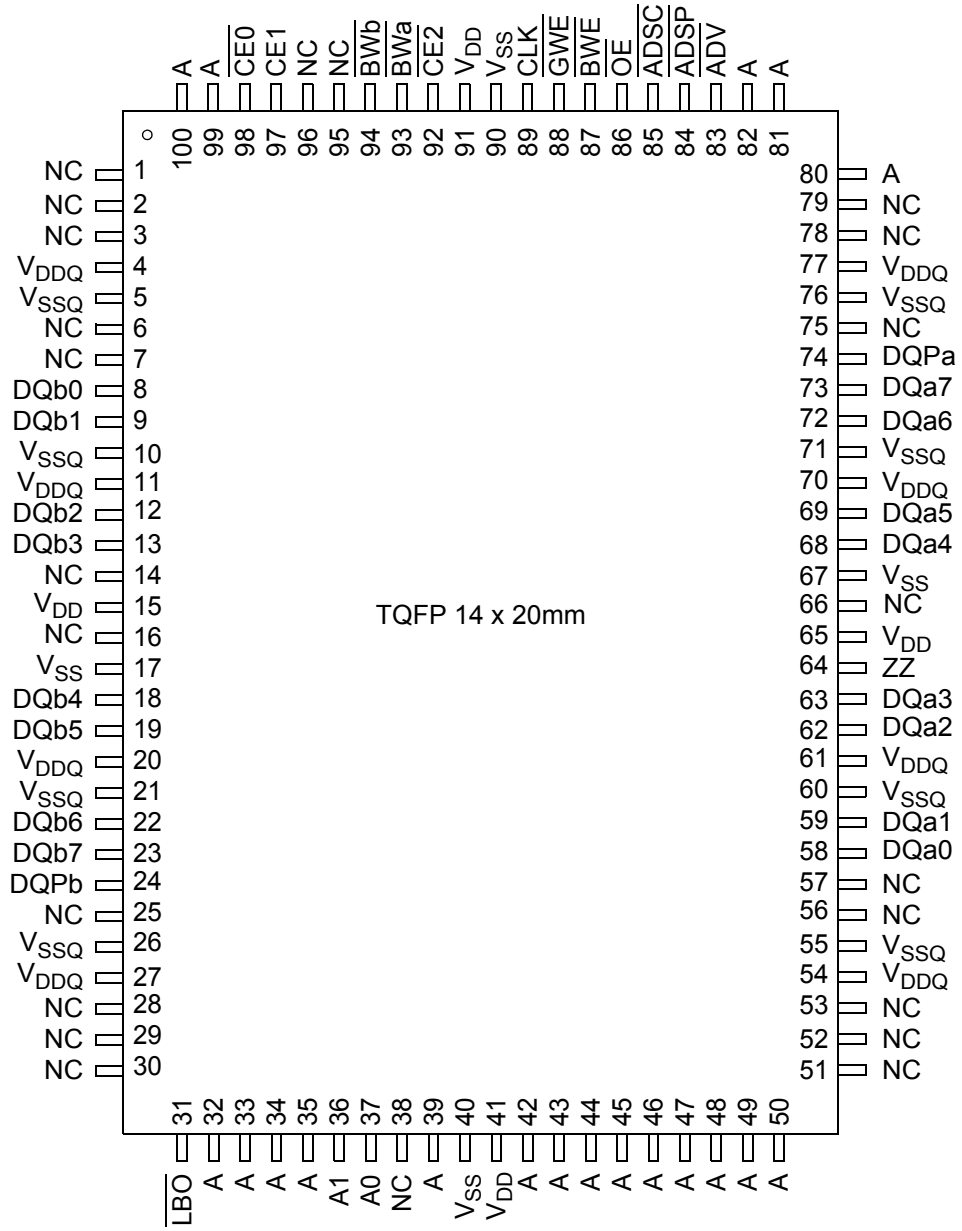
1 Core Power Supply: VDD = 2.5V $\pm$ 0.125V
2 I/O Supply Voltage: VDDQ = 2.5V $\pm$ 0.125V

PL-SCD : Pipelined Burst Synchronous SRAM - Single Cycle Deselect
PL-DCD : Pipelined Burst Synchronous SRAM - Double Cycle Deselect
FT : Flow-through Burst Synchronous SRAM
NTD[1]-PL : Pipelined Burst Synchronous SRAM with NTD™
NTD-FT : Flow-through Burst Synchronous SRAM with NTD™

1NTD: No Turnaround Delay. NTD™ is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners.

## Pin assignment

### 100-pin TQFP - top view



## Functional description

The AS7C252MPFD18A is a high-performance CMOS 32-Mbit synchronous Static Random Access Memory (SRAM) device organized as 2,097,152 words × 18 bits. It incorporates a two-stage register-register pipeline for highest frequency on any given technology.

Fast cycle times of 5/6/7.5 ns with clock access times ($t_{CD}$) of 3.1/3.5/3.8 ns enable 200,167 and 133MHz bus frequencies. Three chip enable ($\overline{CE}$) inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{ADSC}$), or the processor address strobe ($\overline{ADSP}$). The burst advance pin ($\overline{ADV}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register when $\overline{ADSP}$ is sampled low, the chip enables are sampled active, and the output buffer is enabled with $\overline{OE}$. In a read operation, the data accessed by the current address registered in the address registers by the positive edge of CLK are carried to the data-out registers and driven on the output pins on the next positive edge of CLK. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{ADV}$ is sampled low and both address strobes are high. Burst mode is selectable with the $\overline{LBO}$ input. With $\overline{LBO}$ unconnected or driven high, burst operations use an interleaved count sequence. With $\overline{LBO}$ driven low, the device uses a linear count sequence.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting a write command. A global write enable $\overline{GWE}$ writes all 18 bits regardless of the state of individual $\overline{BW}$[a,b] inputs. Alternately, when $\overline{GWE}$ is high, one or more bytes may be written by asserting $\overline{BWE}$ and the appropriate individual byte $\overline{BWn}$ signals.

$\overline{BWn}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but it is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{BWn}$ is sampled LOW regardless of $\overline{OE}$. Data is clocked into the data input register when $\overline{BWn}$ is sampled low. Address is incremented internally to the next burst address if $\overline{BWn}$ and $\overline{ADV}$ are sampled low. This device operates in double-cycle deselect feature during read cycles.

Read or write cycles may also be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows:

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ signals are sampled on the clock edge that samples $\overline{ADSC}$ low (and $\overline{ADSP}$ high).
- Master chip enable $\overline{CE0}$ blocks $\overline{ADSP}$, but not $\overline{ADSC}$.

The AS7C252MPFD18A operates with a 2.5V ± 5% power supply for the device core ($V_{DD}$). These devices are available in a 100-pin TQFP package.

## TQFP capacitance

| Parameter | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$* | $V_{IN}$ = 0V | - | 5 | pF |
| I/O capacitance | $C_{I/O}$* | $V_{OUT}$ = 0V | - | 7 | pF |

* Guaranteed not tested

## TQFP thermal resistance

| Description | Conditions | | Symbol | Typical | Units |
|---|---|---|---|---|---|
| Thermal resistance (junction to ambient)[1] | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 1–layer | $\theta_{JA}$ | 40 | °C/W |
| | | 4–layer | $\theta_{JA}$ | 22 | °C/W |
| Thermal resistance (junction to top of case)[1] | | | $\theta_{JC}$ | 8 | °C/W |

1 This parameter is sampled

## Signal descriptions

| Pin | I/O | Properties | Description |
|---|---|---|---|
| CLK | I | CLOCK | Clock. All inputs except $\overline{OE}$, ZZ, and $\overline{LBO}$ are synchronous to this clock. |
| A,A0,A1 | I | SYNC | Address. Sampled when all chip enables are active and when $\overline{ADSC}$ or $\overline{ADSP}$ are asserted. |
| DQ[a,b] | I/O | SYNC | Data. Driven as output when the chip is enabled and when $\overline{OE}$ is active. |
| $\overline{CE0}$ | I | SYNC | Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE0}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the "Synchronous truth table" for more information. |
| CE1, $\overline{CE2}$ | I | SYNC | Synchronous chip enables, active high, and active low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE0}$ and $\overline{ADSP}$ are active. |
| $\overline{ADSP}$ | I | SYNC | Address strobe processor. Asserted low to load a new address or to enter standby mode. |
| $\overline{ADSC}$ | I | SYNC | Address strobe controller. Asserted low to load a new address or to enter standby mode. |
| $\overline{ADV}$ | I | SYNC | Advance. Asserted low to continue burst read/write. |
| $\overline{GWE}$ | I | SYNC | Global write enable. Asserted low to write all 18 bits. When high, $\overline{BWE}$ and $\overline{BW[a,b]}$ control write enable. |
| $\overline{BWE}$ | I | SYNC | Byte write enable. Asserted low with $\overline{GWE}$ high to enable effect of $\overline{BW[a:d]}$ inputs. |
| $\overline{BW}$[a,b] | I | SYNC | Write enables. Used to control write of individual bytes when $\overline{GWE}$ is high and $\overline{BWE}$ is low. If any of $\overline{BW[a,b]}$ is active with $\overline{GWE}$ high and $\overline{BWE}$ low, the cycle is a write cycle. If all $\overline{BW[a,b]}$ are inactive, the cycle is a read cycle. |
| $\overline{OE}$ | I | ASYNC | Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and chip is in read mode. |
| $\overline{LBO}$ | I | STATIC | Selects Burst mode. When tied to $V_{DD}$ or left floating, device follows interleaved Burst order. When driven Low, device follows linear Burst order. *This signal is internally pulled High.* |
| ZZ | I | ASYNC | Snooze. Places device in low power mode; data is retained. Connect to GND if unused. |
| NC | - | - | No connect |

## Snooze Mode

SNOOZE MODE is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB2}$. The duration of SNOOZE MODE is dictated by the length of time the ZZ is in a High state.

The ZZ pin is an asynchronous, active high input that causes the device to enter SNOOZE MODE.

When the ZZ pin becomes a logic High, $I_{SB2}$ is guaranteed after the time $t_{ZZI}$ is met. After entering SNOOZE MODE, all inputs except ZZ is disabled and all outputs go to High-Z. Any operation pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during $t_{PUS}$, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SNOOZE MODE.

## Write enable truth table (per byte)

| Function | $\overline{GWE}$ | $\overline{BWE}$ | $\overline{BWa}$ | $\overline{BWb}$ |
|---|---|---|---|---|
| Write All Bytes | L | X | X | X |
| | H | L | L | L |
| Write Byte a | H | L | L | H |
| Write Byte b | H | L | H | L |
| Read | H | H | X | X |
| | H | L | H | H |

**Key:** X = don't care, L = low, H = high, n = a, b; $\overline{BWE}$, $\overline{BWn}$ = internal write signal.

## Asynchronous Truth Table

| Operation | ZZ | $\overline{OE}$ | I/O Status |
|---|---|---|---|
| Snooze mode | H | X | High-Z |
| Read | L | L | Dout |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

Notes:
1. X means "Don't Care"
2. ZZ pin is pulled down internally
3. For write cycles that follows read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Snooze mode means power down state of which stand-by current does not depend on cycle times
5. Deselected means power down state of which stand-by current depends on cycle times

## Burst sequence table

| Interleaved burst address ($\overline{LBO}$ = 1) | | | | | Linear burst address ($\overline{LBO}$ = 0) | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | A1 A0 | A1 A0 | A1 A0 | A1 A0 | | A1 A0 | A1 A0 | A1 A0 | A1 A0 |
| Starting Address | 0 0 | 0 1 | 1 0 | 1 1 | Starting Address | 0 0 | 0 1 | 1 0 | 1 1 |
| First Increment | 0 1 | 0 0 | 1 1 | 1 0 | First Increment | 0 1 | 1 0 | 1 1 | 0 0 |
| Second Increment | 1 0 | 1 1 | 0 0 | 0 1 | Second Increment | 1 0 | 1 1 | 0 0 | 0 1 |
| Third Increment | 1 1 | 1 0 | 0 1 | 0 0 | Third Increment | 1 1 | 1 0 | 0 1 | 1 0 |

## Synchronous truth table[4]

| $\overline{CE0}$[1] | CE1 | $\overline{CE2}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$[2] | $\overline{OE}$ | Address accessed | CLK | Operation | DQ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | L | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | L | X | L | X | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | L | X | H | L | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | X | H | L | X | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | X | H | H | L | X | X | X | NA | L to H | Deselect | Hi–Z |
| L | H | L | L | X | X | X | L | External | L to H | Begin read | Q |
| L | H | L | L | X | X | X | H | External | L to H | Begin read | Hi–Z |
| L | H | L | H | L | X | H | L | External | L to H | Begin read | Q |
| L | H | L | H | L | X | H | H | External | L to H | Begin read | Hi–Z |
| X | X | X | H | H | L | H | L | Next | L to H | Continue read | Q |
| X | X | X | H | H | L | H | H | Next | L to H | Continue read | Hi–Z |
| X | X | X | H | H | H | H | L | Current | L to H | Suspend read | Q |
| X | X | X | H | H | H | H | H | Current | L to H | Suspend read | Hi–Z |
| H | X | X | X | H | L | H | L | Next | L to H | Continue read | Q |
| H | X | X | X | H | L | H | H | Next | L to H | Continue read | Hi–Z |
| H | X | X | X | H | H | H | L | Current | L to H | Suspend read | Q |
| H | X | X | X | H | H | H | H | Current | L to H | Suspend read | Hi–Z |
| L | H | L | H | L | X | L | X | External | L to H | Begin write | D[3] |
| X | X | X | H | H | L | L | X | Next | L to H | Continue write | D |
| H | X | X | X | H | L | L | X | Next | L to H | Continue write | D |
| X | X | X | H | H | H | L | X | Current | L to H | Suspend write | D |
| H | X | X | X | H | H | L | X | Current | L to H | Suspend write | D |

1 X = don't care, L = low, H = high

2 For $\overline{WRITE}$, L means any one or more byte write enable signals ($\overline{BWa}$ or $\overline{BWb}$) and $\overline{BWE}$ are LOW or $\overline{GWE}$ is LOW. $\overline{WRITE}$ = HIGH for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GWE}$ HIGH. See "Write enable truth table (per byte)," on page 6 for more information.

3 For write operation following a READ, $\overline{OE}$ must be high before the input data set up time and held high throughout the input hold time

4 ZZ pin is always Low.

## Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power supply voltage relative to GND | $V_{DD}$, $V_{DDQ}$ | –0.3 | +3.6 | V |
| Input voltage relative to GND (input pins) | $V_{IN}$ | –0.3 | $V_{DD}$ + 0.3 | V |
| Input voltage relative to GND (I/O pins) | $V_{IN}$ | –0.3 | $V_{DDQ}$ + 0.3 | V |
| Power dissipation | $P_d$ | – | 1.8 | W |
| Short circuit output current | $I_{OUT}$ | – | 20 | mA |
| Storage temperature | $T_{stg}$ | –65 | +150 | °C |
| Temperature under bias | $T_{bias}$ | –65 | +135 | °C |

Stresses greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

## Recommended operating conditions

| Parameter | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage for inputs | $V_{DD}$ | 2.375 | 2.5 | 2.625 | V |
| Supply voltage for I/O | $V_{DDQ}$ | 2.375 | 2.5 | 2.625 | V |
| Ground supply | Vss | 0 | 0 | 0 | V |

## DC electrical characteristics

| Parameter | Sym | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input leakage current† | $\|I_{LI}\|$ | $V_{DD}$ = Max, OV ≤ $V_{IN}$ ≤ $V_{DD}$ | -2 | 2 | µA |
| Output leakage current | $\|I_{LO}\|$ | OE ≥ $V_{IH}$, $V_{DD}$ = Max, OV ≤ $V_{OUT}$ ≤ $V_{DDQ}$ | -2 | 2 | µA |
| Input high (logic 1) voltage | $V_{IH}$ | Address and control pins | 1.7* | $V_{DD}$+0.3 | V |
| | | I/O pins | 1.7* | $V_{DDQ}$+0.3 | V |
| Input low (logic 0) voltage | $V_{IL}$ | Address and control pins | -0.3** | 0.7 | V |
| | | I/O pins | -0.3** | 0.7 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4 mA, $V_{DDQ}$ = 2.375V | 1.7 | – | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8 mA, $V_{DDQ}$ = 2.625V | – | 0.7 | V |

† $\overline{LBO}$ and ZZ pins have an internal pull-up or pull-down, and input leakage = ±10 µA.

*$V_{IH}$ max < VDD +1.5V for pulse width less than 0.2 X $t_{CYC}$

**$V_{IL}$ min = -1.5 for pulse width less than 0.2 X $t_{CYC}$

## $I_{DD}$ operating conditions and maximum limits

| Parameter | Sym | Conditions | -200 | -166 | -133 | Unit |
|---|---|---|---|---|---|---|
| Operating power supply current[1] | $I_{CC}$ | $\overline{CE0}$ ≤ $V_{IL}$, CE1 ≥ $V_{IH}$, $\overline{CE2}$ ≤ $V_{IL}$, f = $f_{Max}$, $I_{OUT}$ = 0 mA, ZZ ≤ $V_{IL}$ | 450 | 400 | 350 | mA |
| Standby power supply current | $I_{SB}$ | All $V_{IN}$ ≤ 0.2V or ≥ $V_{DD}$ – 0.2V, Deselected, f = $f_{Max}$, ZZ ≤ $V_{IL}$ | 170 | 150 | 140 | mA |
| | $I_{SB1}$ | Deselected, f = 0, ZZ ≤ 0.2V, all $V_{IN}$ ≤ 0.2V or ≥ $V_{DD}$ – 0.2V | 90 | 90 | 90 | |
| | $I_{SB2}$ | Deselected, f = $f_{Max}$, ZZ ≥ $V_{DD}$ – 0.2V, all $V_{IN}$ ≤ $V_{IL}$ or ≥ $V_{IH}$ | 80 | 80 | 80 | |

1 $I_{CC}$ given with no output loading. $I_{CC}$ increases with faster cycle times and greater output loading.

## Timing characteristics over operating range

| Parameter | Sym | –200 | | –166 | | -133 | | Unit | Notes[1] |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock frequency | $f_{Max}$ | – | 200 | – | 166 | – | 133 | MHz | |
| Cycle time | $t_{CYC}$ | 5 | – | 6 | – | 7.5 | – | ns | |
| Clock access time | $t_{CD}$ | – | 3.1 | – | 3.5 | – | 3.8 | ns | |
| Output enable low to data valid | $t_{OE}$ | – | 3.1 | – | 3.5 | – | 3.8 | ns | |
| Clock high to output low Z | $t_{LZC}$ | 0 | – | 0 | – | 0 | – | ns | 2,3,4 |
| Data output invalid from clock high | $t_{OH}$ | 1.5 | – | 1.5 | – | 1.5 | – | ns | 2 |
| Output enable low to output low Z | $t_{LZOE}$ | 0 | – | 0 | – | 0 | – | ns | 2,3,4 |
| Output enable high to output high Z | $t_{HZOE}$ | – | 3.0 | – | 3.4 | – | 3.8 | ns | 2,3,4 |
| Clock high to output high Z | $t_{HZC}$ | – | 3.0 | – | 3.4 | – | 3.8 | ns | 2,3,4 |
| Output enable high to invalid output | $t_{OHOE}$ | 0 | – | 0 | – | 0 | – | ns | |
| Clock high pulse width | $t_{CH}$ | 2.0 | – | 2.4 | – | 2.4 | – | ns | 5 |
| Clock low pulse width | $t_{CL}$ | 2.0 | – | 2.4 | – | 2.4 | – | ns | 5 |
| Address setup to clock high | $t_{AS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| Data setup to clock high | $t_{DS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| Write setup to clock high | $t_{WS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6,7 |
| Chip select setup to clock high | $t_{CSS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6,8 |
| Address hold from clock high | $t_{AH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| Data hold from clock high | $t_{DH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| Write hold from clock high | $t_{WH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6,7 |
| Chip select hold from clock high | $t_{CSH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6,8 |
| $\overline{ADV}$ setup to clock high | $t_{ADVS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| $\overline{ADSP}$ setup to clock high | $t_{ADSPS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| $\overline{ADSC}$ setup to clock high | $t_{ADSCS}$ | 1.4 | – | 1.5 | – | 1.5 | – | ns | 6 |
| $\overline{ADV}$ hold from clock high | $t_{ADVH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| $\overline{ADSP}$ hold from clock high | $t_{ADSPH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |
| $\overline{ADSC}$ hold from clock high | $t_{ADSCH}$ | 0.4 | – | 0.5 | – | 0.5 | – | ns | 6 |

1 See “Notes” on page 15.

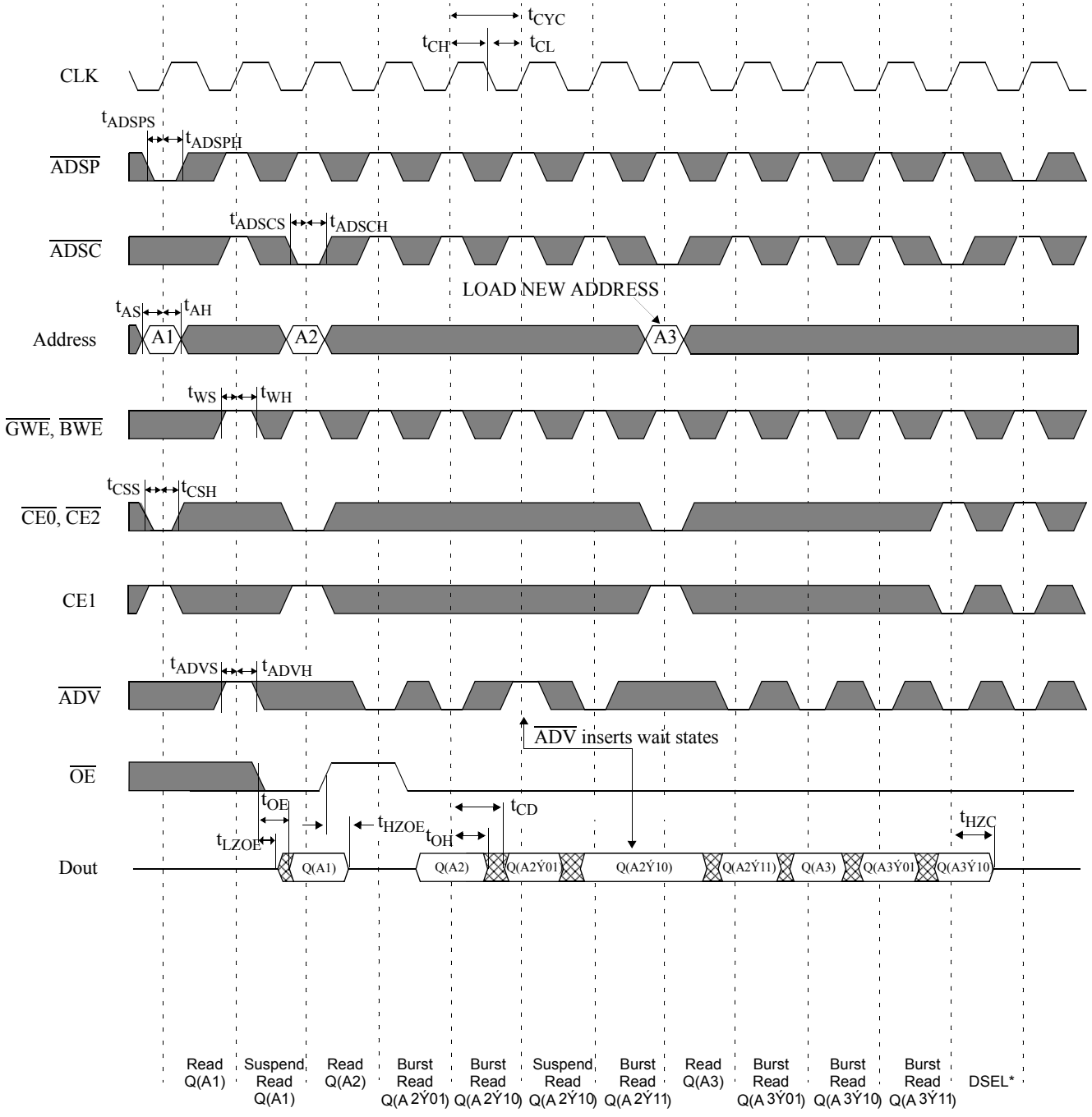
## Snooze Mode Electrical Characteristics

| Description | Conditions | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| Current during Snooze Mode | $ZZ \geq V_{IH}$ | $I_{SB2}$ | | 80 | mA |
| ZZ active to input ignored | | $t_{PDS}$ | 2 | | cycle |
| ZZ inactive to input sampled | | $t_{PUS}$ | 2 | | cycle |
| ZZ active to SNOOZE current | | $t_{ZZI}$ | | 2 | cycle |
| ZZ inactive to exit SNOOZE current | | $t_{RZZI}$ | 0 | | cycle |

## Key to switching waveforms

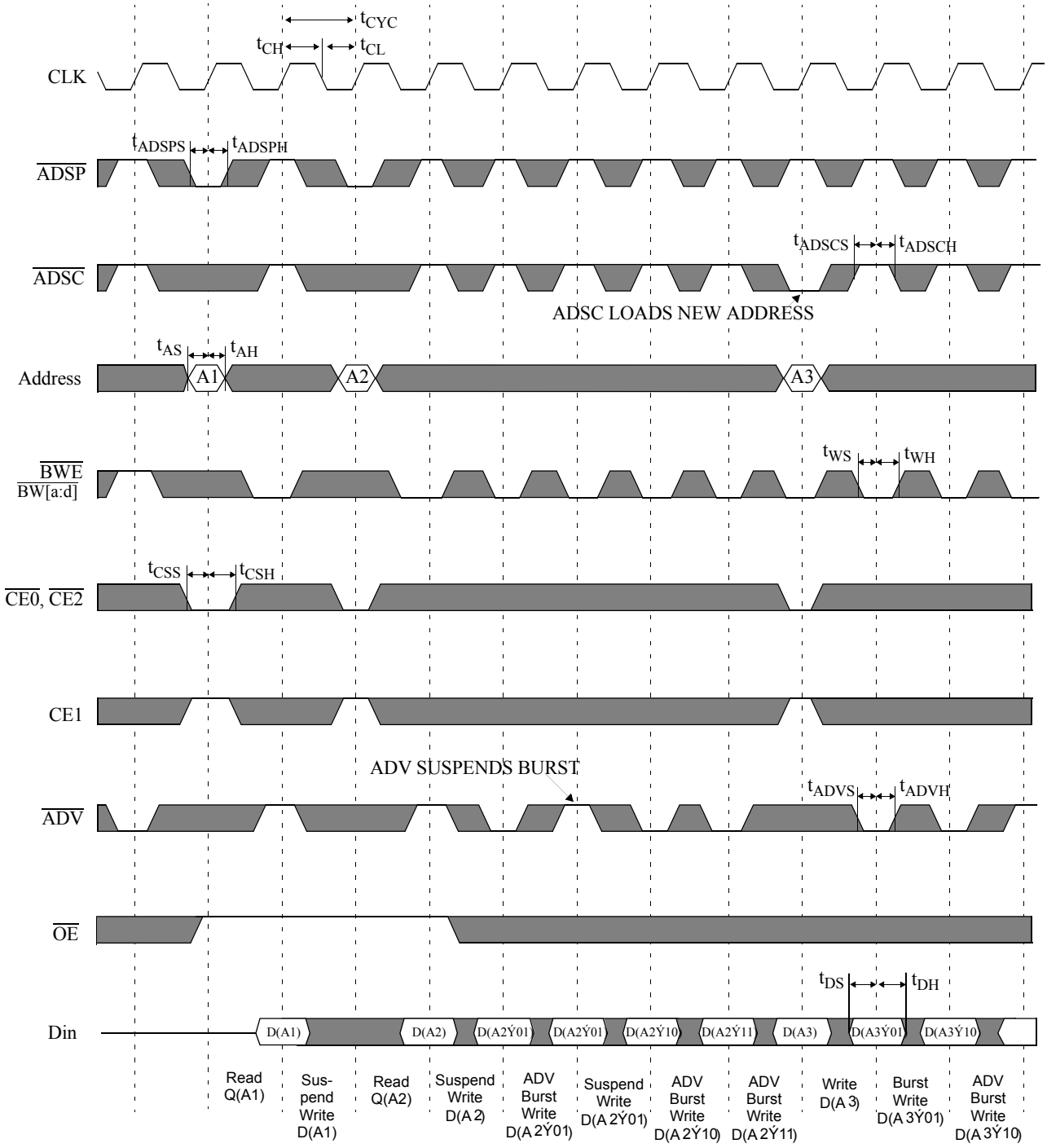
Rising input  Falling input  don't care  Undefined

## Timing waveform of read cycle



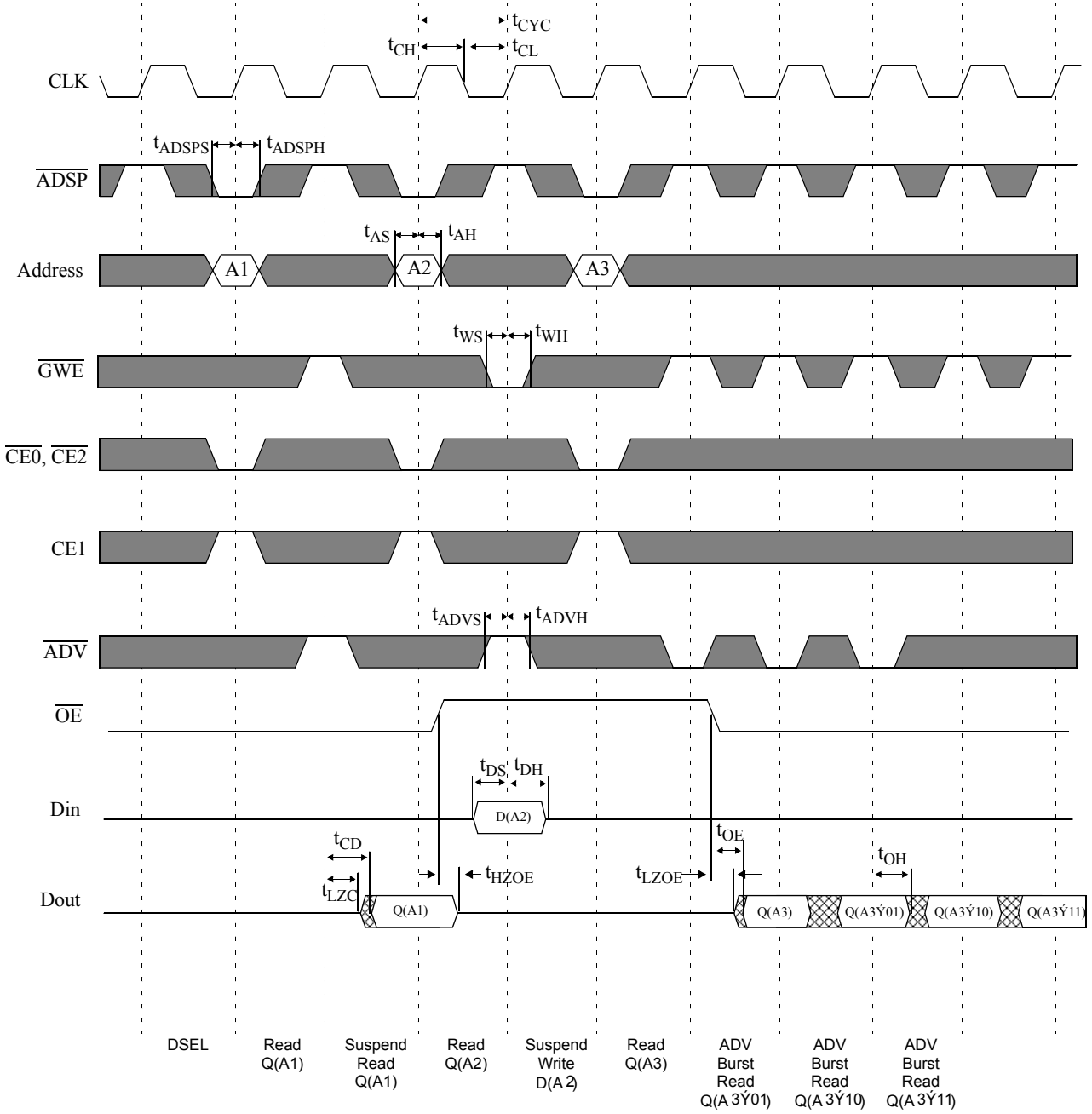

Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low. $\overline{BW[a:d]}$ is don't care.
*Outputs are disabled within two clk cycles after DSEL command

## Timing waveform of write cycle



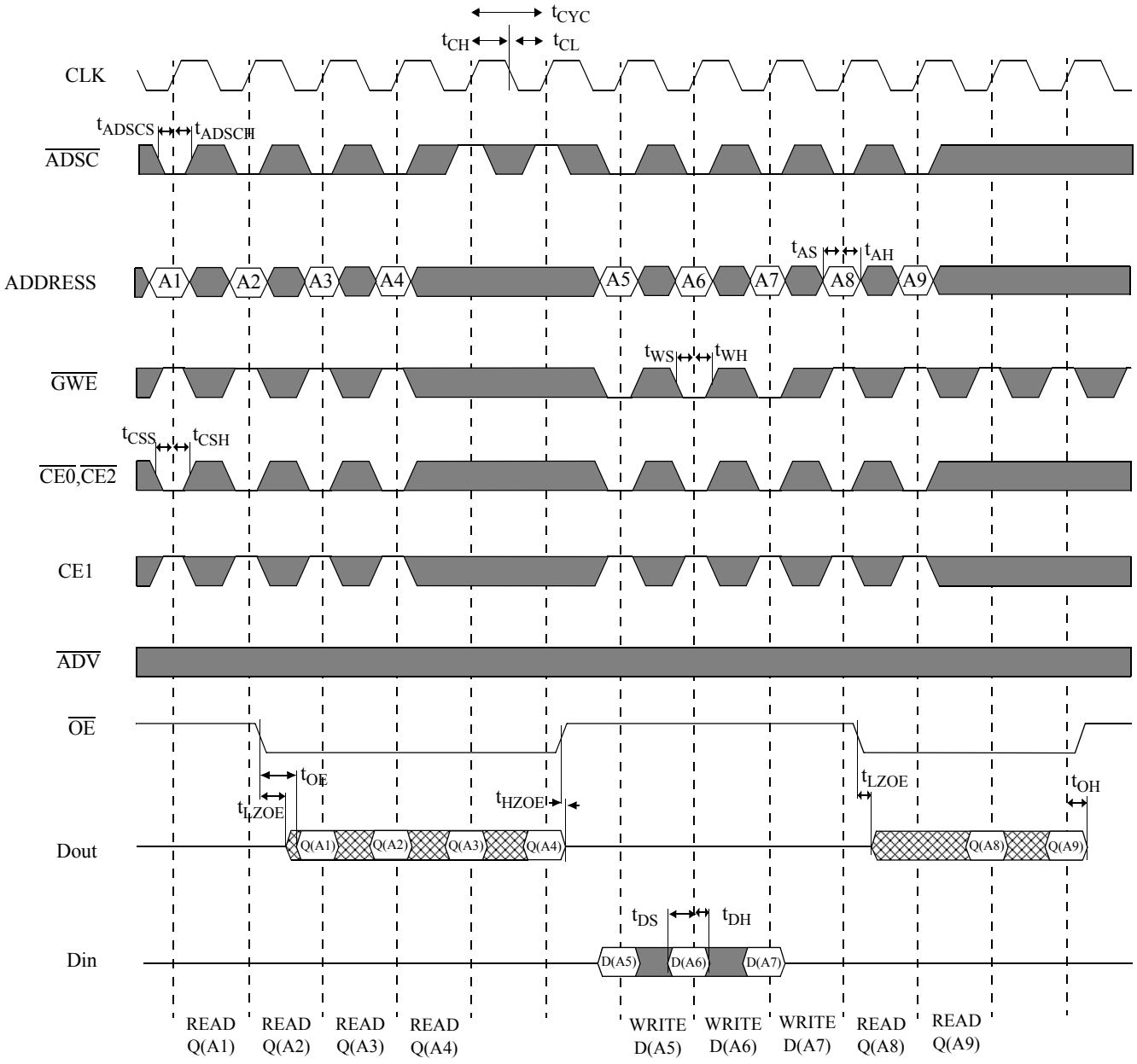

Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low.

## Timing waveform of read/write cycle ($\overline{ADSP}$ Controlled; $\overline{ADSC}$ High)

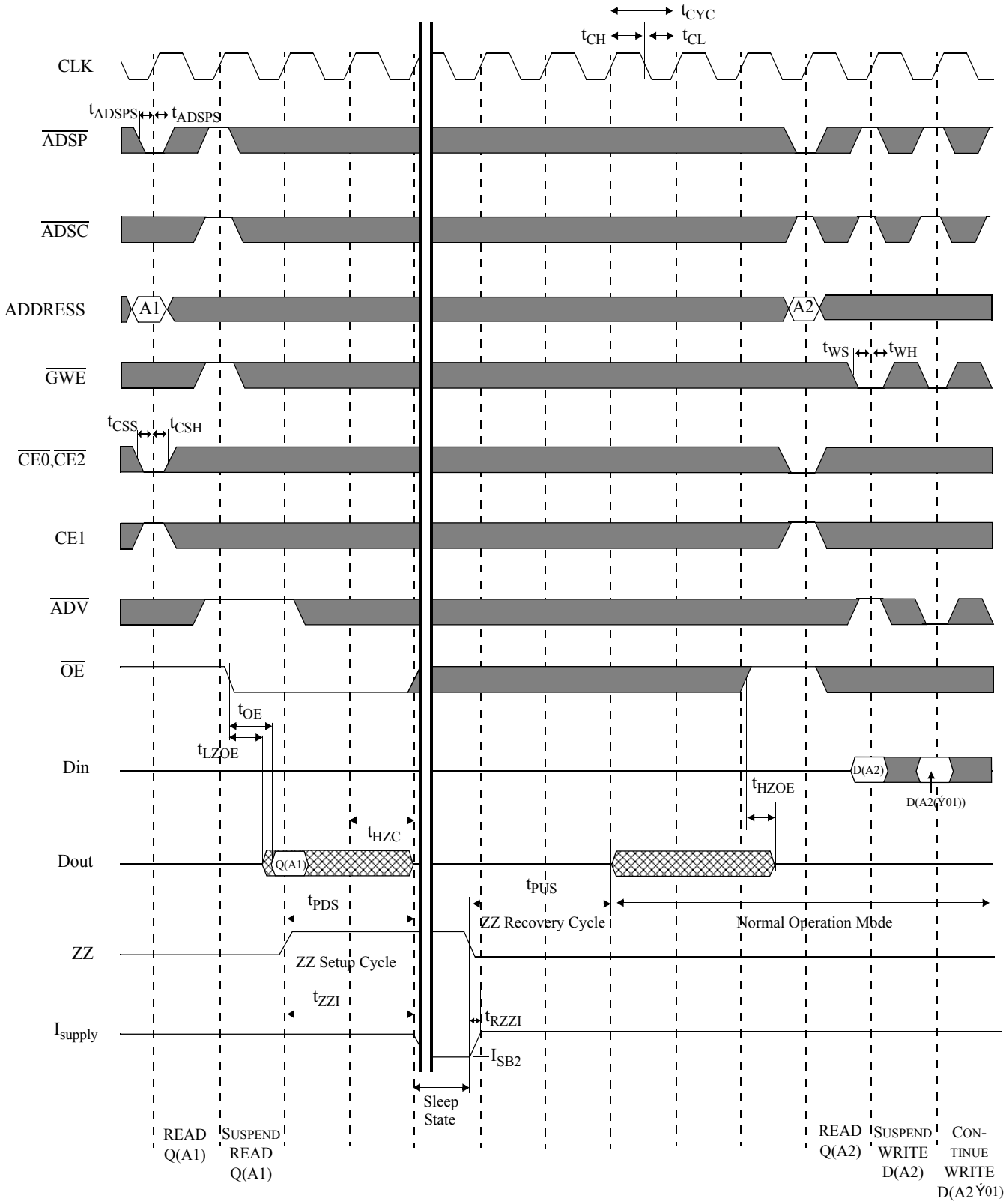



Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low.

## Timing waveform of read/write cycle($\overline{ADSC}$ controlled, $\overline{ADSP}$ = HIGH)



## Timing waveform of power down cycle



## AC test conditions

- Output load: For $t_{LZC}$, $t_{LZOE}$, $t_{HZOE}$, $t_{HZC}$, see Figure C. For all others, see Figure B.
- Input pulse level: GND to 2.5V. See Figure A.
- Input rise and fall time (measured at 0.25V and 2.25V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.25V.

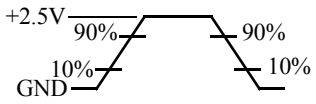



Figure A: Input waveform

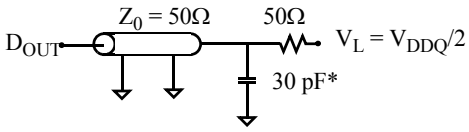



Figure B: Output load (A)

***Thevenin equivalent:***

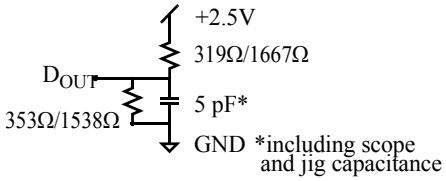



Figure C: Output load(B)

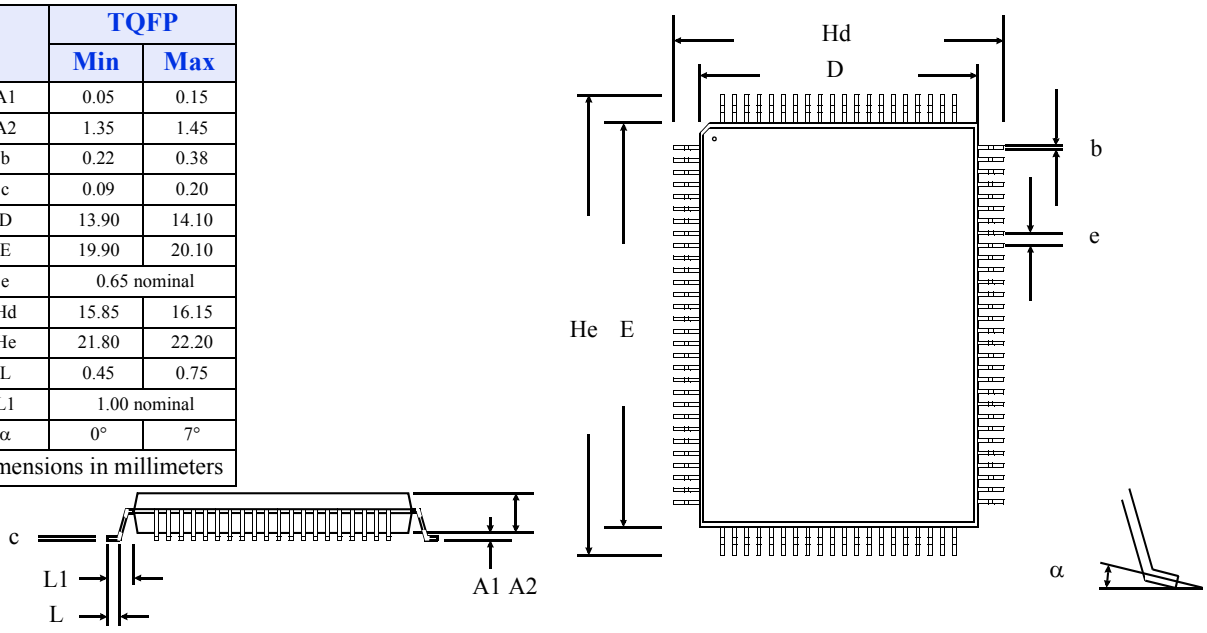
## Notes

1 For test conditions, see "AC test conditions", Figures A, B, and C.
2 This parameter is measured with output load condition in Figure C.
3 This parameter is sampled but not 100% tested.
4 $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZC}$ is less than $t_{LZC}$ at any given temperature and voltage.
5 $t_{CH}$ is measured as high if above VIH, and $t_{CL}$ is measured as low if below VIL.
6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
7 Write refers to $\overline{GWE}$, $\overline{BWE}$, and $\overline{BW[a,b]}$.
8 Chip select refers to $\overline{CE0}$, CE1, and $\overline{CE2}$.

## Package dimensions

### 100-pin quad flat pack (TQFP)

| | TQFP | |
|---|---|---|
| | Min | Max |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.22 | 0.38 |
| c | 0.09 | 0.20 |
| D | 13.90 | 14.10 |
| E | 19.90 | 20.10 |
| e | 0.65 nominal | |
| Hd | 15.85 | 16.15 |
| He | 21.80 | 22.20 |
| L | 0.45 | 0.75 |
| L1 | 1.00 nominal | |
| α | 0° | 7° |
| Dimensions in millimeters | | |



## Ordering information

| Package & Width | -200 | -166 | -133 |
|---|---|---|---|
| TQFP x 18 | AS7C252MPFD18A-200TQC | AS7C252MPFD18A-166TQC | AS7C252MPFD18A-133TQC |
| | AS7C252MPFD18A-200TQI | AS7C252MPFD18A-166TQI | AS7C252MPFD18A-133TQI |

Note:
Add suffix 'N' to the above part numbers for lead free parts (Ex AS7C252MPFD18A-200TQCN)

## Part numbering guide

| AS7C | 25 | 2M | PF | D | 18 | A | –XXX | TQ | C/I | X |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

1. Alliance Semiconductor SRAM prefix
2. Operating voltage: 25 = 2.5V
3. Organization: 2M = 2Meg
4. Pipelined mode
5. Deselect: D = Double cycle deselect
6. Organization: 18 = x 18
7. Production version: A = first production version
8. Clock speed (MHz)
9. Package type: TQ = TQFP
10. Operating temperature: C = commercial (0° C to 70° C); I = industrial (-40° C to 85° C)
11. N = Lead Free Part

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