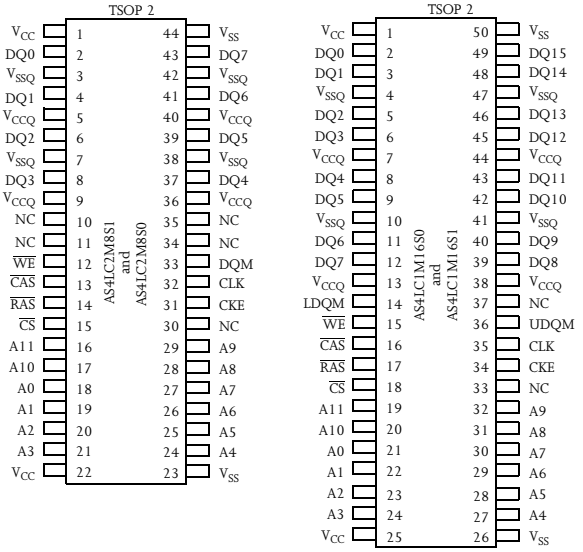
3.3V 2M × 8/1M × 16 CMOS synchronous DRAM

Features

- Organization
  - 1,048,576 words × 8 bits × 2 banks (2M × 8)
    11 row, 9 column address
  - 524,288 words × 16 bits × 2 banks (1M × 16)
    11 row, 8 column address
- All signals referenced to positive edge of clock, fully synchronous
- Dual internal banks controlled by A11 (bank select)
- High speed
  - 143/125/100 MHz
  - 7/8/10 ns clock access time
- Low power consumption
  - Active: 576 mW max
  - Standby: 7.2 mW max, CMOS I/O
- 2048 refresh cycles, 32 ms refresh interval
- 4096 refresh cycles, 64 ms refresh interval
- Auto refresh and self refresh
- PC100 functionality
- Automatic and direct precharge including concurrent autoprecharge
- Burst read, write/Single write
- Random column address assertion in every cycle, pipelined operation
- LVTTL compatible I/O
- 3.3V power supply
- JEDEC standard package, pinout and function
  - 400 mil, 44-pin TSOP 2 (2M × 8)
  - 400 mil, 50-pin TSOP 2 (1M × 16)
- Read/write data masking
- Programmable burst length (1/2/4/8/ full page)
- Programmable burst sequence (sequential/interleaved)
- Programmable $\overline{CAS}$ latency (1/2/3)

Pin arrangement



LEGEND	2M × 8	1M × 16
Configuration	1M × 8 × 2 banks	512K × 16 × 2 banks
Refresh Count	2K/4K	2K/4K
Row Address	(A0 – A10)	(A0 – A10)
Bank Address	2 (BA)	2 (BA)
Column Address	512 (A0 – A8)	256 (A0 – A7)

Pin designation

Pin(s)	Description
DQM (2M × 8) UDQM/LDQM (1M × 16)	Output disable/write mask
A0 to A10	Address inputs RA0 – 10 CA0 – 7 (×16) CA0 – 8 (×8)
A11	Bank address (BA)
DQ0 to DQ7 (2M × 8) DQ0 to DQ15 (1M × 16)	Input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}, V_{CCQ}	Power (3.3V ± 0.3V)
V_{SS}, V_{SSQ}	Ground
CLK	Clock input
CKE	Clock enable

Selection guide

	Symbol	–7	–8	–10	Unit
Bus frequency (CL = 3)	f_{Max}	143	125	100	MHz
Maximum clock access time (CL = 3)	t_{AC}	5.5	6	6	ns
Minimum input setup time	t_S	2	2	2	ns
Minimum input hold time	t_H	1.0	1.0	1.0	ns
Row cycle time (CL = 3, BL = 1)	t_{RC}	70	80	80	ns
Maximum operating current ([×16], RD or WR, CL = 3), BL = 2	I_{CC1}	130	100	100	mA
Maximum CMOS standby current, self refresh	I_{CC6}	1	1	1	mA

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Functional description

The AS4LC2M8S1, AS4LC2M8S0, and AS4LC1M16S1, AS4LC1M16S0 are high-performance 16-megabit CMOS Synchronous Dynamic Random Access Memory (SDRAM) devices organized as 1,048,576 words × 8 bits × 2 banks (2048 rows × 512 columns) and 524,288 words × 16 bits × 2 banks (2048 rows × 256 columns), respectively. Very high bandwidth is achieved using a pipelined architecture where all inputs and outputs are referenced to the rising edge of a common clock. Programmable burst mode can be used to read up to a full page of data (512 bytes for 2M × 8 and 256 bytes for 1M × 16) without selecting a new column address.

The operational advantages of an SDRAM are as follows: (1) the ability to synchronously output data at a high clock frequency with automatic increments of column-address (burst access); (2) bank-interleaving, which hides precharge time and attains seamless operation; and (3) the capability to change column-address randomly on every clock cycle during burst access.

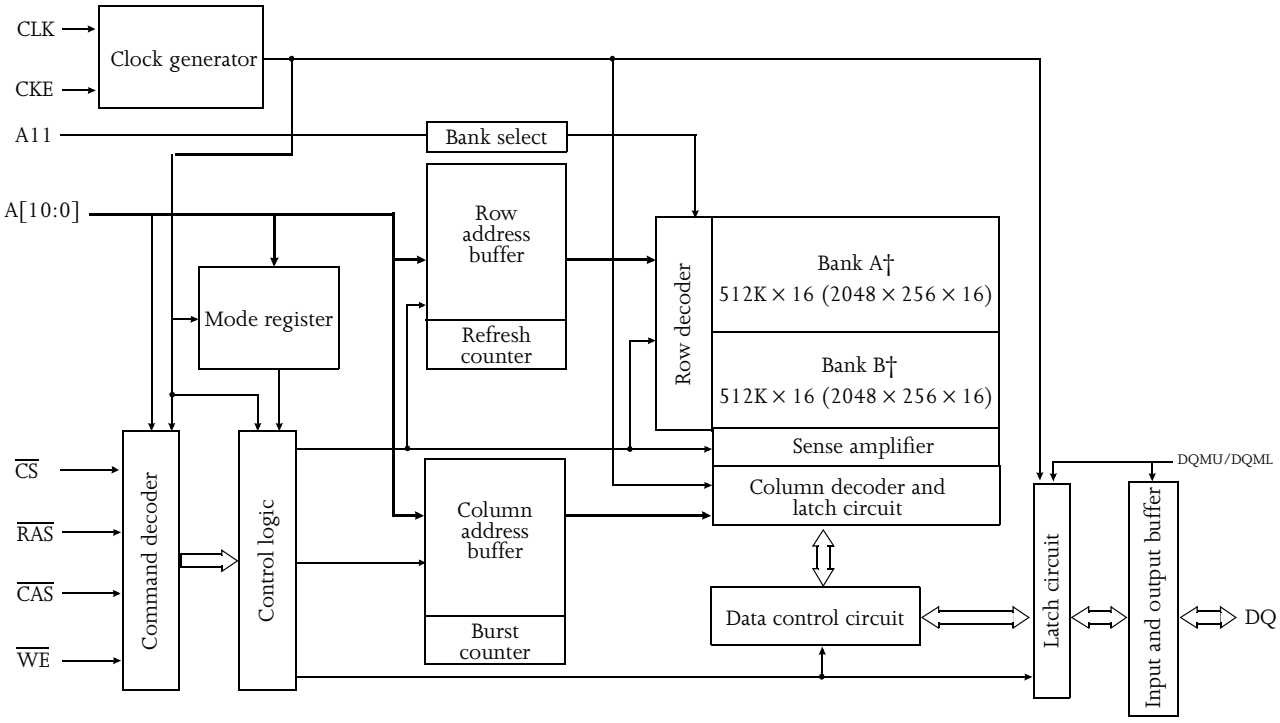
This SDRAM product also features a programmable mode register, allowing users to select read latency as well as burst length and type (sequential or interleaved). Lower latency improves first data access in terms of CLK cycles, while higher latency improves maximum frequency of operation. This feature enables flexible performance optimization for a variety of applications.

SDRAM commands and functions are decoded from control inputs. Basic commands are as follows:

- Mode register set
- Deactivate bank
- Deactivate all banks
- Select row; activate bank
- Select column; write
- Select column; read
- Deselect; power down
- CBR refresh
- Auto precharge with read/write
- Self-refresh

Both devices are available in 400-mil plastic TSOP type 2 package. The AS4LC2M8S1/ AS4LC2M8S0 have 44 pins, and the AS4LC1M16S1/ AS4LC1M16S0 have 50 pins. All devices operate with a power supply of 3.3V ± 0.3V. Multiple power and ground pins are provided for low switching noise and EMI. Inputs and outputs are LVTTL compatible.

Logic block diagram



† For AS4LC2M8S1/AS4LC2M8S0, Banks A and B will read 1M × 8 (2048 × 512 × 8).

Pin descriptions

Pin	Name	Description
CLK	System clock	All operations synchronized to rising edge of CLK.
CKE	Clock enable	Controls CLK input. If CKE is high, the next CLK rising edge is valid. If CKE is low, the internal clock is suspended from the next clock cycle and the burst address and output states are frozen. If both banks are idle and CKE goes low, the SDRAM will enter power down mode from the next clock cycle. When in power down mode and CKE is low, no input commands will be acknowledged. To exit power down mode, raise CKE high before the rising edge of CLK.
$\overline{CS}$	Chip select	Enables or disables device operation by masking or enabling all inputs except CLK, CKE, UDQM/LDQM (×16), DQM (×8).
A0~A10	Address	Row and column addresses are multiplexed. Row address: A0~A10. Column address (2M × 8): A0~A8. Column address (1M × 16): A0~A7.
A11	Bank select	Memory cell array is organized in 2 banks. A11 selects which internal bank will be active. A11 is latched during bank activate, read, write, mode register set, and precharge operations. Asserting A11 low selects Bank A; A11 high selects Bank B.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Row address strobe Column address strobe Write enable	Command inputs. $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, along with $\overline{CS}$, define the command being entered.
×8: DQM ×16: UDQM, LDQM	Output disable/ write mask	Controls I/O buffers. When DQM is high, output buffers are disabled during a read operation and input data is masked during a write operation. DQM latency is 2 clocks for Read and 0 clocks for Write. For ×16, LDQM controls the lower byte (DQ0 – 7) and UDQM controls the upper byte (DQ8 – 15). UDQM and LDQM are considered to be in the same state when referred to jointly as DQM.
DQ0~DQ15	Data input/output	Data inputs/outputs are multiplexed.
V_{CC}/V_{SS}	Power supply/ground	Power and ground for core logic and input buffers.
V_{CCQ}/V_{SSQ}	Data output power/ground	Power and ground for data output buffers.

Operating modes

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9–A0	Note
Mode register set			H	X	L	L	L	L	X		Op code		1,2
Auto refresh			H	H	L	L	L	H	X		X		3
	Self refresh	Entry	H	L	L	L	L	H	X		X		3
		Exit	L	H	L	H	H	H	X		X		3
					H	X	X	X	X		X		3
Bank activate			H	X	L	L	H	H	X	V*	row address		
Read	Auto precharge disable		H	X	L	H	L	H	X	V	L	column address	4
	Auto precharge enable										H		4,5
Write	Auto precharge disable		H	X	L	H	L	L	X	V	L	column address	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X		X		6
Precharge	Selected bank		H	X	L	L	H	L	X	V	L	X	
	Both banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X		X		
					L	V	V	V	X				
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X		X		
					L	H	H	H	X				
		Exit	L	H	H	X	X	X	X				
					L	H	H	H	X				
DQM			H	X	X	X	X	X	V	X	X	X	7
No operation command			H	X	H	X	X	X	X		X		
					L	H	H	H	X				

* V = Valid.

1 OP= operation code.
A0~A11 see page 5.

2 MRS can be issued only when both banks are precharged and no data burst is ongoing. A new command can be issued 2 clock cycles after MRS.

3 Auto refresh functions similarly to CBR DRAM refresh. However, precharge is automatic.
Auto/self refresh can only be issued after both banks are precharged.

4 A11: bank select address. If low during read, write, row active and precharge, bank A is selected.
If high during those states, bank B is selected. Both banks are selected and A11 is ignored if A10 is high during row precharge.

5 A new read/write/deac command to the same bank cannot be issued during a burst read/write with auto precharge.
A new row active command can be issued after t_{RP} from the end of the burst.

6 Burst stop command valid at every burst length except full-page burst.

7 DQM sampled at positive edge of CLK. Data-in may be masked at every CLK (Write DQM latency is 0).
Data-out mask is active 2 CLK cycles after issuance. (Read DQM latency is 2).

Mode register fields

Register programmed with MRS											
Address	A11~A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU†	WBL	TM		$\overline{\text{CAS}}$ latency			BT	Burst length		

† RFU = 0 during MRS cycle.

Write burst length	
A9	Length
0	Programmed burst length
1	Single burst

Burst type	
A3	Type
0	Sequential
1	Interleaved

Test mode		
A8	A7	Type
0	0	Mode register set
0	1	Reserved
1	0	Reserved
1	1	Reserved

CAS latency			
A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	Reserved

Burst length				
A2	A1	A0	BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full page	Reserved

Burst sequence (burst length = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Burst sequence (burst length = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit	Notes
Supply voltage	V_{CC},V_{CCQ}	3.0	3.3	3.6	V	
	GND	0.0	0.0	0.0	V	
Input voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V	8
	V_{IL}	–0.3†	–	0.8	V	8
Output voltage‡	V_{OH}	2.4	–	–	V	
	V_{OL}	–	–	0.4	V	
Ambient operating temperature	T_A	0		70	°C	

† V_{IL} Min = –1.5V for pulse widths less than 5 ns.
‡ I_{OH} = –2mA, and I_{OL} = 2mA.
Recommended operating conditions apply throughout this document unless otherwise specified.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit	Notes
Input voltage	V_{IN},V_{OUT}	–1.0	+4.6	V	
Power supply voltage	V_{CC},V_{CCQ}	–1.0	+4.6	V	
Storage temperature (plastic)	T_{STG}	–55	+150	°C	
Power dissipation	P_D	–	1	W	
Short circuit output current	I_{OUT}	–	50	mA	

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC electrical characteristics

Parameter	Symbol	Test conditions		−7		−8		−10		Unit	Notes
				Min	Max	Min	Max	Min	Max		
Input leakage current	I_{IL}	0V ≤ V_{IN} ≤ V_{CC}, Pins not under test = 0V		−5	+5	−5	+5	−5	+5	µA	
Output leakage current	I_{OL}	D_{OUT} disabled, 0V ≤ V_{OUT} ≤ V_{CCQ}		−10	+10	−10	+10	−10	+10	µA	
Operating current (one bank active)	I_{CC1}	t_{RC} ≥ min, I_O = 0mA, burst length = 1	CL =3	–	140	–	100	–	100	mA	1,3, 4,5
Precharge standby current (power down mode)	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CK} = 15 ns		–	2.0	–	2.0	–	2.0	mA	
	I_{CC2PS}	CKE and CLK ≤ V_{IL}(max), t_{CK} = ∞		–	2.0	–	2.0	–	2.0	mA	
Precharge standby current (non-power-down mode)	I_{CC2N}	CS ≥ V_{IH}(min), CKE ≥ V_{IH}(min), t_{CK} = 15 ns; input signals changed once during 30 ns		–	30	–	30	–	30	mA	1,2,3
	I_{CC2NS}	CLK ≤ V_{IL}(max), CKE ≥ V_{IH}(min), t_{CK} = ∞; input signals stable		–	6	–	6	–	6	mA	1,2,3
Active standby current (power-down mode)	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = 15 ns		–	2	–	2	–	2	mA	1,2,3
	I_{CC3PS}	CLK, CKE ≤ V_{IL}(max), t_{CK} = ∞		–	2	–	2	–	2	mA	1,2,3
Active standby current (non-power-down mode, one bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CK} = 15 ns; input signals changed once during 30 ns		–	35	–	35	–	35	mA	1,2,3
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≥ V_{IL}(max), t_{CK} = ∞; input signals stable		–	10	–	10	–	10	mA	1,2,3
Operating current (burst mode)	I_{CC4}	I_O = 0 mA, Page burst, All banks activated, t_{CCD} = t_{CCD}(min)	CL =3		140	–	130	–	120	mA	1,2, 3,5
			CL =2		125	–	115	–	100		
			CL =1		80	–	70	–	70		
Refresh current	I_{CC5}	t_{RC} ≥ t_{RC}(min)			100	–	90	–	80	mA	1,2, 3,5
Self refresh current	I_{CC6}	CKE ≤ 0.2 V			2	–	2	–	2	mA	
					1	–	1	–	1	mA	15

CL = CAS latency.

AC parameters common to all waveforms

Sym	Parameter	CAS latency	–7		–8		–10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{AC}	CLK to valid output delay	3	–	5.5	–	6	–	6	ns	6
		2	–	8.5	–	7	–	6	ns	6,8
		1	–	18	–	22	–	22	ns	6,8
t_{AH}	Address hold time		–	1	–	1	–	1	ns	7
t_{AS}	Address setup time		2	–	2	–	2	–	ns	7
t_{BDL}	Last data-in to burst stop		0	–	0	–	0	–	t_{CK}	9
t_{CCD}	Read/write command to read/write command		1	–	1	–	1	–	t_{CK}	9
t_{CDL}	Last data-in to new column address delay		1	–	1	–	1	–	t_{CK}	9
t_{CH}	CLK high-level width		2.75	–	3	–	3	–	ns	7
t_{CK}	CLK cycle time	3	7	1000	8	1000	10	1000	ns	10
		2	8.7	1000	10	1000	12	1000	ns	10
		1	20	1000	25	1000	25	1000	ns	10
t_{CKED}	CKE to CLOCK disable or power-down entry mode		1	–	1	–	1	–	t_{CK}	
t_{CKH}	CKE hold time		1	–	1	–	1	–	ns	
t_{CKS}	CKE setup time		2	–	2	–	2	–	ns	
t_{CL}	CLK low-level width		2.75	–	3	–	3.5	–	ns	7
t_{CMH}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM hold time		1	–	1	–	1	–	ns	
t_{CMS}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM setup time		2	–	2	–	2	–	ns	
t_{DAL}	Data-in to ACTIVE command	3	5	–	5	–	5	–	t_{CK}	5,11
		2	5	–	5	–	5	–	t_{CK}	5,11
		1	4	–	4	–	4	–	t_{CK}	5,11
t_{DH}	Data in hold time		1	–	1	–	1	–	ns	
t_{DPL}	Data in to PRECHARGE		2	–	2	–	2	–	t_{CK}	12
t_{DQD}	DQM to input data delay		1	–	1	–	1	–	t_{CK}	9
t_{DQM}	DQM to data mask during writes		0	–	0	–	0	–	t_{CK}	9
t_{DQZ}	DQM to data high Z during reads		2	–	2	–	2	–	t_{CK}	9
t_{DS}	Data in setup time		2	–	2	–	2	–	ns	
t_{DWD}	Write command to input data delay		0	–	0	–	0	–	t_{CK}	9
t_{HZ}	Data-out high-impedance time	3	–	5.5	–	6	–	9	ns	13
		2	–	8.5	–	9	–	9	ns	13
		1	–	18	–	22	–	22	ns	13
t_{LZ}	Data-out low-impedance time		1	–	1	–	1	–	ns	

Sym	Parameter	CAS latency	–7		–8		–10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{MRD}	Load mode register to active/refresh command		2	–	2	–	2	–	t_{CK}	5
t_{OH}	Output data hold time @ 30 pF	3	2	–	2.5	–	3	–	ns	6
		2	2	–	2.5	–	3	–	ns	6
		1	2	–	2.5	–	3	–	ns	6
t_{PED}	CKE to CLOCK enable or power-down exit mode		1	–	1	–	1	–	t_{CK}	
t_{RAS}	Active to precharge command		42	120,000	48	120,000	50	120,000	ns	
t_{RC}	Active command period		70	–	80	–	80	–	ns	8
t_{RCAR}	Auto refresh period		70	–	80	–	80	–	ns	
t_{RCD}	Active to read or write delay	3	3	–	3	–	3	–	t_{CK}	8
t_{REF}	Refresh period—2048 rows		–	64	–	64	–	64	ms	
t_{ROH}	Data-out high Z from precharge/burst stop command	3	3	–	3	–	3	–	t_{CK}	9
		2	2	–	2	–	2	–	t_{CK}	9
		1	1	–	1	–	1	–	t_{CK}	9
t_{RP}	Precharge command period	3	3	–	3	–	3	–	t_{CK}	8
t_{RRD}	Active Bank A to Active Bank B command		14	–	16	–	20	–	ns	
t_T	Transition time		0.3	1.0	0.3	1.0	0.3	1.0	ns	
t_{WR}	WRITE recovery time		2	–	2	–	2	–	t_{CK}	
t_{XSR}	Exit SELF REFRESH to ACTIVE command		70	–	80	–	80	–	ns	20

Notes

1 I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.

2 Other input signals are allowed to transition no more than once in any two-clock period and are otherwise at valid V_{IH} or V_{IL} levels.

3 Address transitions average one transition every two-clock period.

4 The I_{DD} current will decrease as the CAS-latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS-latency is reduced.

5 t_{CK} = 7 ns for –7, 8 ns for –8, and 10 ns for –10.

6 If clock $t_r > 1$ ns, $(t_{r/2} - 0.5)$ns should be added to the parameter.

7 If clock (t_r and t_f) > 1 ns, $[(t_r + t_f)/2 - 1]$ ns should be added to the parameter.

8 V_{IH} overshoot: $V_{IH(max)} = V_{DDQ} + 2V$ for a pulse width ≤ 3 ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL(min)} = -2V$ for a pulse width ≤ 3 ns and the pulse width cannot be greater than one third of the cycle rate.

9 Required clocks are specified by JEDEC functionalisty and are not dependent on any timing parameter.

10 The clock frequency must remain constant during access or precharge states (READ, WRITE, including t_{WR} and PRECHARGE commands). CKE may be used to reduce the data rate.

11 Timing actually specified t_{WR} plus t_{RP}; clock(s) specified as a reference only at minimum cycle rate.

12 Timing actually specified by t_{WR}.

13 t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going to HIGH-Z.

14 CLK must be toggled a minimum of two times during this period.

15 Enables on-chip refresh and address counters.

16 All voltages referenced to V_{SS}.

17 The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (0° C ≤ T_A ≤ 70° C) is endured.

18 A proper power-up initialization sequence (as described on page 10) is needed before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at the same potential.)Two AUTOREFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.

19 AC characteristics assume t_T = 1 ns.

20 In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

21 AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3.0 V with timing referenced to 1.4V crossover point.

22 I_{DD} specifications are tested after the device is properly initialized.

23 Minimum clock cycles = (minimum time/clock cycle time) rounded up.

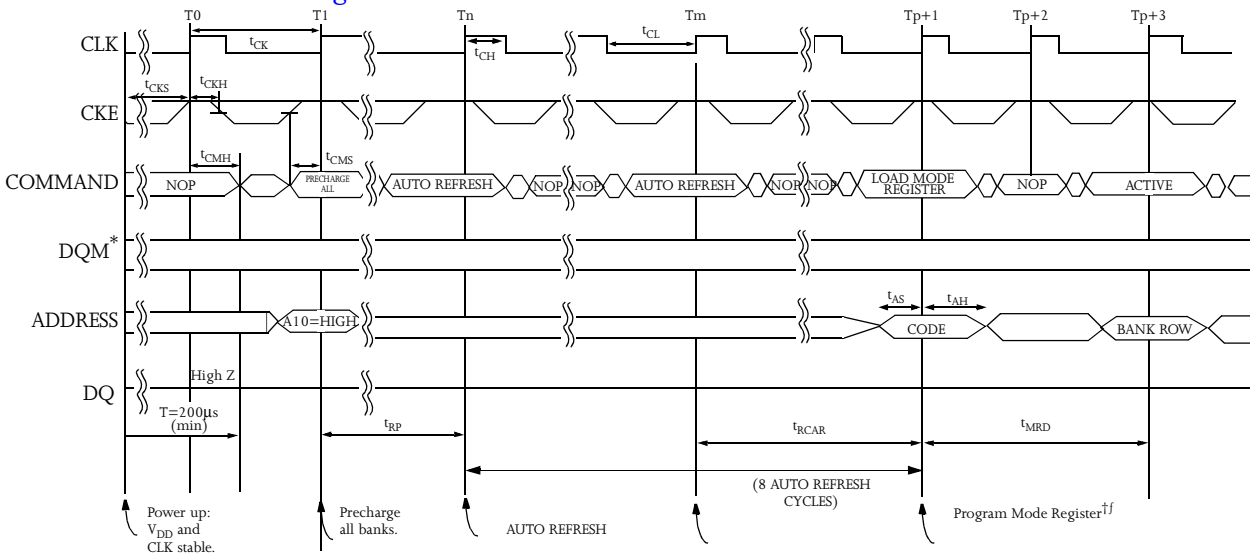
Device operation

Command	Pin settings	Description
Power up		The following sequence is recommended prior to normal operation. 1 Apply power, start clock, and assert CKE and DQM high. All other signals are NOP. 2 After power-up, pause for a minimum of 200µs. CKE/DQM = high; all others NOP. 3 Precharge both banks. 4 Perform Mode Register Set command to initialize mode register. 5 Perform a minimum of 8 auto refresh cycles to stabilize internal circuitry. (Steps 4 and 5 may be interchanged.)
Mode register set	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = low; A0~A11 = opcode	The mode register stores the user selected opcode for the SDRAM operating modes. The CAS latency, burst length, burst type, test mode and other vendor specific functions are selected/programmed during the Mode Register Set command cycle. The default setting of the mode register is not defined after power-up. Therefore, it is recommended that the power-up and mode register set cycle be executed prior to normal SDRAM operation. Refer to the Mode Register Set table and timing for details.
Device deselect and no operation	CS = high, or $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = high	The SDRAM performs a "no operation" (NOP) when $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ = high. Since the NOP performs no operation, it may be used as a wait state in performing normal SDRAM functions. The SDRAM is deselected when $\overline{CS}$ is high. $\overline{CS}$ high disables the command decoder such that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address inputs are ignored. Device deselection is also considered a NOP.
Bank activation	$\overline{CS}$ = $\overline{RAS}$ = low; $\overline{CAS}$ = $\overline{WE}$ = high; A0~A10 = row address; A11 = bank select	The SDRAM is configured with two internal banks. Use the Bank Activate command to select a row in one of the two idle banks. Initiate a read or write operation after t_{RCD}(min) from the time of bank activation.
Burst read	$\overline{CS}$ = $\overline{CAS}$ = A10 = low; $\overline{RAS}$ = $\overline{WE}$ = high; A11 = bank select, A0~A8 = column address; (A9 = don't care for 2M × 8; A8, A9 = don't care for 1M × 16)	Use the Burst Read command to access a consecutive burst of data from an active row in an active bank. Burst read can be initiated on any column address of an active row. The burst length, sequence and latency are determined by the mode register setting. The first output data appears after the $\overline{CAS}$ latency from the read command. The output goes into a high impedance state at the end of the burst (BL = 1,2,4,8) unless a new burst read is initiated to form a gapless output data stream. A full-page burst does not terminate automatically at the end of the burst. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write

Command	Pin settings	Description
Burst write	$\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ = A10 = low; $\overline{RAS}$ = high; A0~A9 = column address; (A9 = don't care for 2M × 8; A8, A9 = don't care for 1M × 16)	Use the Burst Write command to write data into the SDRAM on consecutive clock cycles to adjacent column addresses. The burst length and addressing mode is determined by the mode register opcode. Input the initial write address in the same clock cycle as the Burst Write command. Burst terminate behavior for write is the same as that for read. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write. DQM can also be used to mask the input data.
UDQM/LDQM (×16) DQM (×8) operation		Use DQM to mask input and output data. It disables the output buffers in a read operation and masks input data in a write operation. The output data is invalid 2 clocks after DQM assertion (2 clock latency). Input data is masked on the same clock as DQM assertion (0 clock latency).
Burst stop	$\overline{CS}$ = $\overline{WE}$ = low; $\overline{RAS}$ = $\overline{CAS}$ = high	Use burst stop to terminate burst operation. This command may be used to terminate all legal burst lengths.
Bank precharge	$\overline{CS}$ = A10 = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = high; A11 = bank select; A0~A9 = don't care	The Bank Precharge command precharges the bank specified by A11. The precharged bank is switched from active to idle state and is ready to be activated again. Assert the precharge command after t_{RAS}(min) of the bank activate command in the specified bank. The precharge operation requires a time of t_{RP}(min) to complete.
Precharge all	$\overline{CS}$ = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = A10 = high; A11, A0~A9 = don't care	The Precharge All command precharges both banks simultaneously. Both banks are switched to the idle state on precharge completion.
Auto precharge	Write: $\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ = low ; Read: $\overline{CS}$ = $\overline{CAS}$ = low; A10 = high; A11 = bank select; A0~A9 = column address; (A9 = don't care for 2M × 8; A8, A9 = don't care for 1M × 16)	During auto precharge, the SDRAM adjusts internal timing to satisfy t_{RAS}(min) and t_{RP} for the programmed $\overline{CAS}$ latency and burst length. Couple the auto precharge with a burst read/write operation by asserting A10 to a high state at the same time the burst read/write commands are issued. At auto precharge completion, the specified bank is switched from active to idle state. Note that no new commands (RD/WR/DEAC) can be issued to the same bank until the specified bank achieves the idle state. Auto precharge does not work with full-page burst.
Clock suspend/power down mode entry	CKE = low	When CKE is low, the internal clock is frozen or suspended from the next clock cycle and the state of the output and burst address are frozen. If both banks are idle and CKE goes low, the SDRAM enters power down mode at the next clock cycle. When in power down mode, no input commands are acknowledged as long as CKE remains low. To exit power down mode, raise CKE high before the rising edge of CLK.
Clock suspend/power down mode exit	CKE = high	Resume internal clock operation by asserting CKE high before the rising edge of CLK. Subsequent commands can be issued one clock cycle after the end of the Exit command.

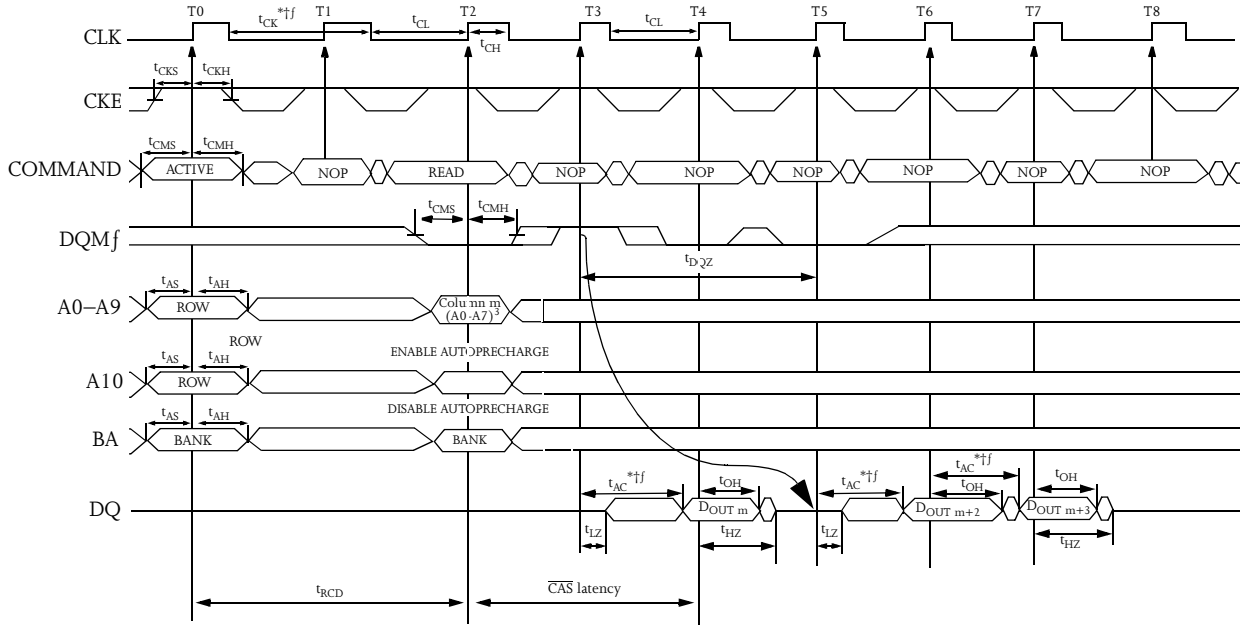
Command	Pin settings	Description
Auto refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = low; $\overline{WE}$ = CKE = high; A0~A11 = don't care	SDRAM storage cells must be refreshed every 64 ms to maintain data integrity. Use the auto refresh command to accomplish the refreshing of all rows in both banks of the SDRAM. The row address is provided by an internal counter which increments automatically. Auto refresh can only be asserted when both banks are idle and the device is not in the power down mode. The time required to complete the auto refresh operation is t_{RC}(min). Use NOPs in the interim until the auto refresh operation is complete. Both banks will be in the idle state after this operation.
Self refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = $\overline{CKE}$ = low; WE = high; A0~A11 = don't care	Self refresh is another mode for refreshing SDRAM cells. In this mode, refresh address and timing are provided internally. Self refresh entry is allowed only when both banks are idle. The internal clock and all input buffers with the exception of CKE are disabled in this mode. Exit self refresh by restarting the external clock and then asserting CKE high. NOPs must follow for a time of t_{RC}(min) for the SDRAM to reach the idle state where normal operation is allowed. If burst auto refresh is used in normal operation, burst 2048 auto refresh cycles immediately after exiting self refresh.

Initialize and load mode register



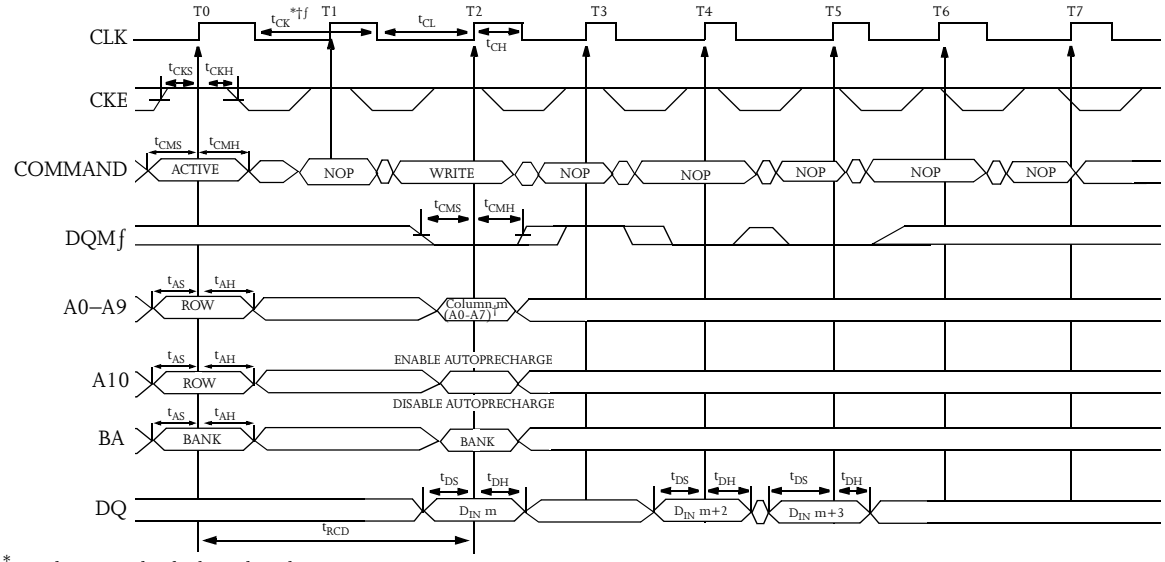
* DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
† The Mode Register may be loaded prior to the auto refresh cycles if desired.
ƒ Outputs are guaranteed High-Z after command is issued.

Read—DQM operation*



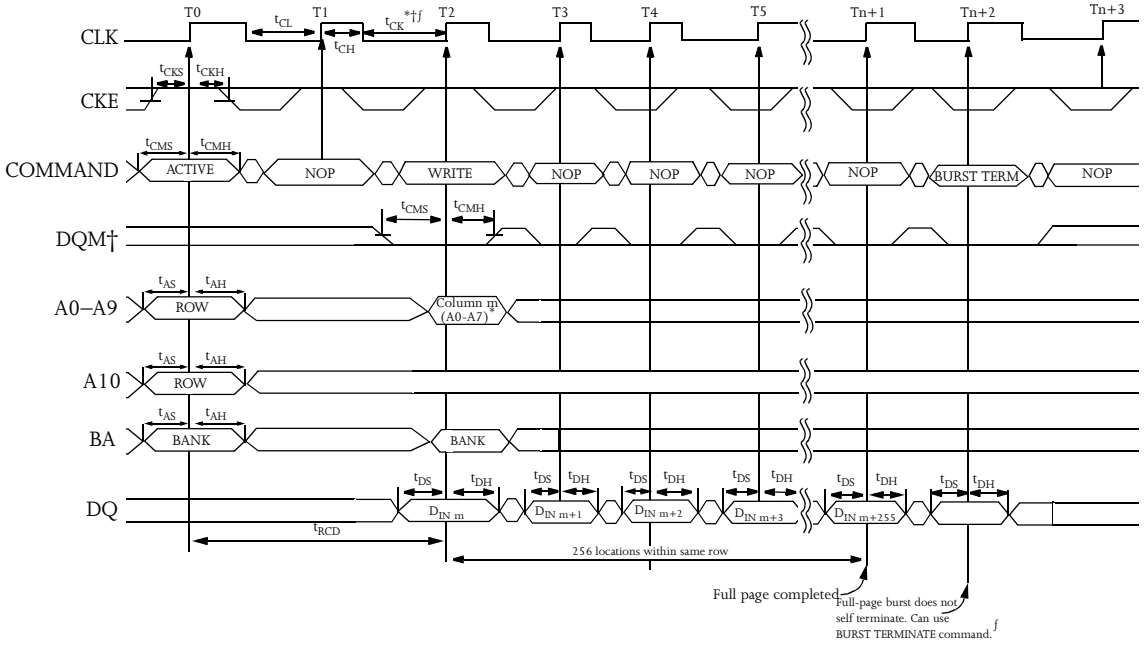
* For this example, the burst length = 4, and the $\overline{CAS}$ latency = 2.
† A8 and A9 = "Don't care."
ƒ DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

Write—DQM operation*



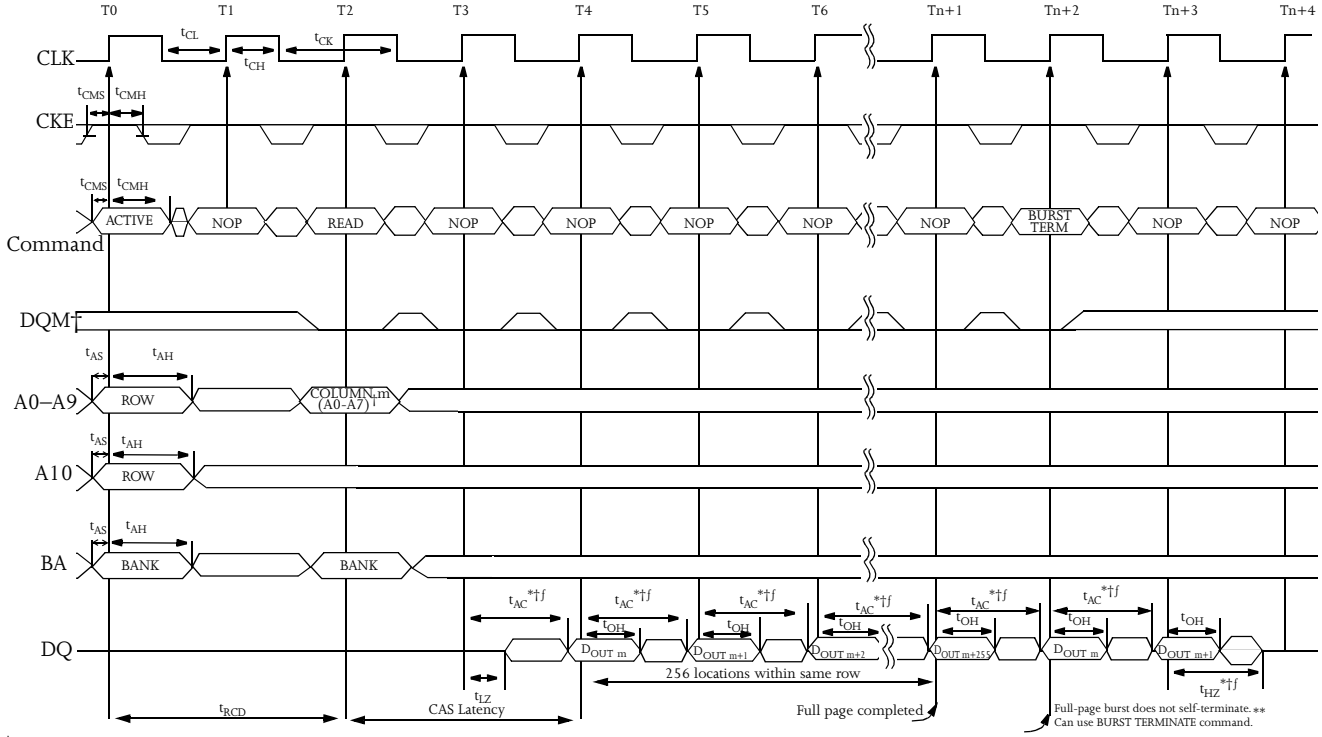
* For this example, the burst length = 4.
† A8 and A9 = "Don't care."
ƒ DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

Write—full-page burst



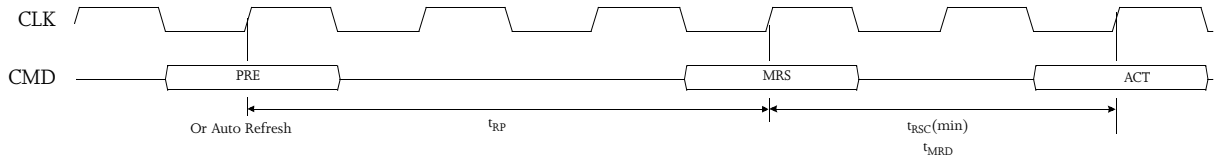
* A8 and A9 = Don't care.
† DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
ʃ Page left open; no t_{RP}.

Read—full-page burst*



* For this example, the CAS latency = 2.
† A8 and A9 = "Don't care."
ʃ DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
** Page left open; no t_{RP}

Mode register set command waveform

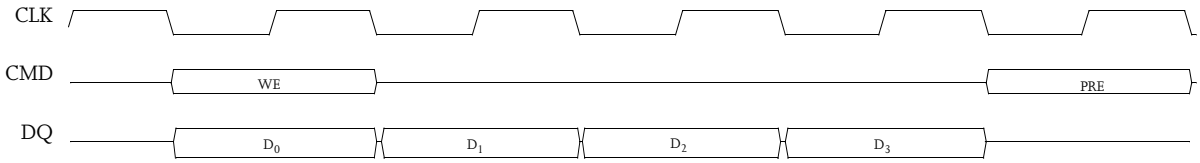


MRS can be issued only when both banks are idle.

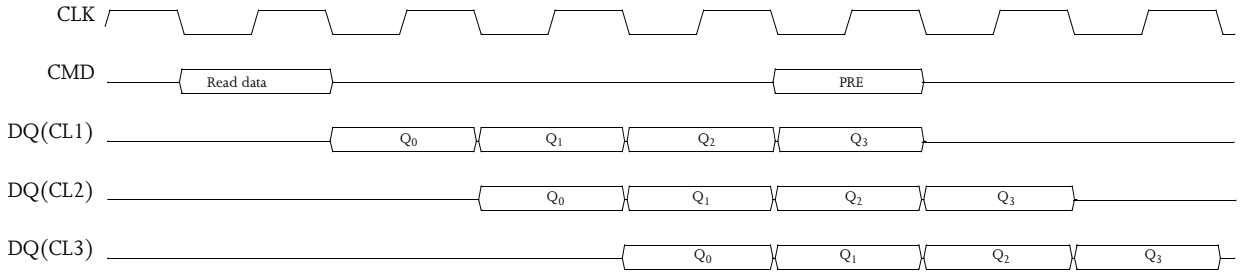
Precharge waveforms

Precharge can be asserted after t_{RAS} (min). The selected bank will enter the idle state after t_{RP}. The earliest assertion of the precharge command without losing any burst data is show below.

(normal write; BL = 4)



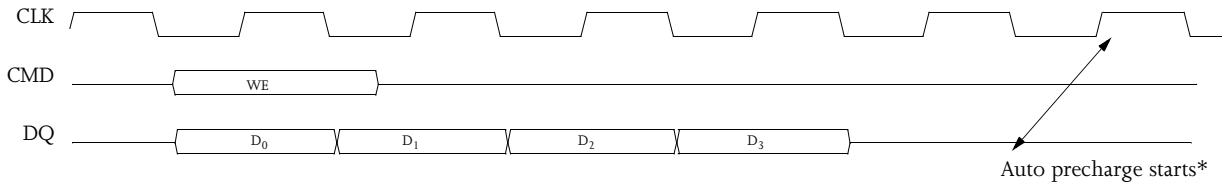
(normal read; BL = 4)



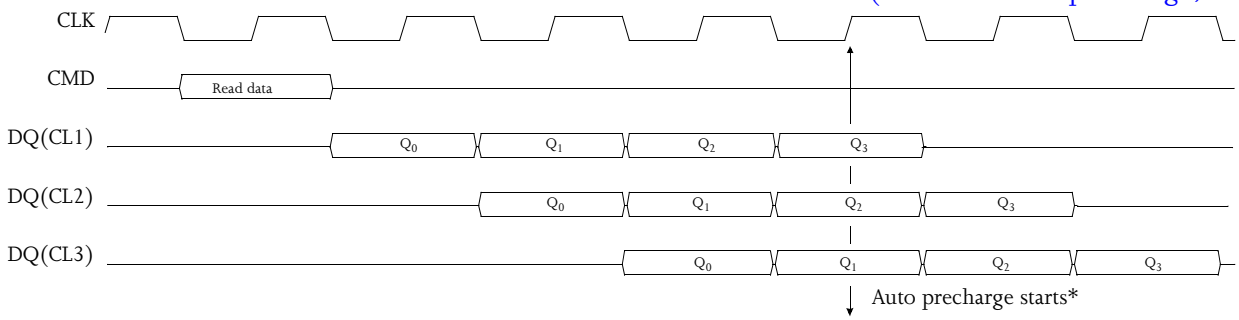
Auto precharge waveforms

A10 controls the selection of auto precharge during the read or write command cycle.

(write with auto precharge; BL = 4)

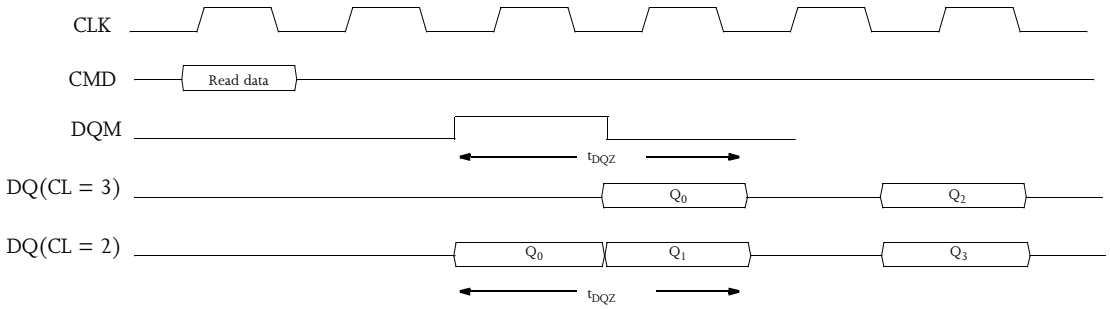


(read with auto precharge; BL = 4)

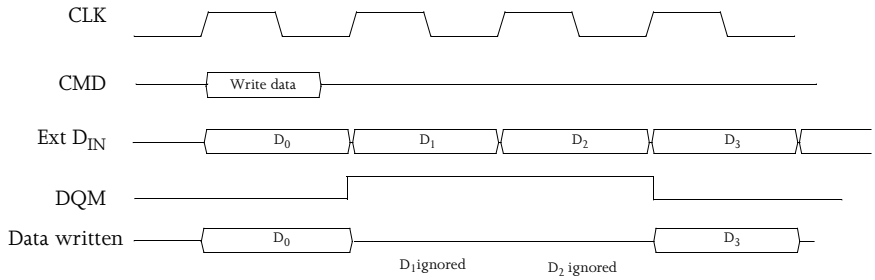


*The row active command of the precharge bank can be issued after tRP from this point. The new read/write command of another activated bank can be issued from this point. At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

DQM waveforms: read (CL = 3, BL = 4)



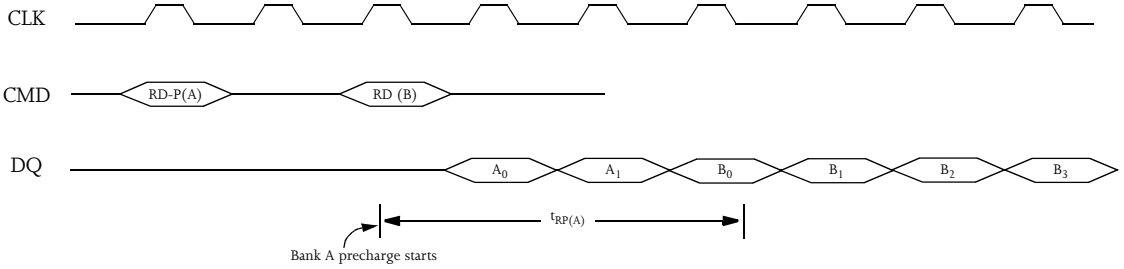
DQM waveforms: write (BL = 4)



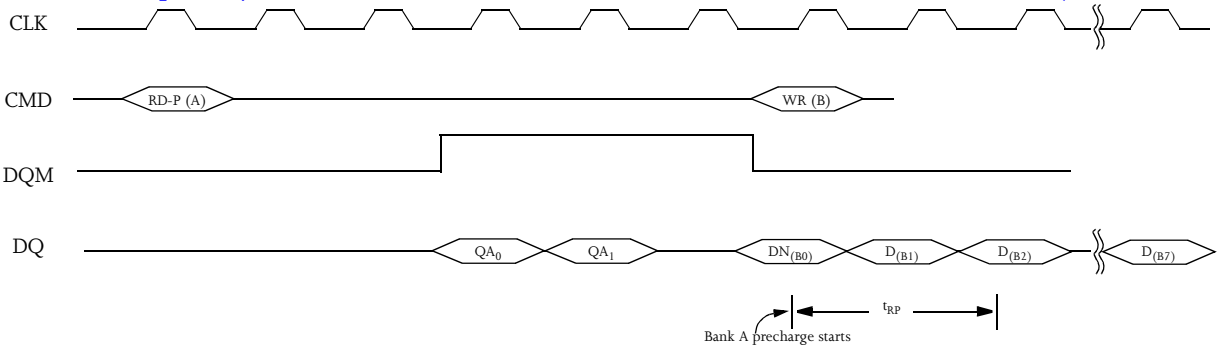
Concurrent Auto-P Waveforms

According to Intel™'s specification, auto-p burst interruption is allowed by another burst provided that the interrupting burst is in a different bank than the ongoing burst.

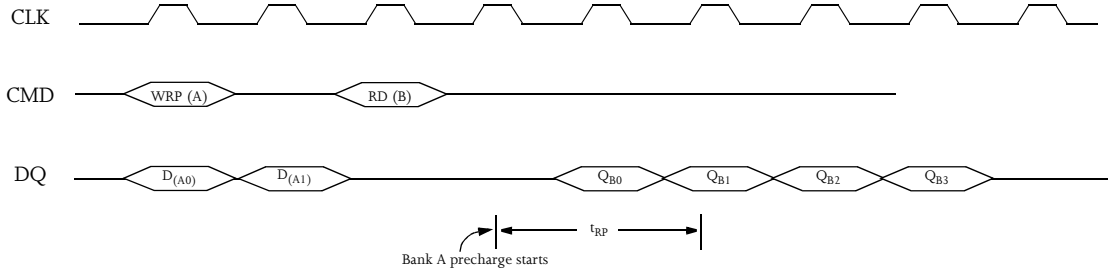
(A) RD-P interrupted by RD in another bank (CL = 3, BL = 4)



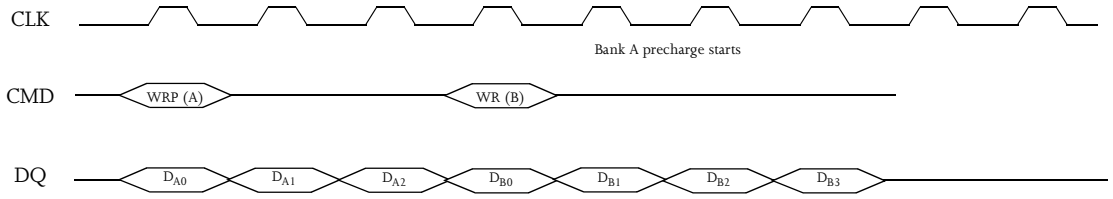
(B) RD-P interrupted by WR in another bank (CL = 3, BL = 8)



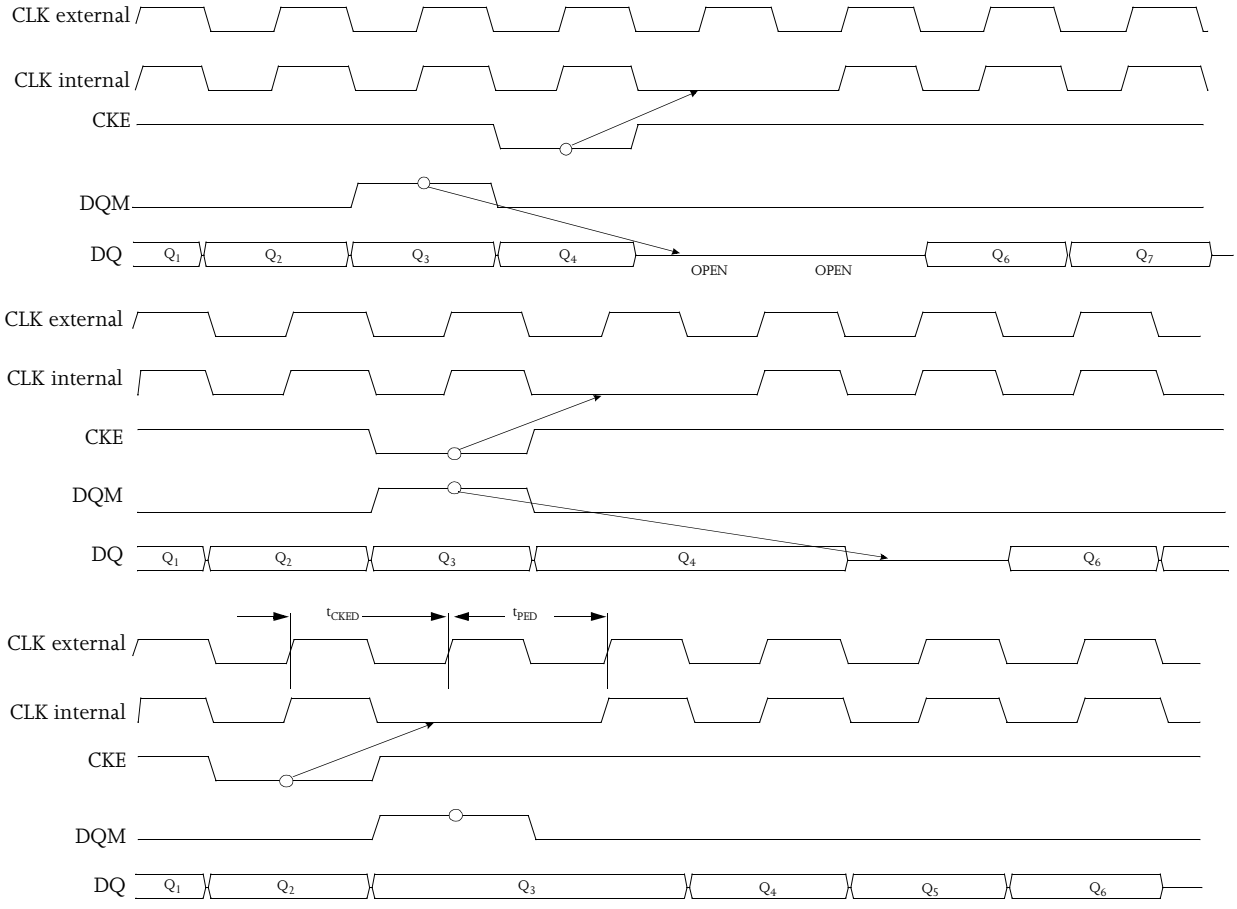
(C) WR-P interrupted by RD in another bank (CL = 2, BL = 4)



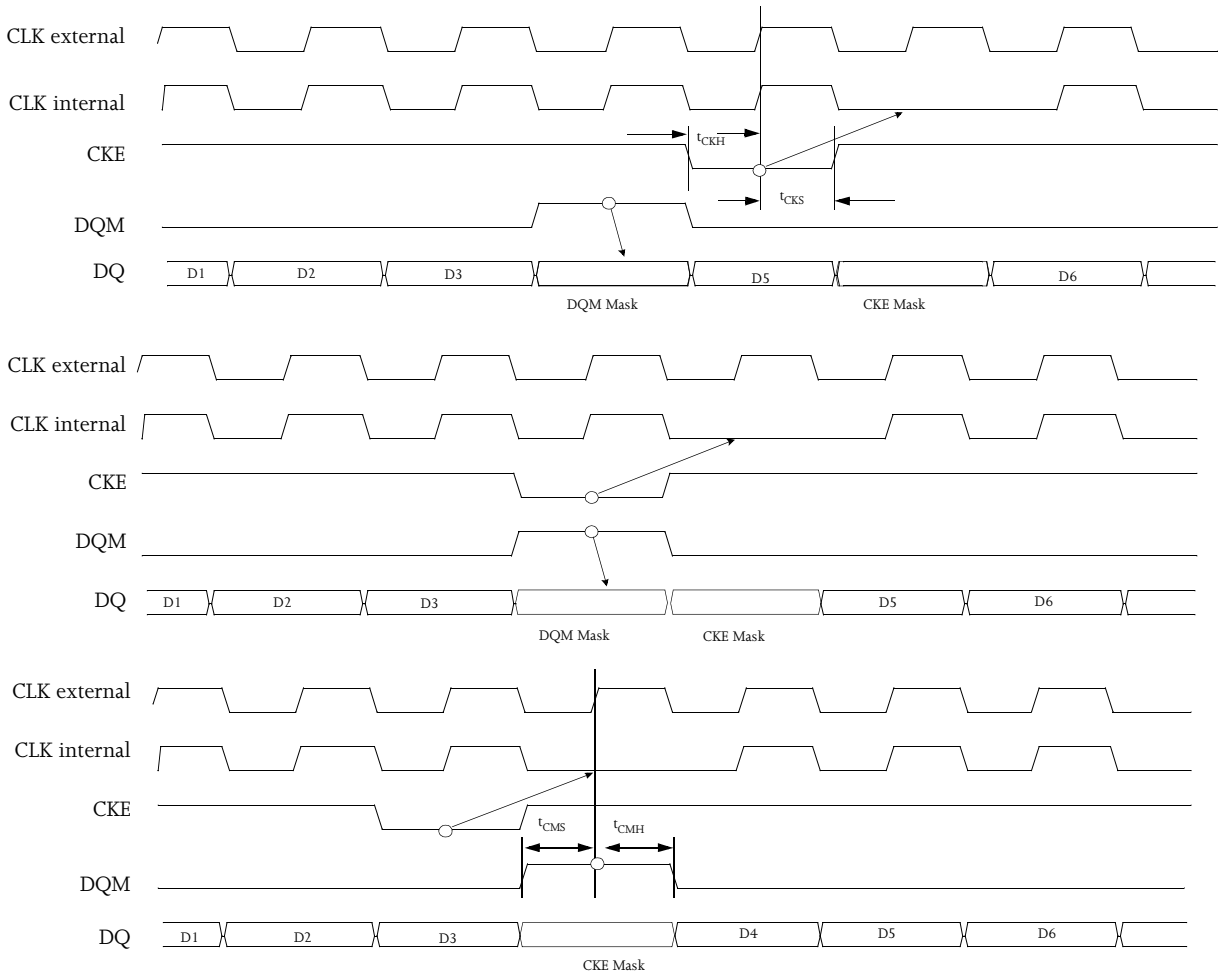
(D) WR-P Interrupted by WR in another bank (CL = 3, BL = 4)



Clock suspension read waveforms (BL = 8)

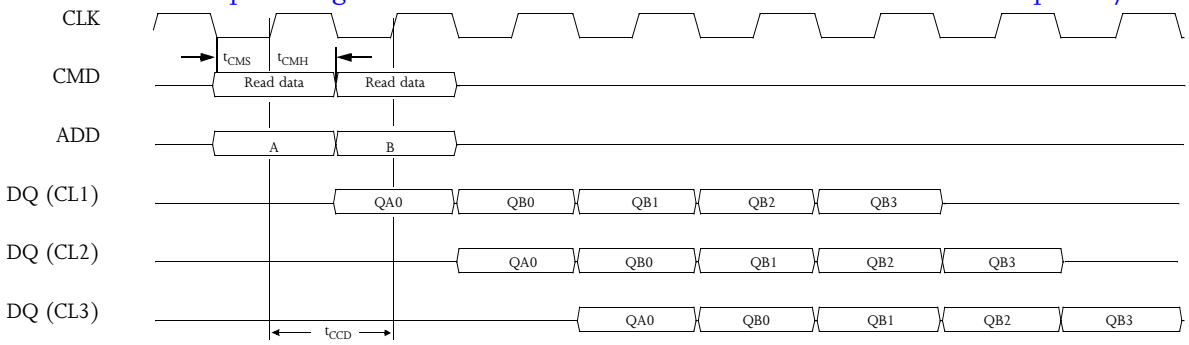


Clock suspension write waveforms



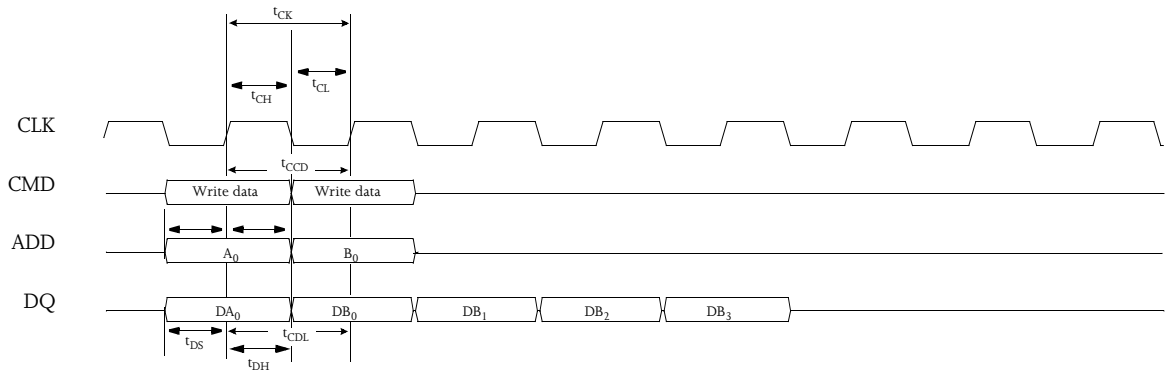
Read/write interrupt timing

read interrupted by read (BL = 4)



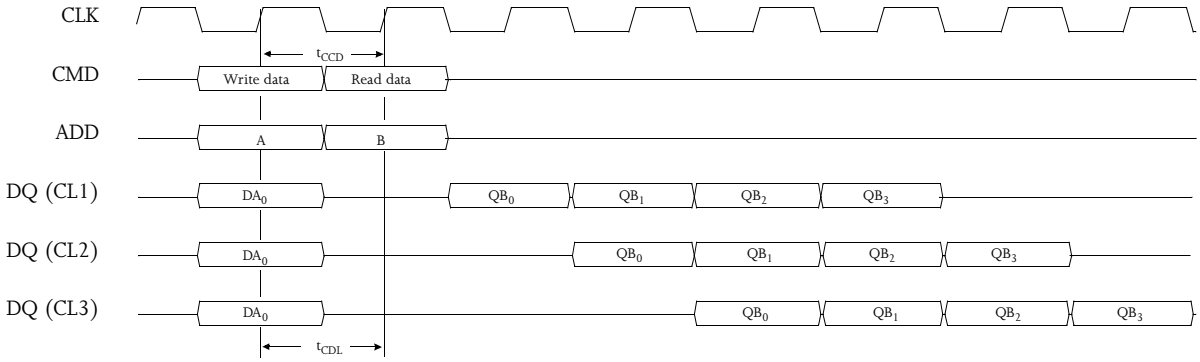
t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK).

write interrupted by write (BL = 4)



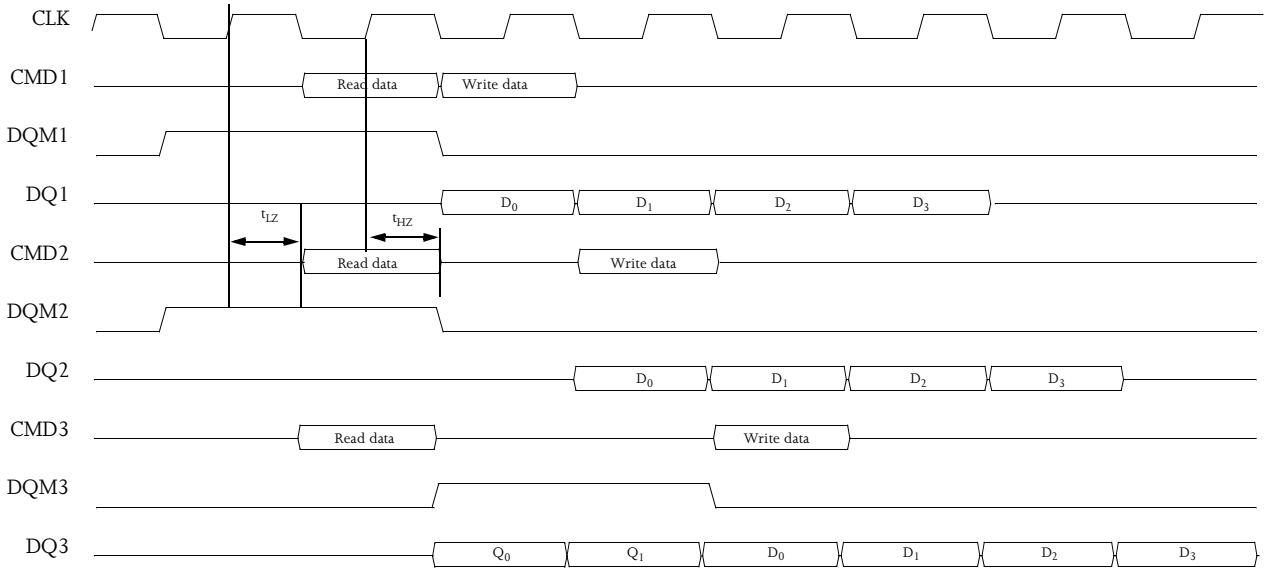
t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK).
t_{CDL} = last address in to new column addres delay (= 1 CLK).

write interrupted by read (BL = 4)



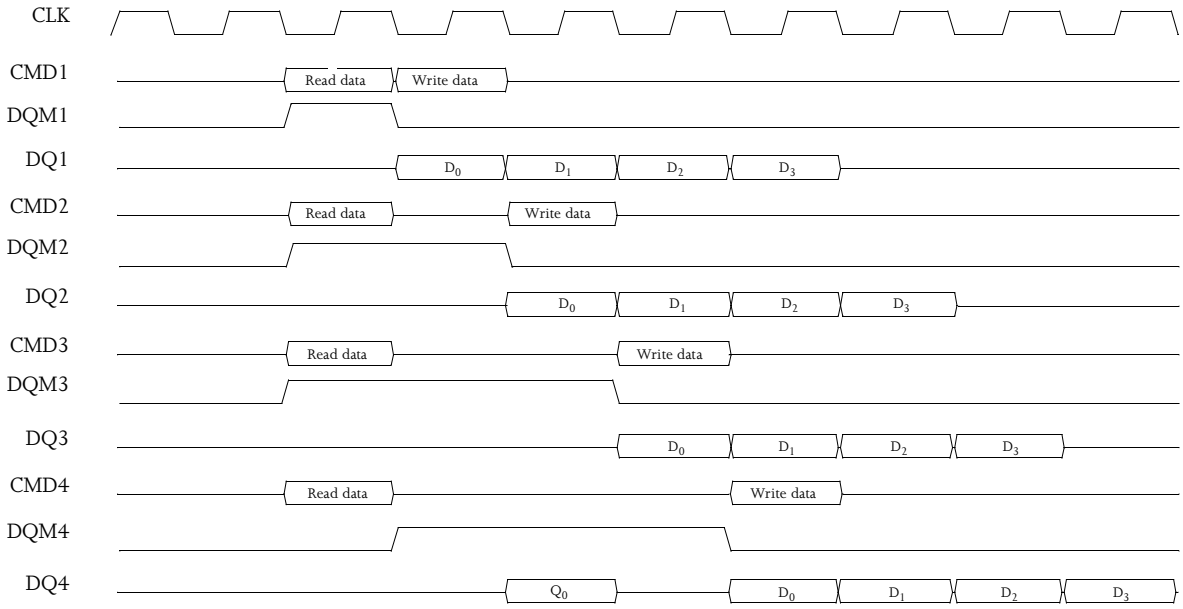
t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK).
t_{CDL} = last address in to new column addres delay (= 1 CLK).
Interrupting RD/WR can be for either the same or different banks.

read interrupted by write (CL = 1, BL = 4)



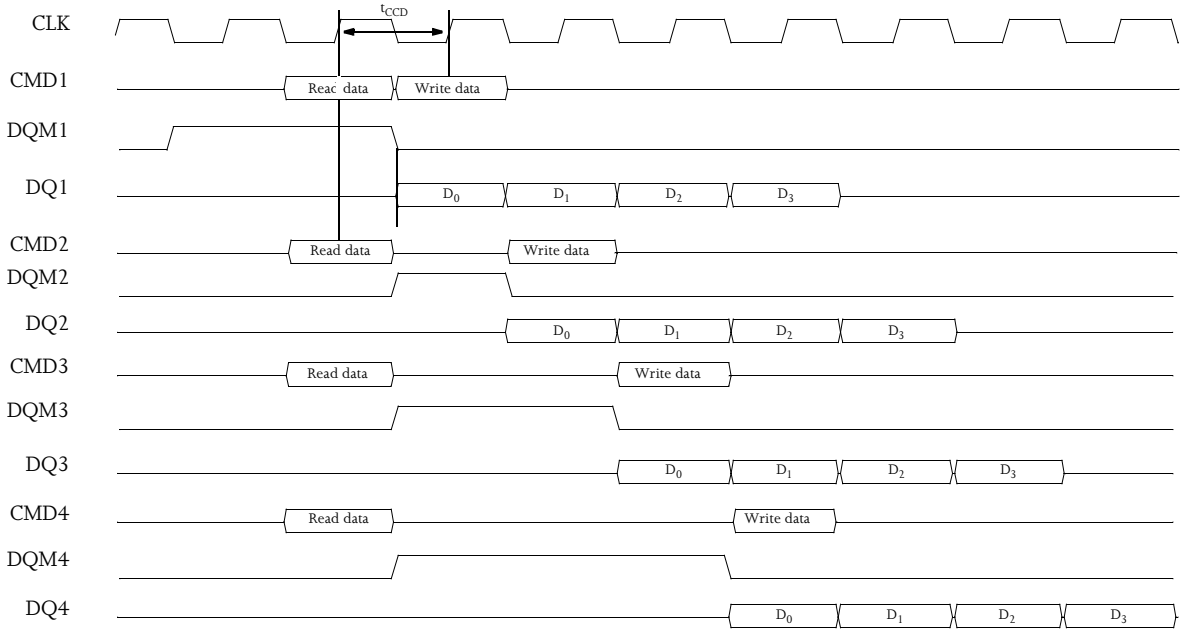
To prevent bus contention, maintain a gap between data in and data out.

read interrupted by write (CL = 2, BL = 4)



To prevent bus contention, maintain a gap between data in and data out.

read interrupted by write (CL = 3, BL = 4)



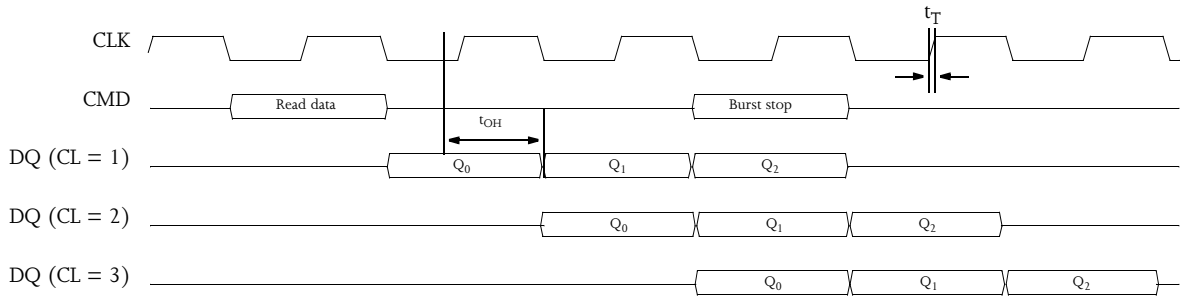
To prevent bus contention, maintain a gap between data in and data out.

Burst termination

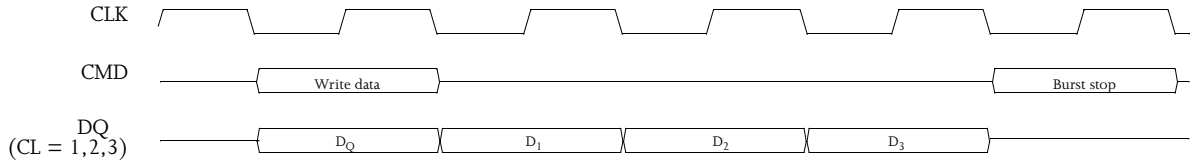
Burst operations may be terminated with a Read, Write, Burst Stop, or Precharge command. When Burst Stop is asserted during the read cycle, burst read data is terminated and the data bus goes to High Z after $\overline{CAS}$ latency. When Burst Stop is asserted during the write cycle, burst write data is terminated and the databus goes to High Z simultaneously.

Burst stop command waveform

read cycle



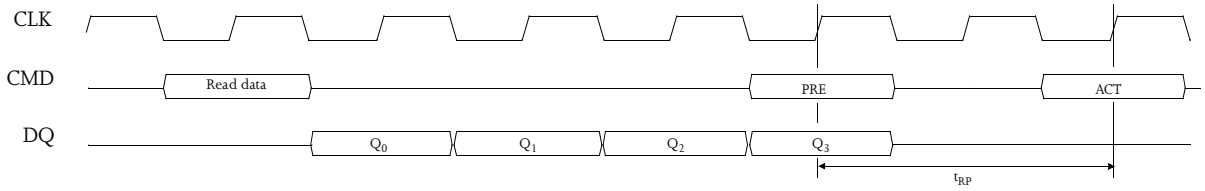
write cycle (BL = 8)



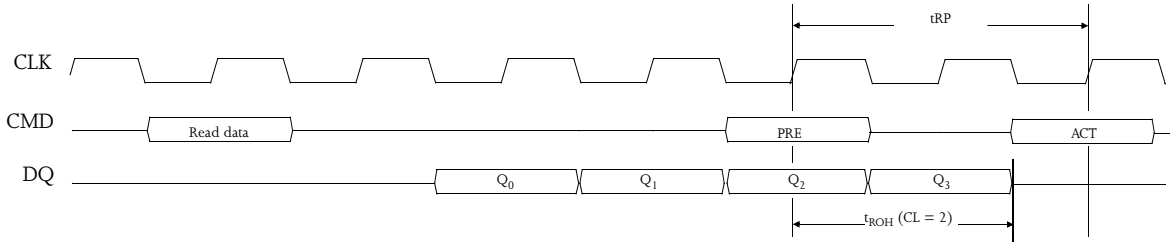
Precharge termination

A Precharge command terminates a burst read/write operation during the read cycle. The same bank can be activated after meeting t_{RP}. If an RD-burst is terminated, o/p will go to High Z after the number of cycles = $\overline{CAS}$ latency.

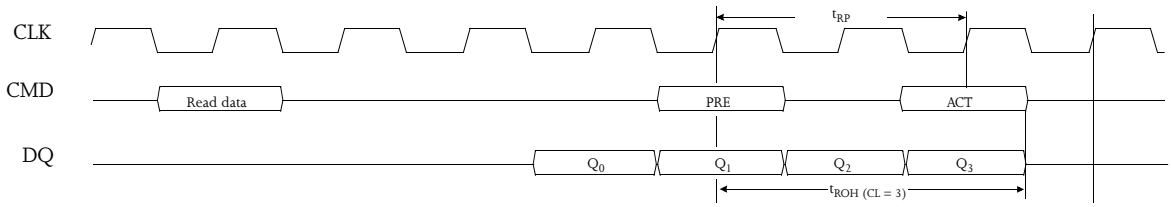
read cycle (CL = 1)



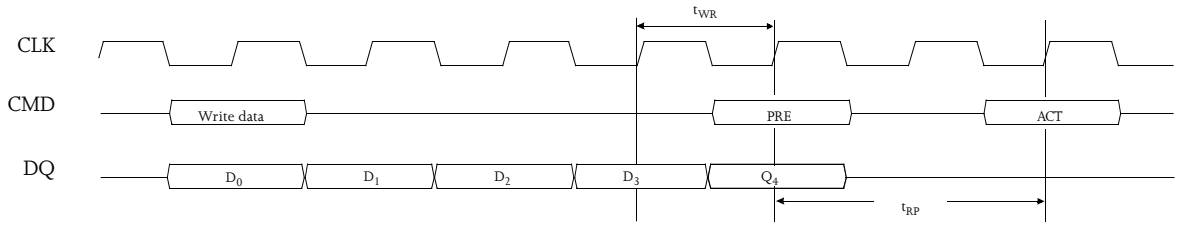
read cycle (CL = 2)



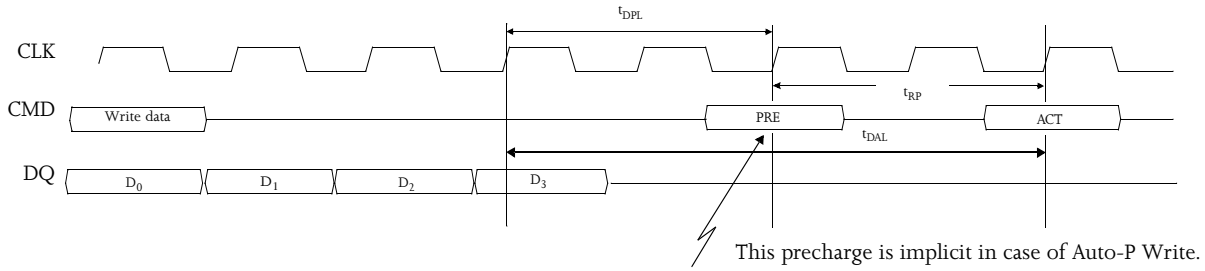
read cycle (CL = 3)



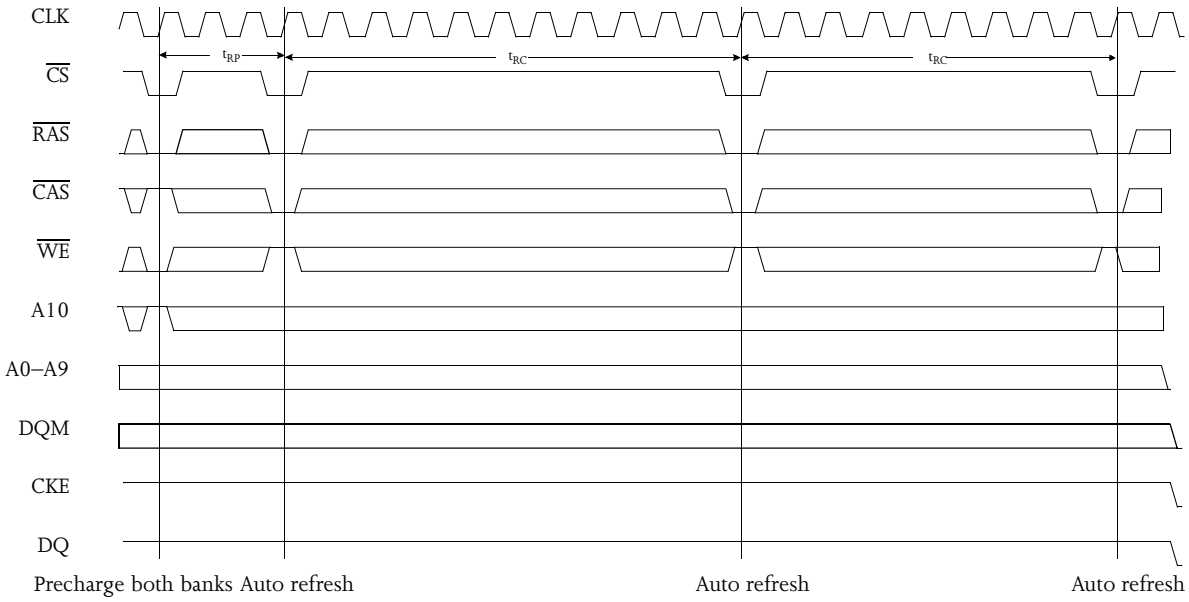
write cycle



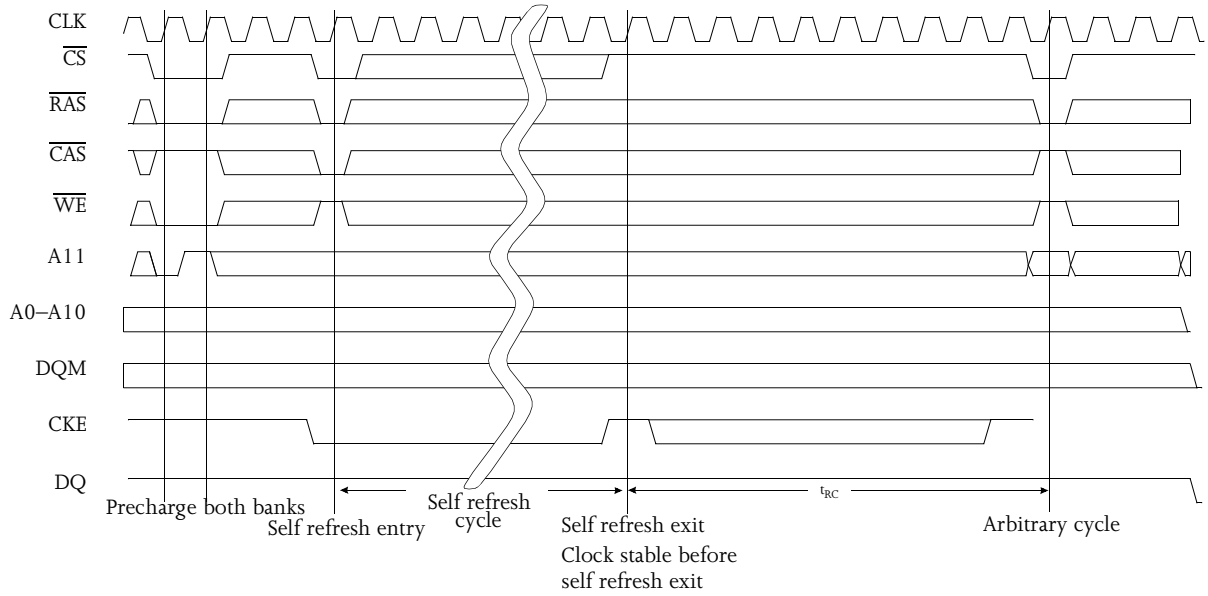
Write recovery (BL = 4)



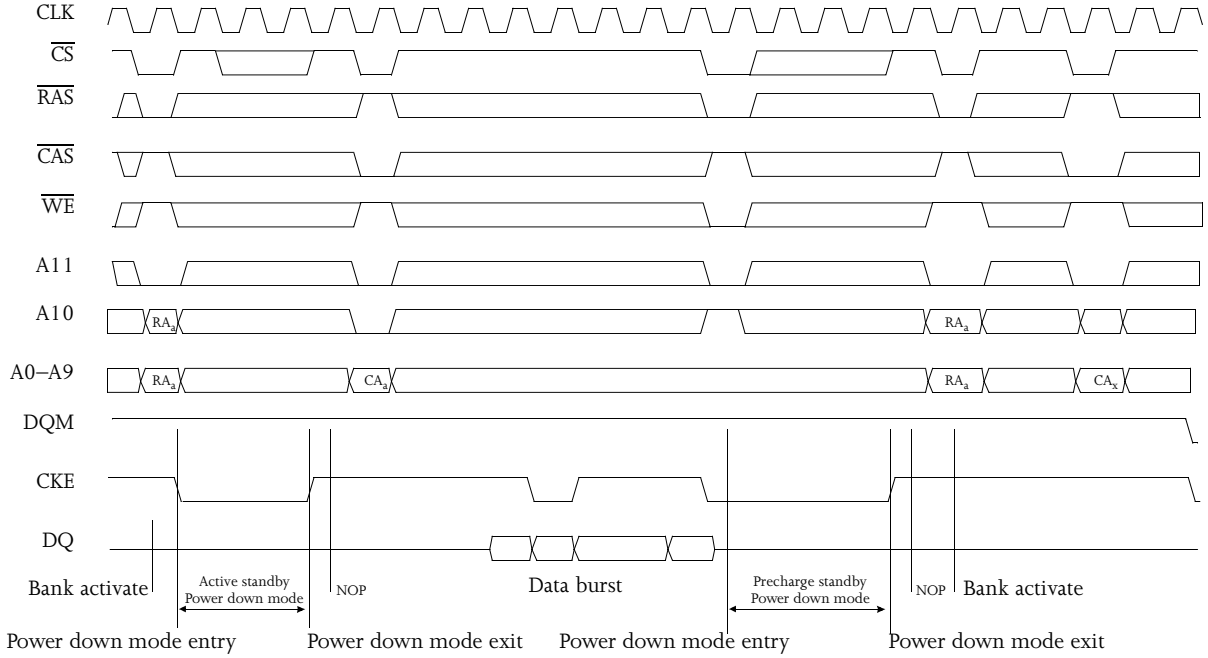
Auto refresh waveform



Self refresh waveform

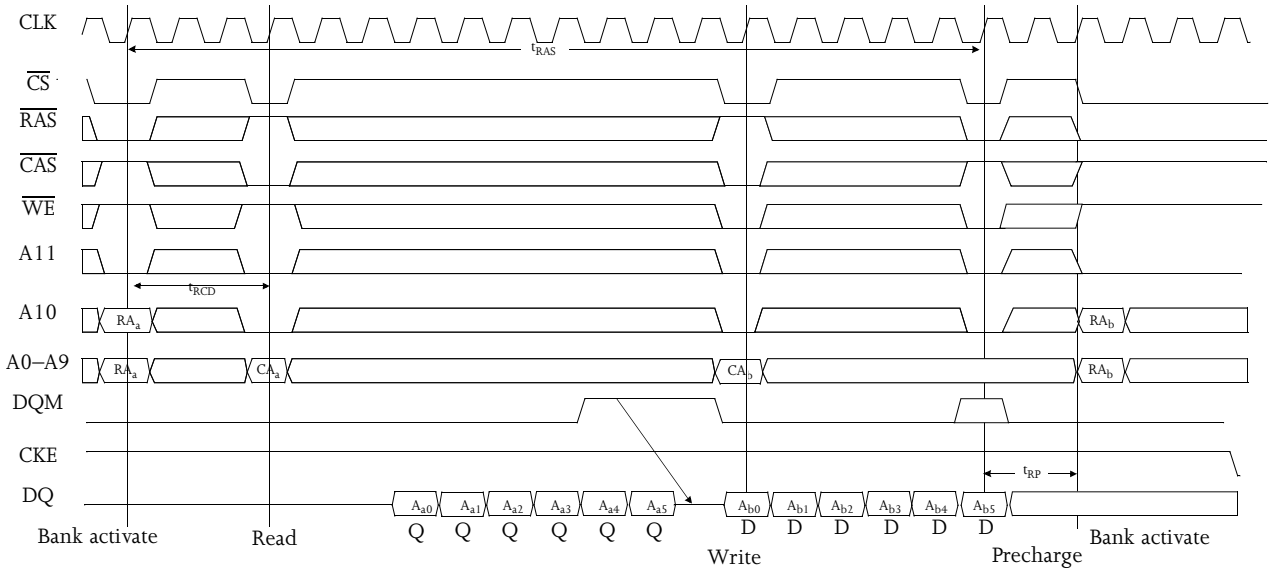


Power down mode waveform (CL = 3)

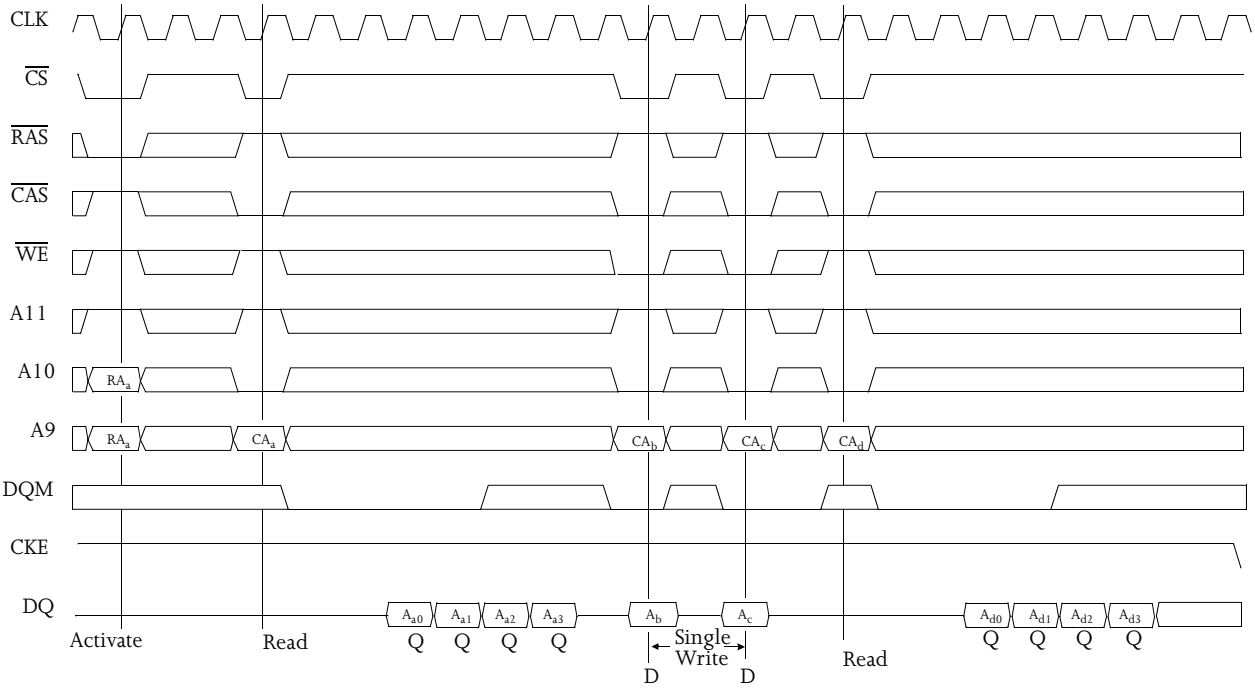


Enter power down mode by pulling CKE low.
All input/output buffers (except CKE buffer) are turned off in power down mode.
When CKE goes high, command input must be equal to no operation at next CLK rising edge.

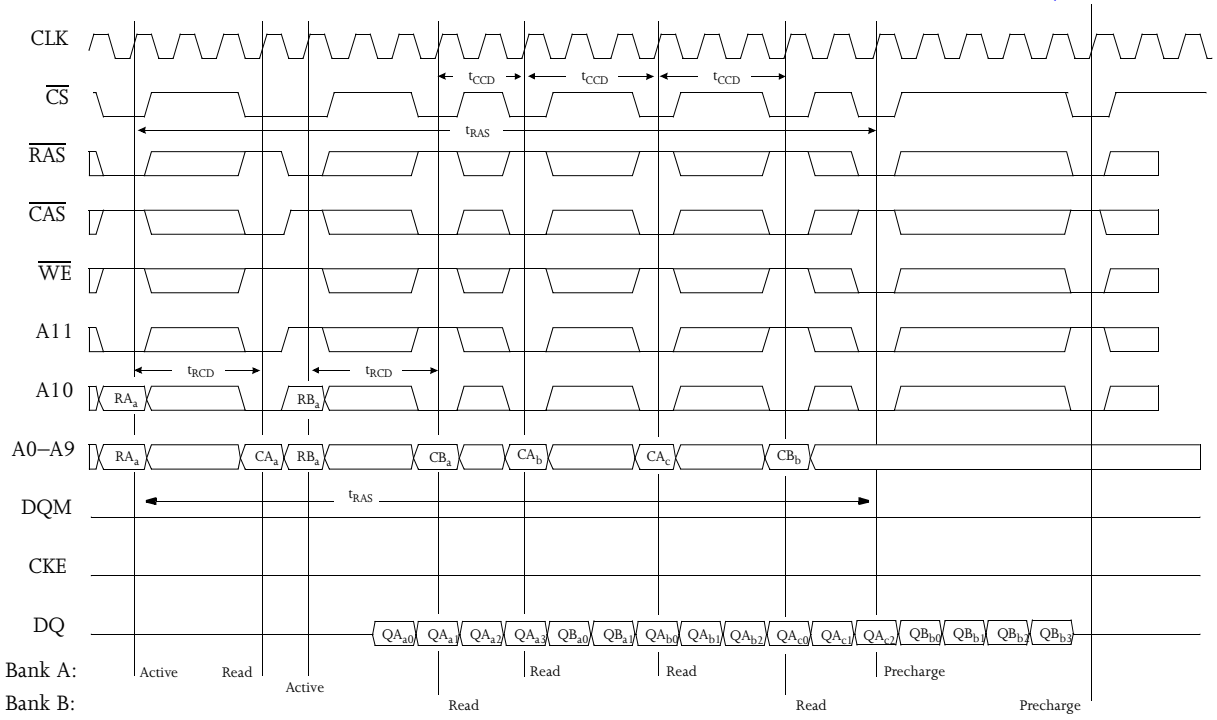
Read/write waveform (BL = 8, CL = 3)



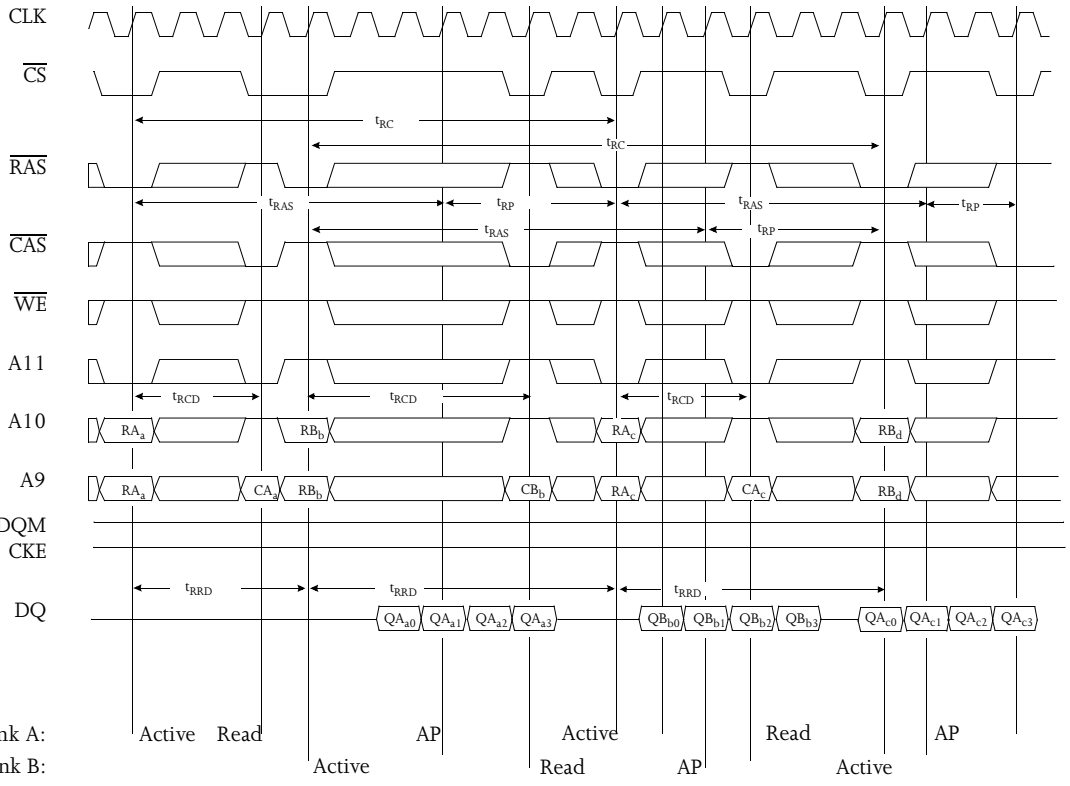
Burst read/single write waveform (BL = 4, CL = 3)



Interleaved bank read waveform (BL = 4, CL = 3)

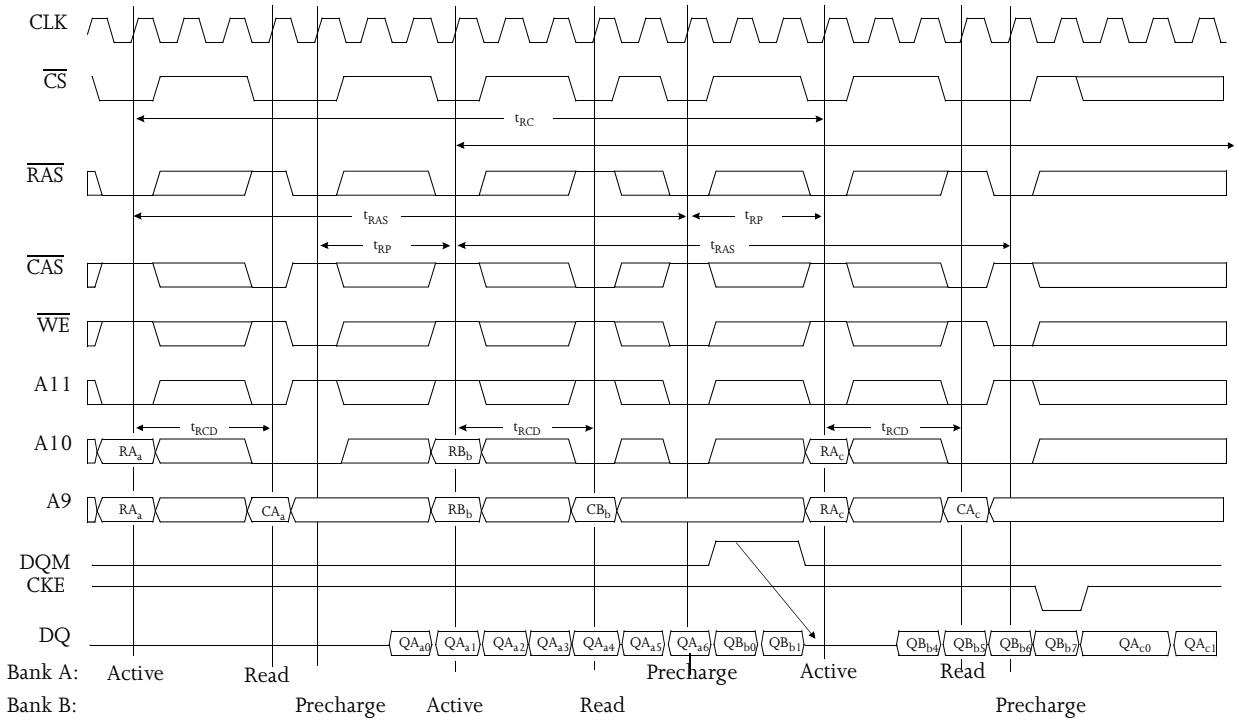


Interleaved bank read waveform (BL = 4, CL = 3, Autoprecharge)

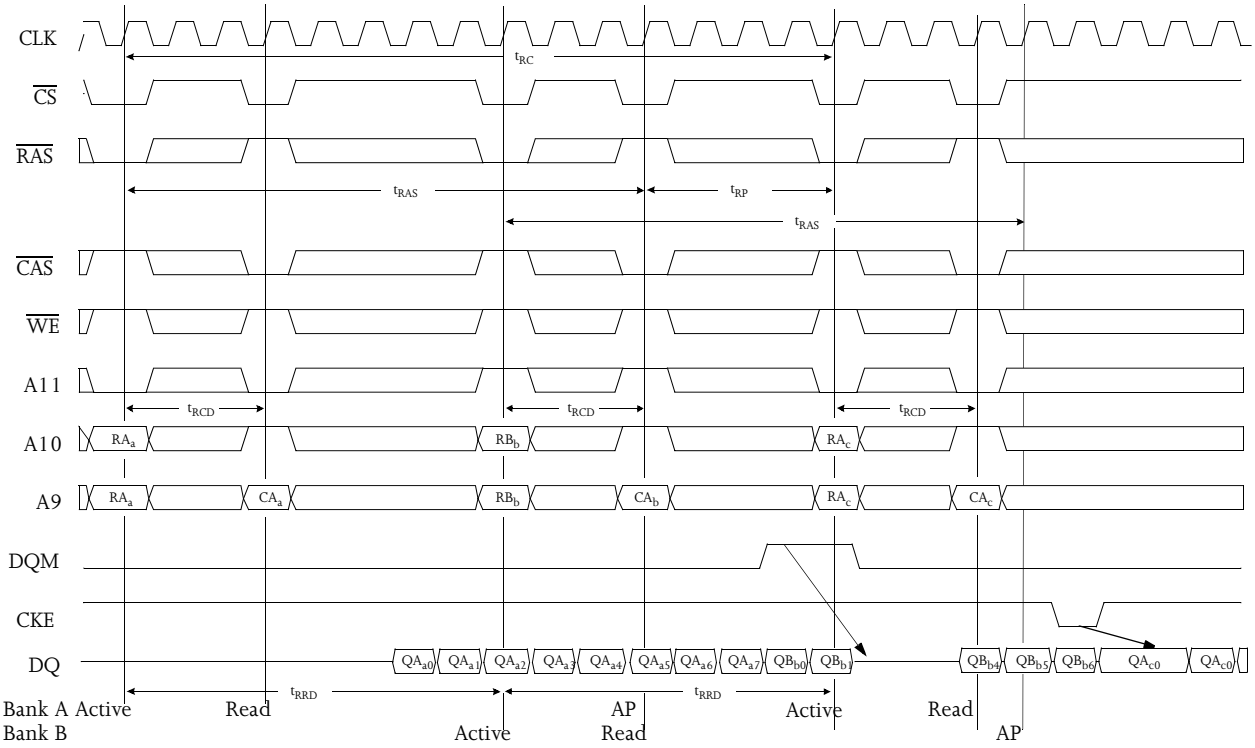


AP = internal precharge begins

Interleaved bank read waveform (BL = 8, CL = 3)

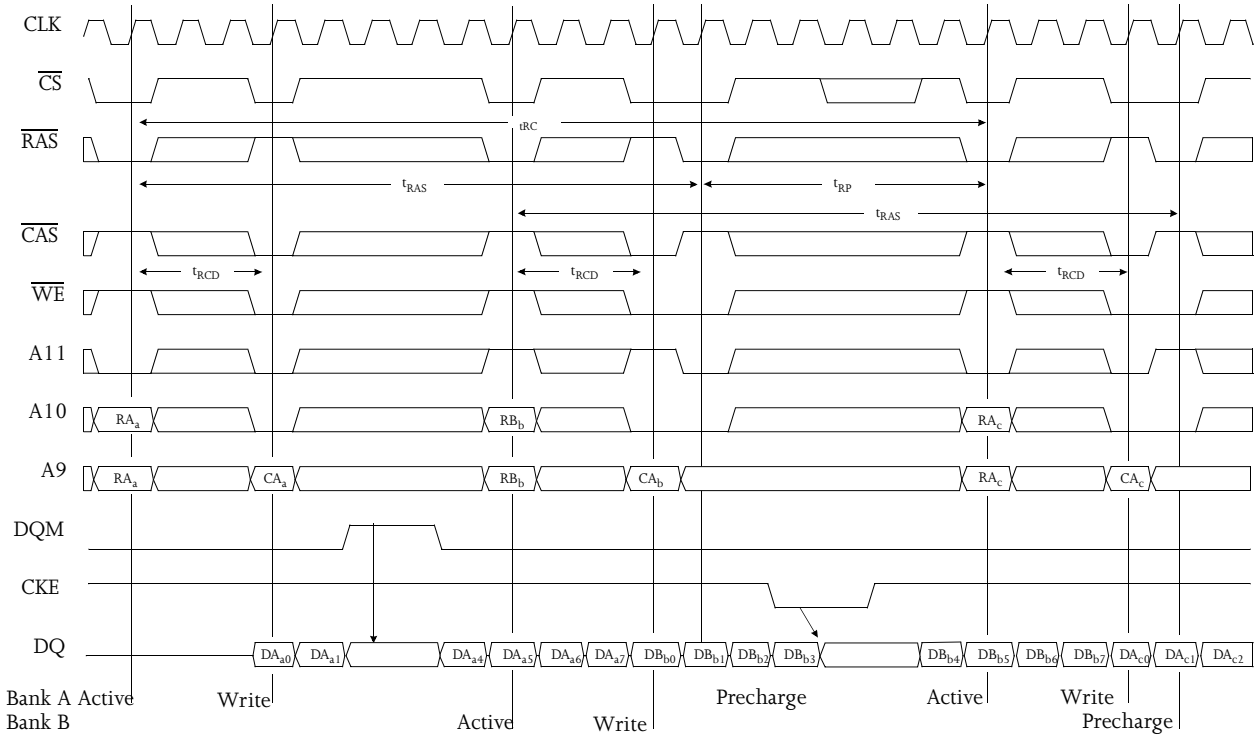


Interleaved bank read waveform (BL = 8, CL = 3, Autoprecharge)

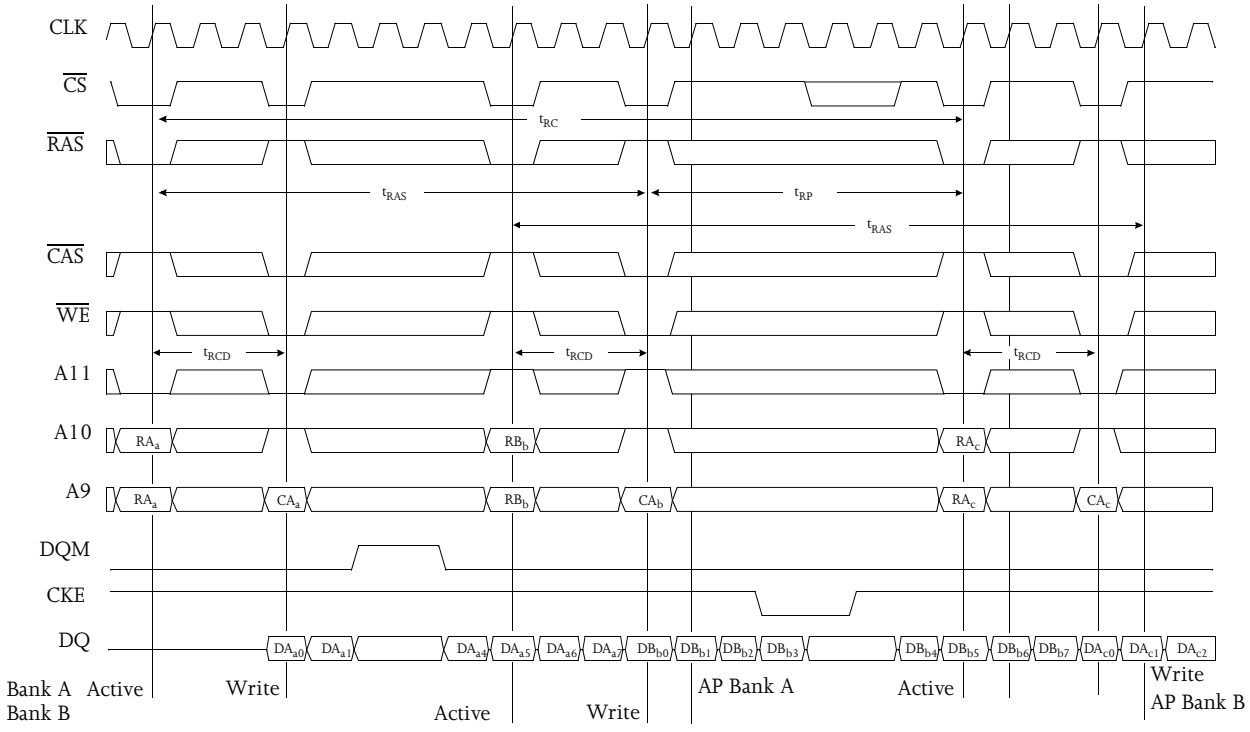


AP = internal precharge begins

Interleaved bank write waveform (BL = 8)

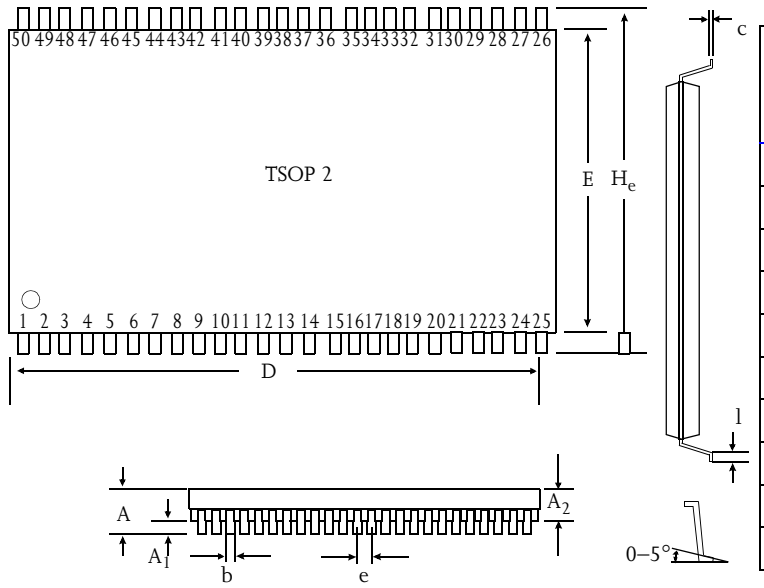


Interleaved bank write (BL = 8, Autoprecharge)



AP = internal precharge begins

Package dimensions



	44-pin TSOP 2		50-pin TSOP 2	
	Min (mm)	Max (mm)	Min (mm)	Max (mm)
A	–	1.2		1.2
A_1	0.05	–	0.05	
A_2	0.95	1.05	0.95	1.05
b	0.30	0.45	0.30	0.45
c	0.127 (typical)		0.12	0.21
D	18.28	18.54	20.85	21.05
E	10.03	10.29	10.03	10.29
H_e	11.56	11.96	11.56	11.96
e	0.80 (typical)		0.80 (typical)	
l	0.40	0.60	0.40	0.60

AC test conditions

- Output reference levels = 1.4V
- Input rise and fall times: 2 ns

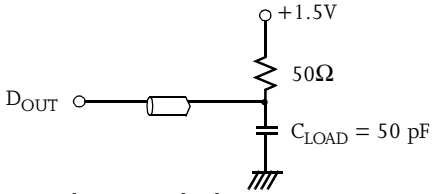


Figure A: Equivalent output load

Capacitance [15]

f = 1 MHz, T_a = 25° C, V_{CC} = 3.3V

Parameter	Symbol	Signals	Max	Unit
Input capacitance	C_{IN1}	A0 to A11	4	pF
	C_{IN2}	DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE,	4	pF
I/O capacitance	$C_{I/O}$	DQ0 to DQ7 (2M × 8) DQ0 to DQ15 (1M × 16)	5	pF

Ordering information

Package \1/ frequency	–7 ns	–8 ns	–10 ns
TSOP 2, 400 mil, 44-pin	AS4LC2M8S1-7TC	AS4LC2M8S1-8TC	AS4LC2M8S1-10TC
TSOP 2, 400 mil, 44-pin	AS4LC2M8S0-7TC	AS4LC2M8S0-8TC	AS4LC2M8S0-10TC
TSOP 2, 400 mil, 50-pin	AS4LC1M16S1-7TC	AS4LC1M16S1-8TC	AS4LC1M16S1-10TC
TSOP 2, 400 mil, 50-pin	AS4LC1M16S0-7TC	AS4LC1M16S0-8TC	AS4LC1M16S0-10TC

Part numbering system

AS4	LC	XXX	SX	–XX	T	C
DRAM prefix	3.3V CMOS	Device number for synchronous DRAM	S1 = 2K refresh S0 = 4K refresh	1/frequency	Package (device dependent): TSOP 2 400 mil, 44 pin TSOP 2 400 mil, 50 pin	Commercial temperature range: 0° C to 70° C

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