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AS3608

System PMU with HV Back Light Driver

1 General Description

The AS3608 is an ultra compact System PMU with integrated battery charger and HV back light driver.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3608. It features 3 DCDC converters as well as 5 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface.

The step-up converter for the backlight can operate up to 30V. Both constant voltage (OLED supply) as well as constant current (white LED backlight) operations with 2 current sinks are possible. An internal voltage protection is limiting the output voltage in the case of external component failures.

AS3608 also contains a Li-Ion battery charger with constant current and constant voltage. The maximum charging current is 1A. An integrated battery switch and an optional external switch are separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries. A programmable current limit can be used to control the maximum current used from a USB supply.

The single supply voltage may vary from 2.7V to 5.5V.

2 Key Features

Power Management

Voltage Generation

- 3 DCDC step down regulators
  - DVM (0.61V-3.3V, 1A@1.2V, 900mA@1.8V 800mA@2.5V)
  - 50µA quiescent current
  - Selectable switching frequency (2 or 1MHz)
  - 2A@1.2V with combined DCDC 2 & 3
- 1 LDO low noise 2.7V (2.3-3.5V), 100mA
- 3 or 4 LDOs low noise
  - 1.2-3.5V; 160/270mA
  - 30µA quiescent current (low power mode)
- Power supply supervision (LDO5)
- 4sec and 8sec emergency shut-down
- Hibernation function

HV Backlight Driver

- Step up for 30V backlight with internal transistor
- Voltage control mode and over-voltage protection
- 2 programmable current sink (max. 38mA)
- Max. 20mA@50V (with ext. transistor) or 500mA@5V
- Possible external PWM dimming input

Battery Charger

- Prog. trickle charging (25-265mA)
- Prog. constant current charging (94-1060mA)
- Prog. constant voltage charging (3.9V-4.25V)
- Charger time-out and temperature supervision
- Selectable current limitation for USB mode
- Integrated battery switch & ideal diode
- External battery switch control output

General

Battery and Temperature Supervisor

4 General Purpose IOs

- 10bit general purpose ADC input
- PWM dimming input or wake-up input
- Status output for: charger, low battery, power good and power-up key

OTP Programmable BOOT Sequence

- Programmable regulator default voltages
- Programmable start-up sequence
- Applicable for LDO 1-4 and DCDC 1-3

Control Interface

- I2C control lines, including watchdog
- Power-Up input
- Interrupt output
- Bidirectional reset, with selectable delay
- Low power standby mode, 180µA with LDO5 on

Power-On Reset Circuit

Packaging

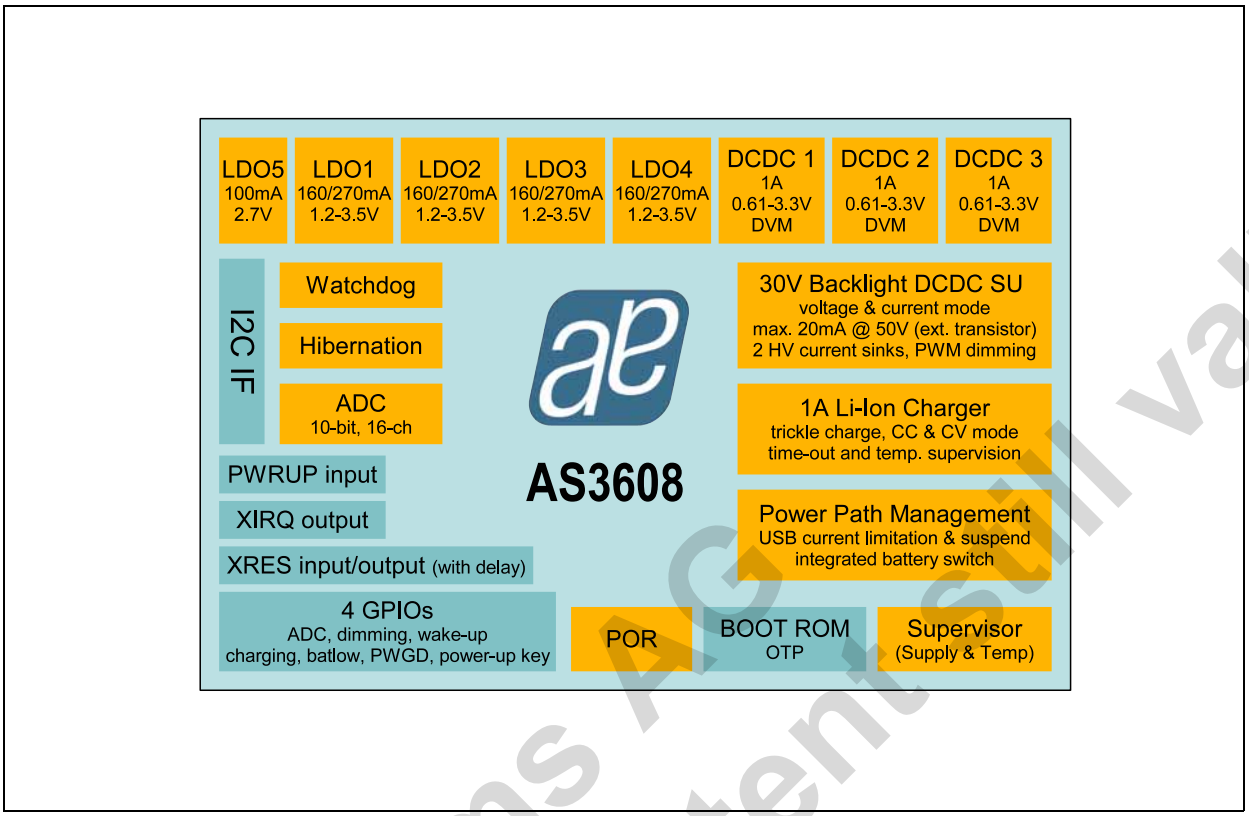
QFN36 6x6mm, 0.5mm pitch

3 Application

The devices are ideal for Portable Media Players and Portable Navigation Devices, e-Books, Tablet PCs, etc

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Figure 1. AS3608 Block Diagram



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Contents

1 General Description 1
2 Key Features 1
3 Application 1
4 Pin Assignments 5
4.1 Pin Descriptions 5
5 Absolute Maximum Ratings 7
6 Electrical Characteristics 8
7 Typical Operating Characteristics 10
8 Detailed Description - Power Management Functions 11
8.1 Low Drop Out Regulators 11
8.1.1 LDO5 11
8.1.2 LDO 1, LDO2, LDO3 & LDO4 12
8.1.3 Parameter 12
8.2 DCDC Step-Down Converter 14
8.2.1 Functional Description 15
8.2.2 Parameter 16
8.3 30V Step-Up DCDC Converter 18
8.3.1 Voltage Feedback and OV Protection 18
8.3.2 Voltage Feedback 18
8.3.3 DLS & Dimming 19
8.3.4 Current Sinks 19
8.3.5 Parameter 19
8.4 Charger 21
8.4.1 Soft Charge/Trickle Charge 22
8.4.2 End of Charge Detection 22
8.4.3 VSUPSW and Temperature Supervision 22
8.4.4 Battery Temperature Supervision 22
8.4.5 No Battery Detection 22
8.4.6 Charger Modes 23
8.4.7 Parameter 23
9 Detailed Description - SYSTEM Functions 25
9.1 SYSTEM 25
9.1.1 Power Up/Down Conditions 25
9.1.2 Start-up Sequence 25
9.2 Hibernation 26
9.3 Supervisor 26
9.3.1 VSUP Supervision 26
9.3.2 VDD27 Supervision 26
9.3.3 Junction Temperature Supervision 26
9.3.4 Power Rail Monitoring 26
9.4 Interrupt Generation 27
9.4.1 IRQ Source Interpretation 27
9.4.2 Interrupt Sources 27
9.5 10-Bit ADC 28
9.5.1 Input Sources 28

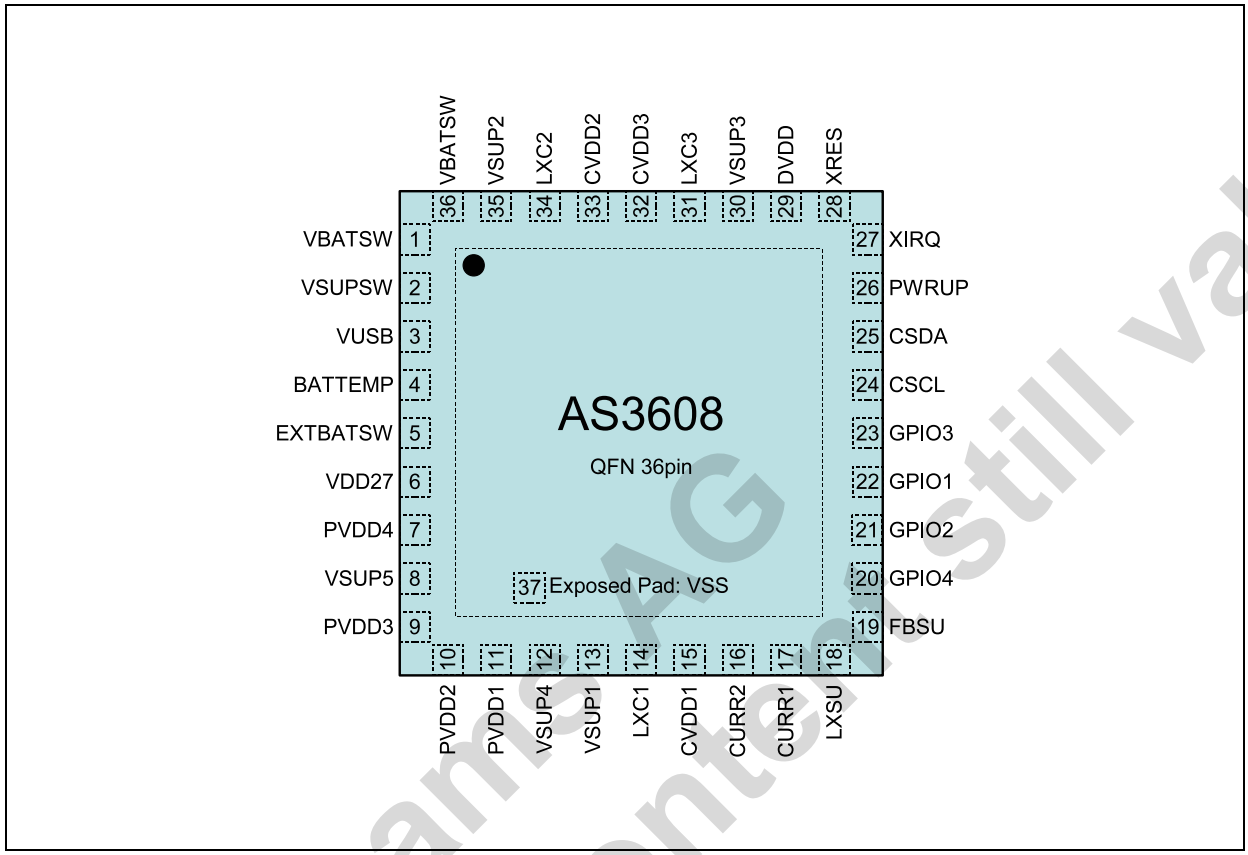
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9.5.2 Parameter 28
9.6 GPIO Pins 29
9.7 2-Wire-Serial Control Interface 30
9.7.1 Protocol 30
9.7.2 Parameter 33
10 Register Definition 34
11 Application Information 61
11.1 Pad Cells 61
11.2 Application Schematics 62
12 Package Drawings and Markings 63
13 Ordering Information 66

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4 Pin Assignments

Figure 2. Pin Assignments (TopView)



4.1 Pin Descriptions

Note: Pin description may change in preliminary data sheets.

Table 1. Pin Description for AS3608

Pin Name	Pin Number AS3608	Type	Description	if not used
VBATSW	1	SUP IO	Battery Switch Terminal to be connected to the Li-Ion battery	open
VSUPSW	2	SUP IO	Battery Switch Terminal to be connected to system supplies VSUPx	always needed
VUSB	3	SUP IN	Charger or USB Bus Power Input	open
BATTEMP	4	ANA IO	Li-Ion Charger Battery Temp. Sensor Input	open
EXTBATSW	5	ANA OUT	External Battery Switch Gate Driver Output	open
VDD27	6	SUP IO	LDO5 Output default 2.7V	always needed
PVDD4	7	ANA OUT	LDO4 Output	open
VSUP5	8	SUP IN	LDO3/4 & LDO5 Pos. Supply Terminal, connect to VSUPSW	always needed
PVDD3	9	ANA OUT	LDO3 Output	open
PVDD2	10	ANA OUT	LDO2 Output	open
PVDD1	11	ANA OUT	LDO1 Output	open
VSUP4	12	SUP IN	LDO1/2 Pos. Supply Terminal	always needed

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Table 1. Pin Description for AS3608

Pin Name	Pin Number AS3608	Type	Description	if not used
VSUP1	13	SUP IN	CVDD1 Step Down Pos. Supply Terminal	always needed
LXC1	14	DIG OUT	CVDD1 Step Down Switch Output to Coil	open
CVDD1	15	ANA IN	CVDD1 and Feedback Pin	open
CURR2	16	ANA IO	Load Current Sink2 Terminal	open
CURR1	17	ANA IO	Load Current Sink1 Terminal	open
LXSU	18	DIG OUT	DCDC Step-Up Switch Output to Coil	open
FBSU	19	ANA IN	DCDC Step-Up Feed-Back	open
GPIO4	20	ANA IO	General Purpose IO 4	open
GPIO2	21	ANA IO	General Purpose IO 2	open
GPIO1	22	ANA IO	General Purpose IO 1	open
GPIO3	23	ANA IO	General Purpose IO 3	open
CSCL	24	DIG IN	2-wire SERIF Clock Input	open
CSDA	25	DIG IO	2-wire SERIF Data I/O	open
PWRUP	26	DIG IN	Power Up Input	open
XIRQ	27	DIG OUT	Interrupt Request Output	open
XRES	28	DIG IO	Reset Output	open
DVDD	29	SUP IN	Digital Periphery Pos. Supply Terminal	always needed
VSUP3	30	SUP IN	CVDD3 Step Down Pos. Supply Terminal	VSUPx
LXC3	31	DIG OUT	CVDD3 Step Down Switch Output to Coil	open
CVDD3	32	ANA IN	CVDD3 and Feedback Pin	open
CVDD2	33	ANA IN	CVDD2 and Feedback Pin	open
LXC2	34	DIG OUT	CVDD2 Step Down Switch Output to Coil	open
VSUP2	35	SUP IN	CVDD2 Step Down Pos. Supply Terminal	always needed
VBATSW	36	SUP IO	Battery Switch Terminal to be connected to the Li-Ion battery	open
VSS	37	SUP IO	Exposed Pad: Neg. Supply Terminal for all blocks	always needed

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5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
5V pins	-0.5	7.0	V	Applicable for pins VBATSW, VSUPSW, VSUP1/2/3/4/5, PWRUP, GPIO1/2/3/4, VBUS
3V pins	-0.5	5.0	V	Applicable for pins DVDD
30V pins	-0.5	32	V	Applicable for pin LXSU, CURR1/2
5V pins with protection to VSUPx	-0.5	7.0 VSUPx+0.5	V	Applicable for pins EXTBATSW, FBSU
3V pins with protection to VDD27	-0.5	5.0 VDD27	V	Applicable for pins BATTEMP
3V pins with protection to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins XIRQ, XRES, CSCL, CSDA
3V pins with protection to VSUPx	-0.5	5.0 VSUPx+0.5	V	Applicable for pins PVDD1/2/3/4, VDD27, CVDD1/2/3, LXC1,/2/3
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
Continuous Power Dissipation (T_A = +85ºC)				
Continuous power dissipation		1	W	P_T[1] for QFN36 package (R_{TH} ~ 30K/W)
Electrostatic Discharge				
Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Junction Temperature		+110	ºC	
Storage Temperature Range	-55	+125	ºC	
Humidity non-condensing	5	85	%	
Temperature (soldering)				
Package Body Temperature		260	ºC	Norm IPC/JEDEC J-STD-020[2] The lead finish for Pb-free leaded packages is matte tin (100% Sn)
Moisture Sensitive Level	3			Represents a max. floor live time of 168h

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

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6 Electrical Characteristics

VSUPx=+2.7V...+5.5V, T_A =-40ºC...+85ºC. Typical values are at VSUPx=+3.6V, T_A=+25ºC, unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBATSW	Battery Supply Voltage	operation, VBUS > 2.7V	0	3.6	5.5	V
		operation from battery	2.7	3.6	5.5	V
VSUPx	Supply Voltage VSUPSW, VSUP1/2/3/4/5		2.7	3.6	5.5	V
VBUS	USB VBUS Voltage	operating, VSUP5 > 2.7V	0	5.0	5.5	V
		charging	4.5	5.0	5.5	V
DVDD	Digital Periphery Supply Voltage		1.8		3.6	V
VDD27	Analog Supply Voltage		2.6	2.7	3.5	V
V_{DELTA+}	Difference of Positive Supplies	VDD27-VSUPx			0	V
T_{AMB}	Operating Temperature Range		-40		+85	ºC
I_{SD}	Shut-down current	@ VBATSW = 4.2V		600		nA
I_q	Quiescent current	All regulators off reference & LDO5 on		180		µA
IO Pins						
VID_{3V}	3V digital input pins XRES, CSCL, CSDA		0		3.6V or DVDD +0.5	V
VIA_{3V}	3V input pin BATTEMP		0		3.6V or VDD27 +0.5	V
VI_{5V}	5V input pins GPIO1/2/3/4		0		5.5V	V
VI_{5V}	5V input pin FBSU		0		5.5V or VSUP5 +0.5	V
VI_{30V}	20V analiog input pins LXSU, CURR1/2		0		30	V
POR & Watchdog						
V_{POR_ON}	Power-on Reset Activation Level	Power-on Reset activation level when VDD27 decreases		2.15		V
V_{POR_OFF}	Power-on Reset Release Level	Power-on Reset release when VDD27 increases		2.0		V
V_{POR_HY}	Power-on Hysteresis			100		mV
PWRUP						
t_{ON_DELAY}	Delay Time of pin PWRUP	Minimum key press time	60			ms
V_{PWRUP_L}	Input Level LOW	Pin PWRUP, VSUP5>3V			0.5	V
V_{PWRUP_H}	Input Level HIGH	Pin PWRUP, VSUP5>3V	VSUP5/3			V
		Pin PWRUP, VSUP5<=3V	1			V
I_{PWRUP}	Internal Pull-down Current Source	Pin PWRUP; @2.7V	10	20	30	µA

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Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital Inputs/Outputs						
V_{DO_DL}	Digital Output Driver Capability (drive LOW)	Pins XRES, XIRQ, GPIOx @ 6mA, open drain mode			20% DVDD	V
I_{PU}	Internal Pull-up Current Source	Pins XIRQ, XRES @ 0V		13		µA
		Pins CSDA, CSCL @ 0V		100		µA
I_{PD}	Internal Pull-down Current Source	Pins GPIOx @ 2.7V	8	13	20	µA
V_{DI_L}	Digital Input Level LOW	Pin GPIOx		30% DVDD		V
V_{DI_H}	Digital Input Level HIGH	Pin GPIOx		70% DVDD		V

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7 Typical Operating Characteristics

VSUPx = +3.6V, T_A = +25ºC, unless otherwise specified.

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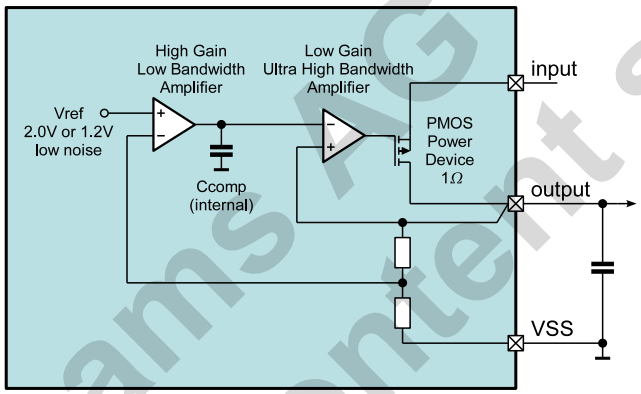
8 Detailed Description - Power Management Functions

8.1 Low Drop Out Regulators

These LDOs are designed to supply sensitive analog circuits, audio devices, AD and DA converters, micro-controller and other peripheral devices. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress high ripple on the battery at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 3. LDO Block Diagram



8.1.1 LDO5

This LDO generates the digital supply voltage used for the PMU itself.

- Input Voltage is VSUP5
- Output Voltage is VDD27 (typ. 2.7V), this LDO always starts at the beginning of the start-up sequence as it is needed for all further operation. The default voltage cannot be changed in the boot ROM.
- Driver strength: 100mA, can be programmed to 200mA

It is set to a default output voltage of 2.7V, 100mA$_{max}$. It supplies the analog and digital part of the PMU. Additional external loads are possible but must not exceed the supply ratings in total together with the operating internal blocks. Further, the external load must not induce noise to the VDD27.

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8.1.2 LDO 1, LDO2, LDO3 & LDO4

These LDOs can be used to generate the periphery voltage for the digital processor or other external components (e.g. ext. DAC, USB-PHY, SD-Cards, NAND-Flashes, FM-Tuner …). LDO4 is only available on AS3608.

- Input Voltage VSUP5 for LDO3 and LDO4, and VSUP4 for LDO2 and LDO1
- Output Voltage is PVDD1, PVDD2, PVDD3 & PVDD4 (1.2V to 3.5V)
- Default value at start-up is defined by the boot ROM, when the boot ROM is not programmed the LDOs will not start-up
- Driver strength: 160mA, can be programmed to 270mA

8.1.3 Parameter

VSUPx=3.6V, T_A= 25ºC, unless otherwise specified.

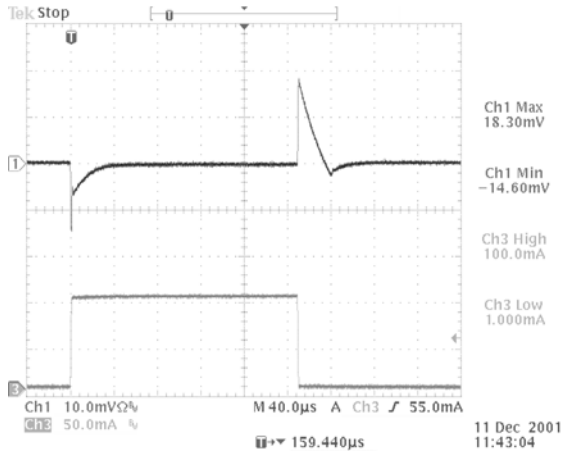
Table 4. LDO Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{ON}	On resistance				1	Ω
PSRR	Power supply rejection ratio	f=1kHz		70		dB
		f=100kHz		40		
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	without load		50		µA
		low power enabled, without load		32		µA
Noise	Output noise	10Hz < f < 100kHz		50		μV_{rms}
t_{start}	Startup time			200		µs
V_{out_tol}	Output voltage tolerance	minimum ±50mV	-2.5%		2.5%	mV
$V_{LineReg}$	Line regulation	Static		<1		mV
		Transient; Slope: t_r=10µs		<10		
$V_{LoadReg}$	Load regulation	Static		<1		mV
		Transient; Slope: t_r=10µs		<10		
I_{LIMIT}	Current limitation	default		200		mA
		has to be enabled via register		370		

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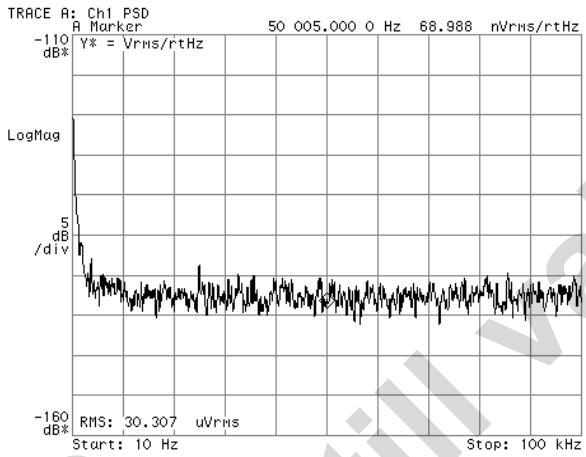
Figure 4. LDO Characteristics

Load Regulation



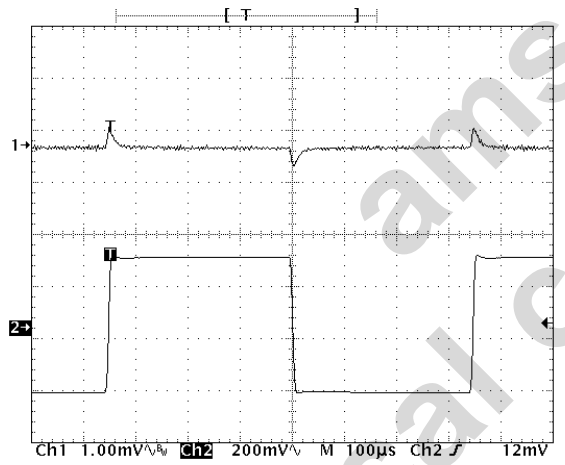
transient load: 1mA – 100mAslope: 1µs

Output Noise



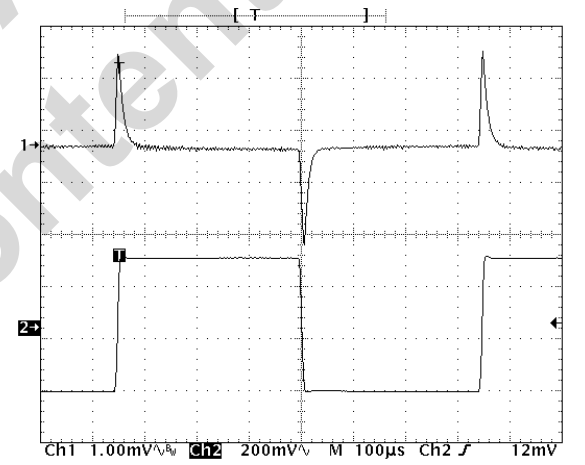
Output load: 150mA

Load Regulation



output load: 10mA
transient input voltage ripple: 500mV

Load Regulation



output load: 150mA
transient input voltage ripple: 500mV

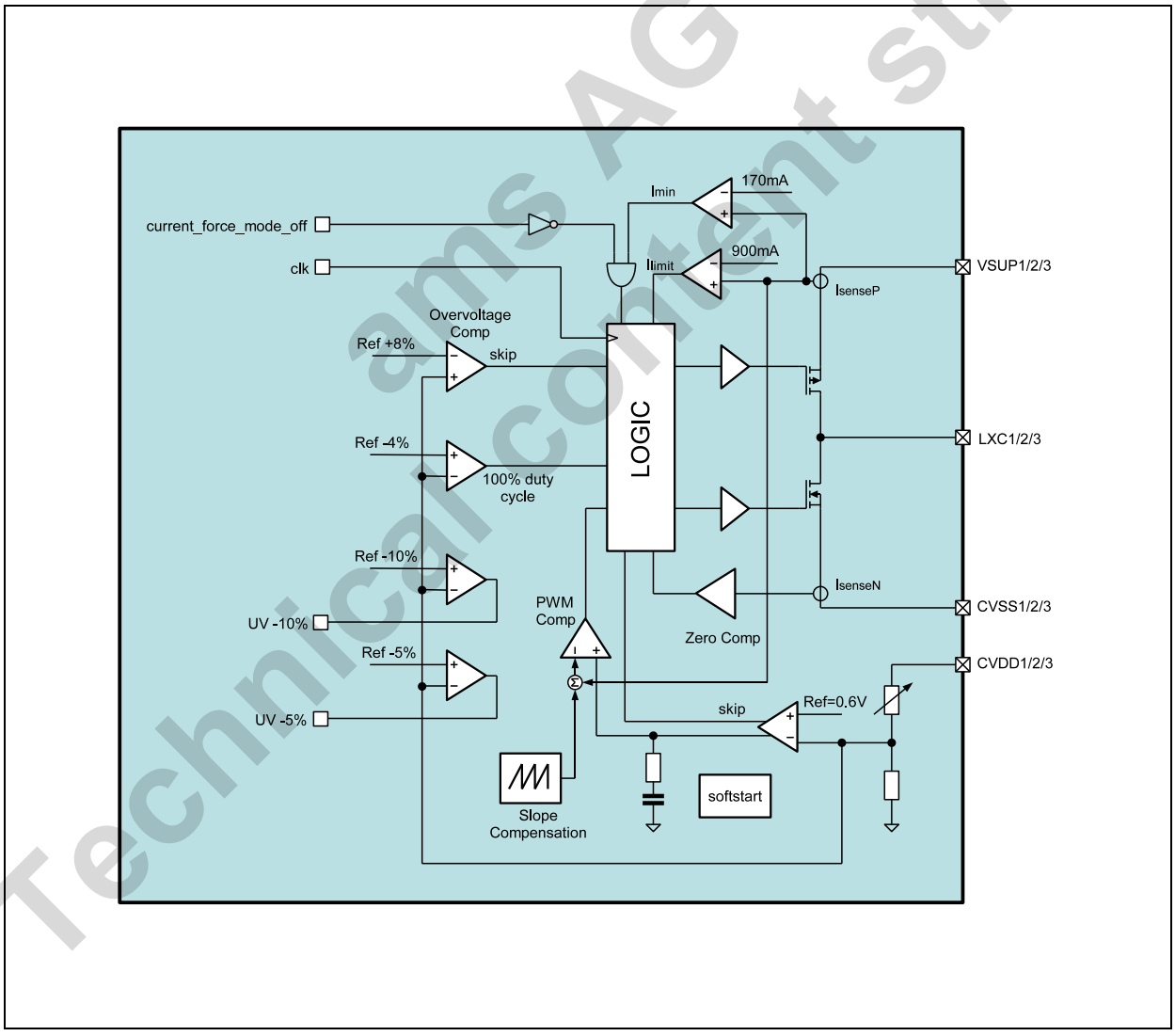
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8.2 DCDC Step-Down Converter

These converters are meant to convert the battery voltage down to voltages which fit to the core and peripheral supply voltage requirements for microprocessors.

- Input Voltage VSUP1/2/3 (usually connected to VSUPSW)
- Output Voltage CVDD1 & CVDD2 & CVDD3
- Output voltage levels can be programmed independently form 0.61V to 3.35V
- The default value at start-up is defined by the boot ROM
- DVM for all three outputs with selectable timings
- Driver strength 1A@1.2V, DCDC2 & 3 can be combined together to double the output current
- Under- and over-voltage detection
- High efficiency current force mode
- 1MHz or 2MHz switching frequency
- Fast regulation mode

Figure 5. DCDC Step-Down Block Diagram



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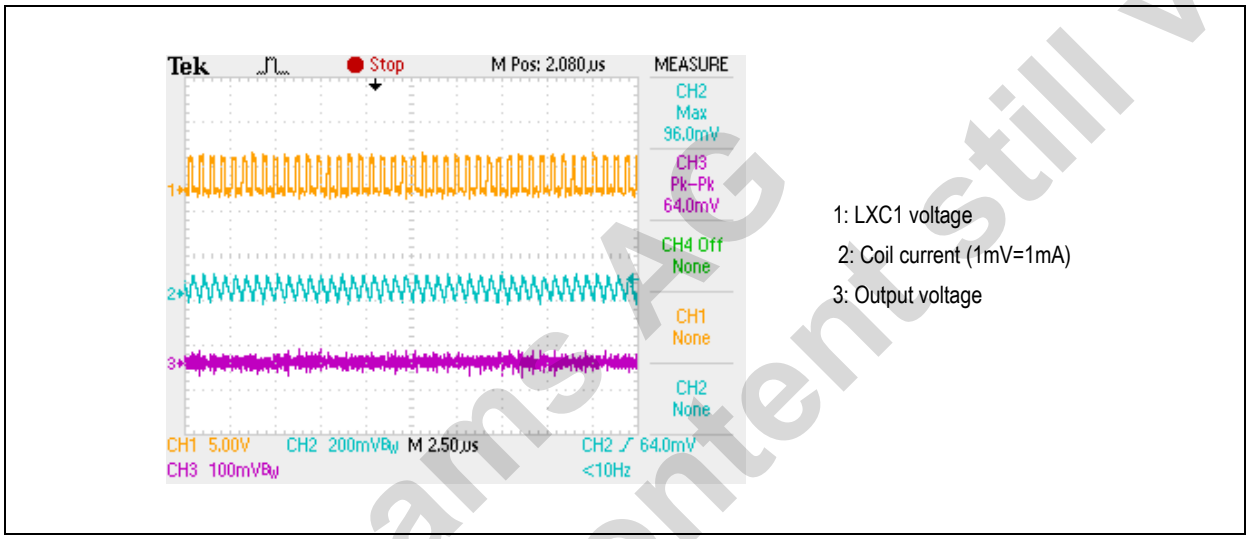
8.2.1 Functional Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 97% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 700mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

To achieve optimized performance in different applications, adjustable settings allow to compromise between high efficiency and low input, output ripple:

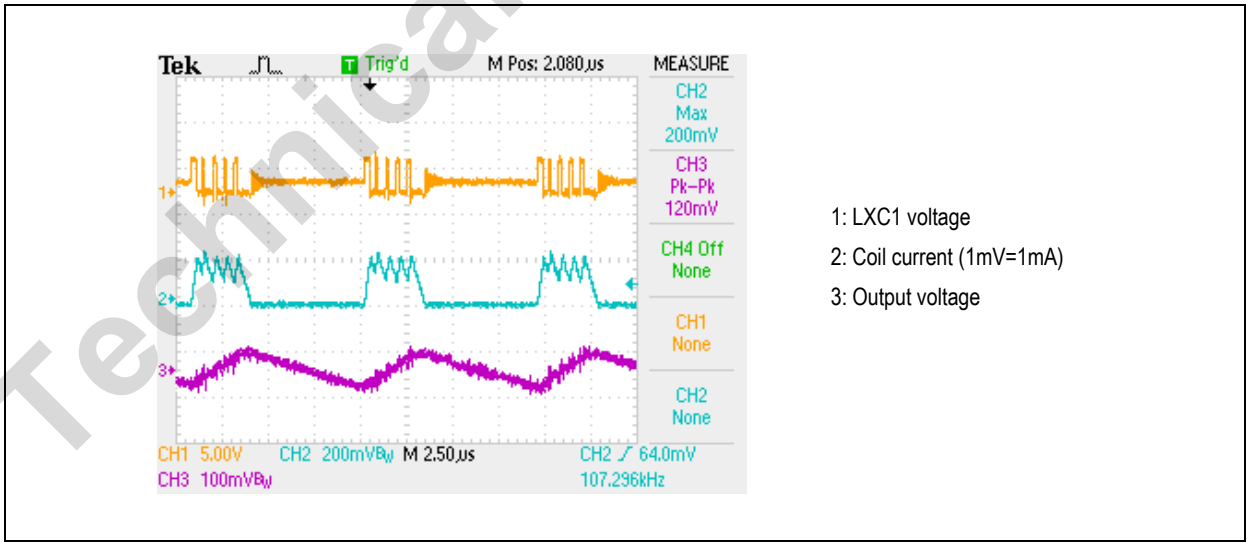
Low Ripple, Low Noise Operation (current force mode = OFF). In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. In the case of an inverted coil current the regulator will not operate in pulse skip mode.

Figure 6. DCDC Buck with Disabled Current Force / Pulse Skip Mode



High Efficiency Operation (current force mode = ON). In this mode, there is a minimum coil current necessary before switching off the PMOS. As result, fewer pulses at low output loads are necessary, and therefore the efficiency at low output load is increased. On the other hand the output voltage ripple increases, and the noisy pulse skip operation is on up to a higher output current.

Figure 7. DCDC Buck with Enabled Current Force / Pulse Skip Mode



It's also possible to switch between these two modes dynamically during operation.

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DVM (Dynamic Voltage Management). To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

Fast Regulation Mode. This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. FRM needs an 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator.

Low Frequency Operation. Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency.

100% PMOS ON Mode for Low Dropout Regulation. For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is than in LDO mode.

8.2.2 Parameter

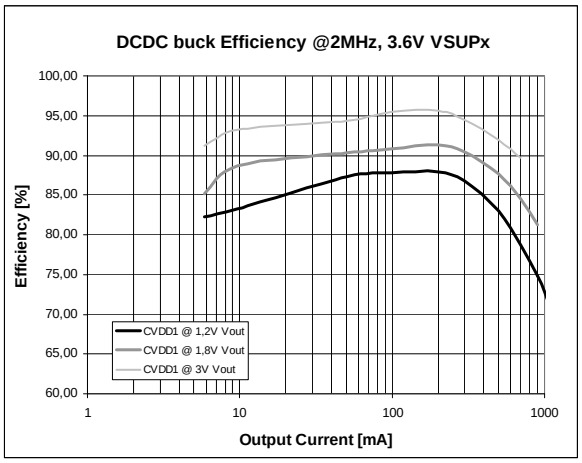
VSUP=3.6, T_A= 25ºC, unless otherwise specified.

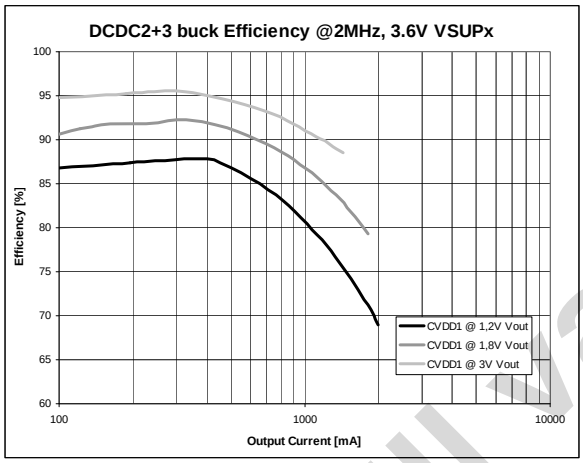
Table 5. DCDC Parameter

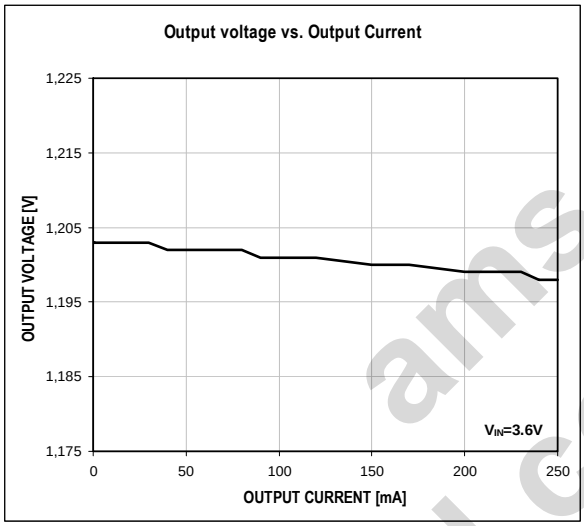
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage	VSUPx	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.6125		3.35	V
V_{OUT_tol}	Output voltage tolerance	minimum ±50mV	-3%		3%	mV
I_{load}	Maximum Load current				700	mA
		Vout=2.5V			800	mA
		Vout=1.8V			900	mA
		Vout=1.2V			1000	mA
I_{load}	Maximum Load current DCDC2+DCDC3				1400	mA
		Vout=2.5V			1600	mA
		Vout=1.8V			1800	mA
		Vout=1.2V			2000	mA
I_{LIMIT}	Current limit			1200		mA
R_{PSW}	P-Switch ON resistance	VSUPx=3.0V		0.5	0.7	Ω
R_{NSW}	N-Switch ON resistance	VSUPx=3.0V		0.5	0.7	Ω
f_{SW}	Switching frequency	depending on DCDC_Cntr settings		1/2		MHz
f_{SWsc}	Switching frequency	in shortcut case		0.6		MHz
C_{out}	Output capacitor	Ceramic, ±10% tolerance		10		µF
Lx	Inductor	±10% tolerance		2.2		µH
η_{eff}	Efficiency	Iout=150mA, Vout=3.0V		97		%
I_{VDD}	Current consumption	Operating current without load Shutdown current		65 0.1		µA
t_{MIN_ON}	Minimum on time			80		ns
t_{MIN_OFF}	Minimum off time			40		ns
$V_{LineReg}$	Line regulation	Static		2		mV
		Transient; Slope: t_r=10µs, 100mV step, 200mA load		10		
$V_{LoadReg}$	Load regulation	Static		5		mV
		Transient; Slope: t_r=10µs, 100mA step		50		

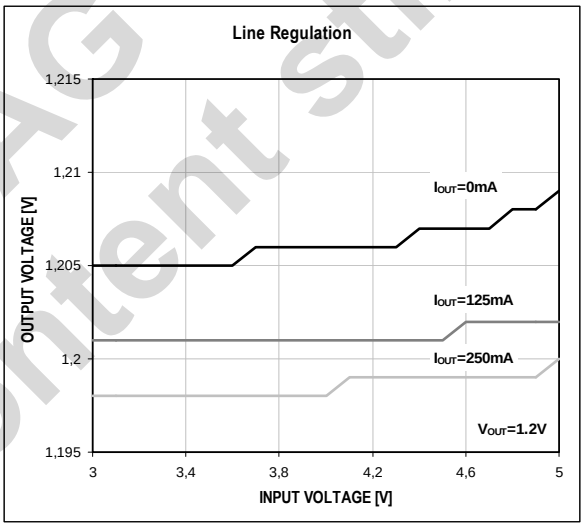
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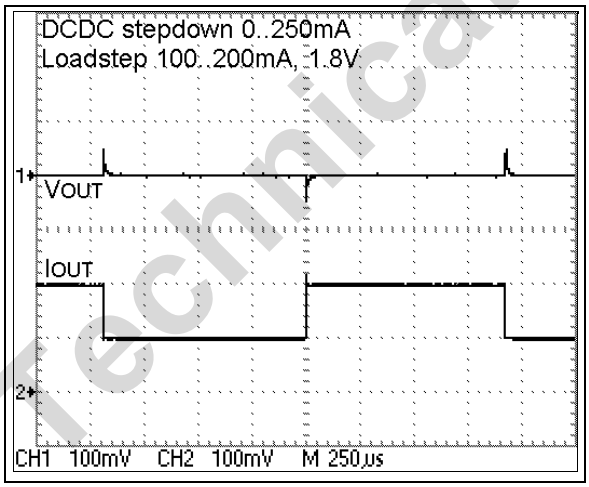
Figure 8. DCDC Step-down Performance Characteristics

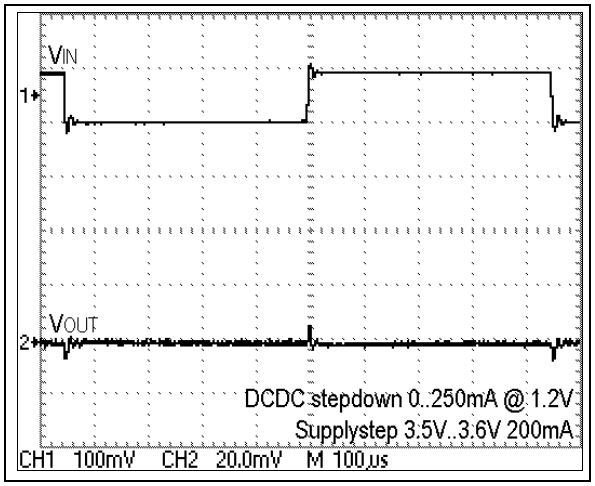












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8.3 30V Step-Up DCDC Converter

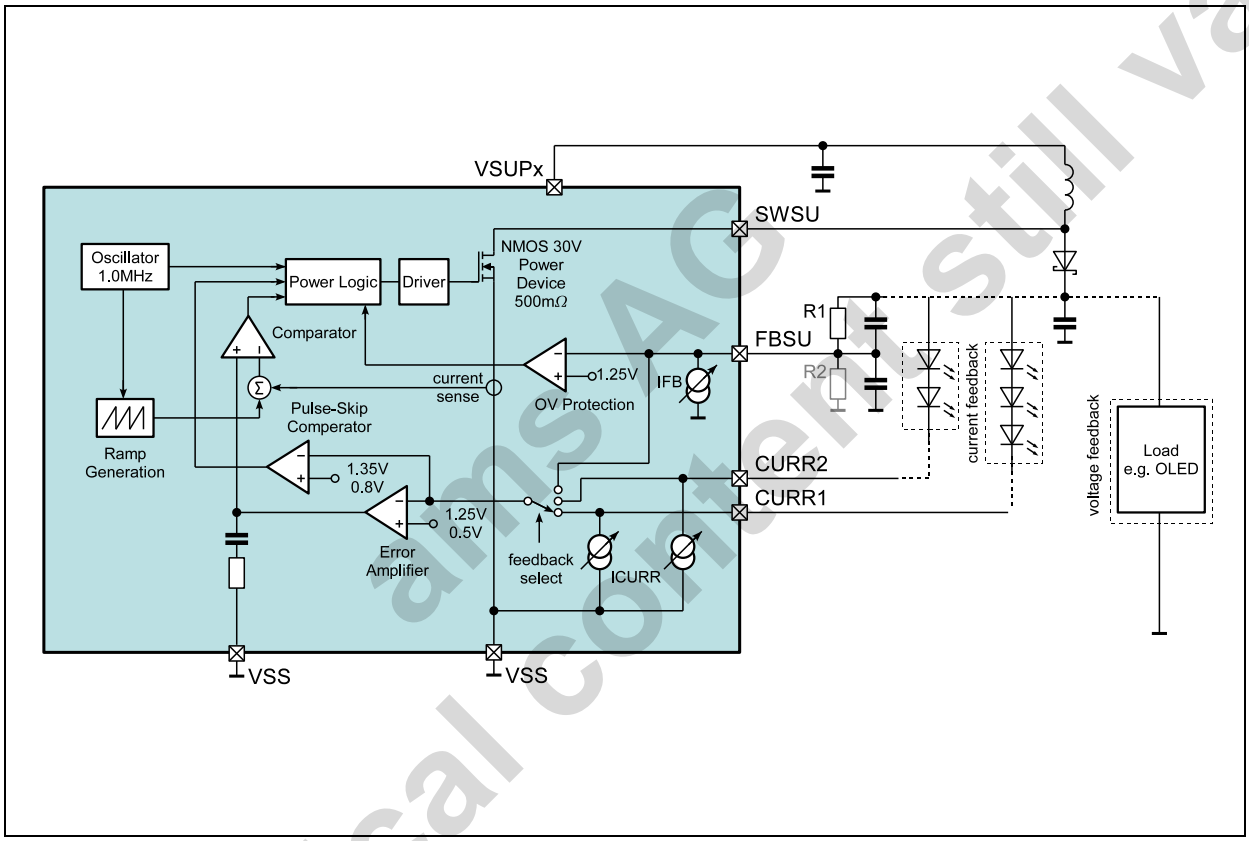
The integrated Step-Up DC/DC Converter is a high efficiency current-mode PWM regulator, providing an output voltage up to 30V. A constant switching-frequency results in a low noise on supply and output voltages.

It has two programmable high voltage current sinks (0 to 38.25mA) for driving e.g. white LEDs as back-light. It can drive also unbalanced strings due to the internal automatic feedback selection.

A voltage feedback mode allows generating constant supply voltages for e.g. OLEDs. The output voltage is set by an external resistor divider and an internal current sink.

An internal protection circuit will shut down the regulator if the voltage on FBSU exceeds the over voltage threshold. No more external protection has to be used to avoid an exceeding of the operation conditions in a no load situation.

Figure 9. DCDC15 Block Diagram



8.3.1 Voltage Feedback and OV Protection

8.3.2 Voltage Feedback

Setting bit **SU_CURR_FB** = 0 enables voltage feedback at pin FBSU.

The output voltage is regulated to a constant value, given by (Bit **SU_GAIN** should be set to 1 in this configuration)

$$U_{Step\ up_out} = (R1+R2)/R2 * 1.25 + I_{FB} * R1 \quad (EQ\ 1)$$

If R2 is not used, the output voltage is by (Bit **SU_GAIN** should be set to 0 in this configuration)

$$U_{Step\ up_out} = 1.25 + I_{FB} * R1 \quad (EQ\ 2)$$

Where:

$U_{Step\ up_out}$ = Step Up DC/DC Converter output voltage

$R1$ = Feedback resistor R1

$R2$ = Feedback resistor R2

I_{FB} = Tuning current at pin FBSU; 0 to 31µA

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Table 6. Voltage Feedback Example Values

IDCDC_FB	$U_{Step\ up_out}$	$U_{Step\ up_out}$
µA	R1 = 1MΩ, R2 not used	R1 = 500kΩ, R2 = 50kΩ
0	-	13.75
1	-	14.25
2	-	14.75
3	-	15.25
4	-	15.75
5	6.25	16.25
6	7.25	16.75
7	8.25	17.25
8	9.25	17.75
9	10.25	18.25
10	11.25	18.75
11	12.25	19.25
12	13.25	19.75
13	14.25	20.25
14	15.25	20.75
15	16.25	21.25
…	…	…
30	31.25	28.75
31	32.25	29.25

Note: The voltage on CURR1 and CURR2 must not exceed 30V.

8.3.3 Over Voltage Protection (OVP)

Setting bit **SU_CURR_FB** = 1 enables feedback via the current sink pins. The voltage on the current sink pin is regulated to **VCURR**. The selection of the current sink with the larger load is done automatically. The pin FBSU acts as an overvoltage protection in this mode. Please be sure to set the voltage to a higher level than needed to drive the longer LED string. The calculation of the resistor can be done the same as described in the chapter above.

8.3.4 DLS & Dimming

AS3608 feature external dimming inputs via CURR1, CURR2, GPIO1 or GPIO2 by directly connecting a PWM output of e.g. the display controller for DLS (dynamic luminance scaling). Manual dimming can be done at any time by setting the sink current via I2C commands.

8.3.5 Current Sinks

The current sinks work independent from each other and can also be used without the booster, or can act as a dimming input if they are not needed as a sink.

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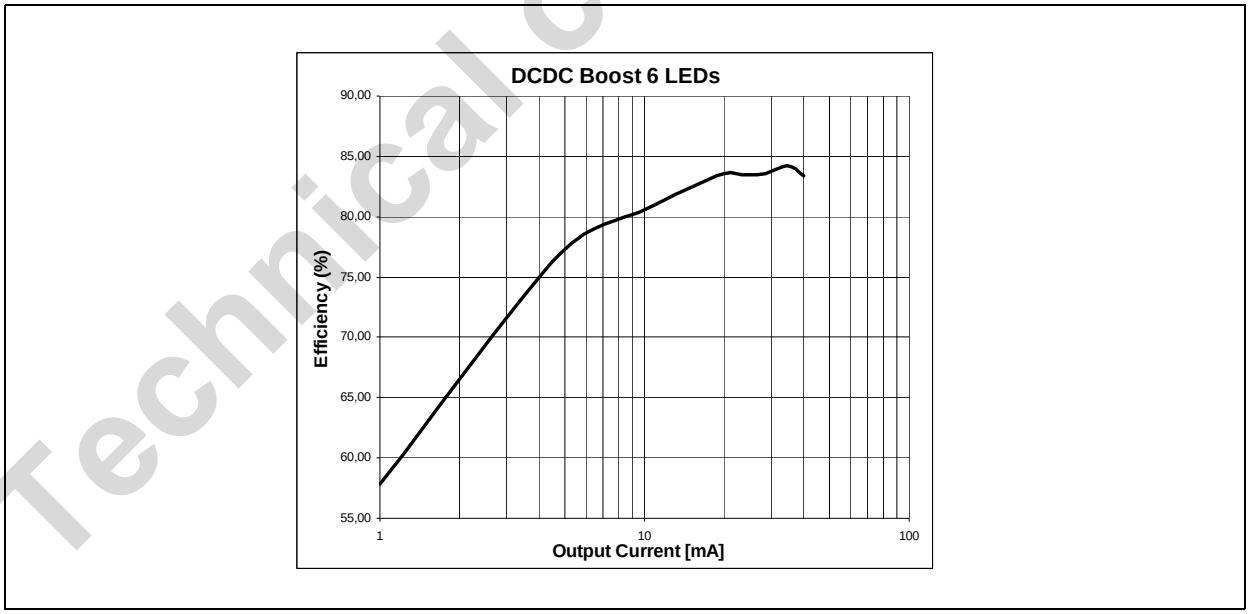
8.3.6 Parameter

VSUPx=3.6V, T_A= 25ºC, unless otherwise specified.

Table 7. DCDC Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SW}	High Voltage Pin	Pin FBSU	0		30	V
I_{VDD}	Quiescent Current	Pulse Skipping mode		140		µA
V_{FB}	Feedback Voltage, Transientt	Pin CURR1 or CURR2	0		30	V
		Pin FBSU	0		5	V
V_{FBSU}	Feedback Voltage, for voltage regulation	Pin FBSU	1.2	1.25	1.3	V
V_{CURR}	Feedback Voltage, for current sink regulation	Pin CURR1 or CURR2	0.4	0.5	0.6	V
I_{DCDC_FB}	Additional Tuning Current at Pin DCDC_FB and over voltage protection	Adjustable by software using Register DCDC control1 1µA step size (0-31µA) $V_{PROTECT}$ = 1.25V + IDCDC_FB * R_1	0		31	µA
	Accuracy of Feedback Current at full scale		-6		6	%
R_{SW}	Switch Resistance				1	Ω
I_{LOAD}	Load Current	@ 30V output voltage	0		50	mA
F_{SW}	Fixed Switching Frequency	SU_FREQU = 0		1		MHz
C_{OUT}	Output Capacitor	Ceramic, ±20%. Use nominal 4.7µF capacitors to obtain at least 0.7µF under all conditions (voltage dependence of capacitors)	0.7	4.7		µF
L	Inductor	Use inductors with small $C_{PARASITIC}$ (<100pF) for high efficiency	7	10	13	µH
t_{MIN_ON}	Minimum On-Time	Guaranteed per design		100	190	ns
MDC	Maximum Duty Cycle	Guaranteed per design	84	90		%

Figure 10. 30V Step-Up Performance Characteristics



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8.4 Charger

This block can be used to charge a 4V Li-Ion accumulator. It supports constant current and constant voltage charging modes with adjustable charging currents (94 to 1000mA) and maximum charging voltage (3.9 to 4.25V).

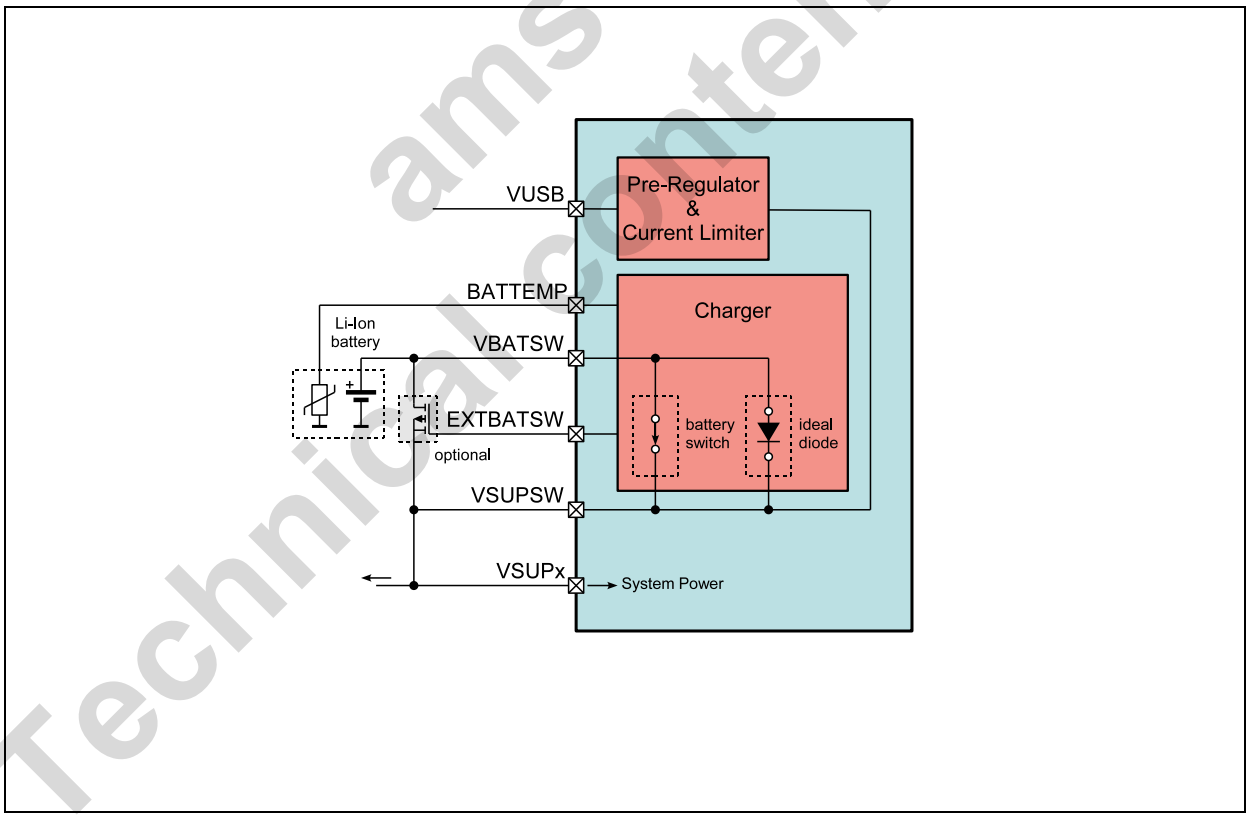
The charger consists basically of a pre-regulator, which limits the current from e.g. the USB input and provides a constant VSUP after reaching EOC (end of charge) and the battery switch, which is controlling the current into the battery.

- Input Voltage of the pre-regulator: VUSB
- Output of the pre-regulator and input for the battery switch and system supply: VSUPSW
- Output of the battery switch and battery terminal: VBATSW
- CVM (constant voltage), CCM (constant current) and trickle charging
- Adjustable EOC voltage and EOC current limit
- Selectable input -, trickle- and charging-current limit
- Auto-resume with selectable resume voltage level
- Charger time-out supervision with selectable time-out setting
- Battery temperature supervision supporting two levels (45 or 50°C) and 100k or 10k NTC types
- No battery detection
- Status register and interrupt generation

Per default the USB current limit is set to 470mA and the charger is switched off.

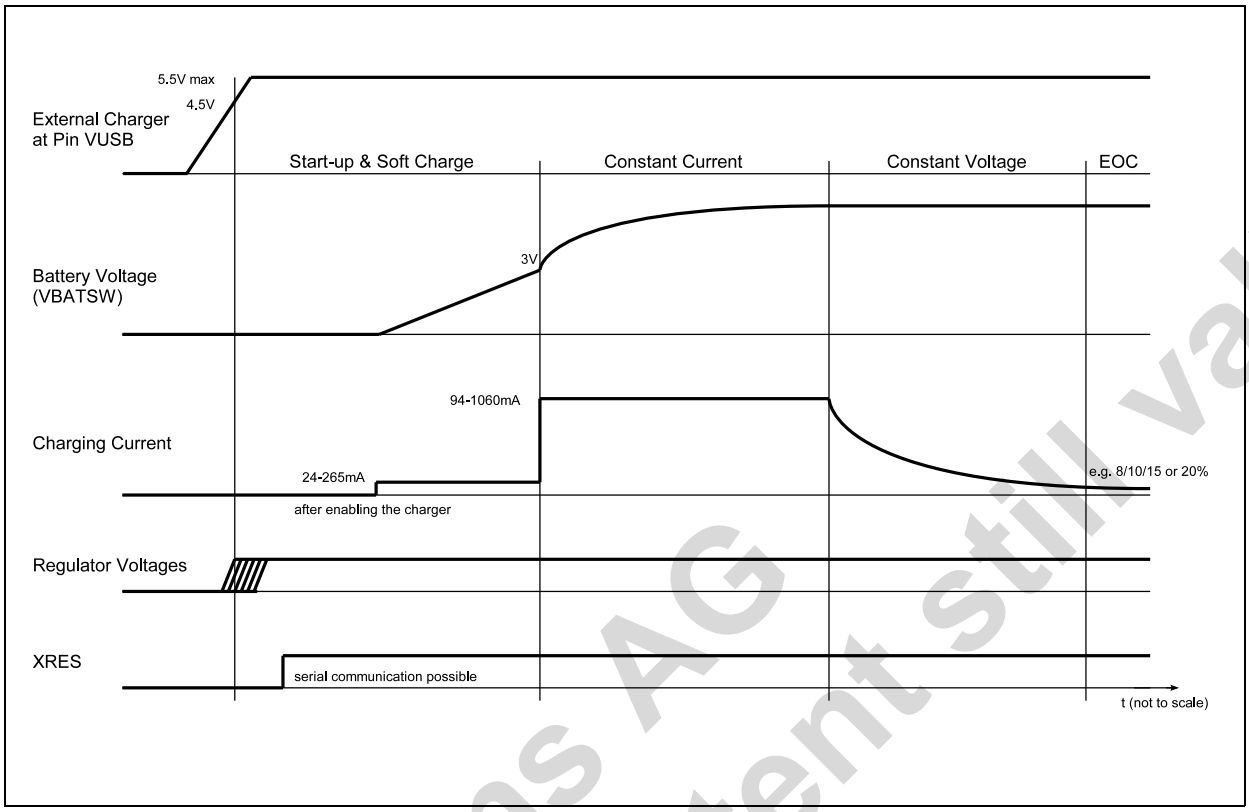
The current battery and charger input voltage can be measured with the general purpose ADC.

Figure 11. Charger Block Diagram



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Figure 12. Charger States



8.4.1 Soft Charge/Trickle Charge

If the battery and therefore VBATSW is below 3V the charger is working in a fixed soft charge mode with a smaller trickle charging current of 24-265mA. After reaching the 3V level the charger switches to the constant current mode with the programmed charging current.

8.4.2 End of Charge Detection

For the EOC level 4 presets can be selected. This makes it possible to monitor the charging progress also during constant voltage mode. If the EOC level is reached an interrupt can be generated, but it is also possible to poll the charger status bits at any time.

8.4.3 VSUPSW and Temperature Supervision

The charger will automatically reduce the charging current if VSUPSW drops below the selected level. It will automatically stop charging when the chip temperature gets too to hot. The charger will return to normal operation as defined in the charger registers if VSUPSW and the chip temperature return to their normal operating range.

8.4.4 Battery Temperature Supervision

This charger block also features a supply for an external NTC resistor to measure the battery temperature while charging. If the temperature is too high (voltage on BATTEMP pin is below **VBATTEMP_ON**) the charger will stop operation. If needed an interrupt can be generated based on this event. When the battery temperature drops the charger the voltage on BATTEMP pin will rise above **VBATTEMP_OFF** and the charger will start charging again. This is forming a temperature hysteresis of about 3 to 5°C to avoid an oscillation of the charger.

The levels for switching off the charger (45ºC or 55ºC) as well as the type of NTC (10k or 100k) can be selected via register settings. The battery temperature supervision via the NTC can be switched off (**NTC_ON** = 0).

The supply for the NTC will be only on when a charger is detected and **NTC_ON** bit is set.

8.4.5 No Battery Detection

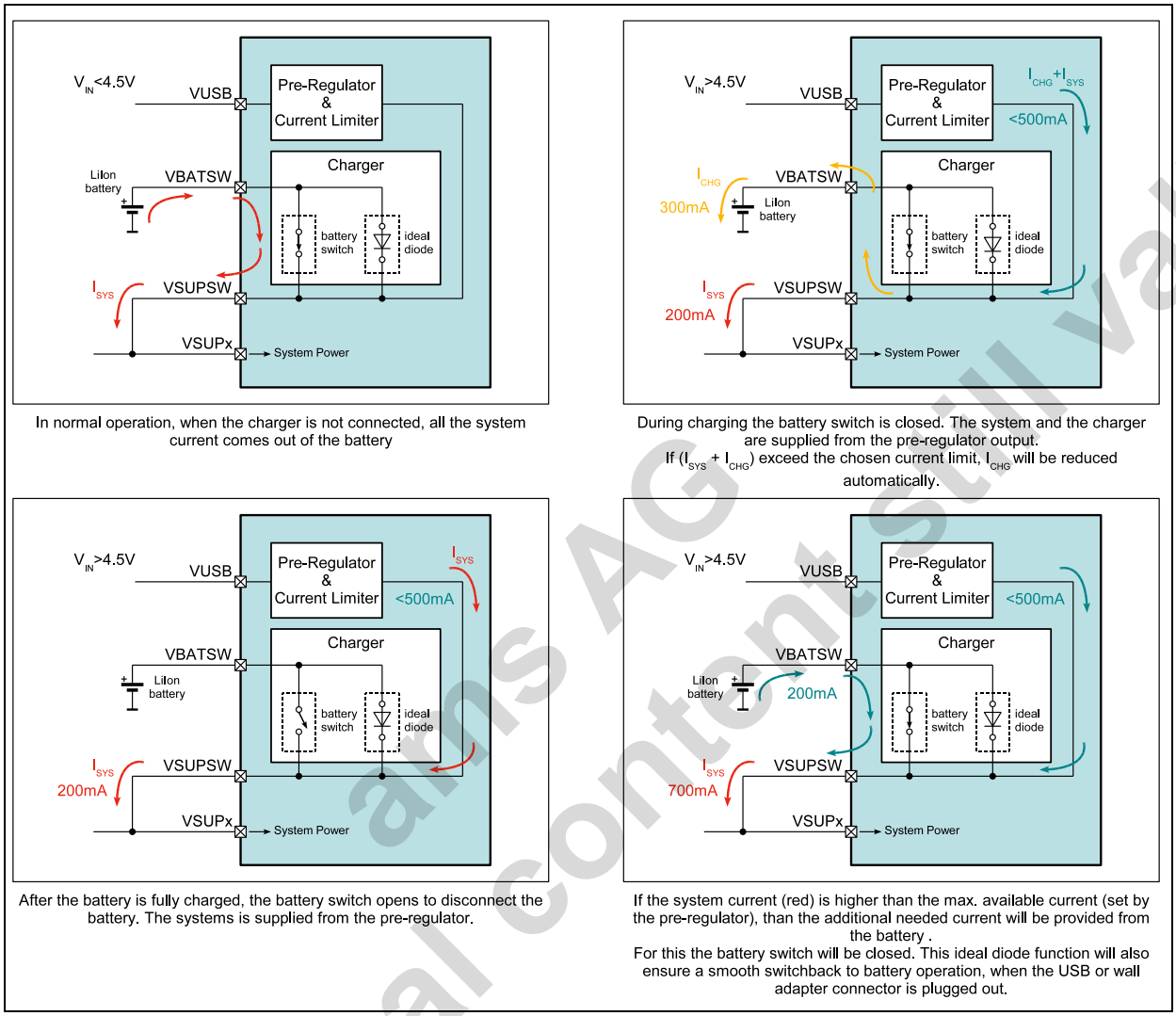
If the charger state machine reaches EOC 2 times within a very short period it assumes that there is no battery connected to the VBATSW terminal.

After this a sensing current of 1uA is applied to the BATTEMP pin to detect if a battery is reconnected.

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8.4.6 Charger Modes

Figure 13. Charger Modes



8.4.7 Parameter

VDD27=2.7, T_A= 25°C, unless otherwise specified.

Table 8. Charger Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CHG} (0-7)	Charging Current	@ 470mA	I_{NOM} -8%	I_{NOM}	I_{NOM} +8%	mA
V_{CHG} (0-7)	Charging Voltage	end of charge is true	V_{NOM} -50mV	V_{NOM}	V_{NOM} +33mV	V
V_{ON_ABS}	Charger On Voltage Detection	rising edge on VUSB start			0.8	V
		rising edge on VUSB end	3.5V			V
V_{ON_REL}		VUSB-VBATSW		170	240	mV
V_{OFF_REL}		VUSB-VBATSW		50		mV
$V_{BATTEMP_ON}$	Battery Temp. high level (45 or 55°C)	VSUP >3V NTC_{beta}=4200		610 or 400		mV

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Table 8. Charger Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BATTEMP_OFF}$	Battery Temp. low level (42 or 50°C)	VSUP >3V NTC_{beta}=4200		700 or 500		mV
$I_{BATTEMP}$	NTC Bias Current	100k 10k		16 160		µA
I_{CHG_OFF}	End Of Charge current level	VSUP >3V		8% 10% 15% 20% I_{NOM}		mA
I_{REV_OFF}	Reverse current shut down	VSUPSW = 5V, VUSB open		<1		µA
R_{ON_BATSW}	Battery Switch On-resistance			0.15		Ω

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9 Detailed Description - SYSTEM Functions

9.1 SYSTEM

The system block handles the power up, power down and regulator voltage settings of the PMU.

9.1.1 Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

Table 9. Power UP Conditions

#	Source	Description
1	PWRUP PwUp	ON_KEY High Level at PWRUP pin of >= 1/3 VBATSW
2	VBUS PwUp	USB Plug-In …. High level at VBUS pin of >= 4.5V and > 2.7V on VSUP5

The chip automatically shuts off if one of the following conditions arises:

Table 10. Power DOWN Conditions

#	Source	Description
1	SERIF MAJOR PwDn	**Power-Down** by SERIF writing 0h to register 20h
2	Emergency PwDn	**Power-Down** if PWRUP pin is HIGH for 8sec. This has to be enabled in register 21h, per default a reset cycle is initiated. It can also be changed to 4s.
3	SERIF Watch-Dog PwDn	write 3h to reg. 20h … enable SERIF watch-dog **Power-Down** if no SERIF read is seen for 500ms.
4	Junction-Temp PwDn	**Power-Down** if junction temperature rises up to 140degC. This threshold can be lowered with bits <4:0> in reg 21h. This supervisor can be disabled with bit 2 in reg. 20h.
5	VDD27 LOW PwDn	**Power-Down** if VDD27 LDO5 has 10% under-voltage for more than 680µs. This supervisor can get disabled with bit 6 in reg. 21h.
6	CVDD1 LOW PwDn	**Power-Down** if enabled with bit 7 in reg. 23h and CVDD1 DCDC has 10% under-voltage for more than 680µs.
7	CVDD2 LOW PwDn	**Power-Down** if enabled with bit 5 in reg. 23h and CVDD2 DCDC has 10% under-voltage for more than 680µs.
8	CVDD3 LOW PwDn	**Power-Down** if enabled with bit 3 in reg. 23h and CVDD3 DCDC has 10% under-voltage for more than 680µs.
9	VSUP LOW PwDn	**Power-Down** if VSUPx goes below the defined level in Reg22h (bits <3:1>) This supervisor has to be enabled with bit 4 in reg. 22h.

9.1.2 Start-up Sequence

The start-up sequence is defined in the boot ROM and will be fixed during the production test.

The sequence and voltage of the regulators can be freely chosen for the start-up sequence with the following limitations:

- VDD27 will always start-up, after a ~5ms delay the sequencer will start-up the other chosen regulators with either 0, 1 or 4ms delay each.
- A maximum of 6 regulators (no matter of DCDC or LDO) or 5 regulators and a changed GPIO configuration can be chosen for the start-up.
- On a 7th time-slot PVDD2 can be started-up, but has reduced setting on the output voltage

PWRGOOD will be activated ~3ms after the last regulator.

XRES will be released 10ms to 110ms (set in the boot ROM) after the last regulator started up.

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9.2 Hibernation

Hibernation allows shutting down a part or the complete system. Hibernation can be terminated by every possible interrupt of the PMU. The interrupt has to be enabled before going to hibernation.

Table 11. Hibernation

State	Description
Enter via GPIO	To enter hibernation mode the following settings have to be done: - Enable just these IRQ sources which should lead to leave hibernation mode. - Make sure that IRQ is inactive (IRQ flags get cleared by Reg 23h-26h readings). - Set the GPIO to input - Select the GPIO for hibernation control (**GPIO_DIMM_HBN_SEL <1:0>**) - Enable hibernation via GPIO (**GPIO_HBN_ON**) - Define which regulators should be kept powered and enter hibernation by writing to Reg 1Ch_0x04 + Reg 17h-4. This register MUST NOT be read back!!! - Drive the selected GPIO to LOW. Note that hibernation will shutdown regulators which are not in the keep list of the mentioned Reg 17h-4 writing and are part of the power-up sequence.
Enter via I2C	To enter hibernation mode the following settings have to be done: - Enable just these IRQ sources which should lead to leave hibernation mode. - Make sure that IRQ is inactive (IRQ flags get cleared by Reg 23h-26h readings). - Set a delay for entering hibernation if needed (**HBN_DELAY<1:0>**) - Define which regulators should be kept powered and enter hibernation by writing to Reg 1Ch_0x04 + Reg 17h-4. This register MUST NOT be read back!!! Note that hibernation will shutdown regulators which are not in the keep list of the mentioned Reg 17h-4 writing and are part of the power-up sequence.
Hibernation	VDD27 chip supply is kept ON All other regulators are switched OFF dependent on the KEEP-Bits XRES goes active (can be disabled in the boot ROM) and PWRGOOD goes inactive
Leave	The chip will come out of Hibernation with - IRQ activation or - GPIO control Start-Up sequence is provided defined by the boot ROM.

9.3 Supervisor

This supervisor function can be used for automatic detection of VSUP brown out or junction over-temperature condition.

9.3.1 VSUP Supervision

The VSUP supervision has a selectable level. If the shutdown is not enabled an interrupt can be generated.

9.3.2 VDD27 Supervision

If VDD27 reaches the “programmed level of VDD27” -10% for typ. 3ms, the PMU shuts down automatically. If the shutdown is not enabled an interrupt can be generated.

9.3.3 Junction Temperature Supervision

The temperature supervision level can also be set by 5 bits (120 to –15ºC). If the temperature reaches this level, an interrupt can be generated. The over-temperature shutdown level is always 20ºC higher. This shutdown can be disabled in Reg. 20h.

9.3.4 Power Rail Monitoring

The 3 DCDC regulators have an extra monitor which observes the output voltage of the regulators. This power rail monitors are independent from the 10bit ADC. To activate these please see related registers. For a shut down the voltage of the regulator has to be 10% or more below the programmed value for more than 3ms.

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9.4 Interrupt Generation

All interrupt sources can get enabled or disabled by corresponding bits in the 4 IRQ-bytes. By default no interrupt source is enabled.

The XIRQ pin can be configured to operate in push/pull (2 different driver strengths), open-drain mode or to be tri-state. The signal polarity can be defined as active-low or active-high. Default state is open-drain active-low.

9.4.1 IRQ Source Interpretation

There are 3 different modules to process interrupt sources:

LEVEL. The IRQ output is kept active as long as the interrupt source is present and this IRQ-Bit is enabled.

EDGE. The IRQ gets active with a high going edge of this source. The IRQ stays active until the corresponding IRQ-Register gets read.

STATUS CHANGE. The IRQ gets active when the source-state changes. The change bit and the status can be read to notice which interrupt was the source. The IRQ stays active until the corresponding interrupt register gets read.De-bouncer

There is a de-bounce function implemented, a de-bounce time of 3ms is selected per default in the IRQ_ENRD_3 register (26h).

9.4.2 Interrupt Sources

These IRQ events will activate the XIRQ pin:

- 10bit ADC end of conversion
- Charger end of charge, connect/disconnect, no battery
- Battery temperature high (at 45ºC or 50ºC with 100/10kΩ NTC)
- Junction temperature high
- Battery low (Brown-out voltage reached)
- Power-up key (pin PWRUP) pressed
- Current sink low voltage
- Power rail monitor: over-voltage CVDD1, CVDD2, CVDD3
- Power rail monitor: under-voltage CVDD1, CVDD2, CVDD3, VDD27

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9.5 10-Bit ADC

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc.

9.5.1 Input Sources

Table 12. ADC10 Input Sources

#	Source	Range	LSB	Description
0	VSUP	5.120V	5mV	check main system supply voltage
1	GPIO3	5.120V	5mV	
2	GPIO4	5.120V	5mV	
3	VBATSW	5.120V	5mV	check battery voltage of 4V Li-Ion accumulator
4	VUSB	5.120V	5mV	check USB/charger input voltage
5		5.120V	5mV	Source defined by DC_TEST in register 18h
6	BATTEMP	2.048V	2mV	check battery charging temperature
7	GPIO1	5.120V	5mV	
8	GPIO2	5.120V	5mV	
9	PWRUP	5.120V	5mV	
A			2mV	reserved
B			2mV	reserved
C	VBE_1µA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = (674 - ADC10<9:0>) / 2
D	VBE_2µA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = (694 - ADC10<9:0>) / 2
E			1mV	reserved
F			1mV	reserved

9.5.2 Parameter

VDD27=2.7, T_A= 25ºC, unless otherwise specified.

Table 13. ADC10 Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ADC_{FS}	ADC Full Scale Range			2.16		V
T_{CON}	Conversion Time		-	34	50	µs

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9.6 GPIO Pins

AS3608 features 4 GPIO pins.

If not re-configured in the start-up sequence GPIO1, GPIO3 and GPIO4 are input per default.GPIO2 is set to output and the pin is driven to low right at the beginning of the startup sequence. GPIO1 and GPIO2 have a dedicated bit to switch the direction between input and output. GPIO3/4 have one state defined as input and three states as output. The following table shows the different input/output options.

Table 14. GPIO Configuration

	GPIO1	GPIO2	GPIO4/3
00	xCharging (1Hz pulses)	LOW	HiZ / HiZ (input)
01	xVSUP_low	xVSUP_low	xVSUP_low / xCharging (1Hz pulses)
10	xPWRUP	HIGH	xPWRUP / PWRGOOD
11	PWRGOOD	xCharging (1Hz pulses)	xEOC / xCharger_active

When configured as input the following functionality is available:

- ADC input, to measure external voltage sources
- Wake-up input to return from hibernation
- Hibernation enable input (GPIO1/2/3 only)
- PWM dimming input (GPIO1/2/3 only)

GPIO pins have a 200kOhm pull-down resistor activated when they are used as an input. (HiZ-mode).

Table 15. GPIO Output Functions

Function	Description
xCharging (1Hz pulses)	The output will be high when the charger is no active. The output toggles between high and low as long as the charging is on going. If EOC, a timeout or overtempertur event stops the charger the output stops toggling.
xCharger_active	The output will be high when the charger is no active or in EOC; it will be low if the charger is active.
xEOC	The output will be high when the charger active; it will be low if the charger is has reached EOC. The output will return back to high if the charger enters resume state.
xPWRUP	The output will get low if the PWRUP pin is high.
PWRGOOD	The output will be high about 3ms after the start-up sequence is finished. It will be low during the sequence. Please be sure to configure the GPIO before the pull-up voltage, otherwise the output will be high as long as the GPIOs are default inputs.
xVSUP_low	The output will get low if the VSUP undervoltage level is reached.
HIGH	The output will be high.
LOW	The output will be low.

Please note that all GPIO pins are open-drain outputs. They can only output a logic “high” if a pull-up and the corresponding pull-up voltage is present.

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9.7 2-Wire-Serial Control Interface

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

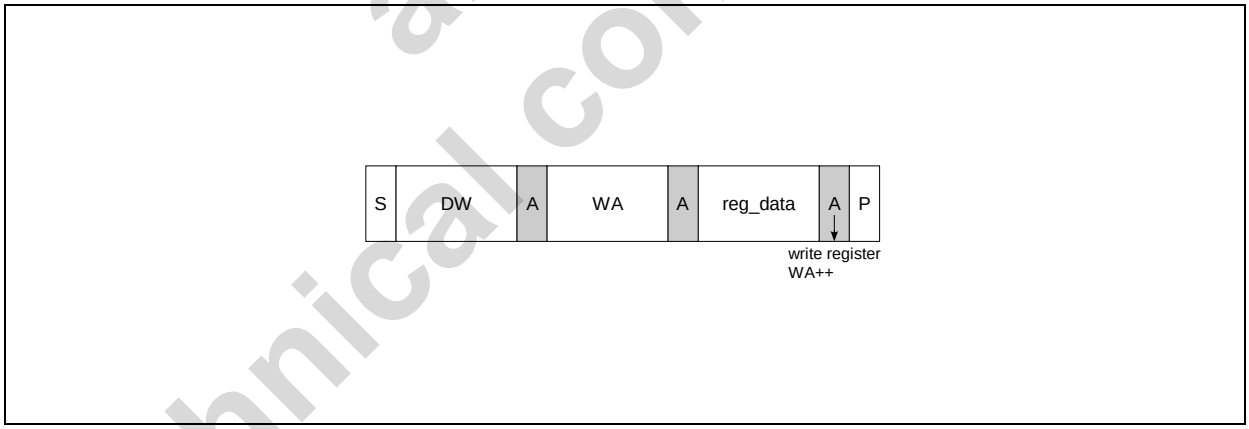
- 8Ch_write
- 8Dh_read

9.7.1 Protocol

Table 16. 2-Wire Serial Symbol Definition

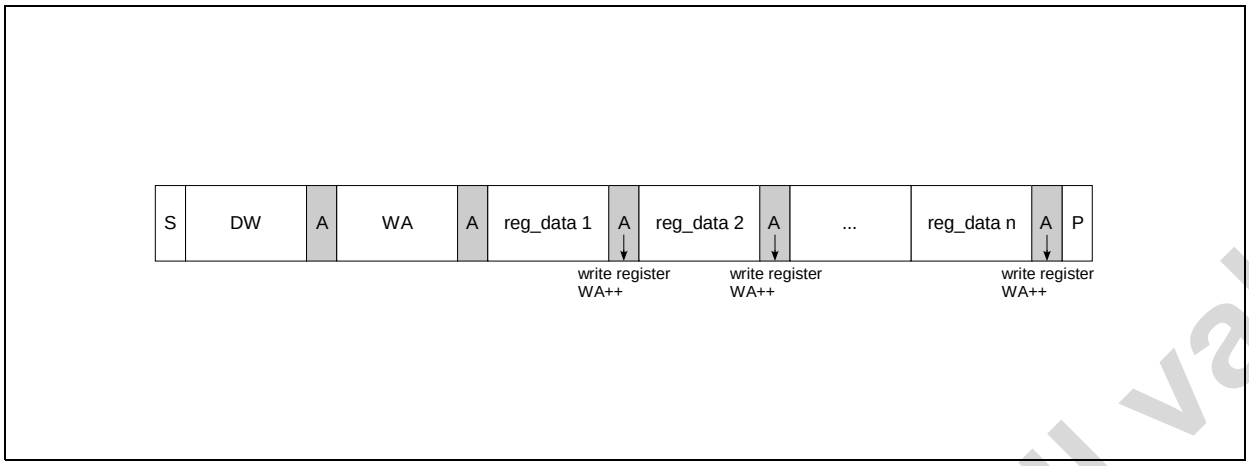
Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1100b (8Ch)
DR	Device address for read	R	1000 1101b (8Dh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge
	AS3608 (=slave) receives data		
	AS3608 (=slave) transmits data		

Figure 14. Byte Write



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Figure 15. Page Write

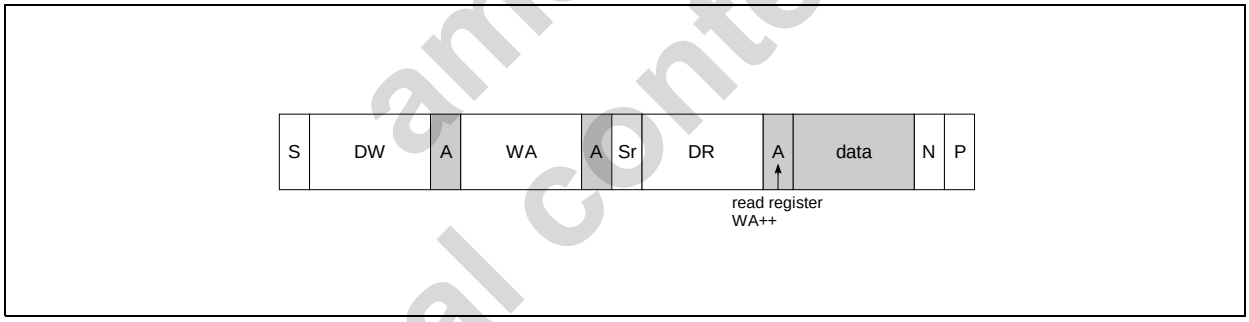


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 16. Random Read



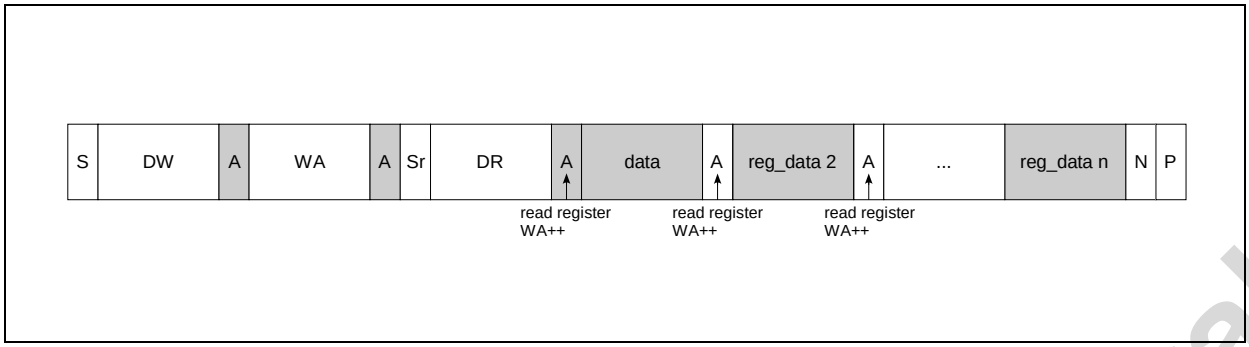
Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

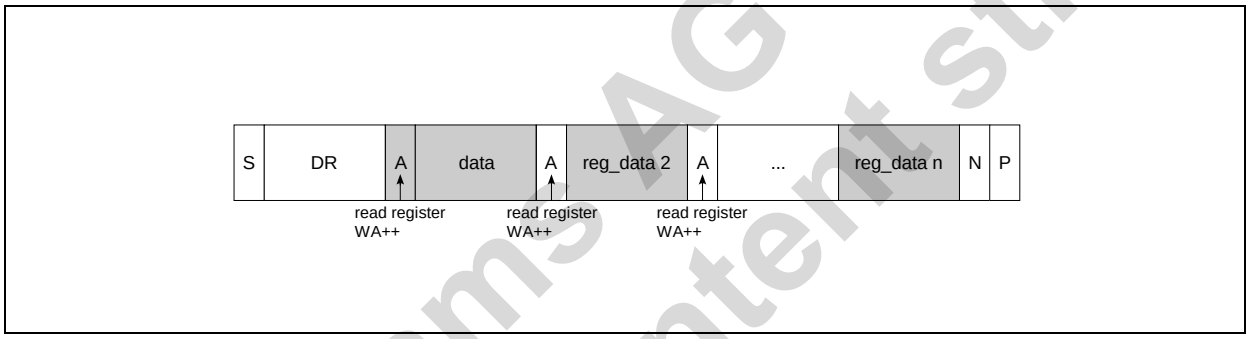
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Figure 17. Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 18. Current Address Read

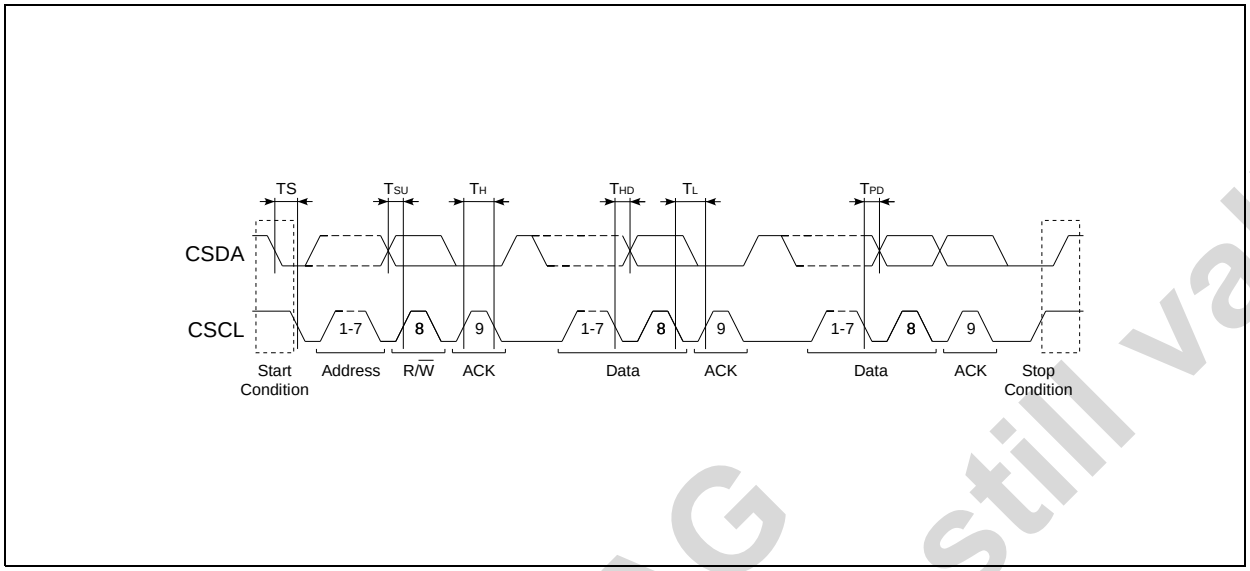


To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

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9.7.2 Parameter

Figure 19. 2-Wire Serial Timing



DVDD =2.9V, T_{amb}=25ºC, unless otherwise specified.

Table 17. 2-Wire Serial Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CSL}	CSCL, CSDA Low Input Level	(max 30%DVDD)	0	-	0.87	V
V_{CSH}	CSCL, CSDA High Input Level	CSCL, CSDA (min 70%DVDD)	2.03	-	5.5	V
HYST	CSCL, CSDA Input Hysteresis		200	450	800	mV
V_{OL}	CSDA Low Output Level	at 3mA	-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
T_H	Clock high time	max. 400kHz clock speed	500			ns
T_L	Clock low time	max. 400kHz clock speed	500			ns
T_{SU}		CSDA has to change Tsetup before rising edge of CSCL	250	-	-	ns
T_{HD}		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_start	200	-	-	ns
T_{PD}		CSDA prop delay relative to lowgoing edge of CSCL		50		ns

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10 Register Definition

Table 18. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
PMU Register									
17h-1	CVDD1	CVDD1_fast 0: Cext=10µF 1: Cext=22µF	VSEL_CVDD1<6:0> 0 … OFF 0x01 – 0x40: 0.6V + VSEL * 12.5mV -> (0.6125V – 1.400V) 0x41 – 0x70: 1.4V + (VSEL-0x40) * 25mV ->(1.425V – 2.600V) 0x71 – 0x7F: 2.6V + (VSEL-0x70) * 50mV -> (2.650V – 3.350V)						
17h-2	CVDD2	CVDD2_fast 0: Cext=10µF 1: Cext=22µF	VSEL_CVDD2<6:0> 0 … OFF 0x01 – 0x40: 0.6V + VSEL * 12.5mV -> (0.6125V – 1.400V) 0x41 – 0x70: 1.4V + (VSEL-0x40) * 25mV ->(1.425V – 2.600V) 0x71 – 0x7F: 2.6V + (VSEL-0x70) * 50mV -> (2.650V – 3.350V)						
17h-3	CVDD3	CVDD3_fast 0: Cext=10µF 1: Cext=22µF	VSEL_CVDD3<6:0> 0 … OFF 0x01 – 0x40: 0.6V + VSEL * 12.5mV -> (0.6125V – 1.400V) 0x41 – 0x70: 1.4V + (VSEL-0x40) * 25mV ->(1.425V – 2.600V) 0x71 – 0x7F: 2.6V + (VSEL-0x70) * 50mV -> (2.650V – 3.350V)						
17h-4	Hibernation	-	KEEP_PVDD4	KEEP_PVDD3	KEEP_PVDD2	KEEP_PVDD1	KEEP_CVDD3	KEEP_CVDD2	KEEP_CVDD1
17h-5	DCDC_Cntr	CFM_CVDD23_OFF 0: pulse skip on 1: pulse skip off	CFM_CVDD1_OFF 0: pulse skip on 1: pulse skip off	CVDD23_FREQ 0: 2MHz 1: 1MHz	CVDD1_FREQ 0: 2MHz 1: 1MHz	DVM_CVDD23<1:0> 0: immediate; 1: 42µs/step; 2: 166µs/step; 3: 666µs/step		DVM_CVDD1<1:0> 0: immediate; 1: 42µs/step; 2: 166µs/step; 3: 666µs/step	
17h-7	GPIO_Cntr	MUX_GPIO43<1:0> 0: HiZ/HiZ; 1: xVSUP_low/xCharging; 2: xPWRUP/PWRGOOD; 3: xEOC/xCharger_active		DRIVE_GPIO2 0: opend drain 1: HiZ	MUX_GPIO2<1:0> 0: LOW; 1: xVSUP_low; 2: HIGH; 3: xCharging		DRIVE_GPIO1 0: HiZ 1: opend drain	MUX_GPIO1<1:0> 0: xCharging; 1: xVSUP_low; 2: xPWRUP; 3: PWRGOOD	
18h-1	PVDD1	PVDD1_ON	ILIM_H_PVDD1 0: 150mA 1: 250mA	LP_PVDD1 0: normal mode 1: low power mode	VSEL_PVDD1<4:0> 0x00 – 0x0F: 1.2V + VSEL * 50mV → (1.2V – 1.95V) 0x10 – 0x1F: 2.0V + (VSEL-0x10) * 100mV → (2.0V – 3.5V)				
18h-2	PVDD2	PVDD2_ON	ILIM_H_PVDD2 0: 150mA 1: 250mA	LP_PVDD2 0: normal mode 1: low power mode	VSEL_PVDD2<4:0> 0x00 – 0x0F: 1.2V + VSEL * 50mV → (1.2V – 1.95V) 0x10 – 0x1F: 2.0V + (VSEL-0x10) * 100mV → (2.0V – 3.5V)				
18h-3	PVDD3	PVDD3_ON	ILIM_H_PVDD3 0: 150mA 1: 250mA	LP_PVDD3 0: normal mode 1: low power mode	VSEL_PVDD3<4:0> 0x00 – 0x0F: 1.2V + VSEL * 50mV → (1.2V – 1.95V) 0x10 – 0x1F: 2.0V + (VSEL-0x10) * 100mV → (2.0V – 3.5V)				

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Table 18. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
18h-4	PVDD4	PVDD4_ON	ILIM_H_PVDD4 0: 150mA 1: 250mA	LP_PVDD4 0: normal mode 1: low power mode	VSEL_PVDD4<4:0> 0x00 – 0x0F: 1.2V + VSEL * 50mV → (1.2V – 1.95V) 0x10 – 0x1F: 2.0V + (VSEL-0x10) * 100mV → (2.0V – 3.5V)				
18h-5	VDD27	PRG_VDD27 0: boot ROM 1:register defined	ILIM_H_VDD27 0: 100mA 1: 200mA	LP_VDD27	-	VSEL_VDD27<3:0> 0x0 – 0x2: 2.3V 0x3 – 0xF: 2.0V + VSEL* 100mV → (2.3V – 3.5V)			
19h-0	CHG_Cntr	BAT_DET_OFF	AUTO_RESUME	BAT_CHARGE_ON	USB_CURRLIM <3:0> 0: 94mA; 1: 141mA; 2: 189mA; 3: 237mA; 4: 285mA; 5: 332mA; 6: 380mA; 7: 428mA; 8: 470mA; 9: 517mA; A: 599mA; B: 760mA; C: 882mA; D: 1060mA; E-F: not defined				USB_PREREG_ON
19h-1	CHG_VCntr	CHG_V_RESUME <2:0> 0: 3.85V; 1: 3.9V; 2: 3.95V; 3: 4.0V; 4: 4.05V; 5: 4.1V; 6:4.15V; 7: 4.2V			VSUP_MIN<1:0> 0: 3.9V; 1: 3.6V; 2: 4.2V; 3: 4.5V		CHG_V_EOC <2:0> 0: 3.9V; 1: 3.95V; 2: 4.0V; 3: 4.05V; 4: 4.1V; 5: 4.15V; 6: 4.2V; 7: 4.25V		
19h-2	CHG_ICntr	CHG_I_CONSTANT <3:0> 0: 94mA; 1: 141mA; 2: 189mA; 3: 237mA; 4: 285mA; 5: 332mA; 6: 380mA; 7: 428mA; 8: 470mA; 9: 517mA; A: 599mA; B: 760mA; C: 882mA; D: 1060mA; E-F: not defined				CHG_I_TRICKLE <3:0> 0: 25mA; 1: 35mA; 2: 47mA; 3: 59mA; 4: 71mA; 5: 83mA; 6: 95mA; 7: 107mA; 8: 118mA; 9: 129mA; A: 150mA; B: 190mA; C: 221mA; D: 265mA; E-F: not defined			
19h-3	CHG_Conf	-			CHG_I_EOC<1:0> 0: 8%; 1: 15%; 2: 10%; 3: 20%		VSUP_EOC <2:0> 0: 4.3V; 1: 4.4V; 2: 4.5V; 3: 4.6V; 4: 4.7V; 5: 4.8V; 6: 4.9V; 7: 5.0V		
19h-4	CHG_NTC	-					NTC_MODE 0: 55°C; 1: 45°C	NTC_10K 0: 100k; 1: 10K;	NTC_ON
19h-5	CHG_TIME	-			TMAX_TIMER	CHG_TIMEOUT <3:0> 0:disabled; 1: 0.5h; 2: 1h; 3: 1,5h; 4: 2h; 5: 2.5h; 6: 3h; 7: 3.5h; 8: 4h; 9: 4.5h; A: 5h; B: 5.5h; C: 6h; D: 6.5h; E: 7h; F:7.5h			
19h-6	CHG_STAT1	NO_BAT	BATTEMP_HIGH	EOC	CV	TRICKLE	RESUME	CC	CHG_DET
19h-7	CHG_STAT2	-						BATSW_MODE <1:0>	
1Ah-1	Out_Cntr	DCDC23_1.4A	GPIO_HBN_ON	HBN_DELAY<1:0> 0: 0ms; 1: 8ms; 2: 16ms; 3: 32ms		DRIVE_XIRQ<1:0> 0: 6mA OD; 1: 6mA PP; 2: 1mA PP; 3: HiZ		MUX_XIRQ<1:0> 0: XIRQ; 1: CLKINT1; 2: CLKINT2; 3: IRQ	
1Ah-2	Clk_Cntr	CLKINT2<1:0> 0: LOW; 1: CLK1Hz (charger); 2: do not use; 3: HIGH		CLKINT1<1:0> 0: 2MHz; 1: 1MHz; 2: 1kHz; 3: 125Hz		GPIO_DIMM_HBN_SEL <1:0> 0: LOW; 1: GPIO1; 2: GPIO2; 3: GPIO3		-	
1Bh-1	Boost_Cntr1	SU_ON	-	SU_SLOWDIM 0: tbd 1: tbd	SU_EXTDIM<1:0> 0: no dimm; 1: CURR1; 2: CURR2; 3: GPIO1/2/3		SU_OVP_OFF	SU_CURR_FB	SU_FASTSKIP
1Bh-2	Boost_Cntr2	SU_IFB<4:0> 0x00 - 0x1F: 1µA * SU_IFB;					SU_CURRLIM	SU_GAIN	SU_FREQ

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Table 18. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
1Bh-3	CURR1	ICURR1<7:0> 0x00 - 0xFF: 150µA * ICURR;							
1Bh-4	CURR2	ICURR2<7:0> 0x00 - 0xFF: 150µA * ICURR;							
1Ch	PMU_Enable	DC_TEST_MUX <3:0> 0: open; 1: PVDD1; 2: PVDD2; 3: PVDD3; 4: PVDD4; 5: VDD27; 6: CVDD1; 7: CVDD2; 8: CVDD3; 9-F: not defined				PMU_GATE	PMU_ENABLE <2:0> SubRegister addresses for registers: 0x17: DCDC regulators 0x18: LDOs regulators 0x19: Charger 0x1A: IO_clock_control 0x1B: BackLight_DCDC		
System Register									
20h	SYSTEM	Design_Version<3:0>				-	JTEMP_SUP_OFF	I2C_WD_ON	PWR_HOLD
21h	SUPERVISOR1	PWRUP_SD_XRES <1:0> 0: XRES; 1: -; 2: SD; 3: SD		SD_XRES_TIME 0: 8s; 1: 4s	JTEMP_SUP<4:0> Temp_ShutDown = 140ºC - JTEMP_SUP*5ºC → (140ºC...5ºC) Temp_IRQ = 120ºC - JTEMP_SUP*5ºC → (120ºC...-15ºC)				
22h	SUPERVISOR2	-	-	VDD27low_SD_OFF	VSUPlow_SD_ON	VSUPlow_SUP<2:0>			VSUPlow_SUP_OFF
23h	IRQENRD_0	CVDD1_SD	CVDD1_IRQ	CVDD2_SD	CVDD2_IRQ	CVDD3_SD	CVDD3_IRQ	-	
		CVDD1_under	CVDD1_over	CVDD2_under	CVDD2_over	CVDD3_under	CVDD3_over	-	
24h	IRQENRD_1	PWRUP_IRQ	GPIO1_IRQ	GPIO2_IRQ	GPIO3_IRQ	GPIO4_IRQ			
25h	IRQENRD_2	CHG_TEMP_IRQ	CHG_EOC_IRQ	CHG_NoBAT_IRQ	CHG_DET_IRQ	-	ICURR_LV_IRQ	VSUP_LOW_IRQ	VDD27_LOW_IRQ
		CHG_TEMP	CHG_EOC	CHG_NoBat	CHG_DET				
26h	IRQENRD_3			T_DEB<1:0> 0: 3ms; 1: off			JTEMP_HIGH	-	ADC_EOC
2Eh	ADC10_0	ADC10_MUX<3:0> 0: VSUP; 1: GPIO3; 2: GPIO4; 3: VSUPSW; 4: VUSB 5: DC_TEST; 6: BATTEMP; 7: GPIO1; 8: GPIO2; 9: PWRUP; A,B: -; C: VBE_1µA; D: VBE_2µA; E,F: -				-	-	ADC10<9:8>	
2Fh	ADC10_1	ADC10<7:0>							

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Table 19. CVDD1 Register

Name		Base		Default
CVDD1		2-wire serial		00h
Offset: 17h-1		CVDD1 DC/DC Buck Regulator Control Register		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CVDD1_fast	0	R/W	Selects a faster regulation mode for CVDD1 suitable for larger load changes. **0: normal mode, Cext=10µF** 1: fast mode, Cext=22µF required
6:0	VSEL_CVDD1<6:0>	000000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h: DC/DC powered down** 01h-40h: CVDD1=0.6V+VSEL_CVDD1*12.5mV 41h-70h: CVDD1=1.4V+(VSEL_CVDD1-40h)*25mV 71h-7Fh: CVDD1=2.6V+(VSEL_CVDD1-70h)*50mV

Table 20. CVDD2 Register

Name		Base		Default
CVDD2		2-wire serial		00h
Offset: 17h-2		CVDD2 DC/DC Buck Regulator Control Register		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CVDD2_fast	0	R/W	Selects a faster regulation mode for CVDD2 suitable for larger load changes. **0: normal mode, Cext=10µF** 1: fast mode, Cext=22µF required
6:0	VSEL_CVDD2<6:0>	000000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h: DC/DC powered down** 01h-40h: CVDD1=0.6V+VSEL_CVDD1*12.5mV 41h-70h: CVDD1=1.4V+(VSEL_CVDD1-40h)*25mV 71h-7Fh: CVDD1=2.6V+(VSEL_CVDD1-70h)*50mV

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Table 21. CVDD3 Register

Name		Base		Default
CVDD3		2-wire serial		00h
Offset: 17h-3		CVDD3 DC/DC Buck Regulator Control Register		
		This is an extended register and needs to be enabled by writing 011b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CVDD3_fast	0	R/W	Selects a faster regulation mode for CVDD3 suitable for larger load changes. **0: normal mode, Cext=10uF** 1: fast mode, Cext=22uF required
6:0	VSEL_CVDD3<6:0>	000000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h: DC/DC powered down** 01h-40h: CVDD1=0.6V+VSEL_CVDD1*12.5mV 41h-70h: CVDD1=1.4V+(VSEL_CVDD1-40h)*25mV 71h-7Fh: CVDD1=2.6V+(VSEL_CVDD1-70h)*50mV

Table 22. Hibernation Register

Name		Base		Default
Hibernation		2-wire serial		00h
Offset: 17h-4		PMU Hibernation Control Register		
		Hibernation starts when writing this register, except hibernation via GPIO is selected. This is an extended register and needs to be enabled by writing 100b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input. This register MUST NOT be read back!!!		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	0	n/a	
6	KEEP_PVDD4	0	W	Keeps the programmed PVDD4 level during hibernation. **0: power down PVDD4** 1: keep PVDD4
5	KEEP_PVDD3	0	W	Keeps the programmed PVDD3 level during hibernation. **0: power down PVDD3** 1: keep PVDD3
4	KEEP_PVDD2	0	W	Keeps the programmed PVDD2 level during hibernation. **0: power down PVDD2** 1: keep PVDD2
3	KEEP_PVDD1	0	W	Keeps the programmed PVDD1 level during hibernation. **0: power down PVDD1** 1: keep PVDD1
2	KEEP_CVDD3	0	W	Keeps the programmed CVDD3 level during hibernation. **0: power down CVDD3** 1: keep CVDD3
1	KEEP_CVDD2	0	W	Keeps the programmed CVDD2 level during hibernation. **0: power down CVDD2** 1: keep CVDD2
0	KEEP_CVDD1	0	W	Keeps the programmed CVDD1 level during hibernation. **0: power down CVDD1** 1: keep CVDD1

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Table 23. DCDC_Cntr Register

Name		Base		Default
DCDC_Cntr		2-wire serial		00h
Offset: 17h-5		DC/DC Step Down Control Register		
		This is an extended register and needs to be enabled by writing 101b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CFM_CVDD23_OFF	0	R/W	Disables pulse skip mode for DCDC2 and DCDC3 **0: current force mode / pulse skip enabled** 1: current force mode / pulse skip disable
6	CFM_CVDD1_OFF	0	R/W	Disables pulse skip mode for DCDC1 **0: current force mode / pulse skip enabled** 1: current force mode / pulse skip disable
5	CVDD23_FREQ	0	R/W	Selects the switching frequency for DCDC2 and DCDC 3 **0: 2MHz** 1: 1MHz
4	CVDD1_FREQ	0	R/W	Selects the switching frequency for DCDC1 **0: 2MHz** 1: 1MHz
3:2	DVM_CVDD23<1:0>	00	R/W	Configures the dynamic voltage management (output voltage slope) for CVDD2 and CVDD3 **00: immediate change of the output voltage** 01: 32µs/step 10: 128µs/step 11: 512µs/step
1:0	DVM_CVDD1<1:0>	00	R/W	Configures the dynamic voltage management (output voltage slope) for CVDD1 **00: immediate change of the output voltage** 01: 32µs/step 10: 128µs/step 11: 512µs/step

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Table 24. GPIO_Cntr Register

Name		Base		Default
GPIO_Cntr		**2-wire serial**		**00h**
Offset: 17h-7		**GPIO Control Register**		
		This is an extended register and needs to be enabled by writing 111b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	MUX_GPIO43<1:0>	00	R/W	Configures GPIO4 and GPIO3 **00: HiZ / HiZ (GPIOs are inputs)** 01: xVSUP_low / xCharging 10: xPWRUP / PWRGOOD 11: xEOC / xCharger_active
5	DRIVE_GPIO2	0	R/W	Configures GPIO2 as input or output **0: open drain (output)** 1: HiZ (input)
4:3	MUX_GPIO2<1:0>	00	R/W	Configures GPIO2 output mode **00: LOW** 01: xVSUP_low 10: HIGH 11: xCharging
2	DRIVE_GPIO1	0	R/W	Configures GPIO1 as input or output **0: HiZ (input)** 1: open drain (output)
1:0	MUX_GPIO1<1:0>	00	R/W	Configures GPIO1 output mode **00: xCharging** 01: xVSUP_low 10: xPWRUP 11: PWRGOOD

Table 25. PVDD1 Register

Name		Base		Default
PVDD1		**2-wire serial**		**00h**
Offset: 18h-1		**PVDD1 Control Register**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVDD1_ON	0	R/W	Enables PVDD1 regulator **0: PVDD1 switched off** 1: PVDD1 switched on
6	ILIM_H_PVDD1	0	R/W	Selects the higher current limit for PVDD1 **0: default mode, 150mA** 1: 250mA mode
5	LP_PVDD1	0	R/W	Selects the low power mode for PVDD1 **0: PVDD1 is in normal operation** 1: PVDD1 supply current is reduced
4:0	VSEL_PVDD1<4:0>	00000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is selected by boot ROM 0x00-0x0F: 1.2V+VSEL*50mV → (1.2V - 1.95V) 0x10-0x1F: 2.0V + (VSEL-0x10)*100mV → (2.0V-3.5V)

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Table 26. PVDD2 Register

Name		Base		Default
PVDD2		2-wire serial		00h
Offset: 18h-2		PVDD2 Control Register		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVDD2_ON	0	R/W	Enables PVDD2 regulator **0: PVDD2 switched off** 1: PVDD2 switched on
6	ILIM_H_PVDD2	0	R/W	Selects the higher current limit for PVDD2 **0: default mode, 150mA** 1: 250mA mode
5	LP_PVDD2	0	R/W	Selects the low power mode for PVDD2 **0: PVDD2 is in normal operation** 1: PVDD2 supply current is reduced
4:0	VSEL_PVDD2<4:0>	00000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is selected by the boot ROM 0x00-0x0F: 1.2V+VSEL*50mV → (1.2V - 1.95V) 0x10-0x1F: 2.0V + (VSEL-0x10)*100mV → (2.0V-3.5V)

Table 27. PVDD3 Register

Name		Base		Default
PVDD3		2-wire serial		00h
Offset: 18h-3		PVDD3 Control Register		
		This is an extended register and needs to be enabled by writing 011b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVDD3_ON	0	R/W	Enables PVDD3 regulator **0: PVDD1 switched off** 1: PVDD1 switched on
6	ILIM_H_PVDD3	0	R/W	Selects the higher current limit for PVDD3 **0: default mode, 150mA** 1: 250mA mode
5	LP_PVDD3	0	R/W	Selects the low power mode for PVDD3 **0: PVDD3 is in normal operation** 1: PVDD3 supply current is reduced
4:0	VSEL_PVDD3<4:0>	00000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is selected by the boot ROM 0x00-0x0F: 1.2V+VSEL*50mV → (1.2V - 1.95V) 0x10-0x1F: 2.0V + (VSEL-0x10)*100mV → (2.0V-3.5V)

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Table 28. PVDD4 Register

Name		Base		Default
PVDD4		2-wire serial		00h
Offset: 18h-4		PVDD4 Control Register		
		This is an extended register and needs to be enabled by writing 100b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVDD4_ON	0	R/W	Enables PVDD4 regulator **0: PVDD4 switched off** 1: PVDD4 switched on
6	ILIM_H_PVDD4	0	R/W	Selects the higher current limit for PVDD4 **0: default mode, 150mA** 1: 250mA mode
5	LP_PVDD4	0	R/W	Selects the low power mode for PVDD4 **0: PVDD4 is in normal operation** 1: PVDD4 supply current is reduced
4:0	VSEL_PVDD4<4:0>	00000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is selected by the boot ROM 0x00-0x0F: 1.2V+VSEL*50mV → (1.2V - 1.95V) 0x10-0x1F: 2.0V + (VSEL-0x10)*100mV → (2.0V-3.5V)

Table 29. VDD27 Register

Name		Base		Default
VDD27		2-wire serial		00h
Offset: 18h-5		VDD27 Control Register		
		This is an extended register and needs to be enabled by writing 101b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PRG_VDD27	0	n/a	Selects the output voltage control mode for VDD27 **0:VDD27 is in default mode** 1: VDD27 is register controlled (Reg. 18-5h)
6	ILIM_H_VDD27	0	R/W	Selects the higher current limit for VDD27 **0: default mode, 100mA** 1: 200mA mode
5	LP_VDD27	0	R/W	Selects the low power mode for VDD27 **0: VDD27 is in normal operation** 1: VDD27 supply current is reduced
5	-	0	n/a	
3:0	VSEL_VDD27<3:0>	0000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is 2.7V) 0x0-0x2: 2.3V 0x3-0xF: 2.0V + VSEL*100mV → (2.3V-3.5V)

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Table 30. CHG_Cntr Register

Name		Base		Default
CHG_Cntr		2-wire serial		C9h
Offset: 19h-0		Charger Control Register		
		This is an extended register but does not need to be enabled as Reg. 1Ch is 000b per default. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BAT_DET_OFF	1	R/W	Disables the battery detection 0: Battery detection switched on **1: Battery detection switched off**
6	AUTO_RESUME	1	R/W	Defines the behavior after end of charge (EOC) 0: auto resume is disabled **1: auto resume enabled, charger will start charging when VBATSW drops below the resume level**
5	BAT_CHARGE_ON	0	R/W	Enables the battery charging **0: VSUP is supplied via USB pre-regulator, but the battery switch is open** 1: normal battery charging operation from USB pre-regulator
4:1	USB_CURRLIM <3:0>	1000	R/W	Sets the USB pre-regulator current limit 0x0: 94mA (USB low current) 0x1: 141mA 0x2: 189mA 0x3: 237mA 0x4: 285mA 0x5: 332mA 0x6: 380mA 0x7: 428mA **0x8: 470mA (USB high current)** 0x9: 517mA 0xA: 599mA 0xB: 760mA 0xC: 882mA 0xD: 1060mA 0xE, 0xF: do not use
0	USB_PREREG_ON	1	R/W	Enables the USB pre-regulator and current limiter 0: USB pre-regulator is switched off **1: USB pre-regulator supplies VSUP from VUSB input**

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Table 31. CHG_VCntr Register

Name		Base		Default
CHG_VCntr		2-wire serial		36h
Offset: 19h-1		Charger Voltage Control Register		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	CHG_V_RESUME <2:0>	001	R/W	Sets the charger auto resume voltage threshold 000: 3.85V **001: 3.90V** 010: 3.95V 011: 4.00V 100: 4.05V 101: 4.10V 110: 4.15V 111: 4.20V
4:3	VSUP_MIN<1:0>	10	R/W	Defines the minimum VSUP voltage during trickle or constant current charging. The charging current will be reduced if VSUP would drop below this threshold. 00: 3.9V 01: 3.6V **10: 4.2V** 11: 4.5V
2:0	CHG_V_EOC <2:0>	110	R/W	Sets the charger end of charge voltage threshold 000: 3.90V 001: 3.95V 010: 4.00V 011: 4.05V 100: 4.10V 101: 4.15V **110: 4.20V** 111: 4.25V

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Table 32. CHG_ICntr Register

Name		Base		Default
CHG_VCntr		2-wire serial		21h
Offset: 19h-2		Charger Current Control Register		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	CHG_I_CONSTANT <3:0>	0010	R/W	Sets the current during constant current charging 0x0: 94mA 0x1: 141mA **0x2: 189mA** 0x3: 237mA 0x4: 285mA 0x5: 332mA 0x6: 380mA 0x7: 428mA 0x8: 470mA 0x9: 517mA 0xA: 599mA 0xB: 760mA 0xC: 882mA 0xD: 1060mA 0xE, 0xF: do not use
3:0	CHG_I_TRICKLE <3:0>	0001	R/W	Sets the current during constant current charging 0x0: 24mA **0x1: 35mA** 0x2: 47mA 0x3: 59mA 0x4: 71mA 0x5: 83mA 0x6: 95mA 0x7: 107mA 0x8: 118mA 0x9: 129mA 0xA: 150mA 0xB: 190mA 0xC: 221mA 0xD: 265mA 0xE, 0xF: do not use

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Table 33. CHG_Config Register

Name		Base		Default
CHG_Config		2-wire serial		15h
Offset: 19h-3		Charger Configuration Register		
		This is an extended register and needs to be enabled by writing 011b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	-	000	n/a	
4:3	CHG_I_EOC<1:0>	10	R/W	Configures the end of charge current threshold. Charging will be stopped if the current drops below the threshold. 00: 8% of constant current setting 01: 15% **10: 10%** 11: 20%
2:0	VSUP_EOC <2:0>	101	R/W	Defines VSUP voltage after EOC and isolated battery. 000: 4.3V 001: 4.4V 010: 4.5V 011: 4.6V 100: 4.7V **101: 4.8V** 110: 4.9V 111: 5.0V

Table 34. CHG_NTC Register

Name		Base		Default
CHG_NTC		2-wire serial		01h
Offset: 19h-4		Charger NTC Control Register		
		This is an extended register and needs to be enabled by writing 100b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	0000 0	n/a	
2	NTC_MODE	0	R/W	Defines the temperature level for the battery temperature supervisor to stop charging. (for beta of NTC = 4250) **0: 55ºC** 1: 45ºC
1	NTC_10K	0	R/W	Defines the type of NTC used for battery temperature supervisor. **0: 100kΩ** 1: 10kΩ
0	NTC_ON	1	R/W	Enables the battery temperature supervisor via NTC resistor. 0: NTC battery temp supervision disabled **1: NTC battery temp supervision enabled**

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Table 35. CHG_TIME Register

Name		Base		Default
CHG_TIME		2-wire serial		07h
Offset: 19h-5		Charger Time Control Register		
		This is an extended register and needs to be enabled by writing 101b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	-	0000 0	n/a	
4	TMAX_TIMER	0	R	Returns the time-out supervision status **0: no time-out reached** 1: charger time-out reached, charging stopped
			W	Resets the charger time supervision 0: - 1: resets time-out counter
3:0	CHG_TIMEOUT <3:0>	0111	R/W	Sets the current during constant current charging 0x0: charger timer disabled 0x1: 0.5h 0x2: 1h 0x3: 1.5h 0x4: 2h 0x5: 2.5h 0x6: 3h **0x7: 3.5h** 0x8: 4h 0x9: 4.5h 0xA: 5h 0xB: 5.5h 0xC: 6h 0xD: 6.5h 0xE: 7h 0xF: 7.5h

Table 36. CHG_STAT1 Register

Name		Base		Default
CHG_STAT1		2-wire serial		xxh
Offset: 19h-6		Charger Status Register 1		
		This is an extended register and needs to be enabled by writing 110b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	NO_BAT	x	R	Status if a battery is detected to the system, by measuring the NTC value on BATTEMP pin. 0: battery detected 1: no battery detected
6	BATTEMP_HIGH	x	R	Only valid if a charger is deducted. 0: battery temperature o.k. 1: battery temperature higher 55ºC/45ºC (seed **NTC_MODE**)
5	EOC	x	R	0: end of charge not reached. Bit is cleared automatically if **USB_PREREG_ON** or **BAT_CHARGE_ON** is cleared or resume state is entered 1: end of charge reached

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Table 36. CHG_STAT1 Register

Name		Base		Default
CHG_STAT1		2-wire serial		xxh
Offset: 19h-6		Charger Status Register 1		
		This is an extended register and needs to be enabled by writing 110b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	CV	x	R	1: if charger is in constant voltage (top-off charge) mode
3	TRICKLE	x	R	1: if charger is in trickle charging mode
2	RESUME	x	R	1: if VBATSW dropped below resume threshold
1	CC	x	R	1: if charger is in constant current charging mode
0	CHG_DET	x	R	1: if a charger adapter is detected on VUSB pin

Table 37. CHG_STAT2 Register

Name		Base		Default
CHG_STAT2		2-wire serial		xxh
Offset: 19h-7		Charger Status Register 2		
		This is an extended register and needs to be enabled by writing 111b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	xxxx xx	n/a	
1:0	BATSW_MODE <1:0>	x	R	Shows the battery switch operation mode 00: battery switch open, no ideal diode operation (just for charger start-up) 01: battery switch open, ideal diode operation (charger connected but EOC reached) 10: battery switch acting as a voltage limited current source (charging) 11: battery switch closed (charger disconnected)

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Table 38. Out_Cntr Register

Name		Base		Default
Out_Cntr		2-wire serial		00h
Offset: 1Ah-1		DCDC mode and XIRQ Output Control Register		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	DCDC23_1.4A	0	R/W	Combines DCDC2 and DCDC3 to one regulator for 1.4A output currents **0: DCDC2 and DCDC3 working independent** 1: DCDC2 & DCDC3 combined for 1.4A (DCDC3 registers have no effect)
6	GPIO_HBN_ON	0	R/W	**0: Hibernation enable via GPIOs disabled** 1: Hibernation enalbe via GPIOs enabled GPIO selected via **GPIO_DIMM_HBN_SEL <1:0>**
5:4	HBN_DELAY<1:0>	00	R/W	Sets the delay time for going into hibernation after writing to register 17-4h **00: 0ms** 01: 8ms 10: 16ms 11: 32ms
3:2	DRIVE_XIRQ<1:0>	00	R/W	Sets the XIRQ output pin to open-drain, push-pull or tri-state and sets various driving strengths **00: 6mA open-drain output** 01: 6mA push-pull output 10: 1mA push-pull output 11: HiZ, tri-state
1:0	MUX_XIRQ<1:0>	00	R/W	Multiplexes various digital signals to the XIRQ output pin **00: XIRQ, active low interrupt request signal** 01: CLKINT1, internal clock signal, see Clk_Cntr register 10: CLKINT2, internal clock signal, see Clk_Cntr register 11: IRQ, active low reset signal

Table 39. Clk_Cntr Register

Name		Base		Default
Clk_Cntr		2-wire serial		00h
Offset: 1Ah-2		Clock Control Register		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	CLKINT2<1:0>	00	R/W	Selects the CLKINT2 input source. Note, this is an internal clock, which can be multiplexed to the XRES output. **00: LOW, drives the signal to logic "0"** 01: CLK1Hz charger 10: do not use 11: HIGH, drives the signal to logic "1"
5:4	CLKINT1<1:0>	00	R/W	Selects the CLKINT1 frequency. Note, this is an internal clock, which can be multiplexed to XIRQ output. **00: 2MHz** 01: 1MHz 10: 1kHz 11: 125Hz

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Table 39. Clk_Cntr Register

Name		Base		Default
Clk_Cntr		**2-wire serial**		**00h**
Offset: 1Ah-2		**Clock Control Register**		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:2	GPIO_DIMM_HBN_SEL <1:0>	00	R/W	Selects input for external dimming or hibernation control **00: disable dimming or hibernation via GPIO** 01: GPIO1 10: GPIO2 11: GPIO3
1:0	-	00	n/a	

Table 40. BOOST_Cntr1 Register

Name		Base		Default
BOOST_Cntr1		**2-wire serial**		**00h**
Offset: 1Bh-1		**DCDC step-up Control Register 1**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SU_ON	0	R/W	Enables the DCDC step-up regulator **0: SU switched off** 1: SU switched on (will be reset if VFB exceeds the maximum and the current drops to zero)
6	-	0	n/a	
5	SU_SLOWDIM	0	R/W	Selects the DCDC step-up regulator external dimming mode **0: for dimming frequencies <1kHz** 1: for dimming frequencies >1kHz
4:3	SU_EXTDIM<1:0>	00	R/W	**Selects the DCDC step-up external PWM dimming input** **00: no ext. dimming** 01: CURR1 controlled 10: CURR2 controlled 11: GPIO1/2/3 controlled (selected via **GPIO_DIMM_HBN_SEL <1:0>**)
2	SU_OVP_OFF	0	R/W	Disables the DCDC step-up over-voltage protection **0: SU OVP switched on** 1: SU OVP switched off
1	SU_CURR_FB	0	R/W	Selects the DCDC step-up feedback mode **0: voltage FB via pin FBSU** 1: current feedback via CURR1 or CURR2 (automatic select)
0	SU_FASTSKIP	0	R/W	Defines the DCDC step-up regulator output voltage at low loads, when pulse skipping is active **0: Accurate output voltage, more ripple** 1: Elevated output voltage, less ripple

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Table 41. BOOST_Cntr2 Register

Name		Base		Default
BOOST_Cntr2		**2-wire serial**		**00h**
Offset: 1Bh-2		**DCDC step-up Control Register 2**		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	SU_IFB<4:0>	0 0000	R/W	Defines the tuning current at pin FBSU. **0x00: 0µA** 0x01: 1µA 0x02: 2µA ... 0x1F: 31µA
2	SU_CURRLIM	0	R/W	Selects the DCDC step-up converter coil current limit **0: normal current limit** 1: current limit increased by about 50%
1	SU_GAIN	0	R/W	DCDC step-up converter feedback gain is selected automatically depending on current or voltage feedback mode. Setting this bit to “1” will choose the alternative feedback gain setting.
0	SU_FREQ	00	R/W	Defines the DCDC step-up switching frequency **0: 1MHz** 1: 500kHz

Table 42. CURR1 Register

Name		Base		Default
CURR1		**2-wire serial**		**00h**
Offset: 1Bh-3		**Current Sink 1 Register**		
		This is an extended register and needs to be enabled by writing 011b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ICURR1<7:0>	0x00	R/W	Sets the current for current sink 1 in 255 steps with 140.626µA stepsize **0x00: Current sink 1 switched off** 0x01: 0.15 mA 0x02: 0.30 mA 0x03: 0.45 mA .. 0xFE: 38,10 mA 0xFF: 38.25 mA

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Table 43. CURR2 Register

Name		Base		Default
CURR2		2-wire serial		00h
Offset: 1Bh-4		Current Sink 2 Register		
		This is an extended register and needs to be enabled by writing 100b to Reg. 1Ch first. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ICURR2<7:0>	0x00	R/W	Sets the current for current sink 2 in 255 steps with 140.626µA stepsize **0x00: Current sink 2 switched off** 0x01: 0.141 mA 0x02: 0.281 mA 0x03: 0.422 mA .. 0xFE: 35,72 mA 0xFF: 35.86 mA

Table 44. PMU_Enable Register

Name		Base		Default
PMU_Enable		2-wire serial		00h
Offset: 1Ch		PMU_Enable Register		
		Selects the extended register on address 17h to 1Bh and enables writing to these PMU register. It also sets the ADC10 multiplexer to measure various regulator voltages This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	DC_TEST_MUX <3:0>	0000	R/W	Allows multiplexing internal and external supply voltages to one DC test node which can be further multiplexed to the ADC10. The accuracy is 5mV/LSB (see reg. 2Eh) **0x0: open** 0x1: PVDD1 0x2: PVDD2 0x3: PVDD3 0x4: PVDD4 0x5: VDD27 0x6: CVDD1 0x7: CVDD2 0x8: CVDD3 0x9-0xF: n/a
3	PMU_GATE	0	R/W	Enables all settings made in registers 17h to 1Bh at once. If this bit is set, changes are activated as soon as they are written to the related register. **0: no change** 1: change at once
2:0	PMU_ENABLE <2:0>	000	R/W	Selects extended registers 17h to 1Bh for the next read or write. This register has to be set before every read or write even if the selection is not changing. **0: 19h-0 selected** 1: 17h-1 to 1Bh-1 selected 2: 17h-2 to 1Bh-2 selected ... 7: 17h-7 to 1Bh-7 selected

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Table 45. SYSTEM Register

Name		Base		Default
SYSTEM		**2-wire serial**		**51h**
Offset: 20h		**SYSTEM Register**		
		This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Design_Version<3:0>	0101	R	Number to identify the design version 0101: for chip version 2v2
3	-	0	n/a	
2	JTEMP_SUP_OFF	0	R/W	Junction temperature supervision (level can be set in register 21h) **0: temperature supervision enabled** 1: temperature supervision disabled
1	I2C_WD_ON	0	R/W	2-wire serial interface watchdog To reset the watchdog counter a 2-wire serial read operation has to be performed at least every 500ms. If the watchdog counter is not reset, the PMU will be powered down. **0: watchdog is disabled** 1: watchdog is enabled
0	PWR_HOLD	1	R/W	0: power up hold is cleared and PMU will power down **1: is automatically set to on after power on**

Table 46. SUPERVISOR1 Register

Name		Base		Default
SUPERVISOR1		**2-wire serial**		**00h**
Offset: 21h		**SUPERVISOR Register 1**		
		This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	PWRUP_SD_XRES <1:0>	00	R/W	Applying a high signal on PWRUP pin for about 10s will **00: perform a reset cycle** 01: have no effect 10: initiate a shut-down 11: initiate a shut-down
5	SD_XRES_TIME	0	n/a	Halfs the time from pulling PWRUP high to XRES or SD **0: 8s** 1: 4s
4:0	JTEMP_SUP<4:0>	0	R/W	Sets the threshold for junction temperature emergency shutdown and junction temperature interrupt Invoke shutdown at: JTemp_SD=140-JTEMP_Sup*5ºC Invoke interrupt at: JTemp_IRQ=120-JTEMP_Sup*5ºC JT_Sup | IRQ | Shutdown **00000 | 120°C | 140°C** 00001 | 115°C | 135°C . | . | . . | . | . 11110 | -30°C | -10°C 11111 | -35°C | -15°C

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Table 47. SUPERVISOR2 Register

Name		Base		Default
SUPERVISOR2		2-wire serial		00h
Offset: 22h		SUPERVISOR Register 2		
		This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	-	00	n/a	
5	VDD27low_SD_OFF	0	R/W	**0: VDD27low (VDD27 -10%) shut down enabled** 1: VDD27low shut down disabled
4	VSUPlow_SD_ON	0	R/W	**0: VSUPlow shut down enabled** 1: VSUPlow shut down disabled
3:1	VSUPlow_SUP<2:0>	000	R/W	Sets the threshold for VSUP supervisor 000: 2.7V 001: 2.9V 010: 3.1V 011: 3.2V 100: 3.3V 101: 3.4V 110: 3.5V 111: 3.6V
0	VSUPlow_SUP_OFF	0	R/W	**0: VSUPlow supervision enabled** 1: VSUPlow supervision disabled

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Table 48. First Interrupt Register

Name		Base		Default
IRQENRD_0		2-wire serial		00h
Offset: 23h		First Interrupt Register		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CVDD1_SD	0	W	Invokes shut-down of the PMU when a –10% under-voltage spike at CVDD1 occurs **0: disable** 1: enable
	CVDD1_under	x	R	This bit is set when a –5% under-voltage at CVDD1 occurs
6	CVDD1_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD1 **0: disable** 1: enable
	CVDD1_over	x	R	This bit is set when a +8% over-voltage at CVDD1 occurs
5	CVDD2_SD	0	W	Invokes shut-down of the PMU when a –10% under-voltage spike at CVDD2 occurs **0: disable** 1: enable
	CVDD2_under	x	R	This bit is set when a –5% under-voltage at CVDD2 occurs
4	CVDD2_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD2 **0: disable** 1: enable
	CVDD2_over	x	R	This bit is set when a +8% over-voltage at CVDD2 occurs
3	CVDD3_SD	0	W	Invokes shut-down of the PMU when a –10% under-voltage spike at CVDD3 occurs **0: disable** 1: enable
	CVDD3_under	x	R	This bit is set when a –5% under-voltage at CVDD3 occurs
2	CVDD3_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD3 **0: disable** 1: enable
	CVDD3_over	x	R	This bit is set when a +8% over-voltage at CVDD3 occurs
1:0	-	00	n/a	

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Table 49. Second Interrupt Register

Name		Base		Default
IRQENRD_1		2-wire serial		00h
Offset: 24h		Second Interrupt Register		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWRUP_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the PWRUP input pin occurs **0: disable** 1: enable
		x	R	This bit is set whenever a high level of min. VSUP/3 at the PWRUP input pin occurs (PWRUP pin is commonly connected to the power-up button)
6	GPIO1_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the GPIO1 input pin occurs **0: disable** 1: enable
		x	R	This bit is set whenever a high level of min. tbd at the GPIO1 input pin occurs
5	GPIO2_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the GPIO2 input pin occurs **0: disable** 1: enable
		x	R	This bit is set whenever a high level of min. tbd at the GPIO2 input pin occurs
4	GPIO3_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the GPIO3 input pin occurs **0: disable** 1: enable
		x	R	This bit is set whenever a high level of min. tbd at the GPIO3 input pin occurs
3	GPIO4_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the GPIO4 input pin occurs **0: disable** 1: enable
		x	R	This bit is set whenever a high level of min. tbd at the GPIO4 input pin occurs
2:0	-	000	n/a	

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Table 50. Third Interrupt Register

Name		Base		Default
IRQENRD_2		**2-wire serial**		**00h**
Offset: 25h		**Third Interrupt Register**		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CHG_TEMP_IRQ (status change)	0	W	Battery over-temperature interrupt setting **0: disable** 1: enable interrupt if **CHG_TEMP** status bit changes
	CHG_TEMP	x	R	Battery over-temperature status reading **0: battery temperature below off-threshold** 1: battery temperature was too high and the charger was turned off. The charger will be turned on again, when the temperature gets below the on-threshold
6	CHG_EOC_IRQ (status change)	0	W	Charger end of charge interrupt setting. **0: disable** 1: enable interrupt if **CHG_EOC** status bit changes
	CHG_EOC	x	R	Charger end of charge status reading **0: battery charging in progress** 1: charging is complete, charging current is below selected level of nominal current, charger was turned off.
5	CHG_NoBAT_IRQ (status change)	0	W	Charger no battery interrupt setting **0: disable** 1: enable interrupt if **CHG_NoBat** status bit changes
	CHG_NoBat	x	R	Charger no battery status reading **0: battery connected** 1: no battery detected at VBATSW pin
4	CHG_DET_IRQ (status change)	0	W	Charger detect interrupt setting. **0: disable** 1: enable interrupt if **CHG_DET** status bit changes
	CHG_DET	x	R	Charger detect status reading **0:charger disconnected** 1: charger connected
3	-	0	n/a	
2	ICURR_LV_IRQ (level)	0	W	Current sink undervoltage interrupt setting. **0: disable** 1: enable interrupt if the outputvoltage of one of the current sinks gets below the target regulation voltage
		x	R	Current sink undervoltage status reading **0: normal voltage on ICURR1 and ICURR2** 1: voltage at ICURR1 or ICURR2 dropped below target voltage

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Table 50. Third Interrupt Register

Name		Base		Default
IRQENRD_2		2-wire serial		00h
Offset: 25h		Third Interrupt Register		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	VSUP_LOW_IRQ (level)	0	W	VSUP under-voltage supervisor interrupt setting **0: disable** 1: enable
		x	R	VSUP supervisor interrupt reading **0: VSUP is above brown out level** 1: VSUP has reached brown out level The threshold can be set with **VSUPlow_SUP<2:0>** in SUPERVISOR2 register (22h). If the shutdown is enabled the interrupt will not occur.
0	VDD27_LOW_IRQ (level)	0	W	VDD27 undervoltage supervisor interrupt setting **0: disable** 1: enable
		x	R	VDD27 supervisor interrupt reading **0: VDD27 is above threshold out level** 1: VDD27 has reached threshold level (VDD27-10%). If the shutdown is enabled the interrupt will not occur.

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Table 51. Fourth Interrupt Register

Name		Base		Default
IRQENRD_3		2-wire serial		00h
Offset: 26h		Fourth Interrupt Register		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a VDD27-POR or XRES input.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	-	00	R/W	
5	T_DEB<1:0>	0	R/W	Sets the de-bounce time all interrupt inputs: **0: 3ms** 1: off
4:3	-	00	R/W	
2	JTEMP_HIGH (level)	0	W	Supervisor junction over-temperature interrupt setting **0: disable** 1: enable
		x	R	Supervisor junction over-temperature interrupt reading 0: chip temperature below threshold 1: chip temperature has reached the threshold The threshold can be set in the SUPERVISOR register (21h)
1	-	0	R/W	
0	ADC_EOC (edge)	0	W	ADC end of conversion interrupt setting **0: disable** 1: enable
		x	R	ADC end of conversion interrupt reading 0: ADC conversion not finished 1: ADC conversion finished. Read out ADC10_0 and ADC10_1 register to get the result (2Eh & 2Fh)

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Table 52. ADC10_0 Register

Name		Base		Default
ADC10_0		2-wire serial		0000 00xxb
Offset: 2Eh		First 10-bit ADC Register		
		Writing to this register will start the measurement of the selected source. This register is reset at a VDD27-POR, exception are bit 0 and 1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ADC10_MUX<3:0>	0000	R/W	Selects ADC input source **0000: VSUP** 0001: GPIO3 0010: GPIO4 0011: VBATSW 0100: VUSB 0101: defined by DC_TEST in register 0x1C 0110: BATTEMP 0111: GPIO1 1000: GPIO2 1001:PWRUP 1010: reserved 1011: reserved 1100: VBE_1uA 1101: VBE_2uA 1110: reserved 1101: reserved
3:2	-	00	n/a	
1:0	ADC10<9:8>	xx	R	ADC result bit 9 to 8

Table 53. ADC10_1 Register

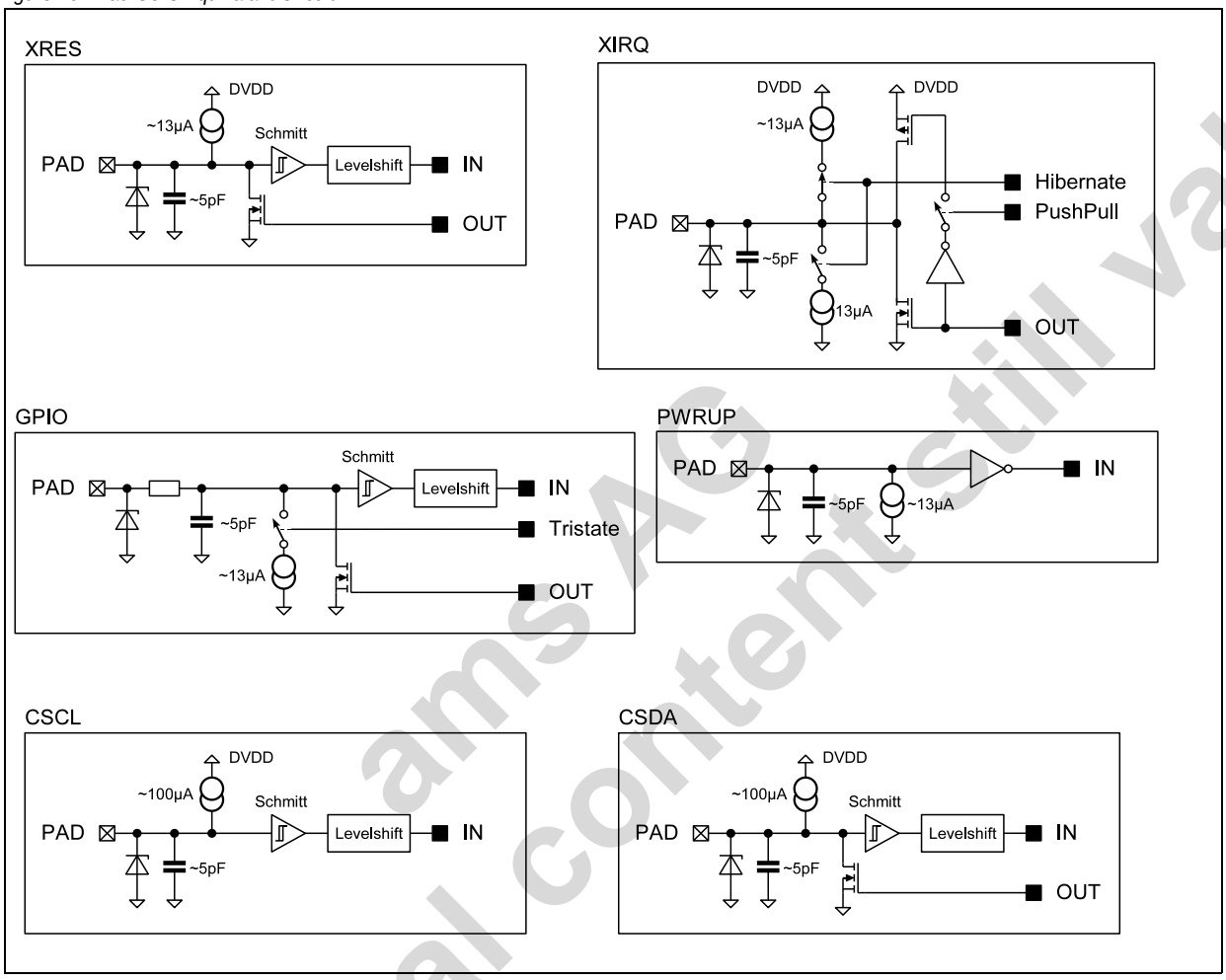
Name		Base		Default
ADC10_1		2-wire serial		xxh
Offset: 2Fh		Second 10-bit ADC Register		
		This register is reset at a VDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ADC10<7:0>	00h	R	ADC results bits 7 to 0

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11 Application Information

11.1 Pad Cells

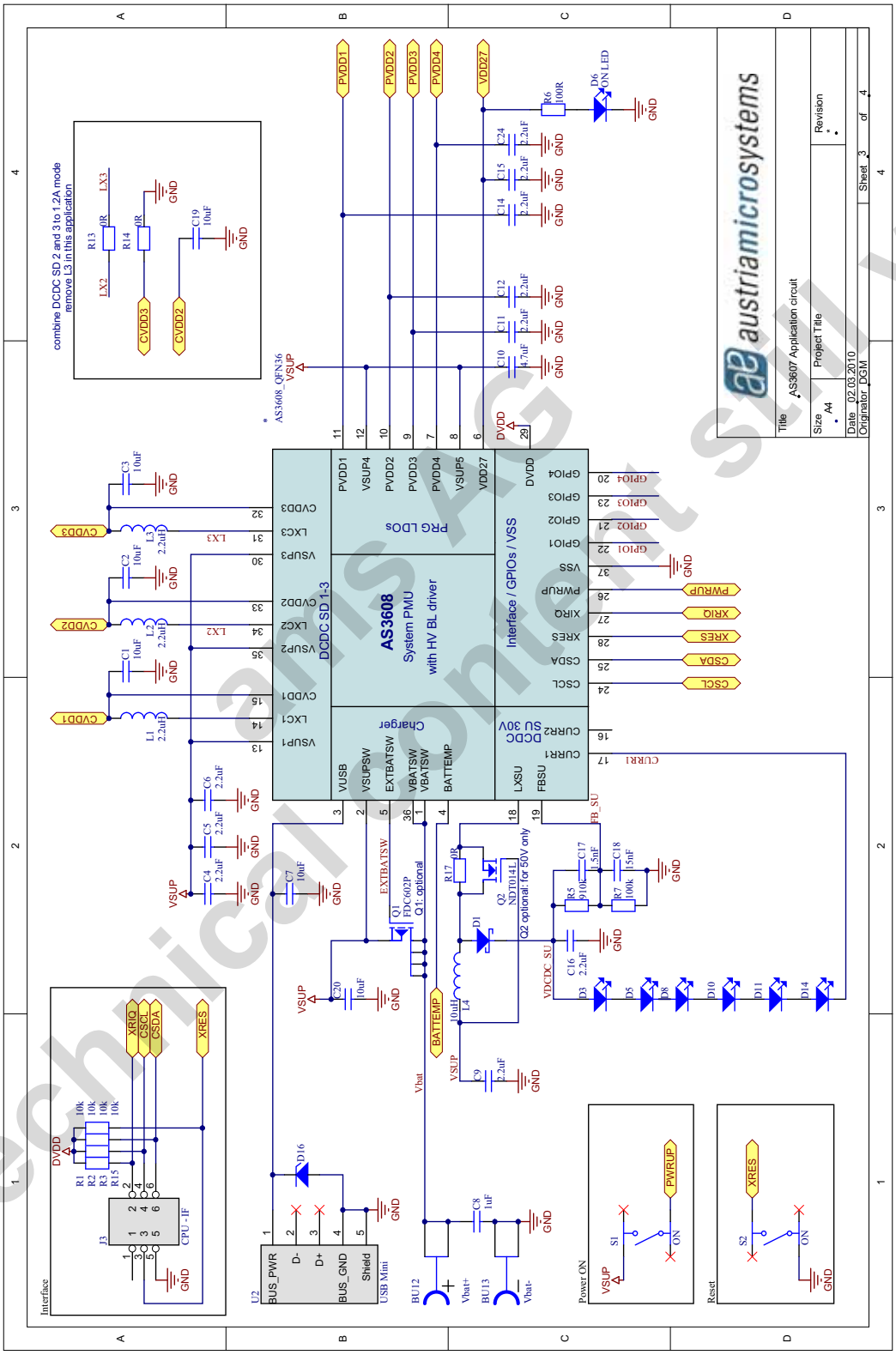
Figure 20. Pad Cells Equivalant Circuit



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11.2 Application Schematics

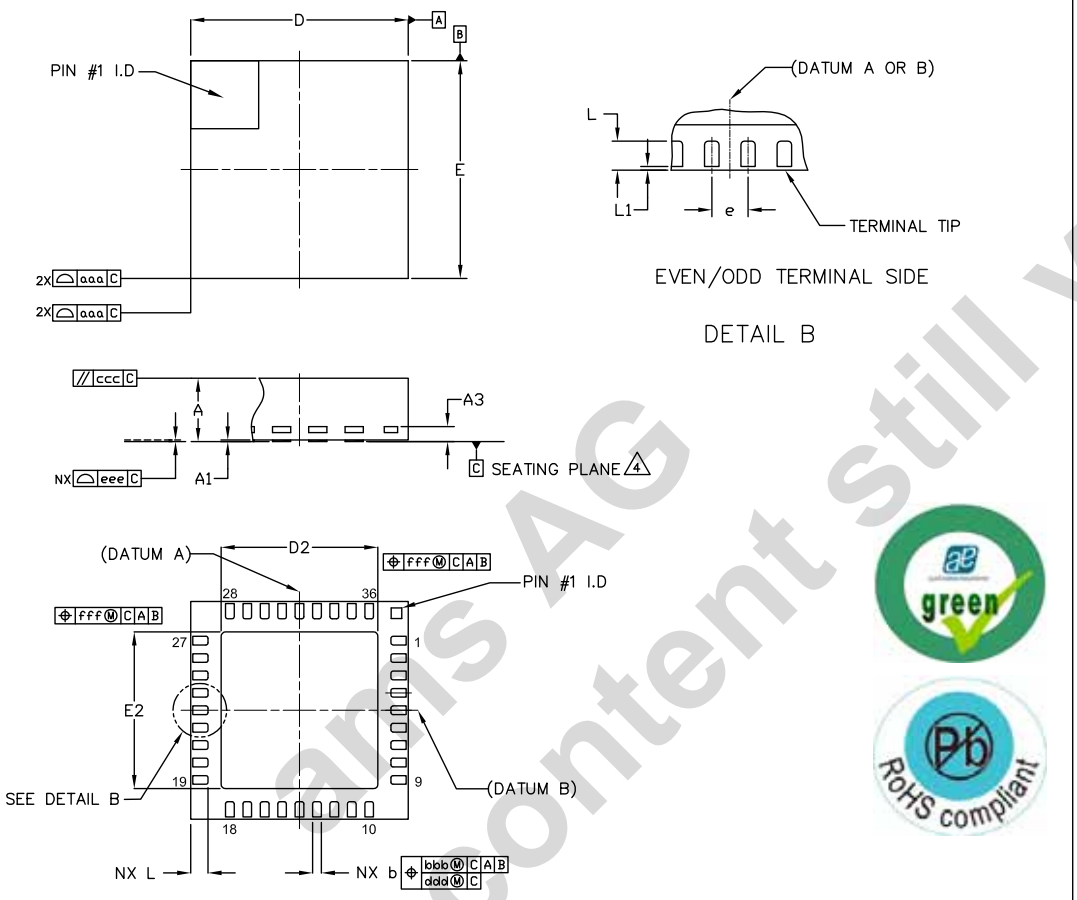
Figure 21. Typical AS3608 Application Schematic



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12 Package Drawings and Markings

Figure 22. AS3608 QFN36, 0.5mm Pitch



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	–	0.20 REF	–
L	0.45	0.55	0.65
L1	0	–	0.15
b	0.18	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
D2	4.04	4.10	4.24
E2	4.04	4.10	4.24
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		36	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

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ASSEMBLY ENGINEERING

DRAWN RH8	DATE 2010.10.27	REV. N/C	TITLE SAWN QFN, PULL BACK, 6x6x0.9mm 36 LEAD, 4.10mm SQ. ePAD	REFERENCE DOCUMENT JEDEC MO – 220 LATEST REVISION
CHECKED GBO	DATE 2010.10.27		DRAWING NO. QCL	UNIT
APPROVED MKR	DATE 2010.10.27	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

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Figure 23. QFN Marking

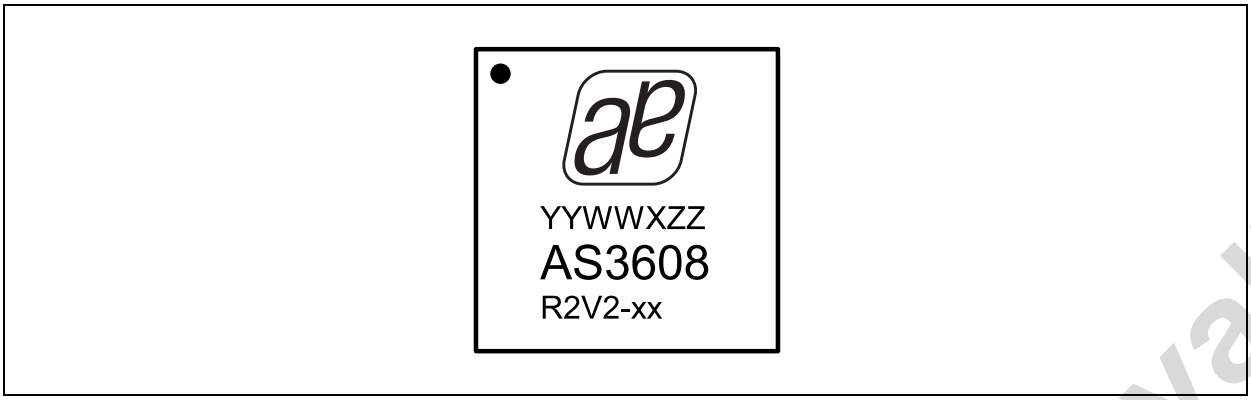


Table 54. Package Code YWWZZZ

YY	WW	X	ZZ
year	working week assembly / packaging	plant identifier	free choice

Table 55. Start-up Revision Code

xx	Sequence
FF	engineering samples, no sequence programmed or sequence programmed on request
00	default sequence (no sequence programmed)
xx	customer specified sequence programmed during production test

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Revision History

Revision	Date	Owner	Description
1.00	7.2010	pkm	first official release
1.01	9.2010	pkm	corrected GPIO2 bit description & GPIO hibernation description updated package drawings
1.02	2010	pkm	corrected charger block diagram
1.03	3.2011	pkm	added NTC supply description, added USB rising edge specification, added DCDC2+3 efficency diagrams

Note: Typos may not be explicitly mentioned under revision history.

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13 Ordering Information

The devices are available as the standard products shown in Table 56.

Table 56. Ordering Information

Ordering Code	Marking	Sequence	Description	Delivery Form	Package
AS3608-BQFP-FF	R2v2-FF	sequence programmable on request	System PMU with HV Backlight	Tape & Reel dry pack	QFN36 6x6 0.5mm pitch
AS3608-BQFP-00	R2v2-00	default sequence	System PMU with HV Backlight	Tape & Reel dry pack	QFN36 6x6 0.5mm pitch
AS3608-BQFP-xx	R2v2-xx	customer specified	System PMU with HV Backlight	Tape & Reel dry pack	QFN36 6x6 0.5mm pitch

Note: All products are RoHS compliant and austriamicrosystems green.
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Technical Support is found at http://www.austriamicrosystems.com/Technical-Support

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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