# AS1970 - AS1975
# Low-Voltage Single/Dual/Quad Comparators

**DataSheet**

## 1 General Description

The AS1970 - AS1975 are single/dual/quad comparators that operate with supplies from 2.5 to 5.5V making them perfect for all 3- and 5-volt applications. The comparators can also operate with dual supplies (±1.25 to ±2.75V), and require very little supply current (down to 8.5µA) with minimal propagation delay (300ns).

Low input bias current (1.0pA, typ), low input offset voltage (0.5mV, typ), and internal hysteresis (3mV) make these comparators ideal for low-power single-cell applications including power-management and power-monitoring systems.

The comparators are available as the standard products listed in Table 1.

*Table 1. Standard Products*

| Model | Output Type |
|---|---|
| AS1970/AS1972/AS1974 | Push/Pull |
| AS1971/AS1973/AS1975 | Open-Drain |

The AS1970/AS1972/AS1974 push/pull output can sink or source current.

The AS1971/AS1973/AS1975 open-drain output can be pulled beyond VCC to a maximum of 5.5V > VEE. These open-drain versions are ideal for logic-level translators or bipolar-to-unipolar converters.

Large internal output drivers allow Rail-to-Rail output swings with loads of up to 8mA.

The AS1970/AS1971 are available in a 5-pin SOT23 package. The AS1972/AS1973 are available in a 8-pin MSOP package. The AS1974/AS1975 are available in a 14-pin TSSOP package.

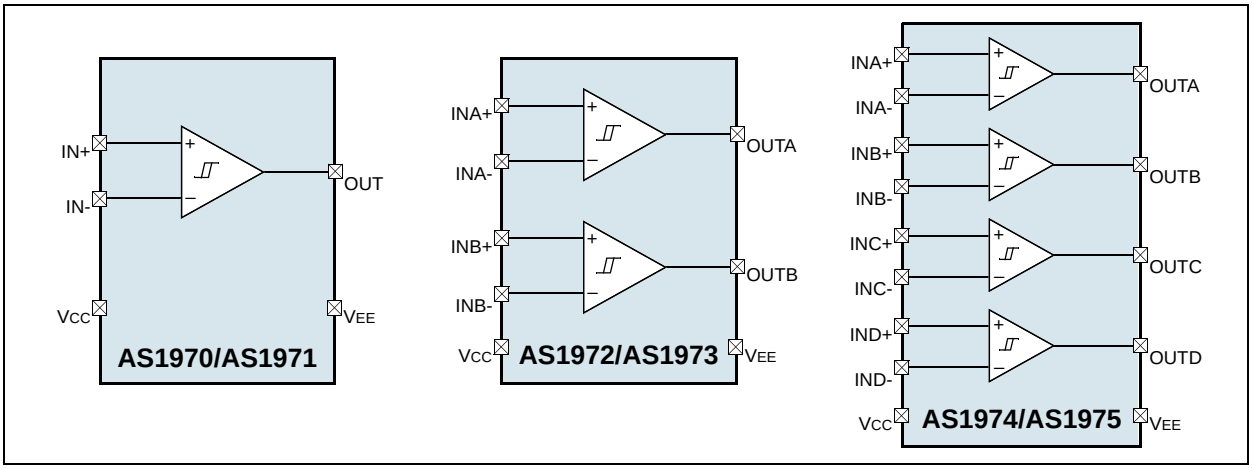
## 2 Key Features

- CMOS Push/Pull Output Sinks and Sources 8mA (AS1970/AS1972/AS1974)
- CMOS Open-Drain Output Voltage Extends Beyond VCC (AS1971/AS1973/AS1975)
- Quiescent Supply Current: 8.5µA per Comparator
- Internal Hysteresis: 3mV
- 3V/5V Logic-Level Translation
- Single-Supply Operation: 2.5 to 5.5V
- Common-Mode Input Voltage Range Extends 250mV Above the Rails
- Low Propagation Delay: 300ns
- Minimized Overall Power Consumption
- Supply Current @1MHz Switching Frequency: 80µA
- No Phase Reversal for Overdriven Inputs
- Package Types:
  - 5-pin SOT23 – AS1970/AS1971
  - 8-pin MSOP – AS1972/AS1973
  - 14-pin TSSOP – AS1974/AS1975

## 3 Applications

The devices are ideal for battery-powered systems, mobile communication devices, zero-crossing detectors, window comparators, level translators, threshold detectors/discriminators, ground/supply-sensing applications, IR receivers or any other space-limited application with low power-consumption requirements.

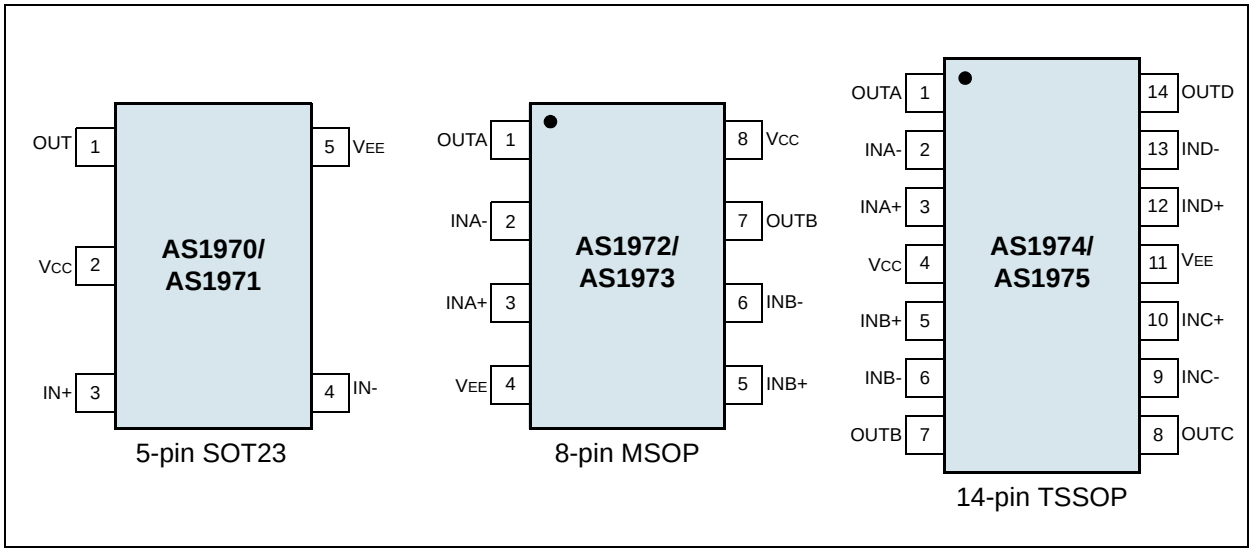
*Figure 1. Block Diagrams*



# 4 Pinout and Packaging

## Pin Assignments

*Figure 2. Pin Assignments (Top View)*




## Pin Descriptions

*Table 2. Pin Descriptions*

| Pin Number | Pin Name | Description |
|---|---|---|
| See Figure 2 | IN- | **Comparator Inverting Input** |
| | IN+ | **Comparator Non-Inverting Input** |
| | INA- | **Comparator A Inverting Input** |
| | INA+ | **Comparator A Non-Inverting Input** |
| | INB- | **Comparator B Inverting Input** |
| | INB+ | **Comparator B Non-Inverting Input** |
| | INC- | **Comparator C Inverting Input** |
| | INC+ | **Comparator C Non-Inverting Input** |
| | IND- | **Comparator D Inverting Input** |
| | IND+ | **Comparator D Non-Inverting Input** |
| | OUT | **Comparator Output** |
| | OUTA | **Comparator A Output** |
| | OUTB | **Comparator B Output** |
| | OUTC | **Comparator C Output** |
| | OUTD | **Comparator D Output** |
| | VCC | **Positive Supply Voltage** |
| | VEE | **Negative Supply Voltage** |

# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 3. Absolute Maximum Ratings*

| Parameter | | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ to $V_{EE}$ | | | 7 | V | |
| IN*x*+, IN*x*- to $V_{EE}$ | | -0.3 | $V_{CC}$ + 0.3 | V | |
| OUT*x* to $V_{EE}$ | AS1970/AS1972/AS1974 | -0.3 | $V_{CC}$ + 0.3 | V | |
| | AS1971/AS1973/AS1975 | -0.3 | +7 | V | |
| OUT*x* Short-Circuit Duration to $V_{EE}$ or $V_{CC}$ | | | 10 | s | |
| Continuous Power Dissipation ($T_{AMB}$ = +70ºC) | 5-pin SOT23 | | 571 | mW | Derate 7.1mW/ºC above +70ºC |
| | 8-pin MSOP | | 727 | mW | Derate 9.1mW/ºC above +70ºC |
| | 14-pin TSSOP | | 727 | mW | Derate 9.1mW/ºC above +70ºC |
| Operating Temperature Range | | -40 | +85 | ºC | |
| Junction Temperature Range | | | +150 | ºC | |
| Storage Temperature Range | | -65 | +150 | ºC | |
| Package Body Temperature | | | 260 | ºC | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn). |

# 6 Electrical Characteristics

*$V_{CC}$ = 2.7 to 5.5V, $V_{EE}$ = 0V, $V_{CM}$ = 0V, $T_{AMB}$ = -40 to +85ºC (unless otherwise specified). Typ values are at $T_{AMB}$ = +25ºC.*

*Table 4. Electrical Characteristics*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Inferred from PSRR test | 2.5 | | 5.5 | V |
| $I_{DD}$ | Supply Current | $V_{CC}$ = 5V, No Load, AS1974/AS1975 | | 36 | 64 | µA |
| | | $V_{CC}$ = 5V, No Load, AS1972/AS1973 | | 18 | 32 | |
| | | $V_{CC}$ = 5V, No Load, AS1970, AS1971 | | 11 | 19 | |
| | | $V_{CC}$ = 2.7V, No Load, AS1974/AS1975 | | 34 | 60 | |
| | | $V_{CC}$ = 2.7V, No Load, AS1972/AS1973 | | 17 | 30 | |
| | | $V_{CC}$ = 2.7V, No Load, AS1970, AS1971 | | 10 | 18 | |
| PSRR | Power-Supply Rejection Ratio | 2.5V ≤ $V_{CC}$ ≤ 5.5V, $T_{AMB}$ = +25ºC | 55 | 80 | | dB |
| $V_{CMR}$ | Common-Mode Voltage Range [1] | $T_{AMB}$ = +25ºC | $V_{EE}$ - 0.25 | | $V_{CC}$ + 0.25 | V |
| | | $T_{AMB}$ = -40 to +85ºC | $V_{EE}$ | | $V_{CC}$ | |
| $V_{OS}$ | Input Offset Voltage [2] | Full Common-Mode Range, $T_{AMB}$ = +25ºC | | ±0.5 | ±6 | mV |
| | | Full Common-Mode Range, $T_{AMB}$ = -40 to +85ºC | | | ±8 | |
| $V_{HYS}$ | Input Hysteresis | | | ±3 | | mV |
| $I_B$ | Input Bias Current [3, 4] | | | 0.001 | 10 | nA |
| $I_{OS}$ | Input Offset Current | | | 0.5 | | pA |
| $C_{IN}$ | Input Capacitance | | | 3.5 | | pF |
| CMRR | Common-Mode Rejection Ratio | $T_{AMB}$ = +25ºC | 52 | 80 | | dB |
| $I_{LEAK}$ | Output Leakage Current | AS1971/AS1973/AS1975 only | | | 1.0 | µA |
| $I_{SC}$ | Output Short-Circuit Current | Sourcing or Sinking, $V_{OUT}$ = $V_{EE}$ or $V_{CC}$, $V_{CC}$ = 5V | | 60 | | mA |
| | | Sourcing or Sinking, $V_{OUT}$ = $V_{EE}$ or $V_{CC}$, $V_{CC}$ = 2.7V | | 18 | | |
| $V_{OL}$ | OUT*x* Output Voltage Low | $V_{CC}$ = 5V, $I_{SINK}$ = 8mA, $T_{AMB}$ = +25ºC | | 0.2 | 0.4 | V |
| | | $V_{CC}$ = 5V, $I_{SINK}$ = 8mA, $T_{AMB}$ = -40 to +85ºC | | | 0.55 | |
| | | $V_{CC}$ = 2.7V, $I_{SINK}$ = 3.5mA, $T_{AMB}$ = +25ºC | | 0.15 | 0.3 | |
| | | $V_{CC}$ = 2.7V, $I_{SINK}$ = 3.5mA, $T_{AMB}$ = -40 to +85ºC | | | 0.4 | |
| $V_{OH}$ | OUT*x* Output Voltage High (AS1970/AS1972/AS1974 only) | $V_{CC}$ = 5V, $I_{SINK}$ = 8mA, $T_{AMB}$ = +25ºC | 4.6 | 4.85 | | V |
| | | $V_{CC}$ = 5V, $I_{SINK}$ = 8mA, $T_{AMB}$ = -40 to +85ºC | 4.45 | | | |
| | | $V_{CC}$ = 2.7V, $I_{SINK}$ = 3.5mA, $T_{AMB}$ = +25ºC | 2.4 | 2.55 | | |
| | | $V_{CC}$ = 2.7V, $I_{SINK}$ = 3.5mA, $T_{AMB}$ = -40 to +85ºC | 2.3 | | | |

*Table 4. Electrical Characteristics (Continued)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RISE}$ | OUT*x* Rise Time (AS1970/AS1972/AS1974 only) | $V_{CC}$ = 5V, $C_{LOAD}$ = 15pF | | 32 | | ns |
| | | $V_{CC}$ = 5V, $C_{LOAD}$ = 50pF | | 50 | | |
| | | $V_{CC}$ = 5V, $C_{LOAD}$ = 200pF | | 80 | | |
| $t_{FALL}$ | OUT*x* Fall Time | $V_{CC}$ = 5V, $C_{LOAD}$ = 15pF | | 22 | | ns |
| | | $V_{CC}$ = 5V, $C_{LOAD}$ = 50pF | | 32 | | |
| | | $V_{CC}$ = 5V, $C_{LOAD}$ = 200pF | | 60 | | |
| $t_{PD-}$ | Propagation Delay | AS1970/AS1972/AS1974 only, $C_{LOAD}$ = 15pF, 10mV Overdrive | | 400 | | ns |
| | | AS1970/AS1972/AS1974 only, $C_{LOAD}$ = 15pF, 100mV Overdrive | | 300 | | |
| | | AS1971/AS1973/AS1975 only, $C_{LOAD}$ = 15pF, $R_{PULLUP}$ = 5.1kΩ, 10mV Overdrive | | 400 | | |
| | | AS1971/AS1973/AS1975 only, $C_{LOAD}$ = 15pF, $R_{PULLUP}$ = 5.1kΩ, 100mV Overdrive | | 300 | | |
| $t_{PD+}$ | | AS1970/AS1972/AS1974 only, $C_{LOAD}$ = 15pF, 10mV Overdrive | | 420 | | |
| | | AS1970/AS1972/AS1974 only, $C_{LOAD}$ = 15pF, 100mV Overdrive | | 270 | | |
| $t_{PU}$ | Power-Up Time | | | 20 | | µs |

1. Inferred from the $V_{OS}$ test. Both or either inputs can be driven 0.3V beyond either supply rail without output phase reversal.
2. $V_{OS}$ is defined as the center of the hysteresis band at the input.
3. $I_B$ is defined as the average of the two input bias currents ($I_{B-}$, $I_{B+}$).
4. Guaranteed by design.

# 7 Typical Operating Characteristics

*Figure 3. Supply Current vs. Temperature (per comparator)*

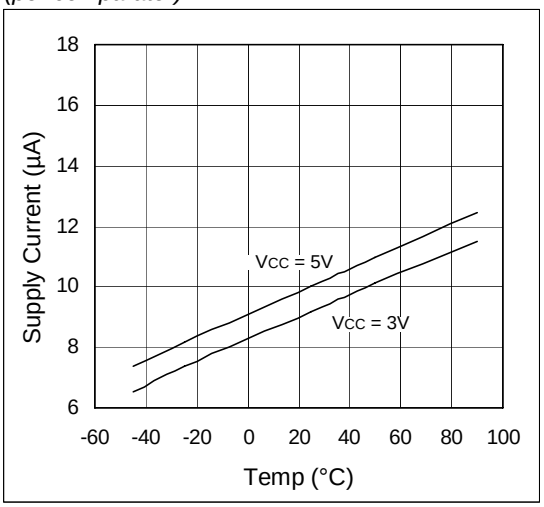



*Figure 4. Supply Current vs. Output Transition Frequency (per comparator)*

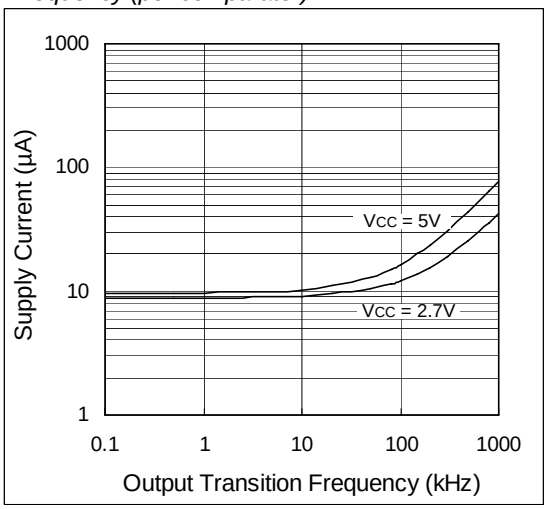



*Figure 5. VOL vs. ISINK; VIN+ < VIN-*

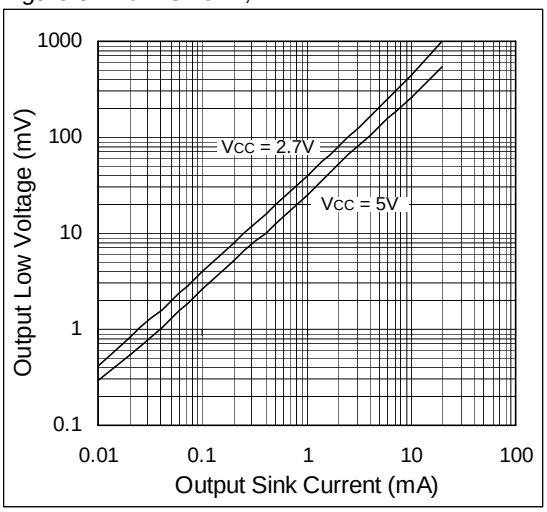



*Figure 6. VOH vs. ISOURCE ; VIN+ > VIN-*

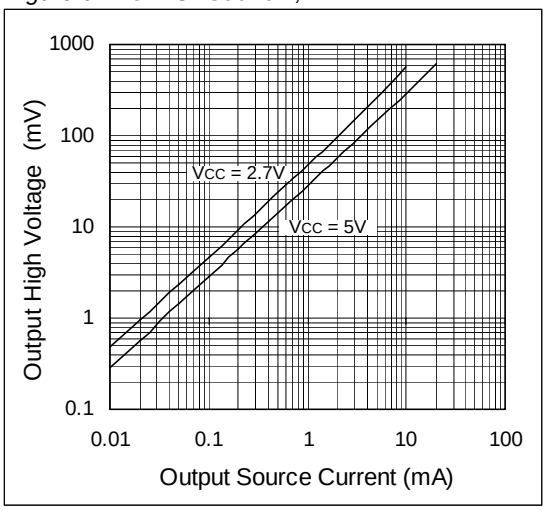



*Figure 7. ISINK vs. Temperature*

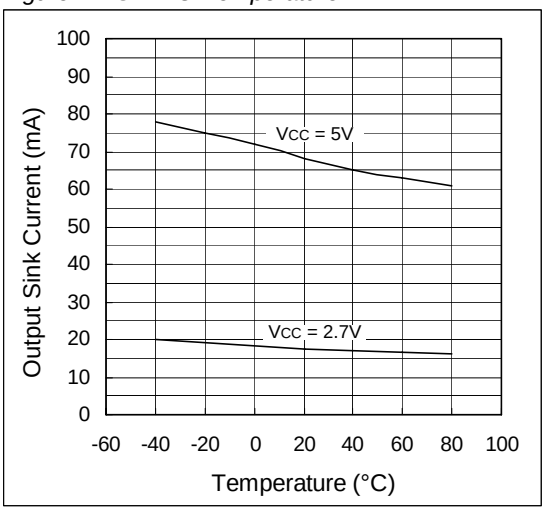



*Figure 8. VOS vs. Temperature*

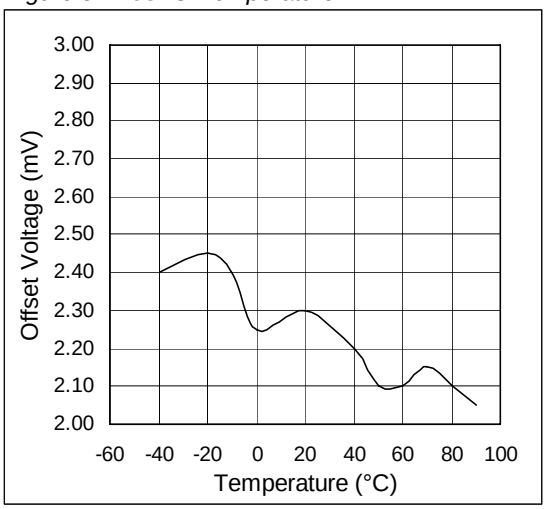


*Figure 9. $t_{PD+}$ vs. $C_{LOAD}$; $V_{CC}$ = 3V, $V_{OD}$ = 50mV*

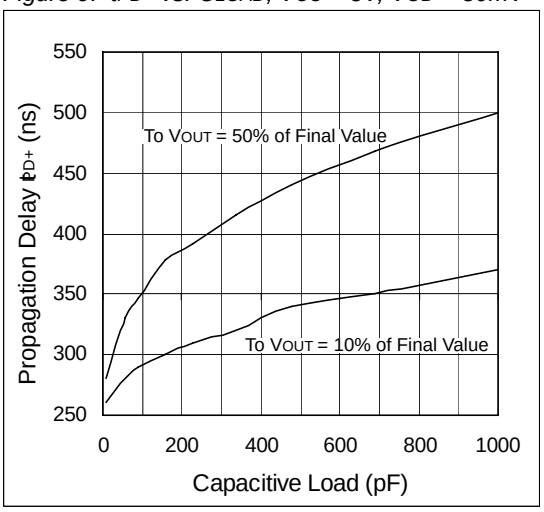



*Figure 10. $t_{PD+}$ vs. $C_{LOAD}$; $V_{CC}$ = 5V, $V_{OD}$ = 50mV*

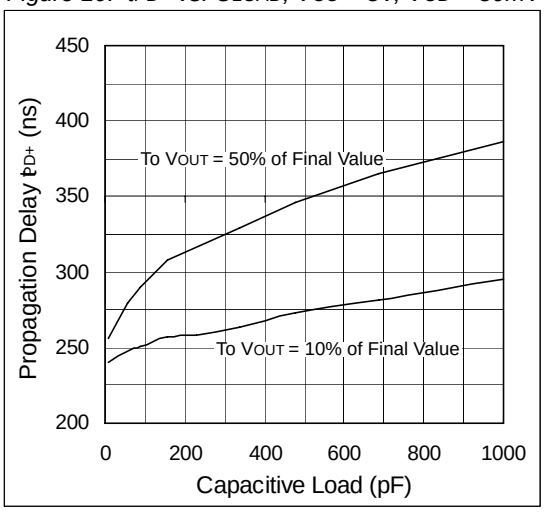



*Figure 11. $t_{PD+}$ vs. Temperature; $V_{OD}$ = 50mV*

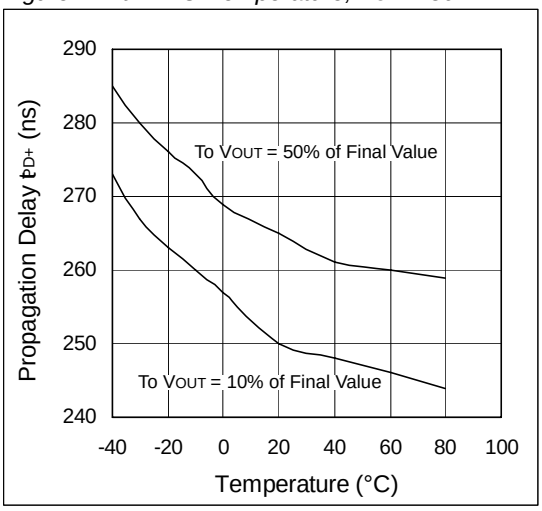



*Figure 12. $t_{PD+}$ vs. $V_{OD}$*

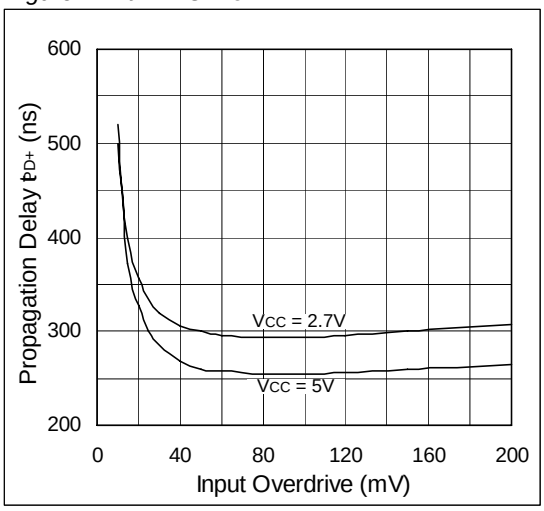



*Figure 13. 1MHz Response; $V_{OD}$ = 50mV*

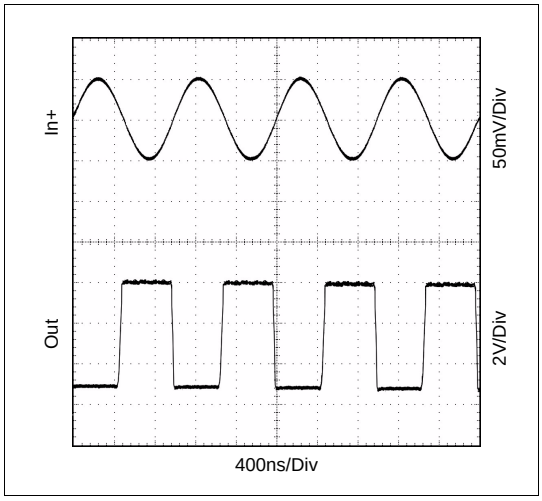



*Figure 14. Power-Up Delay; $V_{OD}$ = 50mV*

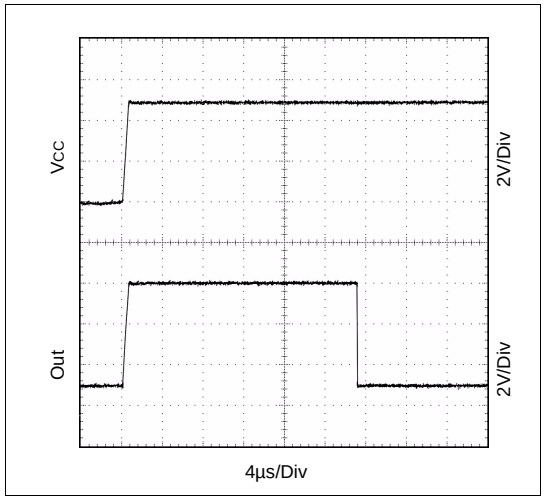


*Figure 15. $t_{PD+}$; $V_{OD}$ = 50mV*

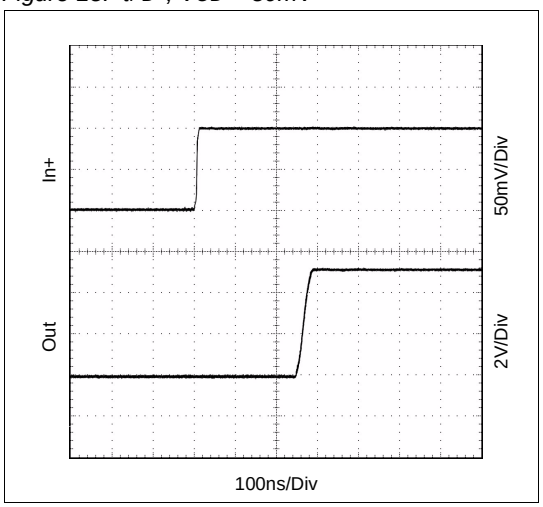
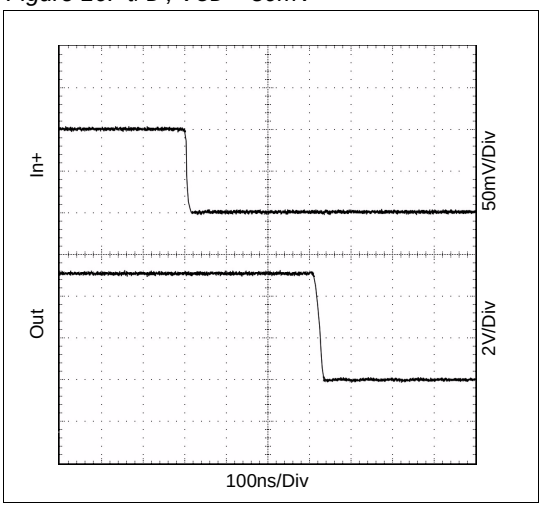



*Figure 16. $t_{PD-}$; $V_{OD}$ = 50mV*



# 8 Detailed Description

The AS1970 - AS1975 are single/dual/quad low-power, comparators. The devices operate with a supply voltage range between 2.5 and 5.5V while consuming down to 8.5µA per comparator. Their common-mode input voltage range extends 0.25V beyond each rail.

Internal hysteresis ensures clean output switching, even with slow input signals. Large internal output drivers allow rail-to-rail output swing with up to 8mA loads.

The output stage design minimizes supply-current surges while switching, virtually eliminating the power supply transients typical. The AS1970/AS1972/AS1974 push/pull output stage sinks and sources current, wheras the AS1971/AS1973/AS1975 open-drain output stage can be pulled beyond $V_{CC}$ to an absolute maximum of 5.5V > $V_{EE}$.

## Input Stage

The input common-mode voltage range extends from -0.25V to ($V_{CC}$ + 0.25V), and the comparators can operate at any differential input voltage within this voltage range. Input bias ($I_B$) current is 1.0pA (typ) if the input voltage is within the common-mode voltage range.

Inputs are protected from over-voltage by internal ESD protection diodes connected to the supply rails. As the input voltage exceeds the supply rails, these diodes become forward biased and begin to conduct and the bias currents increase exponentially as the input voltage exceeds the supply rails.

## Output Stage

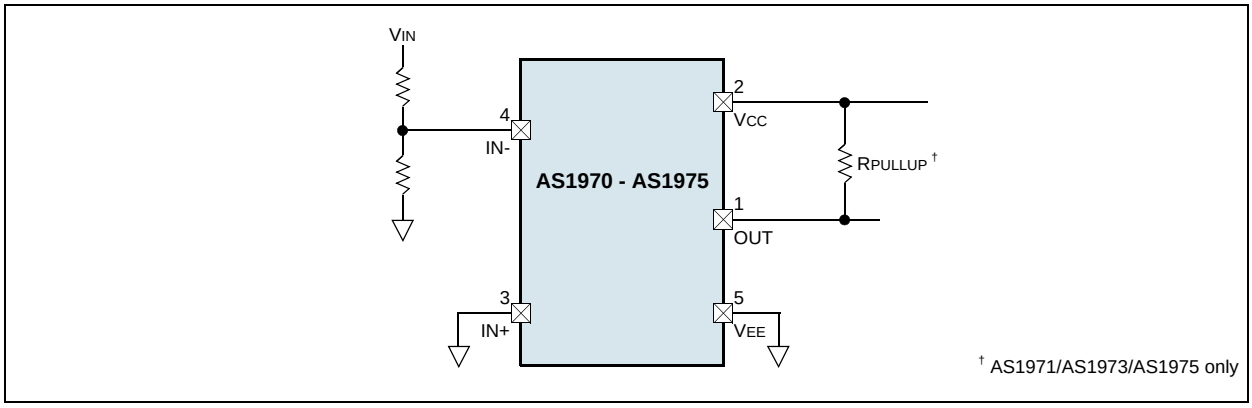
The push/pull and open-drain output stages were designed to provide rail-to-rail operation with up to 8mA loads. Even at loads of up to 8mA, the supply-current change during an output transition is extremely small (see Figure 4 on page 6). Figure 4 shows the minimal supply-current increase as the output switching frequency approaches 1MHz. This characteristic eliminates the need for power-supply filter capacitors to reduce glitches created by comparator switching currents.

Because of the unique design of its output stage, the AS1970 - AS1975 can dramatically increase battery life, even in high-speed applications.

# 9 Application Information

Figure 17 shows a typical application circuit for the AS1970 - AS1975 comparators.

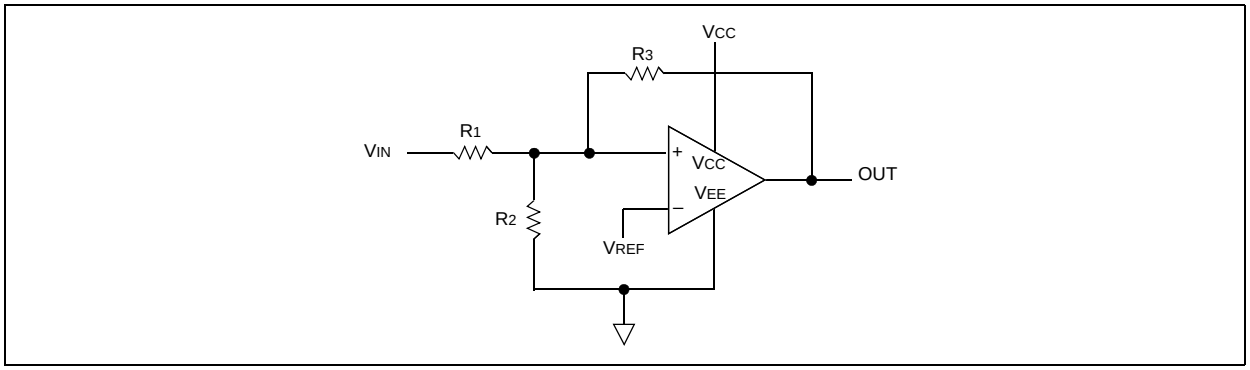
*Figure 17. Typical Application Diagram – Threshold Detector*




## Hysteresis (AS1970/AS1972/AS1974)

The *AS1970/AS1972/AS1974* have 3mV internal hysteresis. Additional hysteresis can be generated with three resistors using positive feedback (Figure 18), however this method also slows hysteresis response time.

*Figure 18. Additional Hysteresis AS1970/AS1972/AS1974*




***Resistor Selection Example***

For the circuit shown in Figure 18, the following steps can be used to calculate values for $R_1$, $R_2$, and $R_3$.

1. Select $R_3$ first. The current through $R_3$ should be at least 1µA to minimize errors caused by leakage current. The current through $R_3$ at the trip point is:

$$(V_{REF} - V_{OUT})/R_3 \quad \textit{(EQ 1)}$$

The two possible output states in solving for $R_3$ yields these two formulas:

$$R_3 = V_{REF}/1\mu A \quad \textit{(EQ 2)}$$

$$R_3 = (V_{REF} - V_{CC})/1\mu A \quad \textit{(EQ 3)}$$

For example, for $V_{REF}$ = 1.2V and $V_{CC}$ = 5V, the two $R_3$ resistor values are 1.2MΩ and 3.8MΩ. Use the smaller of the two resulting resistor values; in this case a standard 1.2MΩ resistor should be used for $R_3$.

2. Choose the hysteresis band ($V_{HB}$). For this example, use $V_{HB}$ = 50mV.
3. Calculate $R_1$ according to the following equation:

$$R_1 = R_3(V_{HB}/V_{CC}) \quad \textit{(EQ 4)}$$

Substituting the example values for $R_3$ and $V_{HB}$ gives:

$$R_1 = 1.2M\Omega(50mV/5V) = 12k\Omega$$

4. Choose the trip point for $V_{IN}$ rising ($V_{THR}$) (see page 12). This is the threshold voltage at which the AS1970 - AS1975 switches its output from low to high as $V_{IN}$ rises above the trip point. For this example, choose $V_{THR}$ = 3V.
5. Calculate $R_2$ as:

$$R_2 = 1/[V_{THR}/(V_{REF} \times R_1) - (1/R_1) - (1/R_3)] \quad \text{(EQ 5)}$$

Substituting the example values gives:

$$R_2 = 1/[3.0V/(1.2V \times 12k\Omega) - (1/12k\Omega) - (1/1.2M\Omega)] = 8.05k\Omega$$

In this example, a standard 8.2kΩ resistor should be used for $R_2$.

6. Verify the trip voltages and hysteresis as:

$$V_{THR} = V_{REF} \times R_1[(1/R_1) + (1/R_2) + (1/R_3)] \quad \text{(EQ 6)}$$

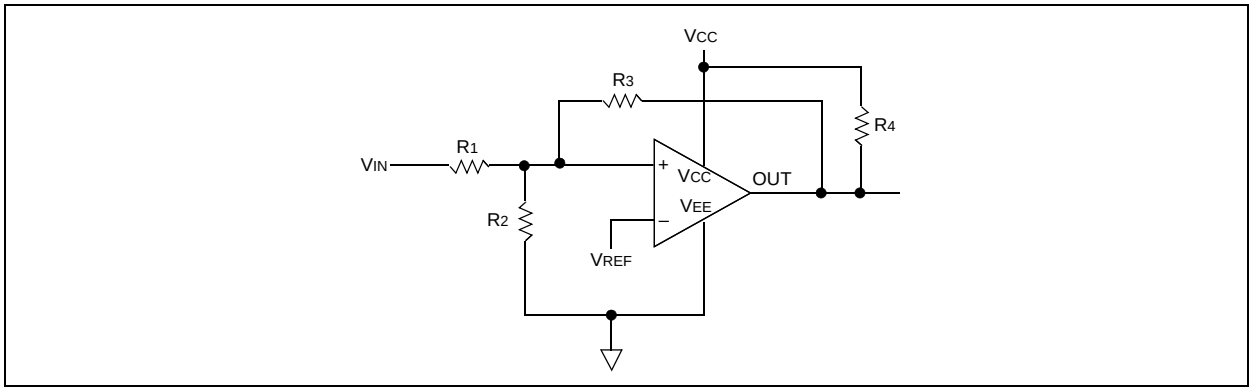
$$V_{THF} = V_{THR} - (R_1 \times V_{CC}/R_3) \quad \text{(EQ 7)}$$

$$Hysteresis = V_{THR} - V_{THF} \quad \text{(EQ 8)}$$

## Hysteresis (AS1971/AS1973/AS1975)

The AS1971/AS1973/AS1975 have 3mV internal hysteresis. Their open-drain outputs require an external pullup resistor (Figure 19), and additional hysteresis can be generated using positive feedback.

*Figure 19. Additional Hysteresis AS1971/AS1973/AS1975*




***Resistor Selection Example***

For the circuit shown in Figure 19, the following steps can be used to calculate values for $R_1$, $R_2$, $R_3$, and $R_4$:

1. Select $R_3$ according to one of:

$$R_3 = V_{REF}/500\mu A \quad \text{(EQ 9)}$$

$$R_3 = (V_{REF} - V_{CC})/500\mu A - R_4 \quad \text{(EQ 10)}$$

Use the smaller of the two resulting resistor values.

2. Choose the hysteresis band required ($V_{HB}$). For this example, use 50mV.
3. Calculate $R_1$ as:

$$R_1 = (R_3 + R_4)(V_{HB}/V_{CC}) \quad \text{(EQ 11)}$$

4. Choose the trip point for $V_{IN}$ rising ($V_{THR}$) (see page 12). This is the threshold voltage at which the comparator switches its output from low to high as $V_{IN}$ rises above the trip point.
5. Calculate $R_2$ as:

$$R_2 = 1/[V_{THR}/(V_{REF} \times R_1) - (1/R_1) - 1/(R_3 + R_4)] \quad \text{(EQ 12)}$$

6. Verify the trip voltages and hysteresis as follows:

$$V_{IN}\ rising:\ V_{THR} = V_{REF} \times R_1 \times [1/R_1 + 1/R_2 + 1/(R_3 + R_4)] \quad \text{(EQ 13)}$$

$$V_{IN}\ falling:\ V_{THF} = V_{REF} \times R_1 \times [1/R_1 + 1/R_2 + 1/(R_3+R_4)] - 1/(R_3+R_4) \times V_{CC} \quad \text{(EQ 14)}$$

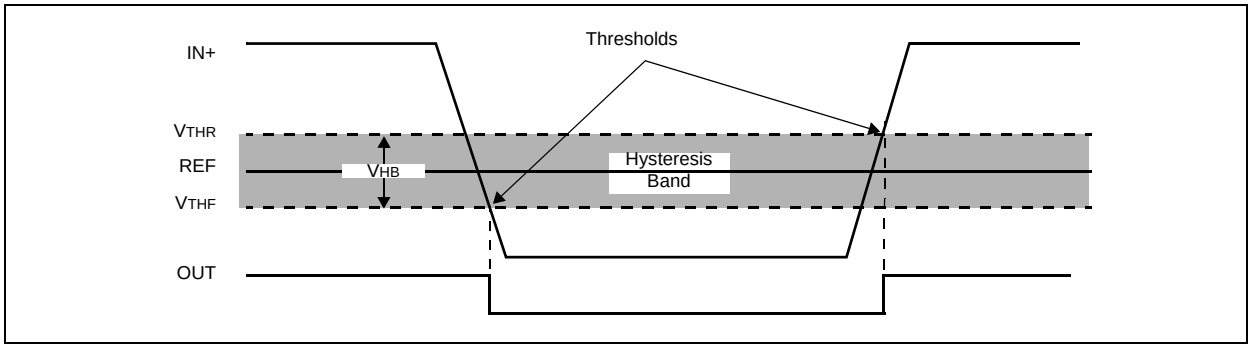
$$Hysteresis = V_{THR} - V_{THF} \quad \text{(EQ 15)}$$

## Hysteresis Band

Internal hysteresis creates two trip points (shown in Figure 20): rising input voltage ($V_{THR}$) and falling input voltage ($V_{THF}$). The area between the trip points is the hysteresis band ($V_{HB}$). When the comparator input voltages are equivalent, the hysteresis effectively causes one comparator input to move quickly past the other, thus taking the input out of the region where oscillation occurs.

In Figure 20 REF has a fixed voltage applied and IN+ is varied. If the inputs are reversed the output will be inverted.

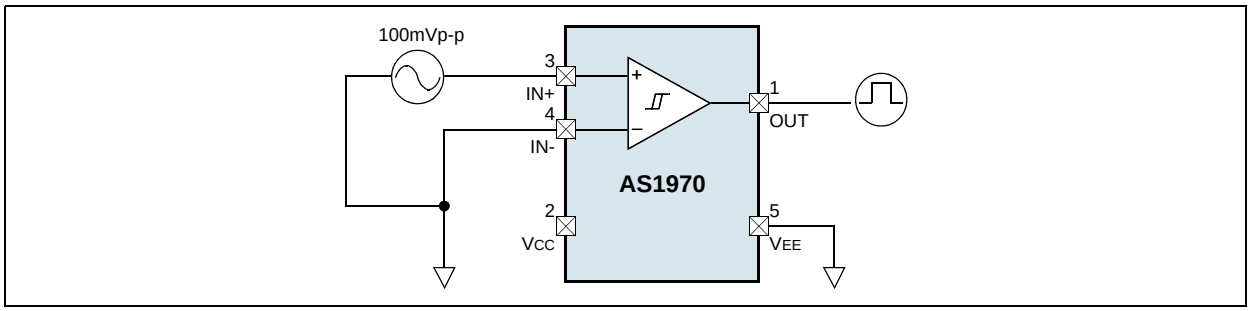
*Figure 20. Threshold Hysteresis Band*




## Zero-Crossing Detector

Figure 21 shows the AS1970 in a zero-crossing detector circuit. The inverting input is connected to ground, and the non-inverting input is connected to a 100mVp-p signal source. As the signal at the non-inverting input crosses 0V, the signal at OUT changes states.

*Figure 21. Zero-Crossing Detector*

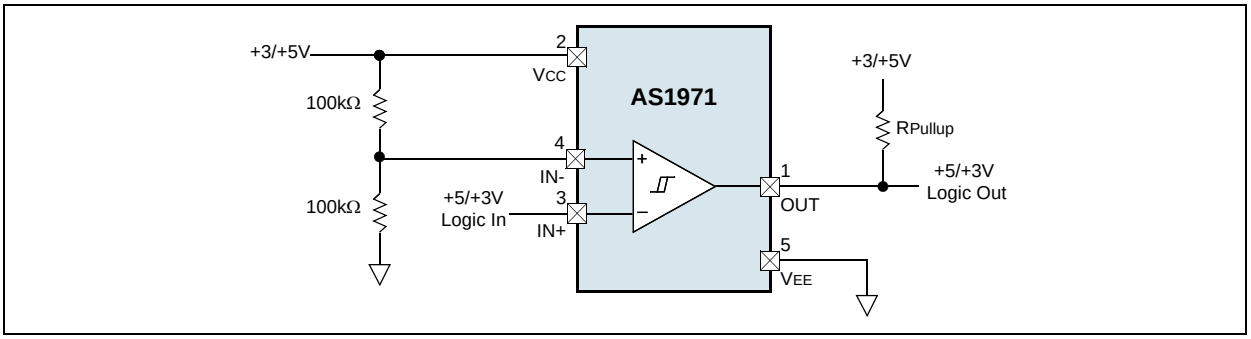



## Logic Level Translator

The comparators can be used as a 5V/3V logic translator as shown in Figure 22. The circuit in Figure 22 converts 5V- to 3V-logic levels, and provides the full 5V logic-swing without creating overvoltage on the 3V logic inputs. When the comparator is powered by a 5V supply, $R_{PULLUP}$ for the open-drain output should be connected to the +3V supply voltage.

For 3V-to-5V logic-level translations, connect the +3V supply voltage to $V_{CC}$ and the +5V supply voltage to $R_{PULLUP}$.

*Figure 22. Logic Level Translator*



## Layout Considerations

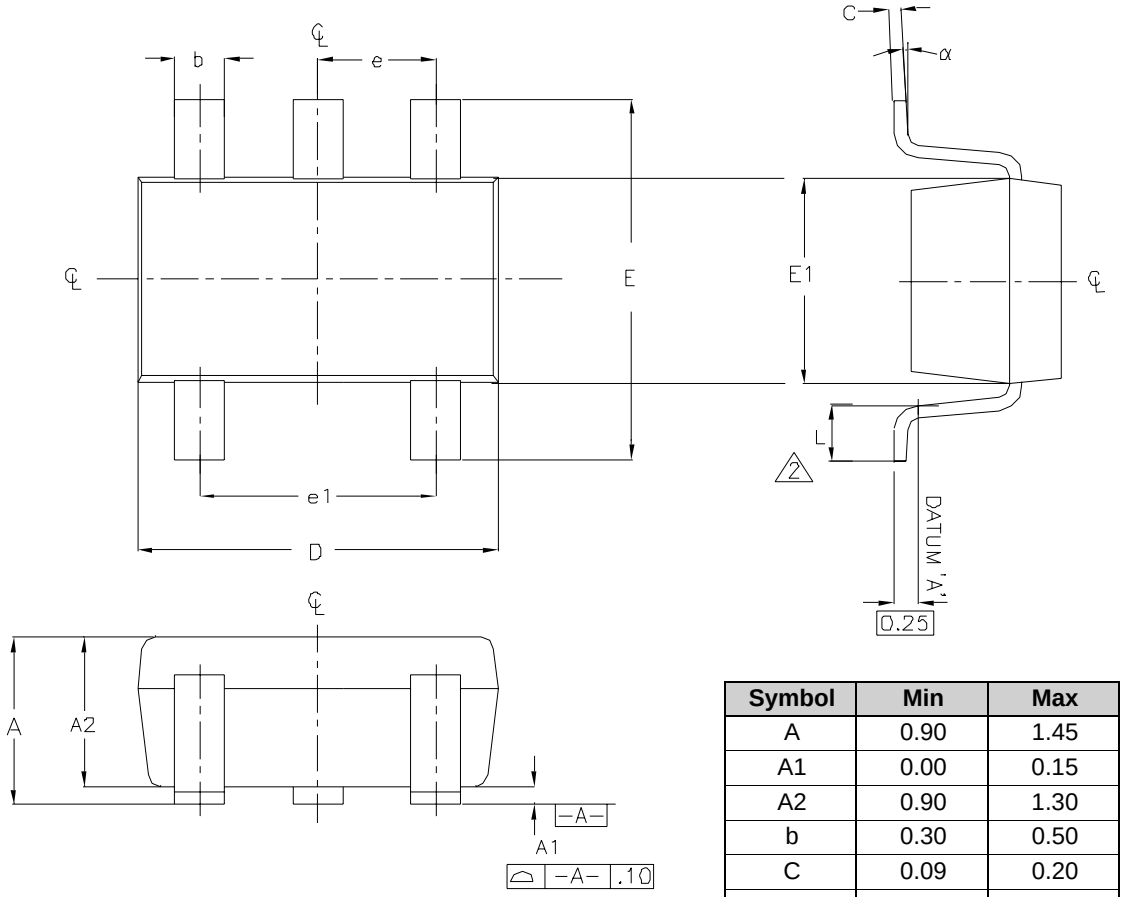
The AS1970 - AS1975 requires proper layout and design techniques for optimum performance.

- Power-supply bypass capacitors are not typically needed, although 100nF bypass capacitors should be used when supply impedance is high, when supply leads are long, or when excessive noise is expected on the supply lines.
- Minimize signal trace lengths to reduce stray capacitance.
- A ground plane and surface-mount components are recommended.

# 10 Package Drawings and Markings

The AS1970 - AS1975 are available in a 5-pin SOT23 package and an 8-pin MSOP package.

*Figure 23. 5-pin SOT23 Package*

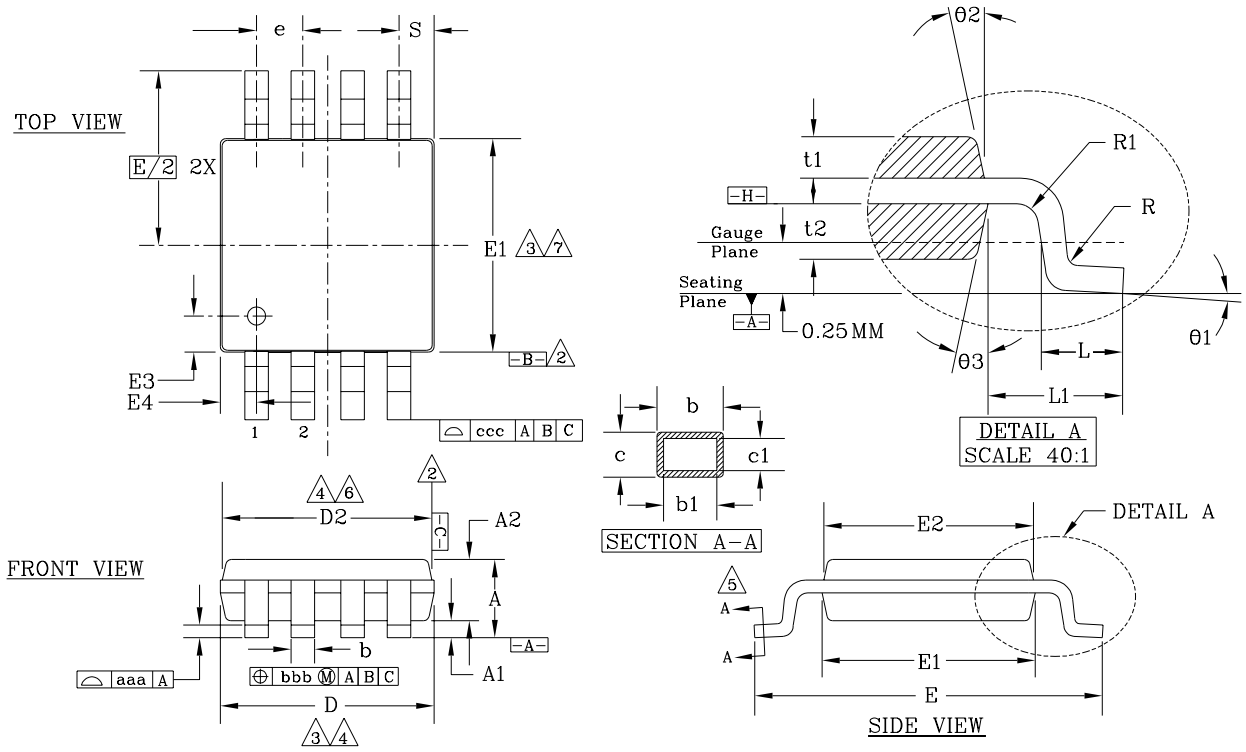



| Symbol | Min | Max |
|---|---|---|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.30 | 0.50 |
| C | 0.09 | 0.20 |
| D | 2.80 | 3.05 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.30 | 0.55 |
| e | 0.95 REF | |
| e1 | 1.90 REF | |
| α | 0º | 8º |

**Notes:**

1. Controlling dimension is millimeters.
2. Foot length measured at intercept point between datum A and lead surface.
3. Package outline exclusive of mold flash and metal burr.
4. Package outline inclusive of solder plating.
5. Meets *JEDEC MO178*.

*Figure 24. 8-pin MSOP Package*

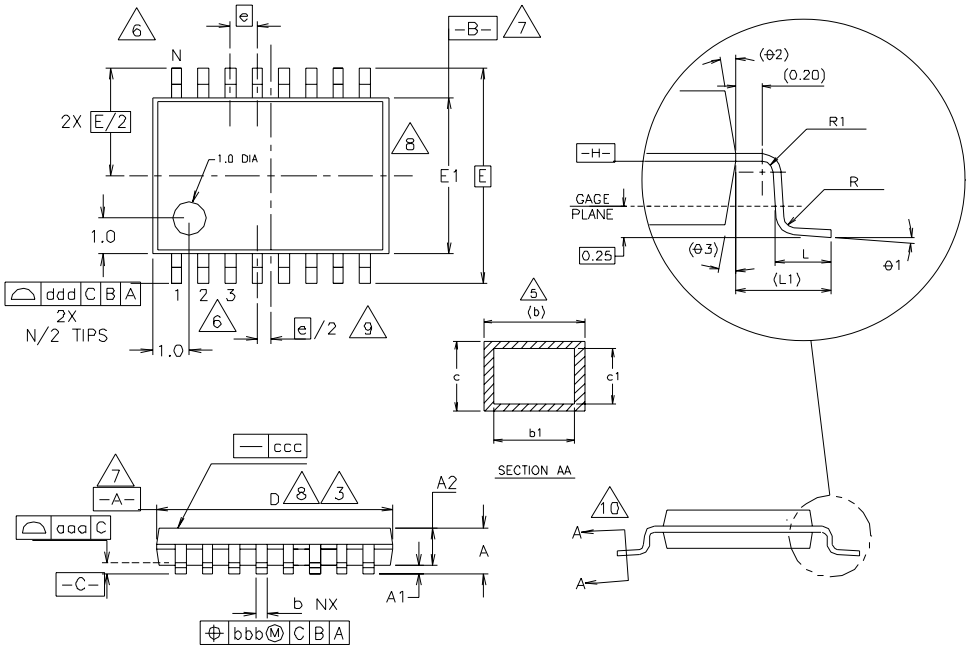



| Symbol | Typ | ±Tol | Symbol | Typ | ±Tol |
|---|---|---|---|---|---|
| A | 1.10 | Max | b | 0.33 | +0.07/-0.08 |
| A1 | 0.10 | ±0.05 | b1 | 0.30 | ±0.05 |
| A2 | 0.86 | ±0.08 | c | 0.18 | ±0.05 |
| D | 3.00 | ±0.10 | c1 | 0.15 | +0.03/-0.02 |
| D2 | 2.95 | ±0.10 | θ1 | 3.0° | ±3.0° |
| E | 4.90 | ±0.15 | θ2 | 12.0° | ±3.0° |
| E1 | 3.00 | ±0.10 | θ3 | 12.0° | ±3.0° |
| E2 | 2.95 | ±0.10 | L | 0.55 | ±0.15 |
| E3 | 0.51 | ±0.13 | L1 | 0.95 BSC | – |
| E4 | 0.51 | ±0.13 | aaa | 0.10 | – |
| R | 0.15 | +0.15/-0.08 | bbb | 0.08 | – |
| R1 | 0.15 | +0.15/-0.08 | ccc | 0.25 | – |
| t1 | 0.31 | ±0.08 | e | 0.65 BSC | – |
| t2 | 0.41 | ±0.08 | S | 0.525 BSC | – |

**Notes:**

1. All dimensions are in millimeters and all angles in degrees (unless otherwise noted).
2. Datums B and C to be determined at datum plane H.
3. Dimensions D and E1 are to be determined at datum plane H.
4. Dimensions D2 and E2 are for the top package; dimensions D and E1 are for the bottom package.
5. Cross section A-A to be determined at 0.13 to 0.25mm from the leadtip.
6. Dimensions D and D2 do not include mold flash, protrusion, or gate burrs.
7. Dimensions E1 and E2 do not include interlead flash or protrusion.

*Figure 25. 14-pin TSSOP Package*




| Symbol | 0.65mm Lead Pitch [1, 2] | | | Note | Symbol | 0.65mm Lead Pitch [1, 2] | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Nom | Max | | | Min | Nom | Max | |
| A | - | - | 1.10 | | θ1 | 0º | - | 8º | |
| A1 | 0.05 | - | 0.15 | | L1 | | 1.0 Ref | | |
| A2 | 0.85 | 0.90 | 0.95 | | aaa | | 0.10 | | |
| L | 0.50 | 0.60 | 0.75 | | bbb | | 0.10 | | |
| R | 0.09 | - | - | | ccc | | 0.05 | | |
| R1 | 0.09 | - | - | | ddd | | 0.20 | | |
| b | 0.19 | - | 0.30 | 5 | e | | 0.65 BSC | | |
| b1 | 0.19 | 0.22 | 0.25 | | θ2 | | 12º Ref | | |
| c | 0.09 | - | 0.20 | | θ3 | | 12º Ref | | |
| c1 | 0.09 | - | 0.16 | | | | | | |
| **Variations** | | | | | | | | | |
| D | 4.90 | 5.00 | 5.10 | 3, 8 | e | | 0.65 BSC | | |
| E1 | 4.30 | 1.40 | 4.50 | 4, 8 | N | | 14 | | 6 |
| E | | 6.4 BSC | | | | | | | |

**Notes:**

1. All dimensions are in millimeters; angles in degrees.
2. Dimensions and tolerancing per *ASME Y14.5M-1994*.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of dimension b at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm for 0.5mm pitch packages.
6. Terminal numbers shown are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side. For variations with an odd number of leads per package, the center lead must be coincident with the package centerline, datum A.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

# 11 Ordering Information

The comparators are available as the standard products shown in Table 5.

*Table 5. Ordering Information*

| Model | Marking | Description | Delivery Form | Package |
|---|---|---|---|---|
| AS1970-T | ASI6 | Low-Voltage Single Comparator, Push/Pull | Tape and Reel | 5-pin SOT23 |
| AS1971-T | ASI7 | Low-Voltage Single Comparator, Open-Drain | Tape and Reel | 5-pin SOT23 |
| AS1972 | 989 | Low-Voltage Dual Comparator, Push/Pull | Tubes | 8-pin MSOP |
| AS1972-T | 989 | Low-Voltage Dual Comparator Push/Pull | Tape and Reel | 8-pin MSOP |
| AS1973 | 990 | Low-Voltage Dual Comparator, Open-Drain | Tubes | 8-pin MSOP |
| AS1973-T | 990 | Low-Voltage Dual Comparator, Open-Drain | Tape and Reel | 8-pin MSOP |
| AS1974 | AS1974 | Low-Voltage Quad Comparator, Push/Pull | Tubes | 14-pin TSSOP |
| AS1974-T | AS1974 | Low-Voltage Quad Comparator, Push/Pull | Tape and Reel | 14-pin TSSOP |
| AS1975 | AS1975 | Low-Voltage Quad Comparator, Open-Drain | Tubes | 14-pin TSSOP |
| AS1975-T | AS1975 | Low-Voltage Quad Comparator, Open-Drain | Tape and Reel | 14-pin TSSOP |

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