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AS1335

1.5A, 1.5MHz, Synchronous DC/DC Step-Down Converter

1 General Description

The AS1335 is a high-efficiency, constant-frequency synchronous buck converter available in a fixed or an adjustable output voltage version. The wide input voltage range (2.6V to 5.25V), the high output current (up to 1.5A) and minimal external component requirements make the AS1335 perfect for any single Li-Ion battery-powered application.

Typical supply current with no load is 400µA and decreases to ≤1µA in shutdown mode. The highly efficient duty cycle (100%) provides low dropout operation, prolonging battery life in portable systems.

The device also offers a power-ok signal with a 215ms delay, which can be reseted or delayed further via the RSI pin.

An internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The internally fixed switching frequency (1.5MHz) allows for the use of small surface mount external components.

The AS1335 is available in a 10-pin TDFN 3x3mm package.

2 Key Features

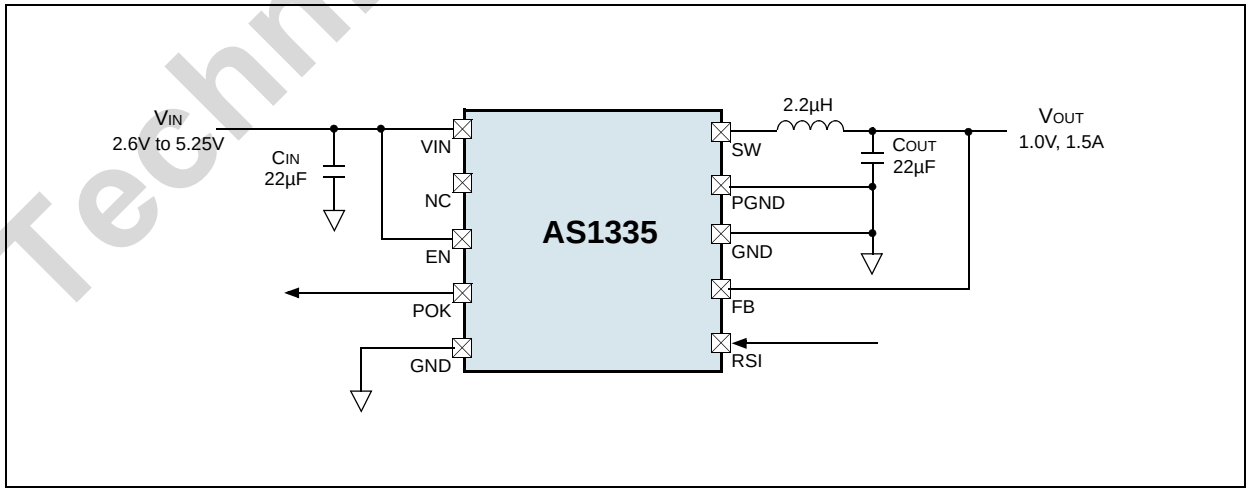
- High Efficiency: Up to 96%
- Output Current: 1.5A
- Input Voltage Range: 2.6V to 5.25V
- Output Voltage Range: 0.6V to VIN
- Constant Frequency Operation: 1.5MHz
- No Schottky Diode Required
- Power OK with 215ms delay
- Low Dropout Operation: 100% Duty Cycle
- Low Quiescent Supply Current: 400µA
- Shutdown Mode Supply Current: ≤1µA
- Current Mode Operation for Excellent Line/Load Transient Response
- Thermal Protection
- 10-pin TDFN 3x3mm Package

3 Applications

The device is ideal for mobile communication devices, laptops and PDAs, ultra-low-power systems, threshold detectors/discriminators, telemetry and remote systems, medical instruments, or any other space-limited application with low power-consumption requirements.

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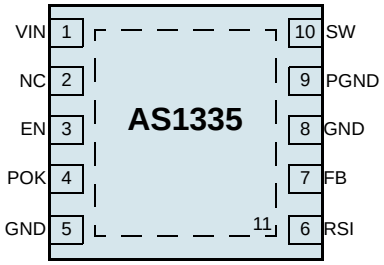
Figure 1. AS1335 - Typical Application Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	VIN	**Positive Supply Voltage**. This pin must be closely decoupled to PGND with a ≥ 22µF ceramic capacitor.
2	NC	**Not Connected.**
3	EN	**Enable Input**. Driving this pin above 1.4V enables the device. Driving this pin below 0.3V puts the device in shutdown mode. In shutdown mode all functions are disabled, drawing ≤1µA supply current. **Note:** This pin should not be left floating.
4	POK	**Power-OK Output.** Open-drain output with 215ms delay. Connect a 100kΩ pull-up resistor to VOUT or pin VIN for logic levels. Leave this pin unconnected if the Power-OK feature is not used. LOW Signal: Out of regulation HIGH signal: Within Regulation (after 215ms delay)
5	GND	**Analog Ground.**
6	RSI	**Reset Input for POK.** This input resets the 215ms timer of the POK signal. As long as RSI is low the POK signal will work as described above. A high input to RSI will reset the 215ms POK timer and delay the signal as long as RSI stays high. A RSI low-to-high transition restarts the 215ms counter as long as the output voltage is within regulation. **Note:** Do not leave this pin floating.
7	FB	**Feedback Pin**. Feedback input to the gm error amplifier. Connect a resistor divider tap to this pin. The output can be adjusted from 0.6V to 5.25V by VOUT = 0.6V[1+(R1/R2)]. If the fixed output voltage version is used, connect this pin to VOUT.
8	GND	**Analog Ground.** GND and PGND should only have one point connection.
9	PGND	**Power-Ground.** Connect all power grounds to this pin.
10	SW	**Switch Node Connection to Inductor.** This pin connects to the drains of the internal main and synchronous power MOSFET switches.
11		**Exposed Pad.** The exposed pad must be connected to PGND. Ensure a good connection to the PCB to achieve optimal thermal performance.

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5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VIN to GND	-0.3	6	V	
SW to GND	-0.3	V_{IN} + 0.3	V	
EN, FB to GND	-0.3	V_{IN}	V	
P-Channel Switch Source Current (DC)		1.5	A	
N-Channel Switch Source Current (DC)		1.5	A	
Peak SW Sink and Source Current		3	A	
Thermal Resistance Θ_{JA}		36.7	ºC/W	on PCB
Latch-Up	-100	100	mA	*@85°C, JEDEC 78*
Electrostatic Discharge	2		kV	*HBM MIL-Std. 883E 3015.7* methods
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Junction Temperature		125	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

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6 Electrical Characteristics

V_{IN} = EN = 3.6V, V_{OUT} = V_{IN}-0.5V, T_{AMB} = -40°C to +85°C, typ. values @ T_{AMB} = +25ºC (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.6		5.25	V
I_Q	Quiescent Supply Current[1]	Normal Operation; V_{FB} = 0.5V or V_{OUT} = 90% of regulated output voltage, I_{LOAD} = 0 A		300	400	µA
I_{OUT}	Output Current RMS			1.5		A
I_{SHDN}	Shutdown Current	Shutdown Mode; V_{EN} = 0V, V_{IN} = 4.2V		0.1	1	µA
Regulation						
V_{OUT}	Regulated Output Voltage	fixed V_{OUT}	0.975	1.0	1.025	V
		adjustable V_{OUT}	0.6		V_{IN} - 0.5V	V
V_{FB}	Regulated Feedback Voltage[2,3]	T_{AMB} = +25°C	0.5880	0.6	0.6120	V
		T_{AMB} = -40°C to +85°C	0.5850	0.6	0.6150	
I_{FB}	Feedback Current[3]		-30		+30	nA
ΔV_{LNR}	Reference Voltage Line Regulation	V_{IN} = 2.6V to 5.25V		100		mV
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	I_{LOAD} = 0A to 1.5A		100		mA
DC-DC Switches						
I_{PK}	Peak Inductor Current	V_{IN} = 3V, V_{FB} = 0.5V or V_{OUT} = 90% of regulated output voltage, Duty Cycle < 35%		2.4		A
R_{PFET}	P-Channel FET $R_{DS(ON)}$	I_{LSW} = 100mA		0.4		Ω
R_{NFET}	N-Channel FET $R_{DS(ON)}$	I_{LSW} = -100mA		0.35		Ω
I_{LSW}	SW Leakage	V_{EN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V	-1	0.01	+1	µA
Enable						
V_{IH}	Logic Input Threshold	Input High	1.4			V
V_{IL}		Input Low			0.4	
I_{EN}	EN Leakage Current	V_{IN} = 3.6V, V_{EN} = 0V to 3.6V	-1	0.01	+1	µA
Power-OK Output						
V_{POK}	Power Good Low Voltage Threshold	Rising	89.5	92	94.5	% V_{OUT}
		Falling	85	88	91	
	Power Good High Voltage Threshold	Rising	108.2	110.7	113.2	% V_{OUT}
		Falling	104	107	110	
t_{DELAY}	POK Delay Time		150	215	275	ms
V_{OL}	POK Output Voltage Low	I_{SINK} = 1mA, V_{FB} = 0.7V			0.3	V

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Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{POK}	POK Output Leakage Current	V_{POK} = V_{IN} = 3.6V		0.01	1	µA
Oscillator						
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V or V_{OUT} = 100% of regulated output voltage	1.2	1.5	1.8	MHz
Thermal Shutdown						
	Thermal Shutdown			150		°C
	Thermal Shutdown Hysteresis			25		°C

1. The dynamic supply current is higher due to the gate charge delivered at the switching frequency. The Quiescent Current is measured while the DC-DC Converter is not switching.
2. The device is tested in a proprietary test mode where V_{FB} is connected to the output of the DC/DC converter.
3. Only valid for the adjustable version;

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

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7 Typical Operating Characteristics

VOUT = 1.0V, IOUT = *100mA,* TAMB = +25°C (unless otherwise specified).

Figure 3. Efficiency vs. Output Current, VOUT = 1.0V

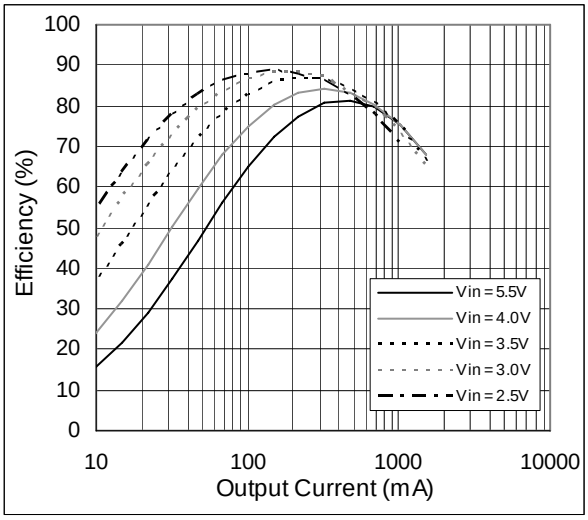


Figure 4. Efficiency vs. Output Current, VOUT = 1.5V

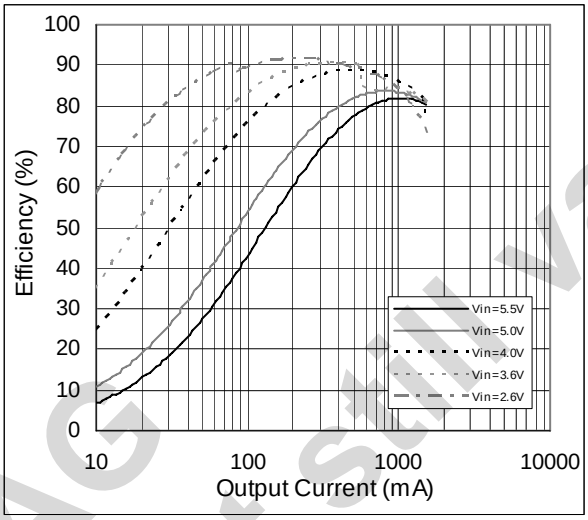


Figure 5. Efficiency vs. Output Current, VOUT = 2.5V

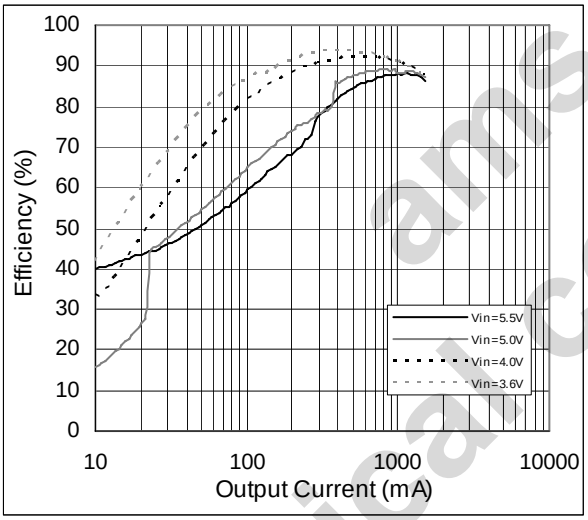


Figure 6. Efficiency vs. Output Current, VOUT = 3.0V

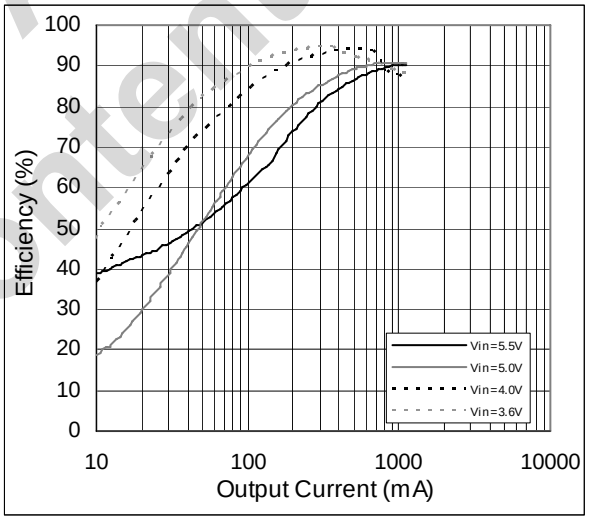


Figure 7. Efficiency vs. Output Current, VOUT = 3.5V

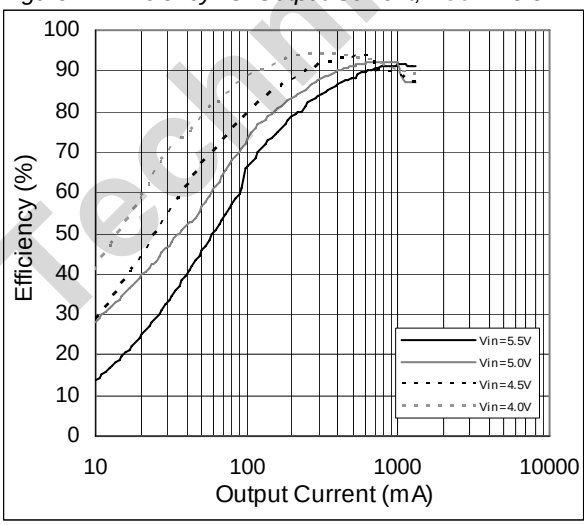
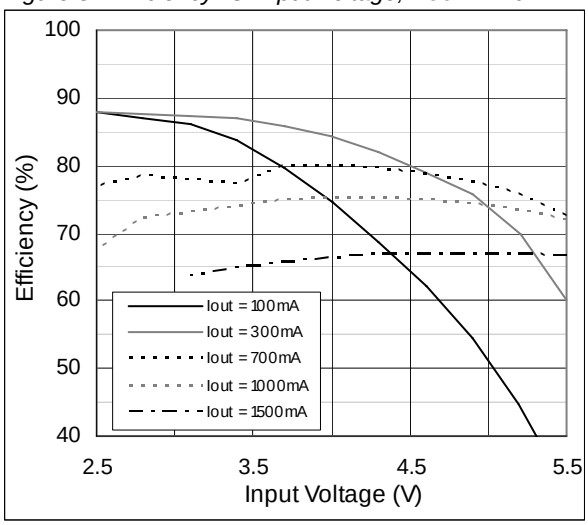


Figure 8. Efficiency vs. Input Voltage, VOUT = 1.0V



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Figure 9. Efficiency vs. Input Voltage, VOUT = 3.5V

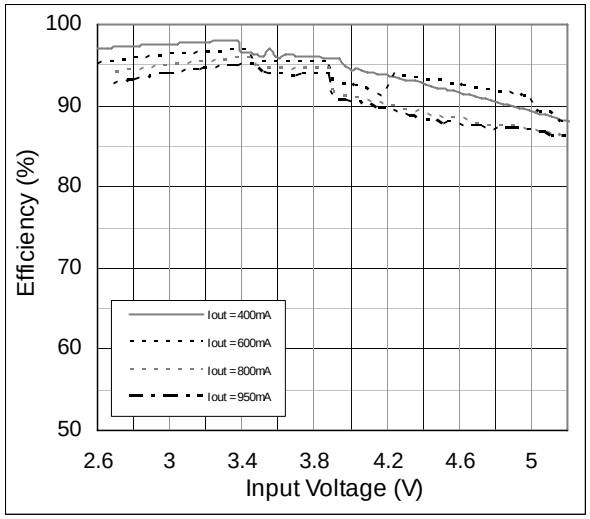


Figure 10. Load Regulation, VOUT = 1.0V

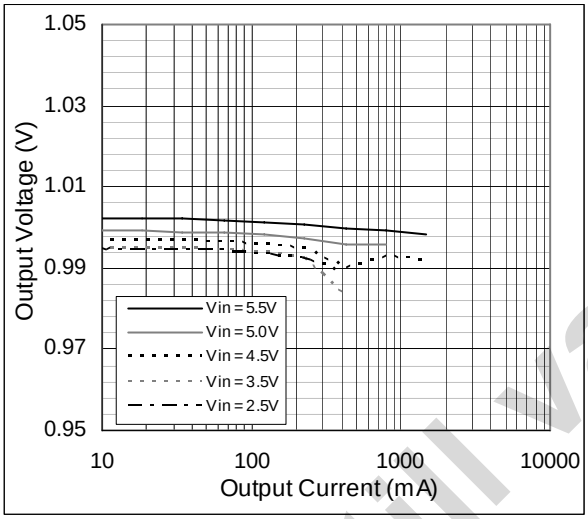


Figure 11. Load Regulation, VOUT = 1.5V

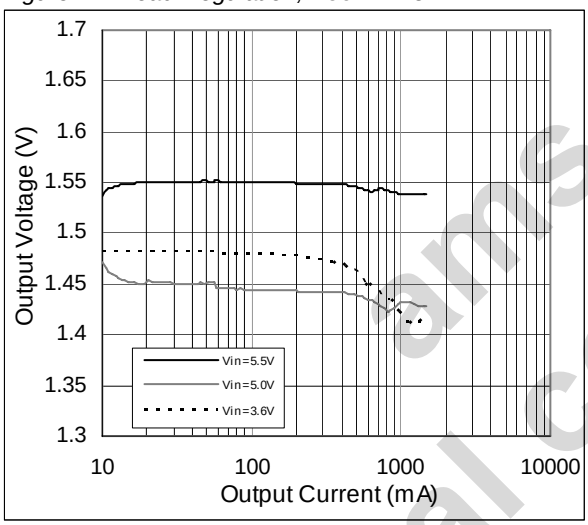


Figure 12. Line Regulation, VOUT vs. VIN;

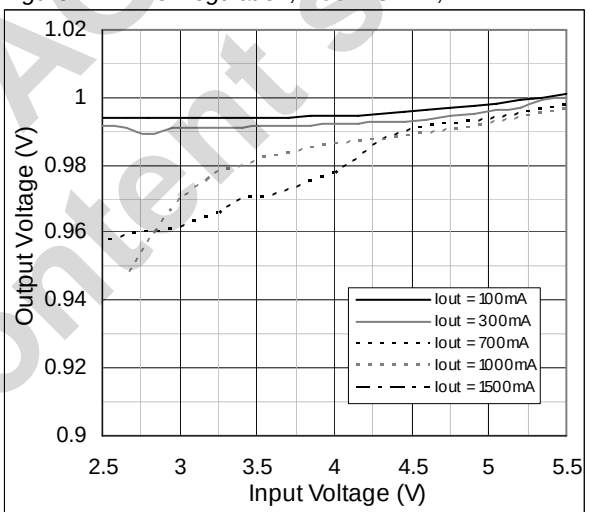


Figure 13. Load Step 40mA to 500mA; VIN = 4V

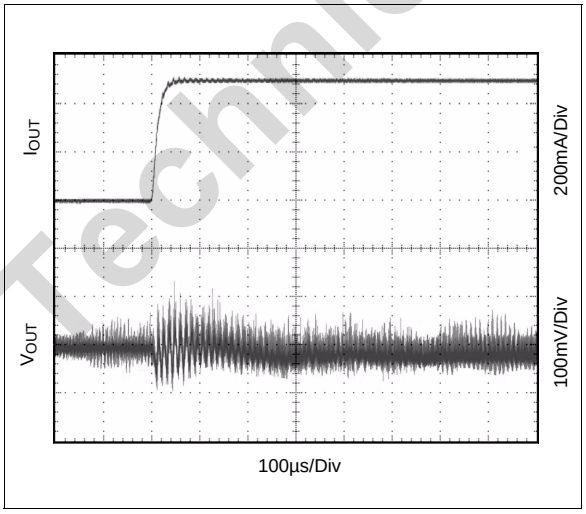
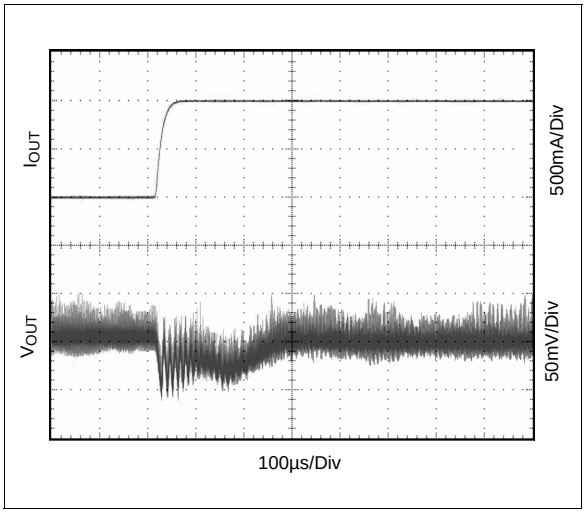


Figure 14. Load Step 40mA to 1A; VIN = 4V



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Figure 15. Shutdown Response; V_{IN} = 3.4V

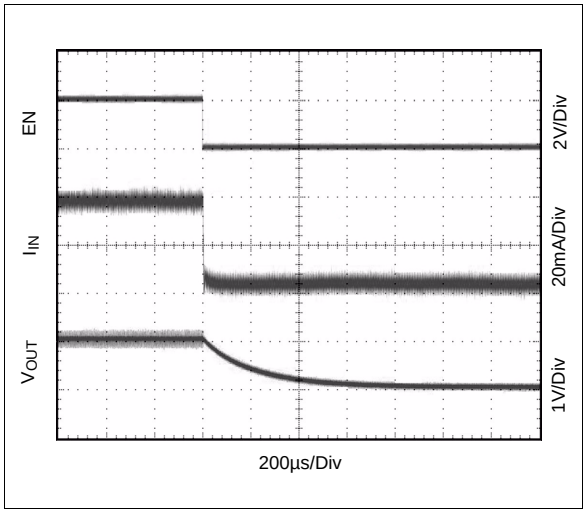


Figure 16. Startup Response; V_{IN} = 3.4V

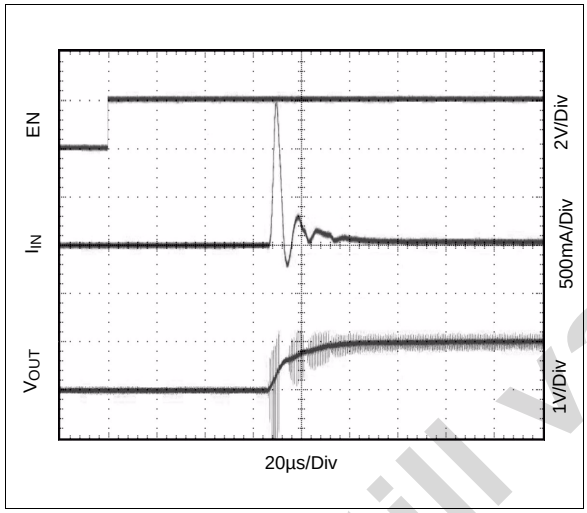
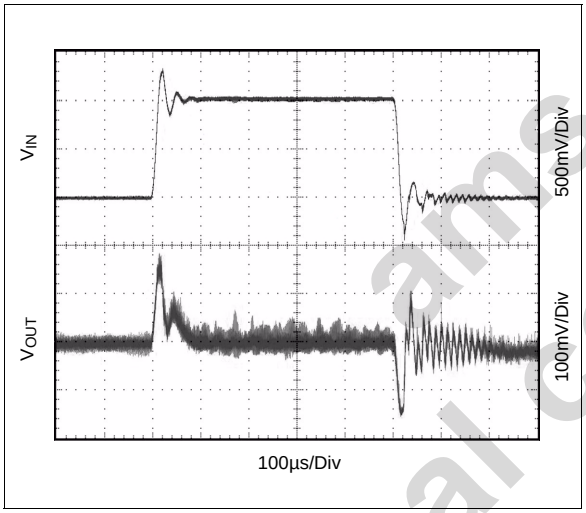


Figure 17. Line Transient Response; V_{IN} = 3.5V to 4.5V, I_{OUT} = 500mA

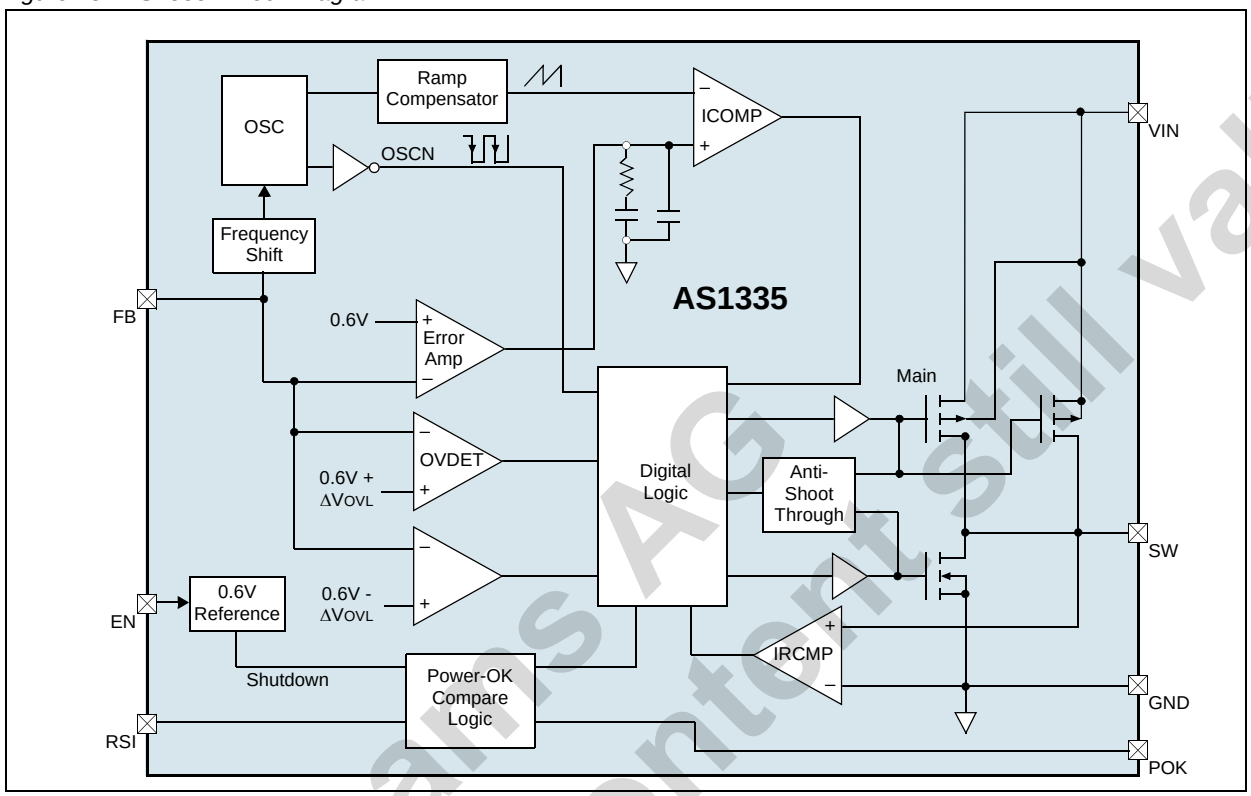


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8 Detailed Description

The AS1335 is a high-efficiency buck converter that uses a constant-frequency current-mode architecture. The device contains two internal MOSFET switches and is available with a user-adjustable output voltage.

Figure 18. AS1335 - Block Diagram



Main Control Loop

During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch. This switch is turned off when the current comparator (ICOMP) resets the RS latch. The peak inductor current (I_{PK}) at which ICOMP resets the RS latch, is controlled by the error amplifier. When I_{LOAD} increases, V_{FB} decreases slightly relative to the internal 0.6V reference, causing the error amplifier's output voltage to increase until the average inductor current matches the new load current.

When the top MOSFET is off, the bottom MOSFET is turned on until the inductor current starts to reverse as indicated by the current reversal comparator (IRCMP), or the next clock cycle begins. The over-voltage detection comparator (OVDET) guards against transient overshoots >7.8% by turning the main switch off and keeping it off until the transient is removed.

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Short-Circuit Protection

This frequency reduction ensures that the inductor current has more time to decay, thus preventing runaway conditions. f_{OSC} will progressively increase to 1.5MHz when V_{OUT} > 0V or V_{FB} > 0V.

Dropout Operation

The AS1335 is working with a low input-to-output voltage difference by operating at 100% duty cycle. In this state, the PMOS is always on. This is particularly useful in battery-powered applications with a 3.3V output.

The AS1335 allows the output to follow the input battery voltage as it drops below the regulation voltage. The quiescent current in this state rises minimally to only 400µA (max), which aids in extending battery life. This dropout (100% duty-cycle) operation achieves long battery life by taking full advantage of the entire battery range.

The input voltage requires maintaining regulation and is a function of the output voltage and the load. The difference between the minimum input voltage and the output voltage is called the dropout voltage. The dropout voltage is therefore a function of the on-resistance of the internal PMOS ($R_{DS(ON)PMOS}$) and the inductor resistance (DCR) and this is proportional to the load current.

Note: At low V_{IN} values, the $R_{DS(ON)}$ of the P-channel switch increases (see Electrical Characteristics on page 4). Therefore, power dissipation should be taken in consideration.

Shutdown

Connecting EN to GND or logic low places the AS1335 in shutdown mode and reduces the supply current to 0.1µA. In shutdown the control circuitry and the internal NMOS and PMOS turn off and SW becomes high impedance disconnecting the input from the output. The output capacitance and load current determine the voltage decay rate. For normal operation connect EN to V_{IN} or logic high.

Note: Pin EN should not be left floating.

Power-OK Functionality

The AS1335's power-ok circuitry offers a 215ms delayed power-ok signal. As long as the output voltage is outside of the power-ok regulation window the POK pin drives an open-drain low signal. As soon as the output voltage is within the regulation window, the internal open-drain MOSFET is turned off and the POK pin can be externally pulled to high. The output of the power-ok signal is delayed by 215ms.

RSI Signal

With the RSI signal the internal power-ok timer can be reseted or delayed. As long as the input to RSI is high the POK signal remains low, regardless of the output voltage condition.

Thermal Shutdown

Due to its high-efficiency design, the AS1335 will not dissipate much heat in most applications. However, in applications where the AS1335 is running at high ambient temperature, uses a low supply voltage, and runs with high duty cycles (such as in dropout) the heat dissipated may exceed the maximum junction temperature of the device.

As soon as the junction temperature reaches approximately 150ºC the AS1335 goes in thermal shutdown. In this mode the internal PMOS & NMOS switch are turned off. The device will power up again, as soon as the temperature falls below +125°C again.

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9 Application Information

The AS1335 is perfect for mobile communications equipment, LED matrix displays, bar-graph displays, instrument-panel meters, dot matrix displays, set-top boxes, white goods, professional audio equipment, medical equipment, industrial controllers to name a few applications.

Adjustable Output Voltage

For the fixed output voltage (V_{OUT}=1.0V) connect pin FB to V_{OUT} (see Figure 19). For the adjustable output voltage version connect a voltage divider to pin FB (see Figure 20).

The voltage divider from V_{OUT} to GND programs the output voltage from 0.6V to 5.25V via pin FB as:

$$V_{OUT} = 0.6V(1 + (R_1/R_2)) \quad \text{(EQ 1)}$$

Figure 19. AS1335 - Step-Down Converter, Single Li-Ion to 1.0V / 1.5A fixed Output

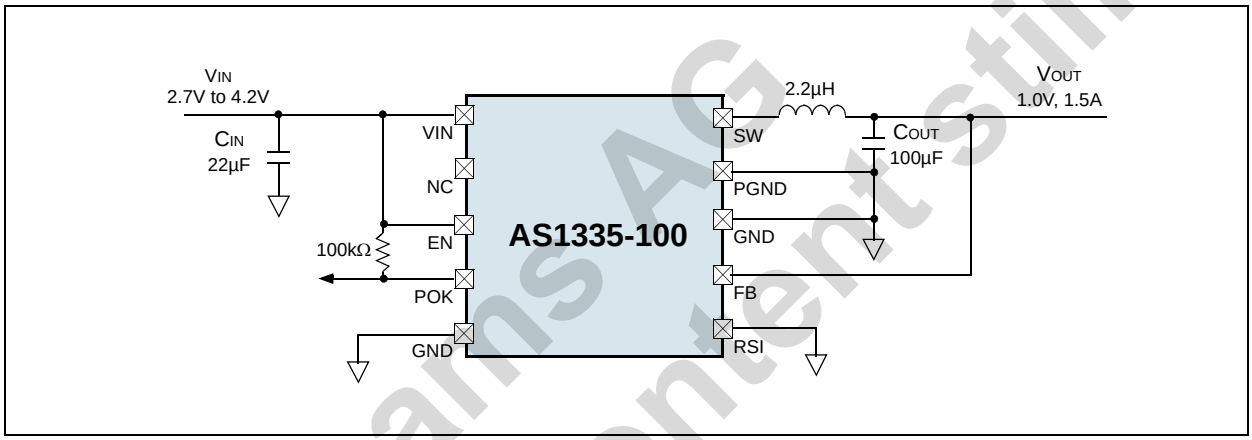
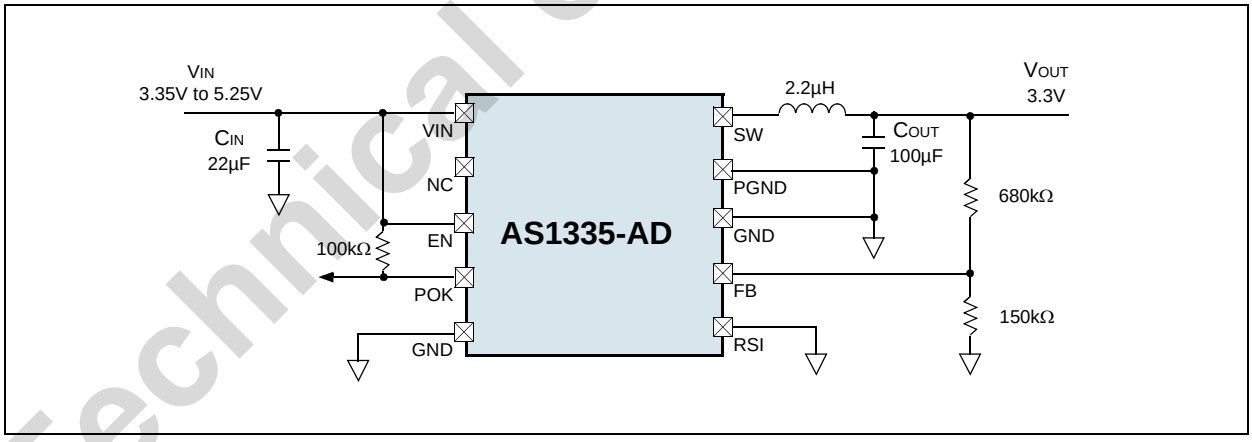


Figure 20. AS1335 - Step-Down Converter, Single Li-Ion to 3.3V adjustable Output



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External Component Selection

Inductor Selection

For most applications the value of the external inductor should be in the range of 2.2µH to 4.7µH as the inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

In Equation (EQ 2) the maximum inductor current in PWM mode under static load conditions is calculated. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation (EQ 3). This is recommended because the inductor current will rise above the calculated value during heavy load transients.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad \textit{(EQ 2)}$$

$$I_{LMAX} = I_{OUTMAX} + \frac{\Delta I_L}{2} \quad \textit{(EQ 3)}$$

f = Switching Frequency (1.5 MHz typical)
L = Inductor Value
I_{Lmax} = Maximum Inductor current
ΔI_L = Peak to Peak inductor ripple current
The recommended starting point for setting ripple current is ΔI_L = 600mA (40% of 1.5A).

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 1.8A rated inductor should be sufficient for most applications (1.5A + 300mA).

Note: For highest efficiency, a low DC-resistance inductor is recommended.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the DC resistance and the following frequency-dependent components:

1. The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies).
2. Additional losses in the conductor from the skin effect (current displacement at high frequencies).
3. Magnetic field losses of the neighboring windings (proximity effect).
4. Radiation losses.

Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the AS1335 allows the use of tiny ceramic capacitors. Because of their lowest output voltage ripple low ESR ceramic capacitors are recommended. X7R or X5R dielectric output capacitor are recommended.

At high load currents, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad \textit{(EQ 4)}$$

While operating in PWM mode the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

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$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad \text{(EQ 5)}$$

Higher value, low cost ceramic capacitors are available in very small case sizes, and their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. Because the AS1335 control loop is not dependant on the output capacitor ESR for stable operation, ceramic capacitors can be used to achieve very low output ripple and accommodate small circuit size.

At light loads, the converter operates in powersave mode and the output voltage ripple is in direct relation to the output capacitor and inductor value used. Larger output capacitor and inductor values minimize the voltage ripple in powersave mode and tighten DC output accuracy in powersave mode.

Input Capacitor Selection

In continuous mode, the source current of the PMOS is a square wave of the duty cycle VOUT/VIN. To prevent large voltage transients while minimizing the interference with other circuits caused by high input voltage spikes, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given as:

$$I_{RMS} = I_{MAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{(EQ 6)}$$

where the maximum average output current IMAX equals the peak current minus half the peak-to-peak ripple current, IMAX = ILIM - ΔIL/2

This formula has a maximum at VIN = 2VOUT where IRMS = IOUT/2. This simple worst-case condition is commonly used for design because even significant deviations only provide negligible affects.

The input capacitor can be increased without any limit for better input voltage filtering. Take care when using small ceramic input capacitors. When a small ceramic capacitor is used at the input, and the power is being supplied through long wires, such as from a wall adapter, a load step at the output, or VIN step on the input, can induce ringing at the VIN pin. This ringing can then couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings.

Ceramic Input and Output Capacitors

When choosing ceramic capacitors for CIN and COUT, the X5R or X7R dielectric formulations are recommended. These dielectrics have the best temperature and voltage characteristics for a given value and size. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and therefore should not be used.

Table 4. Recommended External Components

Name	Part Number	Value	Rating	Type	Size	Manufacturer
COUT	T520B107M006ATE040	100µF	6.3V	Tantal	B (3.5x2.8x1.9mm)	Kemet www.kemet.com
CIN, COUT	GRM21BR60J226ME39	22µF	6.3V	X5R	0805	Murata www.murata.com
L	MOS6020-222ML	2.2µH	3.26A	35mΩ	6.8x6.0x2.4mm	Coilcraft www.coilcraft.com
	MOS6020-472ML	4.7µH	1.82A	50mΩ	6.8x6.0x2.4mm	

Because ceramic capacitors lose a lot of their initial capacitance at their maximum rated voltage, it is recommended that either a higher input capacity or a capacitance with a higher rated voltage is used.

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Efficiency

The efficiency of a switching regulator is equivalent to:

$$Efficiency = (P_{OUT}/P_{IN})x100\% \quad (EQ\ 7)$$

For optimum design, an analysis of the AS1335 is needed to determine efficiency limitations and to determine design changes for improved efficiency. Efficiency can be expressed as:

$$Efficiency = 100\% - (L_1 + L_2 + L_3 + ...) \quad (EQ\ 8)$$

Where:

L_1, L_2, L_3, etc. are the individual losses as a percentage of input power.

Althought all dissipative elements in the circuit produce losses, those four main sources should be considered for efficiency calculation:

Input Voltage Quiescent Current Losses

The V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents.

I²R Losses

Most of the efficiency loss at medium to high load currents are attributed to I²R loss, and are calculated from the resistances of the internal switches (R_{SW}) and the external inductor (R_L). In continuous mode, the average output current flowing through inductor L is split between the internal switches. Therefore, the series resistance looking into the SW pin is a function of both NMOS & PMOS $R_{DS(ON)}$ as well as the the duty cycle (DC) and can be calculated as follows:

$$R_{SW} = (R_{DS(ON)PMOS})(DC) + (R_{DS(ON)NMOS})(1 - DC) \quad (EQ\ 9)$$

The $R_{DS(ON)}$ for both MOSFETs can be obtained from the Electrical Characteristics on page 4. Thus, to obtain I²R losses calculate as follows:

$$I^2R\ losses = I_{OUT}^2(R_{SW} + R_L) \quad (EQ\ 10)$$

Switching Losses

The switching current is the sum of the control currents and the MOSFET driver. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. If a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode:

$$I_{GC} = f(Q_{PMOS} + Q_{NMOS}) \quad (EQ\ 11)$$

Where: Q_{PMOS} and Q_{NMOS} are the gate charges of the internal MOSFET switches.

The losses of the gate charges are proportional to V_{IN} and thus their effects will be more visible at higher supply voltages.

Other Losses

Basic losses in the design of a system should also be considered. Internal battery resistances and copper trace can account for additional efficiency degradations in battery operated systems. By making sure that C_{IN} has adequate charge storage and very low ESR at the given switching frequency, the internal battery and fuse resistance losses can be minimized. C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

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Checking Transient Response

The main loop response can be evaluated by examining the load transient response. Switching regulators normally take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equivalent to:

$$V_{DROP} = \Delta I_{LOAD} \times ESR \quad \text{(EQ 12)}$$

Where:

ESR is the effective series resistance of COUT.

ΔILOAD also begins to charge or discharge COUT, which generates a feedback error signal. The regulator loop then acts to return VOUT to its steady-state value. During this recovery time VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

The AS1335 requires proper layout and design techniques for optimum performance.

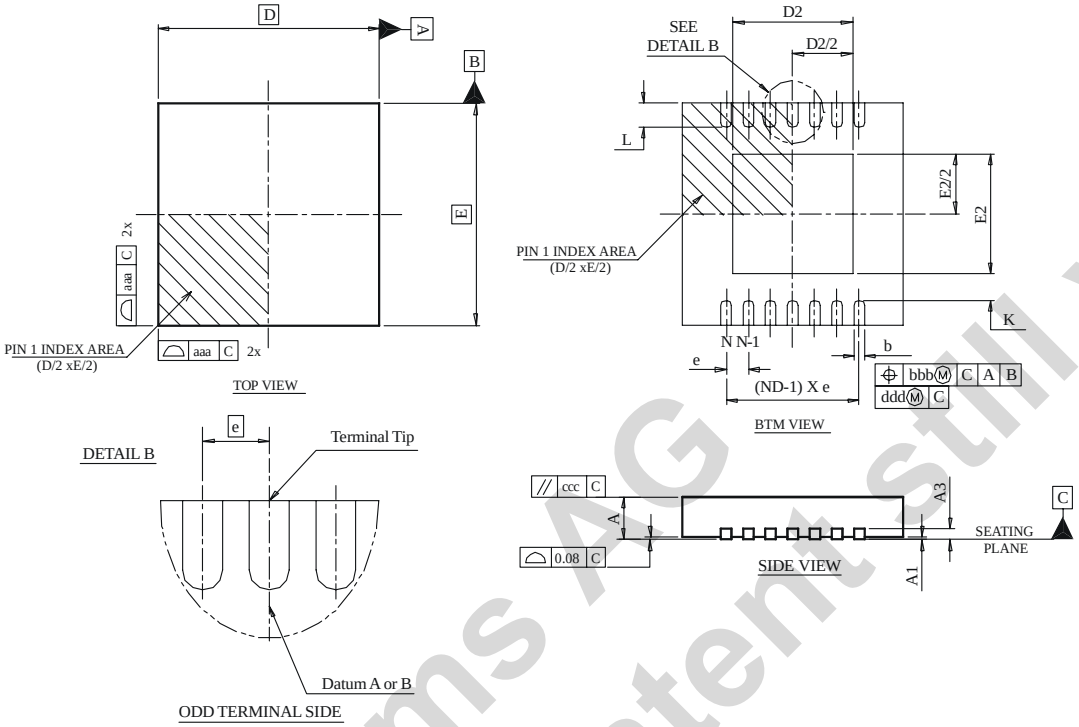
- The power traces (GND, SW, and VIN) should be kept as short, direct, and wide as is practical.
- Pin FB should be connected directly to the Output Voltage.
- The positive plate of CIN should be connected as close to VIN as is practical since CIN provides the AC current to the internal power MOSFETs.
- Switching node SW should be kept far away from the sensitive FB node.
- The negative plates of CIN and COUT should be kept as close to each other as is practical. A starpoint to Ground is recommended.

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10 Package Drawings and Markings

The device is available in an 10-pin TDFN 3x3mm package.

Figure 21. 10-pin TDFN 3x3mm Package



Symbol	Min	Typ	Max	Notes
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
A3		0.20 REF		1, 2
L1	0.03		0.15	1, 2
L2			0.13	1, 2
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
eee		0.08		1, 2
ggg		0.10		1, 2

Symbol	Min	Typ	Max	Notes
D BSC		3.00		1, 2
E BSC		3.00		1, 2
D2	2.20		2.70	1, 2
E2	1.40		1.75	1, 2
L	0.30	0.40	0.50	1, 2
θ	0º		14º	1, 2
K	0.20			1, 2
b	0.18	0.25	0.30	1, 2, 5
e		0.50		
N		10		1, 2
ND		5		1, 2, 5

Notes:

1. Figure 21 is shown for illustration only.
2. All dimensions are in millimeters; angles in degrees.
3. Dimensioning and tolerancing conform to *ASME Y14.5 M-1994*.
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95-1, SPP-012*. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
7. ND refers to the maximum number of terminals on side D.
8. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

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11 Ordering Information

The device is available as the following standard versions.

Table 5. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1335-BTDT-100	ASSI	1.5A, 1.5MHz, Synchronous DC/DC Step-Down Converter, fixed VOUT = 1.0V	Tape and Reel	10-pin TDFN 3x3mm
AS1335-BTDT-AD	ASSC	1.5A, 1.5MHz, Synchronous DC/DC Step-Down Converter, user-adjustable Output Voltage	Tape and Reel	10-pin TDFN 3x3mm

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
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