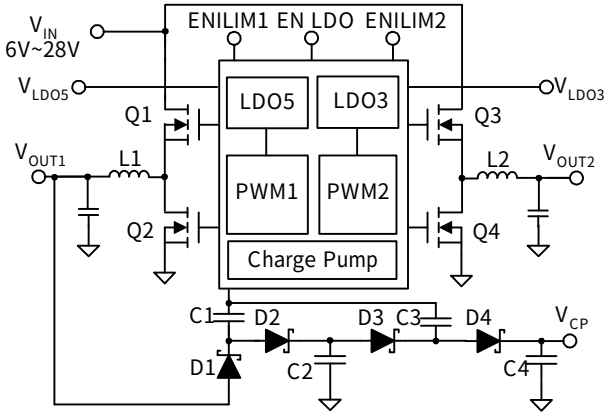
System Power PWM Controller for Notebook Computers with Charge Pump

Features

- Wide Input voltage Range from 6V to 25V
- Provide 5 Independent Outputs with ±1.5% Accuracy Over-Temperature
  - PWM1 Controller with Adjustable (2V to 5.5V) Output
  - PWM2 Controller with Adjustable (2V to 5.5V) Output
  - 100mA Low Dropout Regulator (LDO5) with Fixed 5V Output
  - 100mA Low Dropout Regulator (LDO3) with Fixed 3.3V Output
  - 270kHz Clock Signal for 15V Charge Pump (Used VOUT1 as Its Power Supply)
- Excellent Line/Load Regulations about ±1.5% Over-Temperature Range
- ±1%, (±1.5%, 50㎂) 2.0V Reference Voltage Output
- Built-In POR Control Scheme Implemented
- Selectable Forced-PWM or Automatic PFM/PWM (with Selectable Ultrasonic Operation)
- Constant-On-Time Control Scheme with Frequency Compensation for PWM Mode
- Selectable Switching Frequency in PWM Mode
- Built-in Digital Soft-Start for PWM Outputs and Soft-Stop for PWM Outputs and LDO Outputs
- Integrated Bootstrap Forward P-CH MOSFET
- High Efficiency over Light to Full Load Range (PWMs)
- Built-in Power Good Indicators (PWMs)
- Independent Enable Inputs (PWMs, LDO)
- 70% Under-Voltage and 125% Over-Voltage Protections (PWM)
- Adjustable Current-Limit Protection (PWMs)
  - Using Sense Low-Side MOSFET's $R_{DS(ON)}$
- Over-Temperature Protection
- 4mmx4mm Thin QFN-24 (TQFN4x4-24A) package
- Lead Free and Green Device Available (RoHS Compliant)

Simplified Application Circuit



General Description

The APW8812 integrates dual step-down, constant-on-time, synchronous PWM controllers (that drives dual N-channel MOSFETs for each channel) and two low drop-out regulators as well as various protections into a chip. The PWM controllers step down high voltage of a battery to generate low-voltage for NB applications. The output of PWM1 and PWM2 can be adjusted from 2V to 5.5V by setting a resistive voltage-divider from VOUTx to GND. The linear regulators provide 5V and 3.3V output for standby power supply. The linear regulators provide up to 100mA output current. When the PWMx output voltage is higher than LDOx bypass threshold, the related LDOx regulator is shut off and its output is connected to VOUTx by internal switchover MOSFET. It can save power dissipation. The charge pump circuit with 270kHz clock driver uses VOUT1 as its power supply to generate approximately 15V DC voltage.

The APW8812 provides excellent transient response and accurate DC output voltage in either PFM or PWM Mode. In Pulse-Frequency Mode (PFM), the APW8812 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. The Forced-PWM Mode works nearly at constant frequency for low-noise requirements. The unique ultrasonic mode maintains the switching frequency above 25KHz, which eliminates

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

General Description (Cont.)

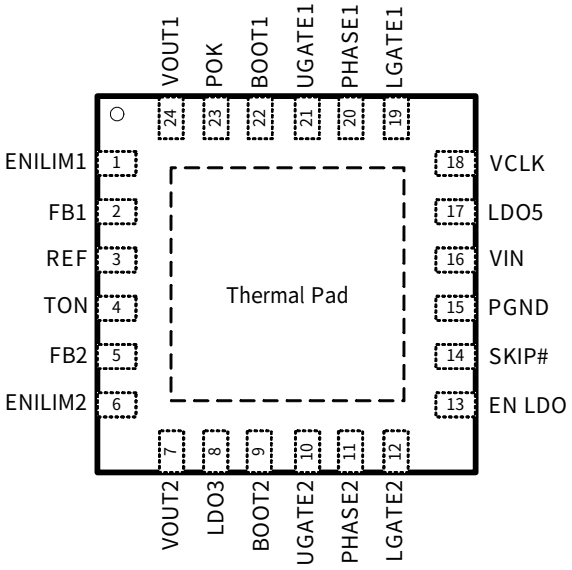
noise in audio applications.

The APW8812 is equipped with accurate sourcing and current-limit, output under-voltage output over-voltage protections, being perfect for NB applications. A 1.7ms (typ.) digital soft-start can reduce the start-up current. A soft-stop function actively discharges the output capacitors by the discharge device. The APW8812 has individual enable controls for each PWM channels and LDOs. Pulling both ENILIM1/2 pin and ENLDO pin low shuts down the whole chip with low quiescent current close to zero. The APW8812 is available in a TQFN4x4-24A package.

Applications

- **Notebook and Sub-Notebook Computers**
- **Portable Devices**
- **DDR1, DDR2, and DDR3 Power Supplies**
- **3-Cell and 4-Cell Li+ Battery-Powered Devices**
- **Graphic Cards**
- **Game Consoles**
- **Telecommunications**

Pin Configuration



TQFN4x4-24A
Top View

= Thermal Pad (connected to GND plane for better heat dissipation)

Ordering and Marking Information

APW8812 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-24A Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8812 QB: APW8812 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

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Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Power Voltage (VIN to GND)	-0.3 ~ 28	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
$V_{UG-PHASE}$	UGATE Voltage (UGATE to PHASE) <400ns pulse width >400ns pulse width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
V_{LG-GND}	LGATE Voltage (LGATE to GND) <400ns pulse width >400ns pulse width	 -5 ~ V_{LDO5}+0.3 -0.3 ~ V_{LDO5}+0.3	V
V_{PHASE}	PHASE Voltage (PHASE to GND) <400ns pulse width >400ns pulse width	 -5 ~ 35 -0.3 ~ 28	V
	All Other Pins (LDOx, FBx, VOUTx, LDO5, LDO3, REF, VCLK, EN LDO, ENILIMx to GND)	-0.3 ~ 6	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient	52	°C/W
θ_{JC}	Thermal Resistance - Junction to Case	7	

Note 2: θ_{JA} and θ_{JC} are measured with the component mounted on a high effective thermal conductivity test board in free air. The thermal pad of package is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	PWM1/2 Converter Input Voltage	6 ~ 25	V
V_{OUT1}	PWM1 Converter Output Voltage	2 ~ 5.5	V
V_{OUT2}	PWM2 Converter Output Voltage	2 ~ 5.5	V
C_{IN}	PWM1/2 Converter Input Capacitor (MLCC)	10 ~	µF
C_{LDO}	LDO Output Capacitor (MLCC)	2.2 ~	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

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Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8812			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY POWER						
I_{VN}	VIN Supply Current	Supply current1, VOUT1 = VOUT2 = 0V, SKIP# = GND, EN LDO = open, ENILIMx = 5V, V_{FB1} = V_{FB2} = 2.05V	-	0.55	1.3	mA
		Supply current2, VOUT1 = 5V, VOUT2 = 3.3V, SKIP# = GND, EN LDO = open, ENILIMx = 5V, V_{FB1} = V_{FB2} = 2.05V, P_{VIN}+P_{LDO5}	-	5	7	mW
		Standby current, EN LDO=open, EN PWM=0V	-	200	-	µA
		Shutdown current, EN LDO= 0V, ENILIMx = 0V	-	20	40	
UNDER-VOLTAGE LOCK OUT PROTECTION (UVLO)						
	LDO5 UVLO threshold	Rising Edge	4.1	4.2	4.3	V
		Hysteresis	-	0.1	-	V
	LDO3 UVLO threshold	Shutdown	-	2.5	-	V
PWM CONTROLLERS						
	Output Voltage Adjust Ranve	VOUT1, VOUT2	2	-	5.5	V
V_{FB}	FBx Reference Voltage	I_{REF} = 0A, T_A= -40°C to 85°C	1.98	2.0	2.02	V
I_{FB}	FBx input current	V_{FBX} = 2.0V, T_A = 25°C	-20	-	20	nA
	PWM 1/2 Load Regulation	SKIP# = LDO5, I_{OUT} = 0A to 5A	-	-1.7	-	%
		SKIP# = REF, I_{OUT} = 0A to 5A	-	-1.5	-	%
		SKIP# = GND, I_{OUT} = 0A to 5A	-	-0.1	-	%
	PWM1/2 Line Regulation	V_{IN} = 6V to 25V	-	0.005	-	%/V
	Soft-Start Ramp Time	ENPWM High to V_{OUT} Full Regulation	-	1.7	-	ms
T_{ON11}	PWM1 On Time seting1	TON = GND, SKIP# = GND, V_{IN} = 12V, PWM1 = 5V	-	2080	-	ns
T_{ON12}	PWM1 On Time seting2	TON = REF, SKIP# = GND, V_{IN}=12V, PWM1=5V	-	1700	-	
T_{ON13}	PWM1 On Time seting3	TON = LDO3, SKIP# = GND, V_{IN} = 12V, PWM1 = 5V	-	1390	-	
T_{ON14}	PWM1 On Time seting4	TON = LDO5, SKIP# = GND, V_{IN}=12V, PWM1=5V	-	1140	-	
T_{ON21}	PWM2 On Time seting1	TON = GND, SKIP# = GND, V_{IN}=12V, PWM2 = 3.3V	-	1100	-	
T_{ON22}	PWM2 On Time seting2	TON = REF, SKIP# = GND, V_{IN}=12V, PWM2 = 3.3V	-	900	-	
T_{ON23}	PWM2 On Time seting3	TON = LDO3, SKIP# = GND, V_{IN} = 12V, PWM2 = 3.3V	-	730	-	
T_{ON24}	PWM2 On Time seting4	TON = LDO5, SKIP# = GND, V_{IN} = 12V, PWM2 = 3.3V	-	600	-	
	UGATEx Minimum Off-Time		350	450	550	ns

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Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8812			Unit
			Min.	Typ.	Max.	
PWM CONTROLLERS (CONT.)						
	UGATEx Minimum On-Time		80	110	140	ns
	Minimum Ultrasonic SKIP Operating Frequency		25	37	-	kHz
LOW DROUPUT LINEAR REGULATORS (LDO5/LDO3)						
	LDO5 Output Voltage	VOUT1 = GND, 6V < V_{IN} < 25V, 0< I_{LDO} < 100mA	4.8	5.0	5.2	V
	LDO3 Output Voltage	VOUT2 = GND, 6V < V_{IN} < 25V, 0< I_{LDO3} < 100mA	3.2	3.33	3.46	V
V_{THBYP5}	LDO5 Bypass Threshold for VOUT1-to-LDO5 Switch On	VOUT1 Regulation Voltage Rising	4.55	4.7	4.85	V
		Hysteresis	0.15	0.25	0.3	
V_{THBYP3}	LDO3 Bypass Threshold for VOUT2-to-LDO3 Switch On	VOUT2 Regulation Voltage Rising	3.05	3.15	3.25	V
		Hysteresis	0.1	0.2	0.25	
	VOUTx-to-LDOx Switch On Resistance	VOUTx to LDOx, 10mA	-	1.5	3	Ω
	LDOx Current-Limit	VOUTx = GND, LDOx = GND	150	-	-	mA
	LDOx Discharge On Resistance		-	40	65	Ω
REFFERENCE						
	REF Output Voltage	I_{REF} = 0A	1.98	2.00	2.02	V
	REF Load Regulation	I_{LOAD} = 0 to 50µA	-	10	-	mV
	REF Sink Current	REF in Regulation	10	-	-	µA
CHARGE PUMP CLOCK						
V_{CLKH}	High Level Voltage	I_{VCLK} = -10mA, LDO5 = 5V, T_A = 25°C	4.84	4.92	-	V
V_{CLKL}	Low Level Voltage	I_{VCLK} = 10mA, LDO5 = 5V, T_A = 25°C	-	0.06	0.12	
F_{CLK}	Clock Frequency	T_A = 25°C	175	270	325	kHz
PWM 1/2 PROTECTIONS						
	Over-Voltage Protection Threshold	V_{OUTX} RIsing	120	125	130	%
	Over-Voltage Fault Propagation Delay	Delta voltage = 10mV	-	1.5	-	µs
	Current-Limit Current Source	V_{ILIM} = 920mV, T_A = 25°C	9.4	10	10.6	µA
		On the basis of 25 °C	-	4500	-	ppm/°C
	ILIMx Adjustment Range	$V_{ENILIMx-GND}$	0.7	-	2	V
	Maximum setting voltage	$V_{ENILIMx}$ = 5V, Setting Current-Limit Threshold	205	250	-	mV
	Current-limit comparator offset	($V_{ENILIMx-GND}$-$V_{PGND-PHASEx}$), $V_{ENILIMx}$ = 920mV	-8	0	8	mV
	Zero-Crossing Threshold	SKIP# = REF or LDOx, $V_{PGND-PHASE}$	-5	0	5	mV
	Under-Voltage Protection Threshold		65	70	75	%
	Under-Voltage Protection Hysteresis		-	3	-	%
	Under-Voltage Protection Debounce Interval		22	32	42	µs

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Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8812			Unit
			Min.	Typ.	Max.	
PWM 1/2 PROTECTIONS (CONT.)						
	Under-Voltage Protection Enable Blanking Time	From EN signal go high to UVP workable	-	2	2.6	ms
	Over-Temperature Protection THreshold	T_J Rising	-	160	-	°C
		Hysteresis	-	25	-	
POWER GOOD						
	POK Threshold	POK in from Lower (POK goes high)	87	90	93	%
		POK in from higher (POK goes low)	120	125	130	
		POK hysteresis	-	3	-	
	POK Propagation Delay	V_{FBX} falling and rising	43	63	85	µs
	POK Enable Delay	ENILMx goes high to POK goes High	-	2	-	ms
	POK Sink Current	V_{POK} = 500mV	2.5	7.5	-	mA
	POK Leakage Current	V_{POK} = 5V	-	0.1	1	µA
LOGIC LEVELS						
	SKIP# Input Voltage	Forced PWM Mode	-	-	1.5	V
		Automatic PFG/PWM Mode	1.9	-	2.1	V
		Auto Skip with Ultrasonic	2.7	-	-	V
	TON Input Voltage	200kHz/250kHz	-	-	1.5	V
		245kHz/305kHz	1.9	-	2.1	V
		300kHz/375kHz	2.7	-	3.6	V
		365kHz/460kHz	4.7	-	-	V
	ENILIMx Input Voltage	Enable	450	-	-	mV
		Disable	-	-	400	
	EN LDO Input Voltage	Shutdown	-	-	0.4	V
		Enable, VCLK = off	0.8	-	1.6	
		Enable, VCLK = on	2.4	-	-	
	Input Leakage Current	$V_{SKIP\#}$ = V_{TON} = 0V or 5V	-1	-	1	µA
		$I_{EN\ LDO}$	0.5	1	3	µA
GATE DRIVERS						
	UG Pull-Up Resistance	V_{BOOTx} – V_{UGATEx} = 100mV	-	4	8	Ω
	UG Sink Resistance	V_{UGATEx} – V_{PHASEx} = 100mV	-	1.5	4	Ω
	LG Pull-Up Resistance	V_{LDO5} – V_{LGATEx} = 100mV	-	4	8	Ω
	LG Sink Resistance	V_{LGATEx} – V_{PGND} = 100mV	-	1.5	4	Ω
	Dead-Time	UG falling to LG rising	-	40	-	ns
		LG falling to UG rising	-	40	-	ns
	VOUT1/2 Discharge On Resistance		-	40	80	Ω

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Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8812			Unit
			Min.	Typ.	Max.	
BOOTSTRAP SWITCH						
V_F	Forward Voltage	$V_{LDO5x} - V_{BOOTx-GND}$, I_F = 10mA	-	0.5	0.8	V
I_R	Reverse Leakage	$V_{BOOTx-GND}$ = 30V, V_{PHASEx} = 25V, V_{LDO5} = 5V	-	-	0.5	µA

Pin Description

PIN		FUNCTION
NO.	NAME	
1	ENILIM1	PWM1 Enable and Current-Limit Adjustment. There is an internal 10μA current source from LDO5 to ENILIM1 and connected a resistor from ENILIM1 to GND to set the current-limit threshold. The PGND-PHASE1 current-limit threshold is 1/10th the voltage set at ENILIM1 over a 0.7 to 2V range. The logic current-limit threshold is default to 250mV value if ENILIM1 is 5V PWM1 is enabled when ENILIM1=1. When ENILIM1=0, PWM1 is in shutdown.
2	FB1	Output voltage feedback pin (PWM1). It can use a resistive divider from VOUT1 to GND to adjust the output from 2V to 5.5V.
3	REF	2V Reference Output. Bypass to GND with a 0.1μF (minimum) capacitor. REF can supply external loads for 50μA (maximum). REF load-regulation error will degrade feedback and output accuracy.
4	TON	Frequency Selection Input. Connect to LDO5 for 365kHz(PWM1)/460kHz(PWM2) operation and to LDO3 for 300kHz/375kHz operation. Connect to REF for 245kHz/305kHz operation and to GND for 200kHz/250kHz operation.
5	FB2	Output voltage feedback pin (PWM2). It can use a resistive divider from VOUT2 to GND to adjust the output from 2V to 5.5V.
6	ENILIM2	PWM2 Enable and Current-Limit Adjustment. There is an internal 10μA current source from LDO5 to ENILIM2 and connected a resistor from ENILIM2 to GND to set the current-limit threshold. The PGND-PHASE2 current-limit threshold is 1/10th the voltage set at ENILIM2 over a 0.7 to 2V range. The logic current-limit threshold is default to 250mV value if ENILIM2 is 5V PWM2 is enabled when ENILIM2=1. When ENILIM2=0, PWM2 is in shutdown.
7	VOUT2	PWM2 Output Voltage-Sense Input. The VOUT2 pin makes a direct measurement of the PWM2 output voltage. VOUT2 is an input to the constant-on-time PWM one-time one-shot circuit.
8	LDO3	3.3V Linear Regulator Output. LDO3 can provide a total of 100mA, 3.3V external loads. When LDO3 is at 3.3V and PWM2 output voltage is over 3.15V bypass threshold, the internal LDO will shut down, and LDO3 output pin connects to VOUT2 through a 1.5Ω switch. Bypass to GND with a minimum of 2.2μF ceramic capacitor for stability.
9	BOOT2	Supply Input for The UGATE2 Gate Driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
10	UGATE2	Output of The High-Side MOSFET Driver for PWM2. Connect this pin to Gate of the high-side MOSFET.
11	PHASE2	Junction Point of The High-Side MOSFET Source, Output Filter Inductor and The Low-Side MOSFET Drain for PWM2. Connect this pin to the Source of the high-side MOSFET. PHASE2 serves as the lower supply rail for the UGATE2 high-side gate driver. PHASE2 is the current-sense input for the PWM2.
12	LGATE2	Output of The Low-Side MOSFET Driver for PWM2. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to LDO5.
13	EN LDO	Master Enable Input. The LDOx is enabled when EN LDO=1. When ENLDO=0, the LDO is shutdown. See the table 2 “Power-Up Control Logics.”
14	SKIP#	PWM1 and 2 Controller Operation Mode Control. Connect SKIP# to GND for forced-PWM mode, to REF for auto PWM/PFM mode and to LDO3 or LDO5 for ultra-sonic mode,
15	PGND	Power Ground of The LGATE Low-Side MOSFET Drivers. Connect the pin to the source of the low-side MOSFETs.
16	VIN	Battery voltage input pin. VIN powers linear regulators and is also used for the constant-on-time PWM on-time one-shot circuits. Connect VIN to the battery input and bypass with a 1μF capacitor for noise interference.
17	LDO5	5V Linear Regulator Output. LDO5 can provide a total of 100mA, 5V external loads. When LDO5 is at 5V and PWM1 output voltage is over 4.7V bypass threshold, the internal LDO will shut down, and LDO5 output pin connects to VOUT1 through a 1.5Ω switch. Bypass to GND with a minimum of 2.2μF ceramic capacitor for stability.
18	VCLK	270kHz Clock Output for 15V Charge Pump.
19	LGATE1	Output of The Low-Side MOSFET Driver for PWM1. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to LDO5.
20	PHASE1	Junction Point of The High-Side MOSFET Source, Output Filter Inductor and The Low-Side MOSFET Drain for PWM1. Connect this pin to the Source of the high-side MOSFET. PHASE1 serves as the lower supply rail for the UGATE1 high-side gate driver. PHASE1 is the current-sense input for the PWM1.

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Pin Description (Cont.)

PIN		FUNCTION
NO.	NAME	
21	UGATE1	Output of The High-Side MOSFET Driver for PWM1. Connect this pin to Gate of the high-side MOSFET.
22	BOOT1	Supply Input for The UGATE1 Gate Driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
23	POK	Power-Good Output Pin of Both PWMs.(Logic AND) POK is an open-drain output used to indicate the status of the PWMx output voltage. Connect the POK in to +5V through a pull-high resistor.
24	VOUT1	PWM1 Output Voltage-Sense Input. The VOUT1 pin makes a direct measurement of the PWM1 output voltage. VOUT1 is an input to the constant-on-time PWM one-time one-shot circuit.
Thermal Pad	GND	Signal Ground for The IC.

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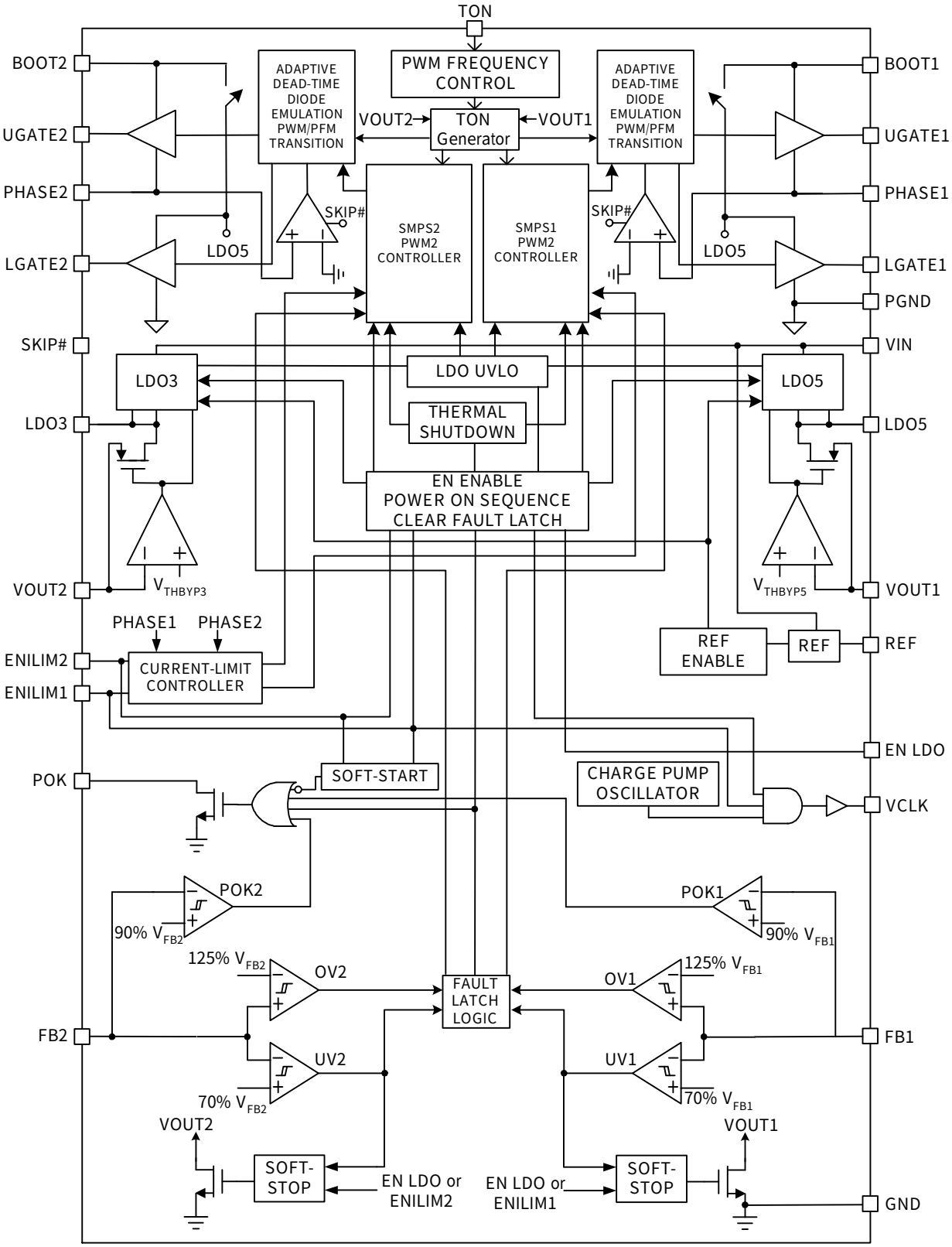
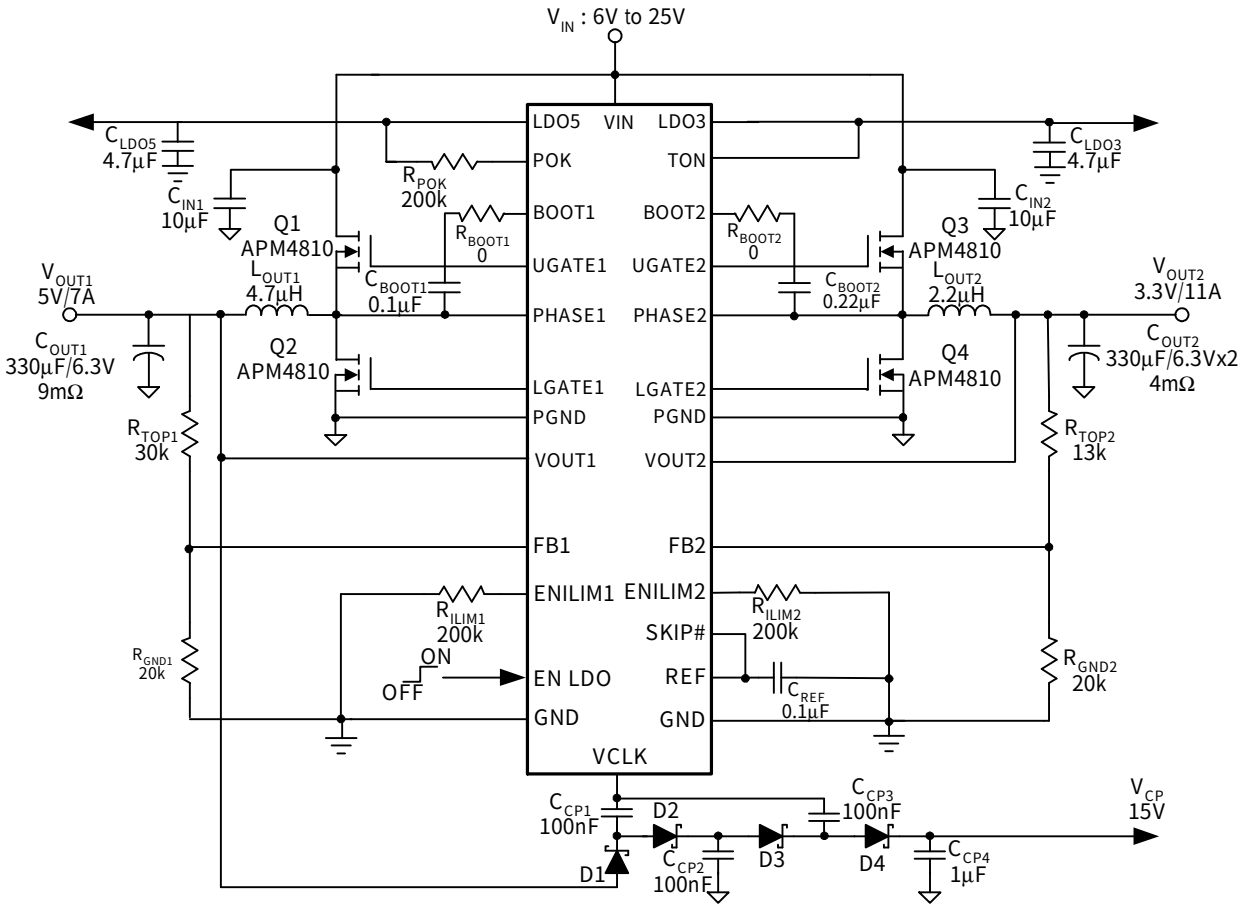
Block Diagram



Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typ.: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM) Mode

Connect SKIP# to REF for normal PFM operation. In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON\text{-}PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode. Similarly, the on-time of ultrasonic mode is the same with PFM mode. The description of ultrasonic mode will be illustrated later.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM}$$

$$= \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Forced-PWM Mode

Connect SKIP# to GND for normal Forced-PWM operation. The Forced-PWM mode disables the zero-crossing comparator, which truncates the low-side switch on-time at the inductor current zero crossing. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while UGATE maintains a duty factor of V_{OUT}/V_{IN}. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced-PWM mode is the most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

Ultrasonic Mode

Connecting SKIP# to LDO3 or LDO5 for ultrasonic mode. The ultrasonic mode activates a unique PFM mode with a minimum switching frequency of 37kHz. The minimum frequency 37KHz of ultrasonic mode eliminates audio-frequency interference in light load condition. It will transit to unique PFM mode when output loading makes the frequency bigger than ultrasonic frequency. In ultrasonic mode, the controller automatically transits to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{LOAD(PFM\ to\ PWM)}$).

When the controller detects that no switching has occurred within about 27µs (typ.), an ultrasonic pulse will occurre. The ultrasonic controller turns on the low-side MOSFET first to reduce the output voltage. After feedback voltage drops below the internal reference voltage, the

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Function Description (Cont.)

Ultrasonic Mode (Cont.)

controller turns off the low-side MOSFET and triggers a constant-on-time. When the constant-on-time has expired, the controller turns on the low-side MOSFET again until the inductor current is below the zero-crossing threshold. The behavior is the same with PFM mode.

Reference Voltages and Linear Regulator (REF and LDO3/5)

The 2V reference, REF, is accurate to ±1% over-temperature. Bypass to GND with a 0.1μF (minimum) capacitor. REF can source up to 50μA for external loads. However, avoid loading REF if extremely accurate specifications for both the main output voltages and REF are essential. In addition, REF voltage must be bigger than its rising enable threshold, and then the LDO output starts to rise up.

The LDO3 and LDO5 regulators can supply up to 100mA for external loads. Bypass to GND with a minimum of 2.2μF ceramic capacitor for stability. When ENLDO is enabled, the V_{LDO3} is fixed 3.33V and the V_{LDO5} is fixed 5V in standby mode. When PWMx output voltage is over whose bypass threshold(PWM1 is 4.7V and PWM2 is 3.15V), the switchover between the internal LDOx and VOUTx is workable. These actions change the current path to power the loads from the PWMx regulateon voltage, rather than from the internal linear regulator.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls. The POR function continually monitors the supply voltage on the LDO5 pins. LDO5 POR circuitry inhibits wrong switching. When the rising V_{LDO5} voltage reaches the rising POR threshold (4.2V typ.), the output voltages begin to ramp up. When the LDO5 voltage is lower than 4.1V(typ.) or LDO3 voltage is lower than 2.5V(typ.), both switch power supplies are shut off. This is non-latch protection. LDO5 POR threshold could reset the under-voltage, over-voltage.

Digital Soft-Start

The APW8812 integrates digital soft-start circuit to ramp up the PWMx output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of PWMx output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. When the ENILIMx pin is pulled above the rising threshold voltage, the related PWM initiates a soft-start process to ramp up the output voltage. The soft-start interval is 1.7ms(typ.) and independent of the UGATE switching frequency.

Enable Controls

The APW8812 has two independent enable controls for PWM and LDO. When the ENLDO pin is higher than 0.8V, the REF, LDO3 and LDO5 are enabled to standby mode. It means that the PWM1 and PWM2 are ready to enable at this mode. When the ENPWM pin is high (ENILIMx=1) at standby mode, the PWMx initiates a soft-start process to ramp up the output voltage. The PWM1 and PWM2 are controlled individually by ENILIM1 and ENILIM2. When ENLDO, ENILIM1 and ENILIM2 are low, the chip is in its low-power shutdown state. The APW8812 only consumes 20μA of quiescent current while in shutdown. When the ENLDO is higher than 2.4V and ENILIM1 is high (ENILIM1=1), the clock signal becomes available from VCLK pin. Both PWM outputs are discharged to 0V through a 25Ω switch and both LDO outputs are discharged to 0V through a 40W switch in shutdown mode. Driving ENILIM1 and ENILIM2 (logic AND) or ENLDO below 0.4V clears the over-voltage, under-voltage and over-temperature fault latches.

Charge Pump

The condition for the 270kHz clock signal to be used is that the ENLDO is higher than 2.4V and ENILIM1 is high (ENILIM1=1). When VOUT1 regulates at 5V and the clock signal uses VOUT1 as its power supply, the charge pump circuit can generate approximately 15V DC voltage. The example of charge pump circuit is shown in typical application circuit.

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Function Description (Cont.)

Soft-Stop (PWMs)

In the event of PWM under-voltage or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the PWM output voltages to GND through an internal 25Ω switch. The reference remains active to provide an accurate threshold and to provide over-voltage protection.

Power Sequencing

ENILIM1, ENILIM2 and ENLDO are enable signals for PWM1, PWM2 and LDOs. In the single channel mode, when ENILIM1 or ENILIM2 higher than 630mV, the PWM controller enables the respective outputs, and when ENILIM1 or ENILIM2 is lower than 600mV, it disables the respective outputs. Also, ENILIM1 and ENILIM2 signal timing will control PWM1 and PWM2 power-up sequence. If ENILIMx pin is high (ENILIMx=1) while other channel is starting up, its soft-start will be postponed until the other channel reaches regulation. On the other hand, if both ENILIM1 and ENILIM2 become high state at the same time (within 60µs), both channels ramp up at the same time. About power off sequencing, both supplies begin their power-down sequence immediately when the first supply turns off.

Power Good Indicator (PWMs)

POK is actively held low in shutdown, standby, and soft-start. In the soft-start process, the POK is an open-drain output, and it is released with enable delay after the latest ENILIMx goes high (about 2ms typ.). In normal operation, the POK window is from 90% to its OVP threshold of the converter reference voltage. Both of VOUT1 and VOUT2 have to stay within this window for POK to be high (AND gated). In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (PWMs)

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than the value of current-limit threshold, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold for at least 2µs, the PWM controller starts a soft-stop process to shut down the output gradually. As long as either of PWM channels triggers under-voltage, both of PWM channels active under-voltage protection and latched off when the soft-stop process is completed. The under-voltage threshold is 70% of the nominal output voltage. Under-voltage protection is ignored for at least 2ms (typ.) after a rising edge on EN. Toggling ENLDO or ENPWM signal will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP)

Should the output voltage of V_{OUT1} and V_{OUT2} increase over 25% of the setting voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection will active. As long as either of PWM channels triggers over-voltage, both of PWM channels active over-voltage protection. Over-voltage protection will force the low-side MOSFET gate driver fully turn on. This action actively pulls down the output voltage. When the OVP occurs, the POK pin will pull down and latch-off the converter. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can be reset by toggling ENLDO or ENILIM1 and ENILIM2 (logic AND) signal.

Over-Temperature Protection

When the junction temperature increases above the rising threshold temperature 160°C, the IC will enter the over-temperature protection (OTP). When the OTP occurs, REF, LDO and PWM controllers circuitry shuts down. It is non-latch protection.

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Function Description (Cont.)

Current-Limit (PWMs)

The current-limit circuit employs a “valley” current-sensing algorithm (See Figure 1). The APW8812 uses the low-side MOSFET’s $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage.

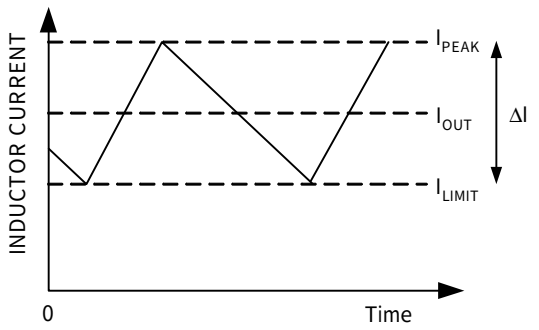

Figure 1. Current-Limit Algorithm

Both PWM controllers use the low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. The MOSFET’s $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacture’s datasheet.

The current-limit threshold of APW8812 is adjusted with an external resistor. The ENILIMx pin adjustment range is from 700mV to 2V. In the adjustable mode, the current-limit threshold voltage is 1/10th the voltage at ENILIMx pin. As shown in Figure 2, The ENILIMx pin can source 10μA. The voltage at ENILIMx pin is equal to 10μA x R_{ILIM}. Connect ILIM to REF for a fixed 200mV threshold. The logic current-limit threshold is default to 250mV value if ENILIMx is 5V. The relationship between the sampled voltage V_{ILIM} and the current-limit threshold I_{LIMIT} is given by:

$$\frac{1}{10} \times V_{ENILIMX} = I_{LIMIT} \times R_{DS(ON)}$$

Where $V_{ENILIMX}$ is the voltage at the ENILIMx pin. $R_{DS(ON)}$ is the low side MOSFETs conducive resistance. I_{LIMIT} is the setting current-limit threshold. I_{LIMIT} can be expressed as I_{OUT} minus half of peak-to-peak inductor current.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

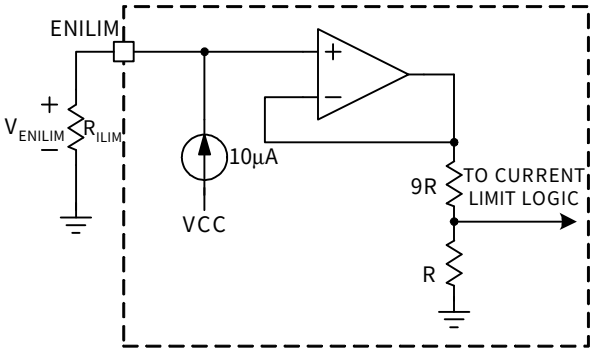

Figure 2. Current-Limit Setting Block Diagram

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Function Description (Cont.)

Table 1. Operating Mode Truth Table

MODE	CONDITION	COMMENT
Run	ENLDO = 1, ENILIMx =1	PWM is in normal operation.
Standby & Soft-Stop	ENPWM=0, ENLDO=1	If PWMx is in shutdown, discharge switch (25 Ω) connects their VOUTx to GND. LDOx and REF active.
Shutdown	EN PWM=0 and EN LDO=0	PWMx output discharge switch (25 Ω) connects VOUTx to GND. LDOx discharge switch (40 Ω) connects LDOx to GND. In this mode, all circuitry is off.
UVP	Either V_{OUT1}, or V_{OUT2} < 70% of nominal output voltage	The internal 25Ω switch turns on to pull low output voltage. LDOx and REF are active. Reset by toggling ENILIM1 and ENILIM2 (logic AND) or EN LDO single.
OVP	Either V_{OUT1} and V_{OUT2} > 125% of normal output voltage	LGATE of two PWM channel are forced high. LDOx and REF active. Reset by toggling ENILIM1 and ENILIM2 (logic AND) or ENLDO single.
OTP	T_J > +160 °C	All circuitry off. It is non-latch protection after the junction temperature cools by 25°C.

Table 2. Power-Up Control Logics

V_{ENLDO}	$V_{ENILIM1}$	$V_{ENILIM2}$	LDO5	LDO3	PWM1	PWM2	VCLK
Low	Don't Care	Don't Care	OFF	OFF	OFF	OFF	OFF
0.8V ~ 1.6V	Low	Low	ON	ON	OFF	OFF	OFF
0.8V ~ 1.6V	High	High	ON	ON	ON	ON	OFF
0.8V ~ 1.6V	High	Low	ON	ON	ON	OFF	OFF
0.8V ~ 1.6V	Low	High	ON	ON	OFF	ON	OFF
0.8V ~ 1.6V	High	High (after ENILIM1 is high without 60µs)	ON	ON	ON	ON (after PWM1 is POK)	OFF
0.8V ~ 1.6V	High (after ENILIM2 is high without 60µs)	High	ON	ON	ON (after PWM2 is POK)	ON	OFF
> 2.4V	Low	Low	ON	ON	OFF	OFF	OFF
> 2.4V	High	High	ON	ON	ON	ON	ON
> 2.4V	High	Low	ON	ON	ON	OFF	ON
> 2.4V	Low	High	ON	ON	OFF	ON	OFF
> 2.4V	High	High(after ENILIM1 is high without 60µs)	ON	ON	ON	ON (after PWM1 is POK)	ON
> 2.4V	High(after ENILIM2 is high without 60µs)	High	ON	ON	ON (after PWM2 is POK)	ON	ON

Application Information

Output Voltage Selection

The output voltage of PWM1 can be adjusted from 2V to 5.5V with a resistor-driver at FB1 between VOUT1 and GND. Using 1% or better resistors for the resistive divider is recommended. The FB1 pin is the inverter input of the error amplifier, and the reference voltage is 2V. Take the example, the output voltage of PWM1 is determined by:

$$V_{OUTI} = 2 \times \left(1 + \frac{R_{TOP1}}{R_{GND1}}\right)$$

Where R_{TOP1} is the resistor connected from V_{OUTI} to V_{FB1} and R_{GND1} is the resistor connected from FB1 to GND. Similarly, the output voltage of PWM2 can be alsoadjusted from 2V to 5.5V.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determines the inductor ripple current and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current can be approxminated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Increasing the inductor value and frequency will reduce the ripple current and voltage. However, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will be result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

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Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook appliactions, ceramic capacitors are remmended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

- For the low-side MOSFET, before it is turned on, the body diode has been conducted. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.
- In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, the less the $R_{DS(ON)}$ of the low-side MOSFET, the less the power loss. The gate charge for this MOSFET is usually a secondary consideration. The high-side MOSFET does not have this zero voltage switching condition, and because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^2(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$
$$P_{low\text{-}side} = I_{OUT}^2(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

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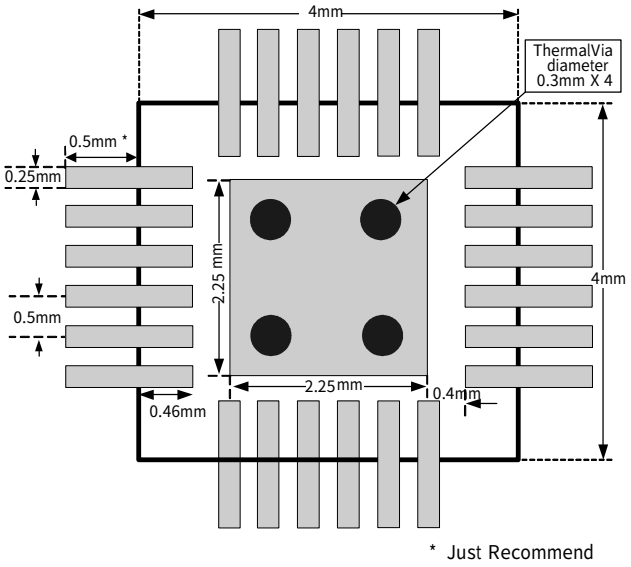
Application Information (Cont.)

Layout Consideration (Cont.)

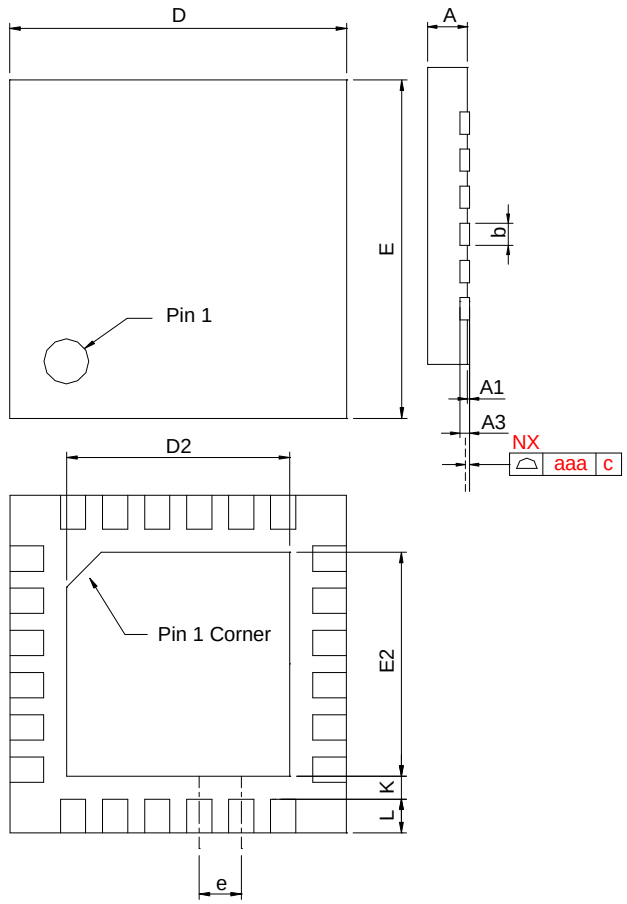
- Keep the switching nodes (UGATEx, LGATEx, BOOTx, and PHASEx) away from sensitive small signal nodes (REF, ILIMx, and FBx) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt, with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATEx and LGATEx) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, the resistor dividers, boot capacitors, and current-limit stetting resistor should be close to their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placednear the drain).
- The input capacitor should be near the drain of the upper MOSFET; the high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASEx nodes) should be a large plane for heat sinking. And PHASEx pin traces are also the return path for UGATEx. Connect these pins to the respective converter's upper MOSFET source.
- The controller used ripple mode control. Build the resistor divider close to the FB1 pin so that the high impedance trace is shorter when the output voltage is in ad justable mode. And the FB1 pin traces can't be close to the switching signal traces (UGATEx, LGATEx, BOOTx, and PHASEx).
- The PGND trace should be a separate trace, and independently go to the source of the low-side MOSFETs for current-limit accuracy.

TQFN4x4-24A



Package Information

TQFN4x4-24A



SYMBOL	TQFN4x4-24A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.90	4.10	0.154	0.161
D2	2.00	2.50	0.079	0.098
E	3.90	4.10	0.154	0.161
E2	2.00	2.50	0.079	0.098
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

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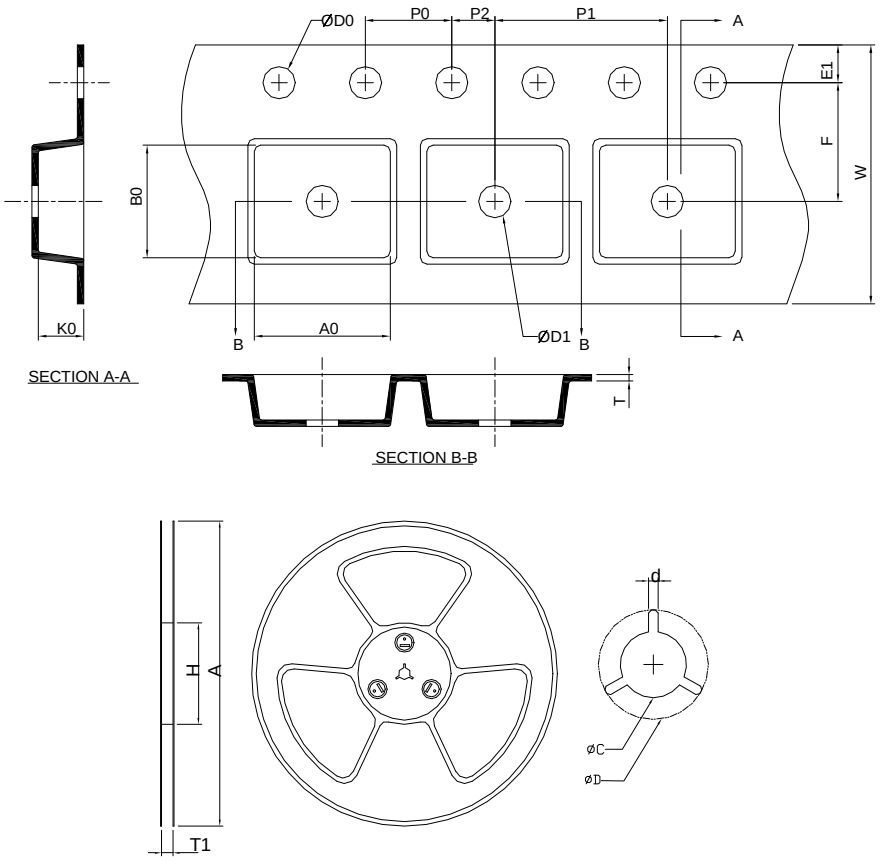
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4-24A	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.25±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
TQFN4x4-24A	Tape & Reel	3000

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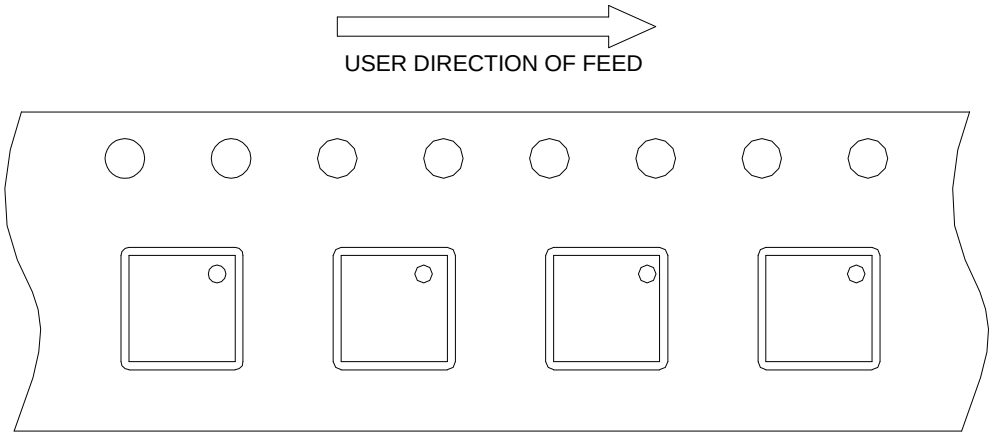
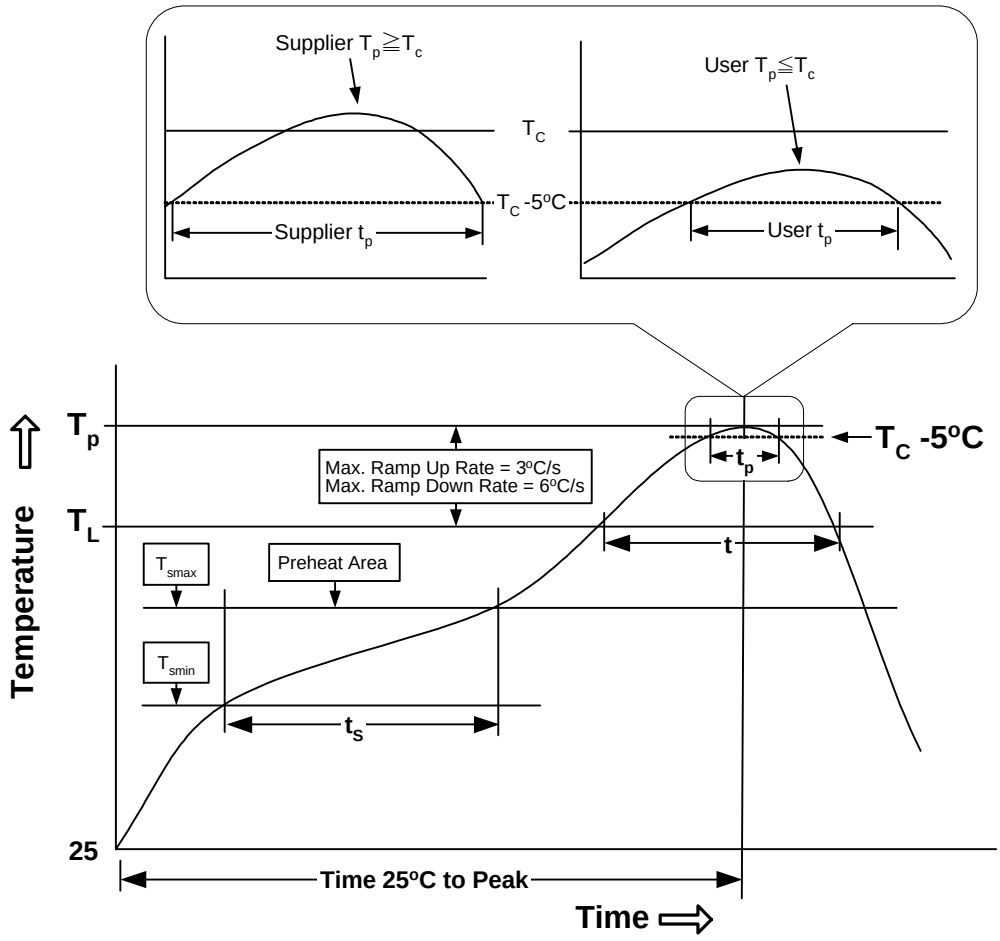
Taping Direction Information

TQFN4x4-24A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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