2A 24V 340kHz synchronous Buck Converter

Features

- **Wide Input Voltage from 4.5V to 24V**
- **2A Continuous Output Current**
- **Adjustable Output Voltage from 0.925V to 20V**
- **Intergrated High/Low Side MOSFET**
- **PFM/PWM mode Operation**
- **Fixed 340kHz Switching Frequency**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Power-On-Reset Detection**
- **Programmable Soft-Start**
- **Over-Temperature Protection**
- **Current-Limit Protection with Frequency Foldback**
- **Enable/Shutdown Function**
- **Small SOP-8 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

APW7300 is a 2A synchronous buck converter with integrated power MOSFETs. The APW7300 design with a current-mode control scheme, can convert wide input voltage of 4.5V to 24V to the output voltage adjustable from 0.925V to 20V to provide excellent output voltage regulation. The APW7300 is equipped with an automatic PFM/PWM mode operation. At light load, the IC operates in the PFM mode to reduce the switching losses. At heavy load, the IC works in PWM.

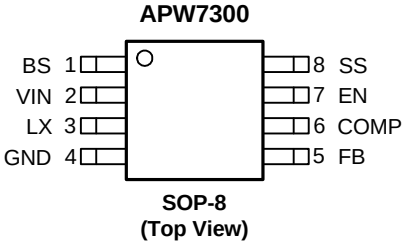
The APW7300 is also equipped with Power-on-reset, soft- start, soft-stop, and whole protections (under-voltage, over-temperature, and current-limit) into a single package.

This device, available SOP-8, provides a very compact system solution external components and PCB area.

Applications

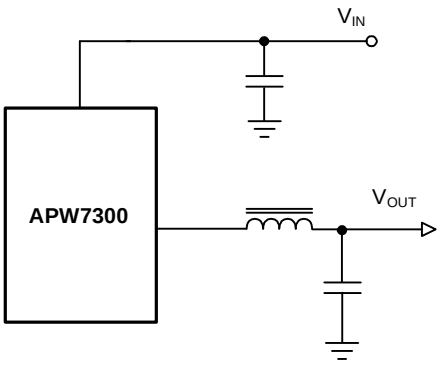
- **LCD Monitor/TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Notebook Computer**

Pin Configuration



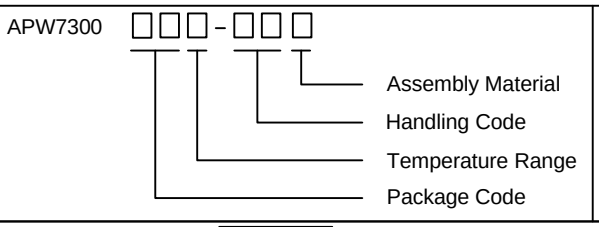
SOP-8
(Top View)

Simplified Application Circuit



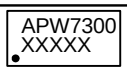
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information



Package Code
K : SOP-8
Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW7300 K :



XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 30	V
V_{LX}	LX to GND Voltage	-1 ~V_{IN}+0.3	V
	EN, FB, COMP, SS to GND Voltage	-0.3 ~ 6	V
V_{BS}	BS to GND Voltage	V_{LX}-0.3 ~ V_{LX}+6	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) SOP-8	110	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air SOP-8	30	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	4.5 ~ 24	V
V_{OUT}	Converter Output Voltage	0.925~20	V
I_{OUT}	Converter Output Current	0~2	A

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Recommended Operating Conditions (Cont.) (Note 4)

Symbol	Parameter	Range	Unit
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V, V_{EN}=3V and T_A=25°C.

Symbol	Parameter	Test Conditions	APW7300			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{FB}=1V, V_{EN}=3V, LX=NC	-	1.9	-	mA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{EN}=0V	-	0.3	-	μA
POWER-ON-RESET (POR)						
	VIN POR Voltage Threshold	V_{IN} Rising	3.8	4.05	4.4	V
	VIN POR Hysteresis		-	0.3	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Regulated on FB pin	0.9	0.925	0.943	V
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency		300	340	380	kHz
	Foldback Frequency	V_{FB}=0V	-	110	-	kHz
	Maximum Converter's Duty	V_{FB}=0.925V	-	90	-	%
	Minimum On Time	(Note 5)	-	220	-	ns
PFM MODE OPERATION						
I_{PK_PFM}	PFM Mode Current Limit		-	0.8	-	A
I_{PK_TH}	PWM to PFM Inductor Peak Threshold		-	0.6	-	A
POWER MOSFET						
	High/low Side MOSFET On Resistance		-	110	-	mΩ
	High/Low Side MOSFET Leakage Current	V_{EN}=0V, V_{LX}=0V	-	-	10	μA
CURRENT-MODE PWM CONVERTER						
G_{EA}	Error Amplifier Transconductance		-	820	-	μA/V
	Error Amplifier Voltage Gain		-	400	-	V/V
	Switch Current to COMP Voltage Transconductance		-	4.5	-	A/V

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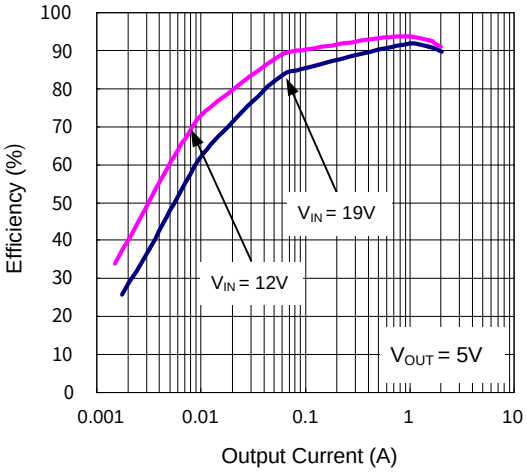
Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V, V_{EN}=3V and T_A= 25°C.

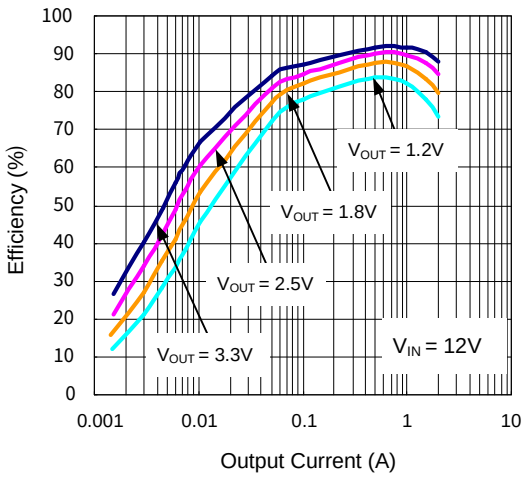
Symbol	Parameter	Test Conditions	APW7300			Unit
			Min.	Typ.	Max.	
PROTECTIONS						
I_{LIM}	High Side MOSFET Current-Limit	Peak Current	-	3.75	-	A
T_{OTP}	Over-Temperature Trip Point		-	160	-	°C
	Over-Temperature Hysteresis		-	50	-	°C
	Over-Voltage Protection		-	120	-	%
SOFT-START, ENABLE AND INPUT CURRENTS						
I_{SS}	Soft-Start Current		-	6	-	µA
	EN Under-Voltage Lockout (UVLO) Threshold	V_{EN} rising	2.2	2.5	2.7	V
	EN UVLO Hysteresis		-	100	-	mV

Typical Operating Characteristics

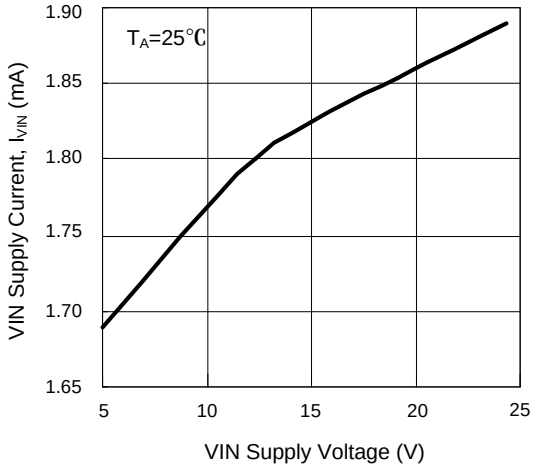
Efficiency vs. Output Current



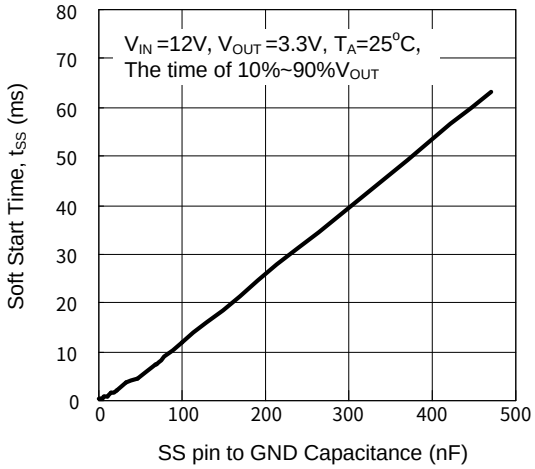
Efficiency vs. Output Current



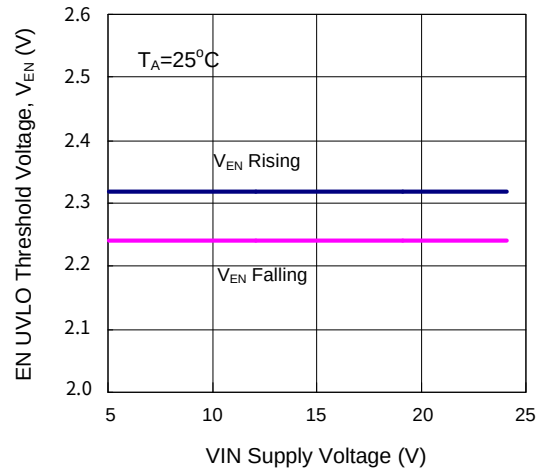
VIN Supply Current vs. VIN Supply Voltage



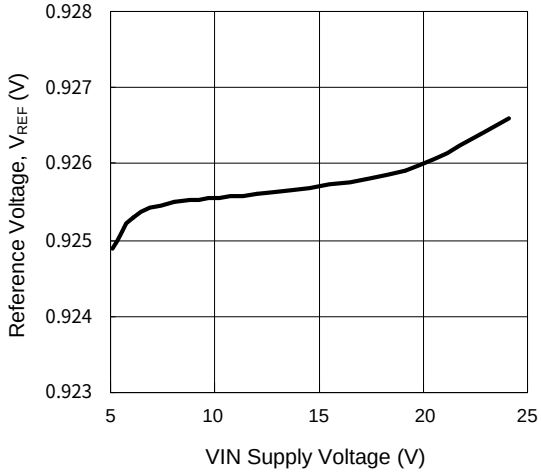
Soft Start Time vs. SS pin to GND Capacitance



EN UVLO Threshold Voltage vs. VIN Supply Voltage

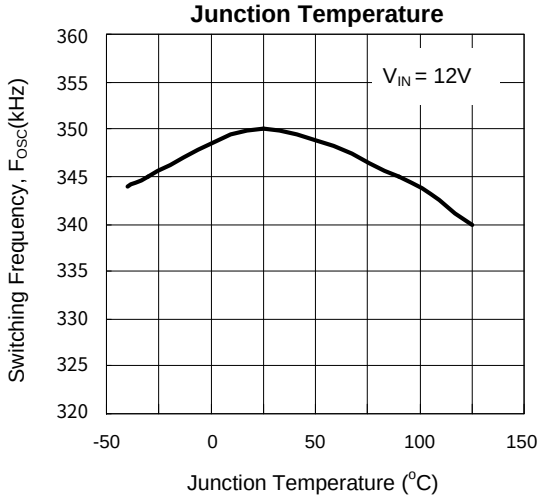


Reference Voltage vs. VIN Supply Voltage

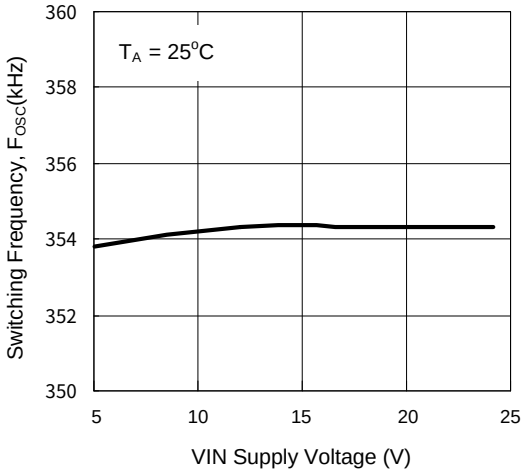


Typical Operating Characteristics

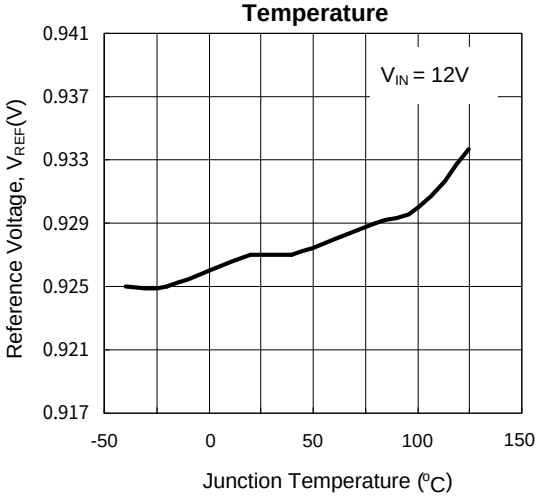
Switching Frequency vs. Junction Temperature



Switching Frequency vs. VIN Supply Voltage



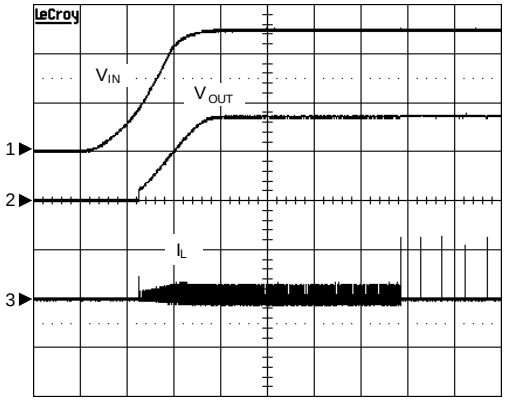
Reference Voltage vs. Junction Temperature



Operating Waveforms

The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Power On



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH, no load

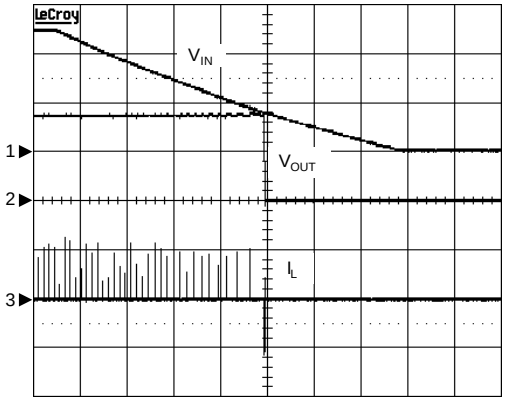
CH1: V_{IN}, 5V/Div, DC

CH2: V_{OUT}, 2V/Div, DC

CH3: I_L, 0.5A/Div, DC

TIME: 10ms/Div

Power Off



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH, no load

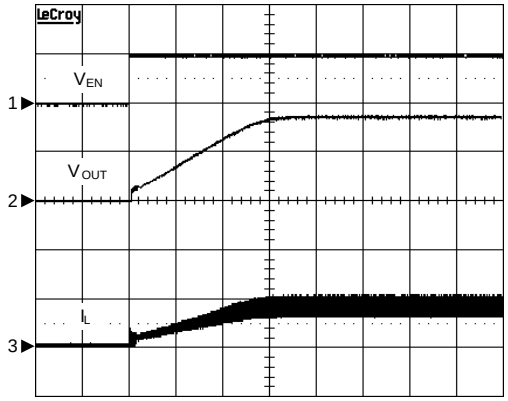
CH1: V_{IN}, 5V/Div, DC

CH2: V_{OUT}, 2V/Div, DC

CH3: I_L, 0.5A/Div, DC

TIME: 50ms/Div

Enable



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH, R_{LOAD} =2Ω

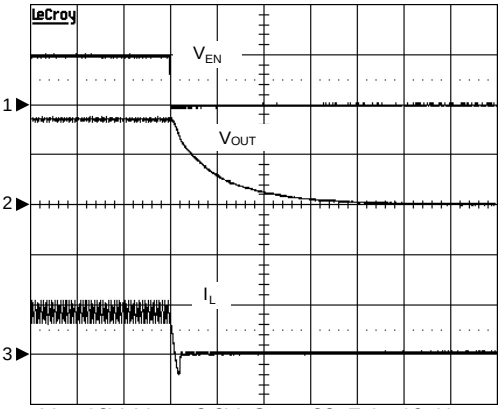
CH1: V_{EN}, 5V/Div, DC

CH2: V_{OUT}, 2V/Div, DC

CH3: I_L, 2A/Div, DC

TIME: 5ms/Div

Shutdown



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH, R_{LOAD} =2Ω

CH1: V_{EN}, 5V/Div, DC

CH2: V_{OUT}, 2V/Div, DC

CH3: I_L, 2A/Div, DC

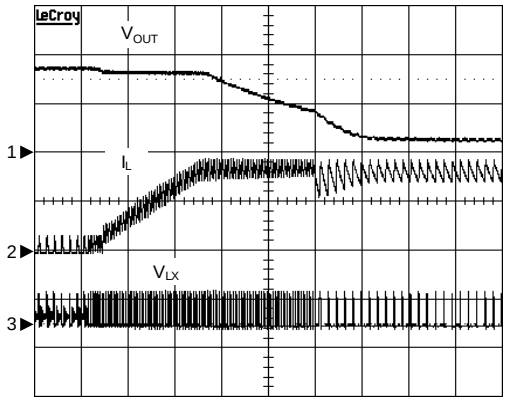
TIME:50µs/Div

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Operating Waveforms

The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

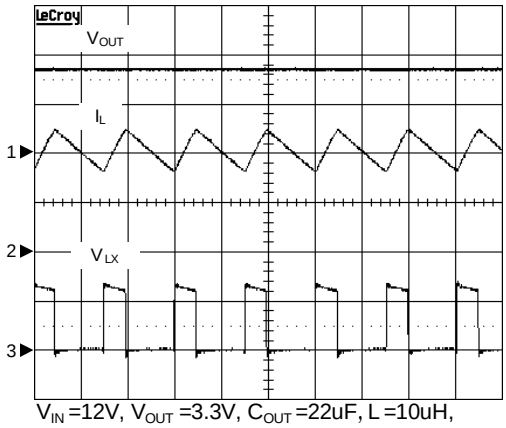
Current Limit & Frequency Foldback



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH,
Ramp up I_{OUT} into current limit

CH1: V_{EN}, 5V/Div, DC
CH2: I_L, 2A/Div, DC
CH3: V_{LX}, 20V/Div, DC
TIME: 50µs/Div

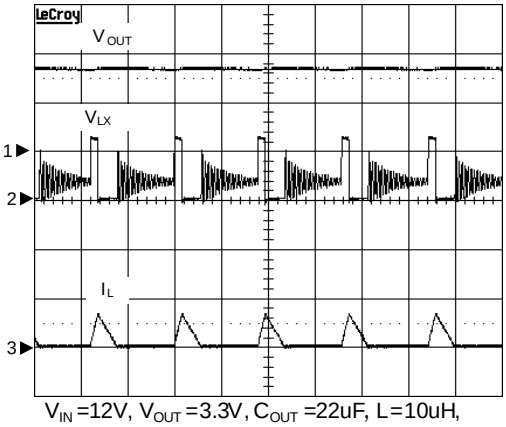
Normal Operation in Heavy Load



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH,
I_{OUT} =2A

CH1: V_{OUT}, 2V/Div, DC
CH2: I_L, 1A/Div, DC
CH3: V_{LX}, 10V/Div, DC
TIME: 2µs/Div

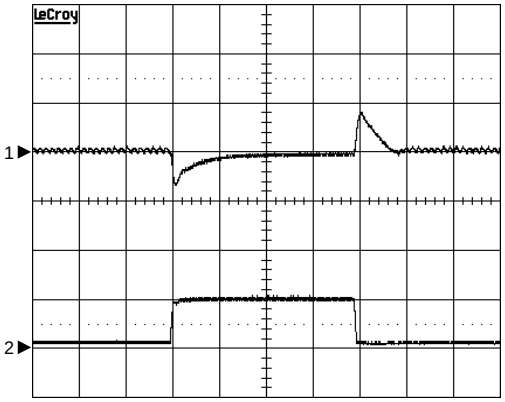
Normal Operation in Light Load



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L=10uH,
I_{OUT} =100mA

CH1: V_{OUT}, 2V/Div, DC
CH2: I_L, 1A/Div, DC
CH3: V_{LX}, 10V/Div, DC
TIME: 5µs/Div

Load Transient



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH,
COMP=6.8kΩ+3.9nF, I_{OUT} =200mA-2A-200mA

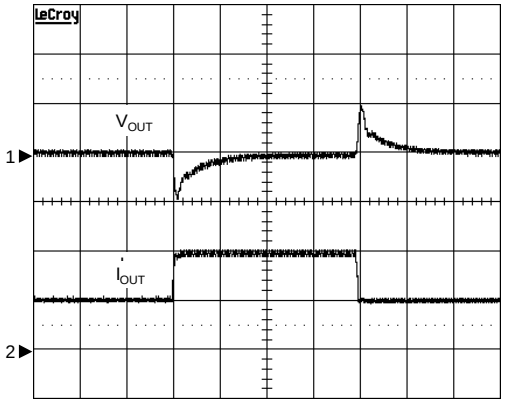
CH1: V_{OUT}, 0.5V/Div, offset=3.3V
CH2: I_{OUT}, 2A/Div, DC
TIME: 50µs/Div

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Operating Waveforms

The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

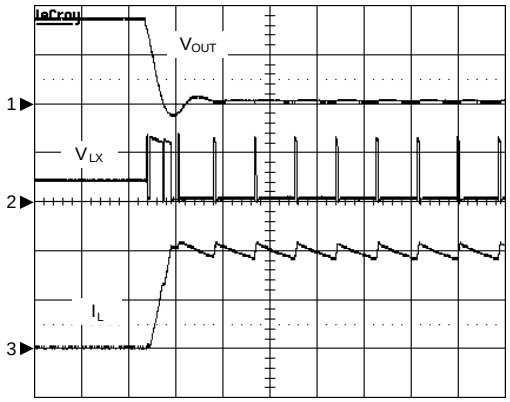
Load Transient



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH,
COMP=6.8kΩ+3.9nF, I_{OUT} =1A-2A-1A

CH1: V_{OUT}, 0.2V/Div, offset=3.3V
CH2: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

Short Circuit



V_{IN} =12V, V_{OUT} =3.3V, C_{OUT} =22uF, L =10uH,
V_{OUT} short to ground

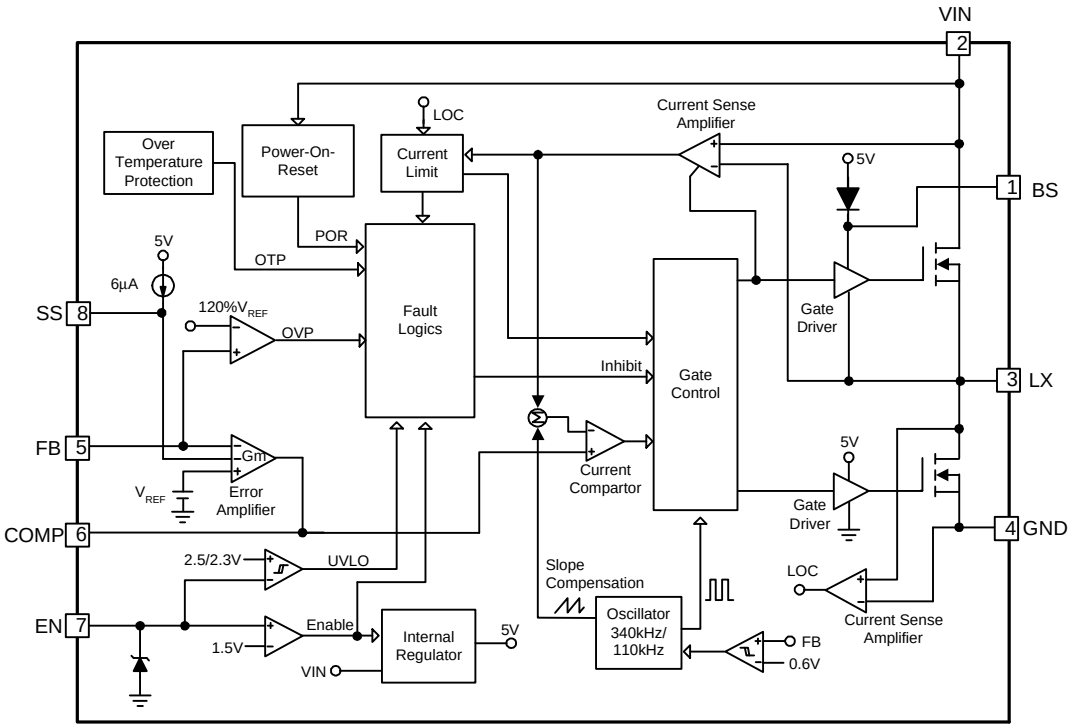
CH1: V_{OUT}, 2V/Div, DC
CH2: V_{LX}, 10V/Div, DC
CH3: I_L, 2A/Div, DC
TIME: 10µs/Div

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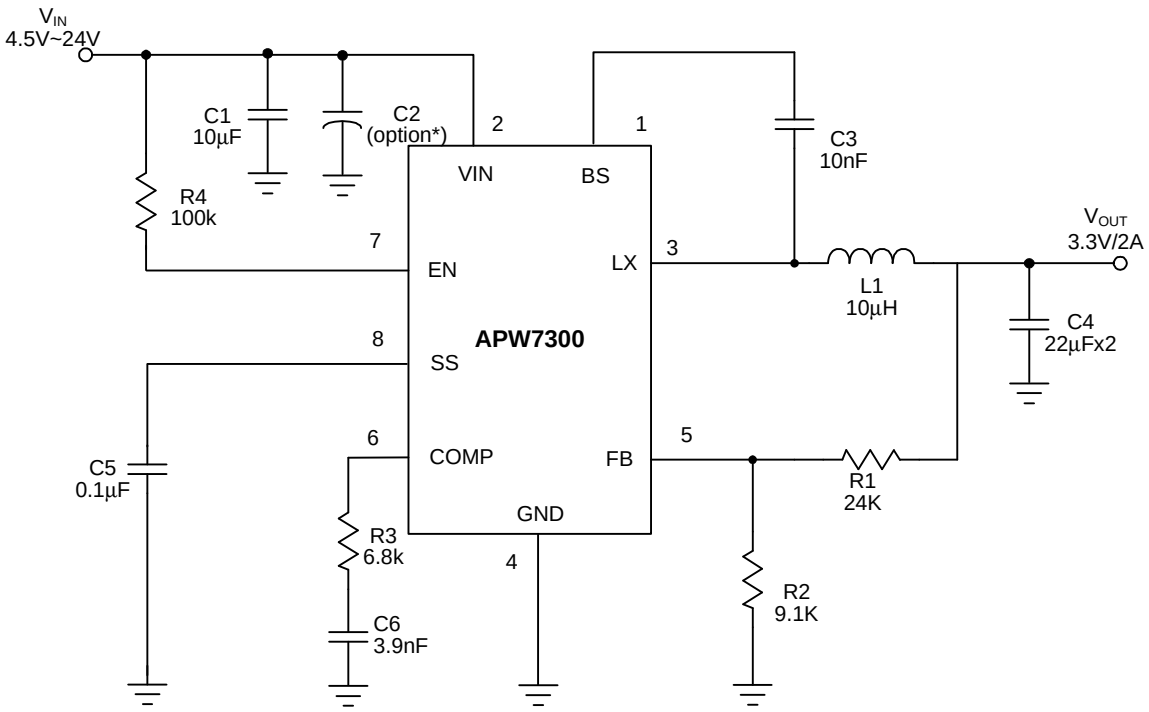
Pin Description

PIN		FUNCTION
SOP-8	NAME	
1	BS	High-Side Gate Drive Boost Input. BS supplies the voltage to drive the high-side N-channel MOSFET. At least 10nF capacitor should be connected from LX to BS to supply the high side switch.
2	VIN	Power Input. VIN supplies the power (4.5V to 24V) to the control circuitry, gate drivers and step-down converter switches. Connecting a ceramic bypass capacitor and a suitably large capacitor between VIN and GND eliminates switching noise and voltage ripple on the input to the IC.
3	LX	Power Switching Output. LX is the Drain of the N-Channel power MOSFET to supply power to the output LC filter.
4	GND	Ground.
5	FB	Output feedback Input. The APW7300 senses the feedback voltage via FB and regulates the voltage at 0.925V. Connecting FB with a resistor-divider from the converter's output sets the output voltage from 0.925V to 20V.
6	COMP	Output of the error amplifier. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. EN threshold is 2.5V with 0.2V hysteresis. Pull up with 100kΩ resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

Block Diagram



Typical Application Circuit



* For cirtical condition, like plug in, the large capacitace and high voltage rating are needed to avoid the high spike voltage.

Recommended Feedback Compensation Value

Vin(V)	V_{OUT}(V)	L1(µH)	C4(µF)	R1(KΩ)	R2(KΩ)	R3(KΩ)	C6(nF)
24	5	10	22(Ceremic)	39	9.1	6.8	3.9
12	5	10	44 (Ceremic)	39	9.1	5	1.5
12	3.3	10	22 (Ceremic)	24	9.1	6.8	3.9
12	2.5	10	22 (Ceremic)	15	9.1	6.8	3.9

Function Description

Main Control Loop

The APW7300 is a constant frequency current mode switching regulator. During normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and would be turned off when an internal current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier (EAMP). An external resistive divider connected between VOUT and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.925V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

VIN Power-On-Reset (POR) and EN Under-voltage Lockout

The APW7300 keep monitoring the voltage on VIN pin to prevent wrong logic operations which may occur when VIN voltage is not high enough for the internal control circuitry to operate. The VIN POR has a rising threshold of 4.05V (typical) with 0.3V of hysteresis.

An external under-voltage lockout (UVLO) is sensed at the EN pin. The EN UVLO has a rising threshold of 2.5V with 0.2V of hysteresis. The EN pin should be connected a resistor divider from VIN to EN .

After the VIN and EN voltages exceed their respective voltage thresholds, the IC starts a start-up process and then ramps up the output voltage to the setting of output voltage.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7300When the junction temperature exceeds T_J=+160°C, a thermal sensor turns off the power MOSFET, allowing the device to cool down. The thermal sensor allows the converter to start a start-up process and regulate the output voltage again after the junction temperature cools by 50°C.

The OTP designed with a 50°C hysteresis lowers the average T_J during continuous thermal overload conditions, increasing life time of the IC.

Enable/Shutdown

Driving EN to ground places the APW7300 in shutdown. When in shutdown, the internal N-Channel power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to 0.3μA.

Current-Limit Protection

The APW7300 monitors the output current, flowing through the N-Channel power MOSFET, and limits the IC from damages during overload, short-circuit and over-voltage conditions.

Frequency Foldback

The foldback frequency is controlled by the FB voltage. When the FB pin voltage is under 0.6V, the frequency of the oscillator will be reduced to 110kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will switch to its designed rate when the feedback voltage on FB rises above the rising frequency foldback threshold (0.6V, typical) again.

Over-Voltage Protection

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increase over 120% of the reference voltage, the over-voltage protection comparator will force the high-and low-side MOSFET gate driver off. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The chip will restore its normal operation.

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Application Information

Setting Output Voltage

The regulated output voltage is determined by:

$$VOUT = 0.925 \times (1 + \frac{R_1}{R_2}) \cdot (V)$$

To prevent stray pickup, please locate resistors R1 and R2 close to APW7300.

Input Capacitor Selection

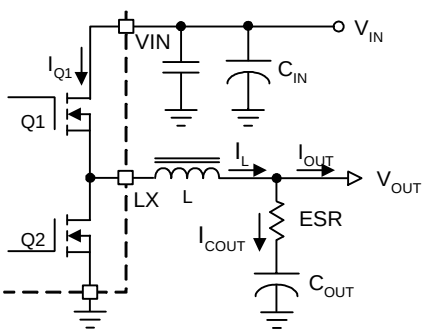
Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time the N-channel power MOSFET (Q1) turns on. Place the small ceramic capacitors physically close to the VIN and between the VIN and GND.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current (IRMS) of the bulk input capacitor is calculated as the following equation:

$$I_{RMS} = I_{OUT}\sqrt{D \times (1-D)} \cdot (A)$$

where D is the duty cycle of the power MOSFET.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.



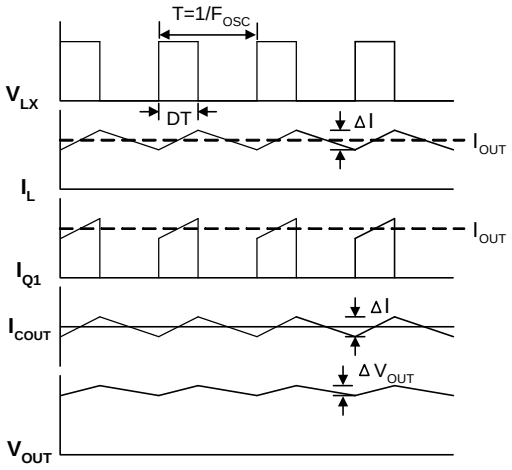
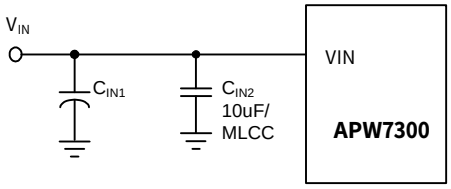


Figure 1. Converter Waveforms

In critical condition, like input voltage plug in, it will cause the high spike voltage. It is recommended to place large capacitance and higher voltage rating to reduce the spike voltage. In general, to parallel a electrolytic capacitor with large capacitance can reduce the spike voltage in critical condition. This electrolytic capacitor must also be short pin wire to make it as close as to the power plane or trace.



Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are the function of the switching frequency and the ripple current (DI). The output ripple is the sum of the voltages, having phase shift, across the ESR and the ideal output capacitor. The peak-to-peak voltage of the ESR is calcuated as the following equations:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{..... (1)}$$

$$\Delta I = \frac{V_{OUT} \times (1-D)}{F_{OSC} \times L} \quad \text{..... (2)}$$

$$V_{ESR} = \Delta I \times ESR \quad \text{..... (3)}$$

Application Information(Cont.)

Output Capacitor Selection (Cont.)

The peak- to-peak voltage of the ideal output capacitor is calculated as the following equations:

$$\Delta V_{COUT} = \frac{\Delta I}{8 \times F_{OSC} \times C_{OUT}} \quad \text{..... (4)}$$

For the applications using bulk capacitors, the ΔV_{COUT} is much smaller than the V_{ESR} and can be ignored. Therefore, the AC peak-to-peak output voltage(ΔV_{OUT}) is shown below:

$$\Delta V_{OUT} = \Delta I \times ESR \cdot (V) \quad \text{..... (5)}$$

For the applications using bulk capacitors, the V_{ESR} is much smaller than the ΔV_{COUT} and can be ignored. Therefore, the AC peak-to-peak output voltage(ΔV_{OUT}) is to ΔV_{COUT}.

The load transient requirements are the function of the slew rate (di/dt) and the magnitude of the transient load urrent. These requirements are generally met with a mix of capacitors and careful layout. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Table1 Capacitor Selection Guide

Vender	Model	Capacitance (µF)	TC	Voltage Rating(V)	Si2e
muRata	GRM31CR61E106K	10	X5R	25	1206
muRata	GRM31CR61C226K	22	X5R	16	1206

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses. The equation (2) shows that the inductance value has a direct effect on ripple current.

Accepting larger values of ripple current allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I \leq 0.4 \times I_{OUT}(max)$. Please be noticed that the maximum ripple current occurs at the maximum input voltage. The minimum inductance of the inductor is calculated by using the following equation:

$$\frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{340000 \cdot L \cdot V_{IN}} \leq 1.2$$

$$L \geq \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{408000 \cdot V_{IN}} \quad (H) \quad \text{..... (6)}$$

where $V_{IN} = V_{IN(MAX)}$

Table2 Inductor Selection Guide

Vender	Part number	Inductance (µH)	DCR (mΩ)	Current Rating(A)
CYNTEC	PCMB063T-100MS	10	62	4
Chilisin	MHCC10040-100M	10	30	6.5
Gausstek	PL94P051M-10U	10	38	3.8

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Application Information (Cont.)

Thermal Consideration

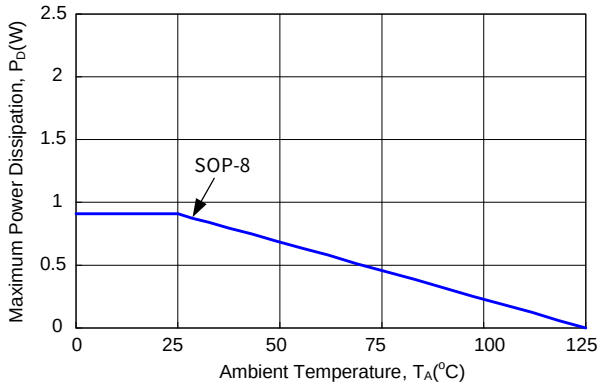
The APW7300 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air.

For normal operation, do not exceed the maximum junction temperature rating of T_J = 125°C. The calculated power dissipation should less than:

$$P_D = (125-25)/110=0.90(W)\text{-----(SOP-8)}$$



Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedance should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separating and finally combined using the ground plane construction or single point grounding. Figure 3 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Begin the layout by placing the power components first. Orient the power circuitry to achieve a clean power flow path. If possible, make all the connections on one side of the PCB with wide, copper filled areas.
2. In Figure 3, the loops with same color bold lines conduct high slew rate current. These interconnecting impedances should be minimized by using wide and short printed circuit traces.
3. Keep the sensitive small signal nodes (FB, COMP) away from switching nodes (LX or others) on the PCB and it should be placed near the IC as close as possible. Therefore, place the feedback divider and the feedback compensation network close to the IC to avoid switching noise. Connect the ground of feedback divider directly to the GND pin of the IC using a dedicated ground trace.
4. Place the decoupling ceramic capacitor C1 near the VIN as close as possible. Use a wide power ground plane to connect the C1, C2, and Schottky diode to provide a low impedance path between the components for large and high slew rate current.

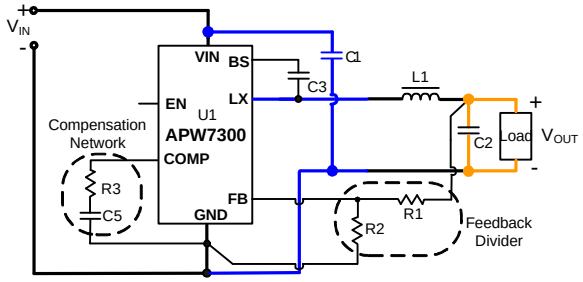


Figure 2. Current Path Diagram

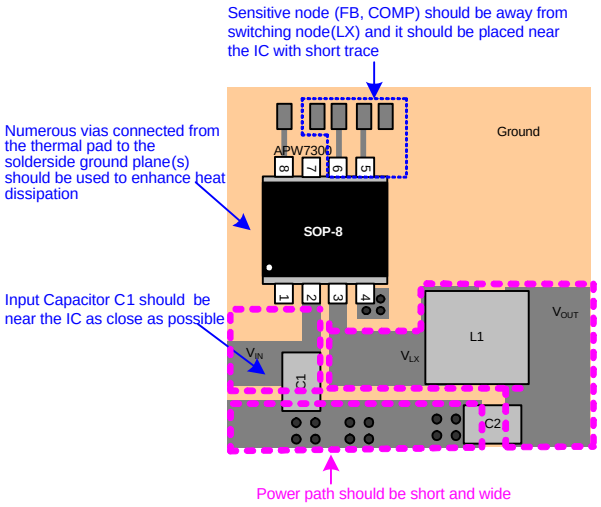
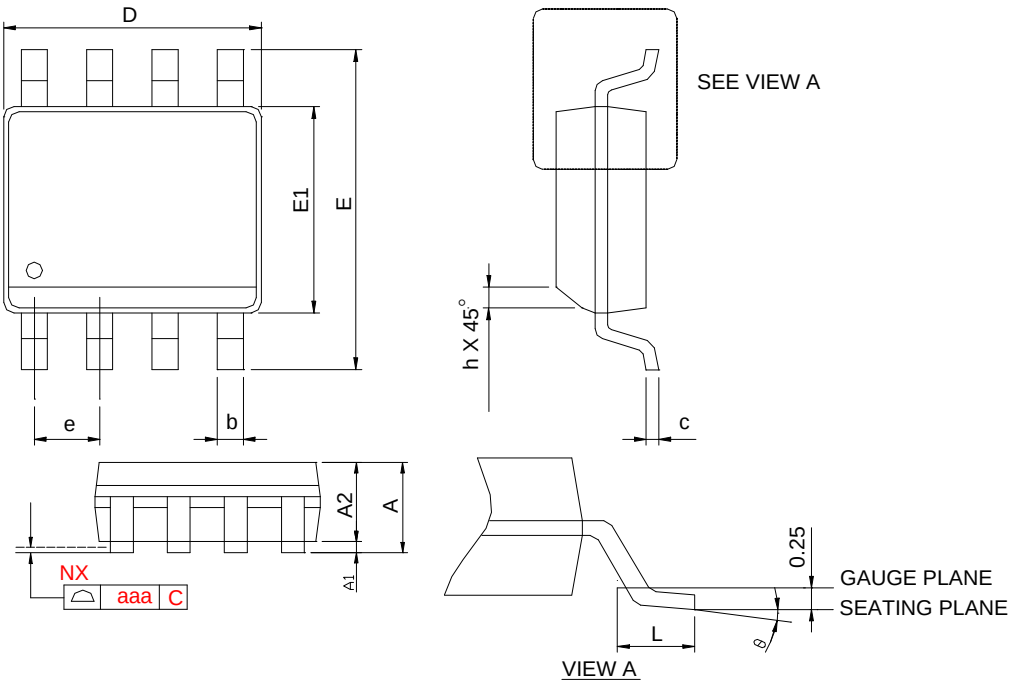


Figure 3. Recommended Layout Diagram

Package Information

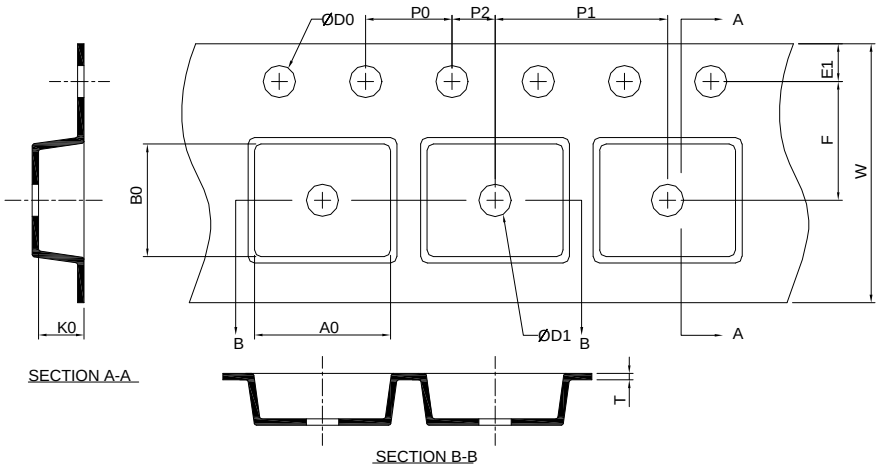
SOP-8

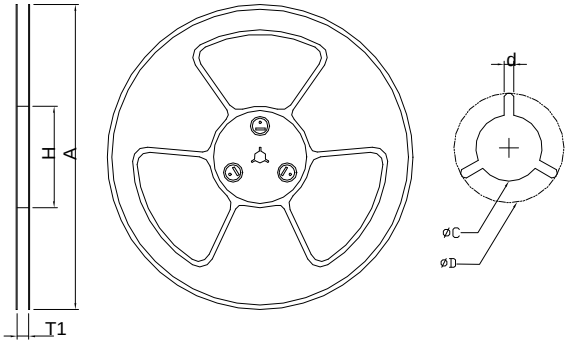


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
aaa	0.10		0.004	

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

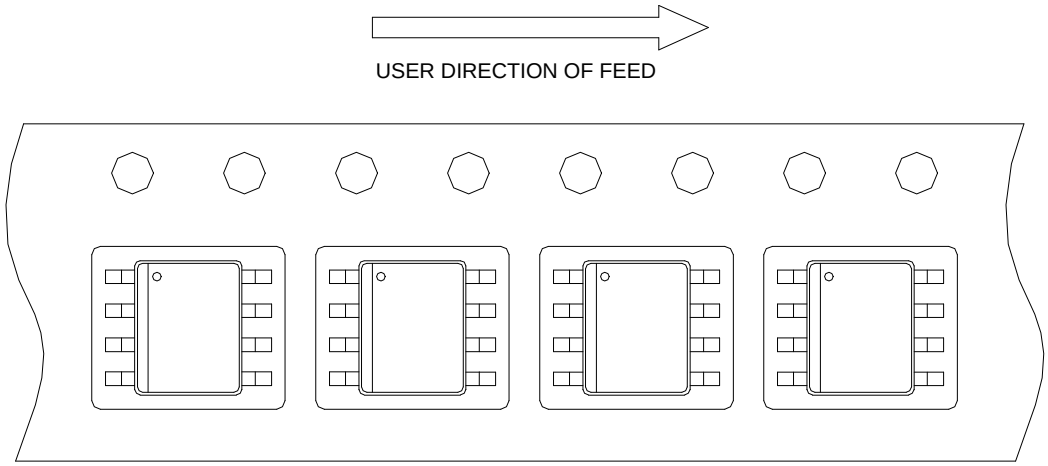
Devices Per Unit

Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

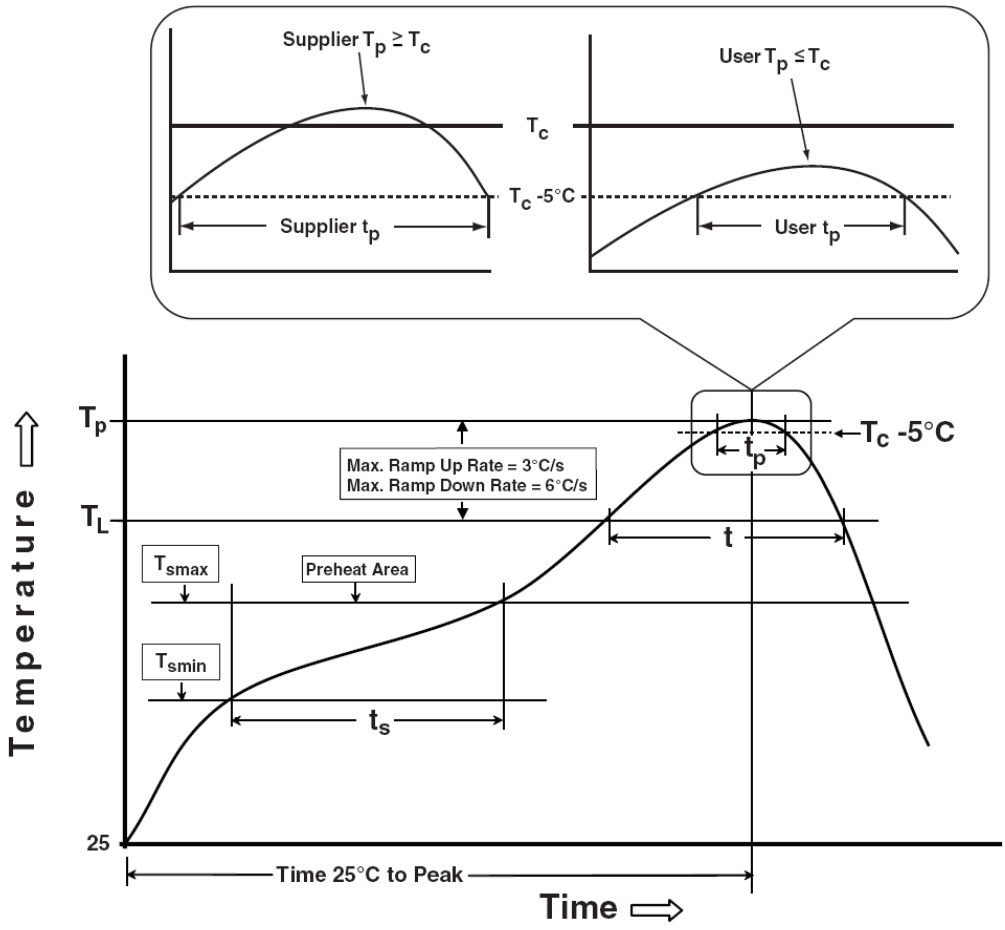
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Taping Direction Information

SOP-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838