Dual Channel 300mA Low Dropout Linear Regulator

Features

- **Dual Regulator Outputs**
- **Low Dropout Voltage: Typical 240mV at 300mA**
- **Wide Input Voltage Range: 2.5V to 5.5V**
- **Low Quiescent Current: Typical 58μA**
- **High PSRR: 70dB at 1kHz**
- **Low Shutdown Current: <1μA**
- **Shutdown Function**
- **Output Current-Limit Protection**
- **Short-Circuit Current-Limit Protection**
- **Over-Temperature Protection**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

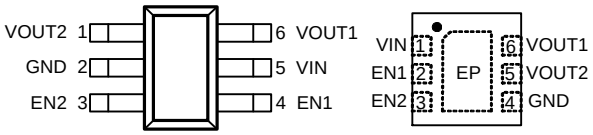
- **Mobile Phone**
- **GPS Navigation**
- **Blue Tooth Headset**

General Description

The APL5537 is a dual channel low dropout linear regulator, which operates from 2.5V to 5.5V input voltage and delivers up to 300mA output current at each channel. Typical dropout voltage is only 240mV at 300mA.

The APL5537 with low quiescent current, high PSRR, and low noise is ideal for battery powered system appliances. Other features include logic-controlled shutdown mode, over-temperature protection, short-circuit current-limit, and current-limit protection to ensure specified output current. The APL5537 is available in the TSOT-23-6A and TDFN 1.6x1.6-6 packages.

Pin Configurations



TSOT-23-6A (Top View) **TDFN1.6x1.6-6 (Top View)**

Ordering and Marking Information

APL5537 □□□□□-□□□ Assembly Material Handling Code Temperature Range Package Code Voltage Code	Voltage Code See Voltage Code Table Package Code CT : TSOT-23-6A QB : TDFN1.6x1.6-6 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL5537-VVCT: 7VVX	VV - Voltage Code X - Date Code
APL5537-VVQB: 7VV X	VV - Voltage Code X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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Voltage Code Table

Output Voltage		Voltage Code	Output Voltage		Voltage Code
V_{OUT1} (V)	V_{OUT2} (V)		V_{OUT1} (V)	V_{OUT2} (V)	
1.30	2.80	7M	1.20	2.80	5M
1.85	1.85	bb	1.85	1.50	b9
1.50	1.50	99	1.50	2.80	9M
1.80	1.20	C5	1.80	2.60	CK
2.50	1.80	JC	1.80	3.30	CR
2.50	3.00	JO	2.50	2.80	JM
2.80	2.85	Ud	2.50	3.30	JR
2.85	2.85	dd	2.85	1.85	db
2.80	1.80	MC	2.85	1.80	dC
2.80	3.30	MR	2.80	2.80	MM
2.80	3.00	MO	3.00	1.80	OC
3.30	2.85	Rd	3.00	3.00	OO
3.30	3.30	RR	3.30	3.00	RO
3.15	2.80	eM	3.30	3.10	RP

Available Voltage Version

Code	5	7	9	A	C	b	D	E	F	J	K
Voltage	1.20	1.30	1.50	1.60	1.80	1.85	1.90	2.00	2.10	2.50	2.60
Code	c	L	M	d	N	O	P	e	Q	R	
Voltage	2.65	2.70	2.80	2.85	2.90	3.00	3.10	3.15	3.20	3.30	

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Input Voltage (VIN to GND)	-0.3 ~ 7	V
V_{EN1}, V_{EN2}	EN1, EN2 to GND Voltage	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)		°C/W
	TSOT-23-6A	220	
	TDFN1.6x1.6-6	165	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

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Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage (VIN to GND)	2.5 ~ 5.5	V
V_{EN1}, V_{EN2}	EN1, EN2 to GND Voltage	0 ~ 5.5	V
I_{OUT}	VOUT Output Current	0 ~ 300	mA
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=V_{OUT}+1V, V_{EN1}= V_{EN2}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

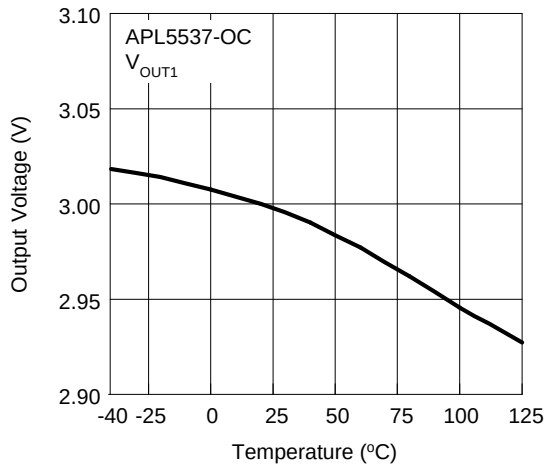
Symbol	Parameter	Test Conditions		APL5537			Unit
				Min.	Typ.	Max.	
UNDER-VOLTAGE LOCKOUT (UVLO) AND SUPPLY CURRENT							
	VIN UVLO Threshold Voltage	V_{IN} rising, T_A= -40 to 85 °C		1.9	2.2	2.45	V
	VIN UVLO Hysteresis			-	0.1	-	V
I_Q	VIN Supply Current	No load, V_{EN1}= V_{EN2}=5V		-	58	90	µA
		No load, V_{EN1}= V_{EN2}=0V		-	-	1	µA
OUTPUT VOLTAGE (REGULATOR1 AND REGULATOR2)							
	Output Voltage Accuracy	I_{OUT}=1mA, T_A= 25 °C		-1	-	+1	%
		I_{OUT}=1mA to 300mA, T_A= -40 °C to 85 °C		-3	-	+3	%
	Line Regulation	I_{OUT}=1mA, V_{IN}=V_{OUT}+0.3V to 5.5V, or V_{IN}=2.5V to 5.5V		-	-	0.2	%/V
	Load Regulation	I_{OUT}=1mA to 300mA		-	-	0.6	%
V_{DROP}	Dropout Voltage (Note 4)	I_{OUT}=300mA		-	240	330	mV
PSRR	Power Supply Rejection Ratio	I_{OUT}=50mA, C_{OUT}=2.2µF	f=100Hz	-	70	-	dB
			f=1kHz	-	70	-	
			f=10kHz	-	60	-	
			f=100kHz	-	35	-	
	Output Noise	I_{OUT}=1mA, BW=10 to 100kHz, C_{OUT}=10µF		-	100	-	μV_{RMS}
	VOUT Discharge Resistance	V_{EN1}= V_{EN2}=0V		-	0.7	-	kΩ
ENABLE/DISABLE (EN1 AND EN2)							
V_{IH}	EN Input Logic HIGH	V_{IN}=2.5V to 5.5V		1.5	-	-	V
V_{IL}	EN Input Logic LOW	V_{IN}=2.5V to 5.5V		-	-	0.4	V
	EN Input Current	V_{EN1}= V_{EN2}=5V		-	0.2	-	µA
PROTECTIONS (REGULATOR1 AND REGULATOR2)							
I_{LIMIT}	Current Limit Threshold			330	450	750	mA
I_{SHORT}	Short-Circuit Output Current			-	50	-	mA
	Over-Temperature Threshold			-	160	-	°C
	Over-Temperature Hysteresis			-	40	-	°C
	Soft-Start Time			-	60	-	µs

Note 4: The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 1V.

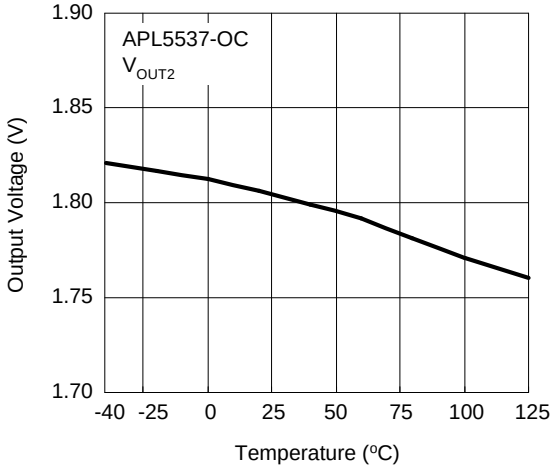
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Typical Operating Characteristics

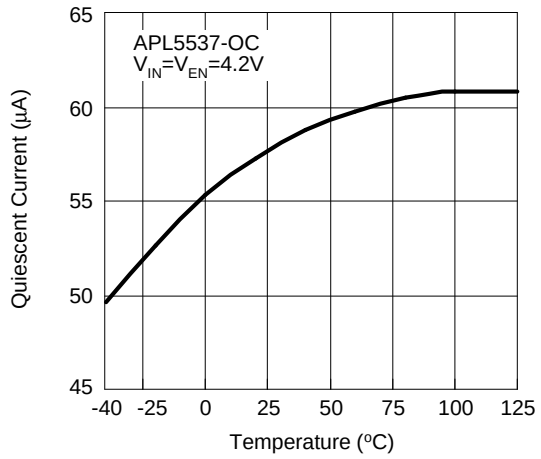
Output Voltage vs. Temperature



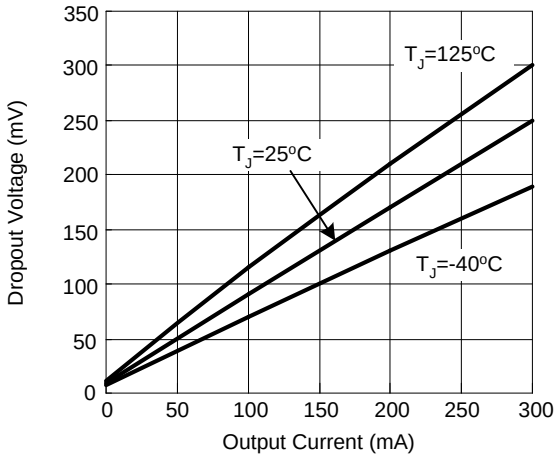
Output Voltage vs. Temperature



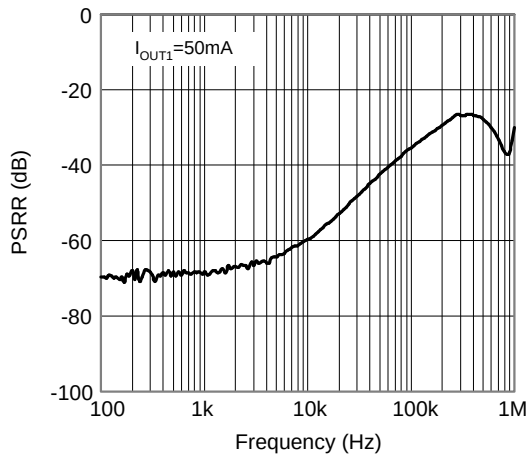
Quiescent Current vs. Temperature



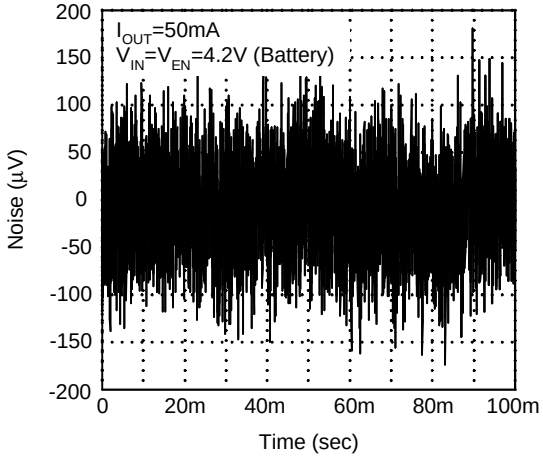
Dropout Voltage vs. Output Current



PSRR vs. Frequency



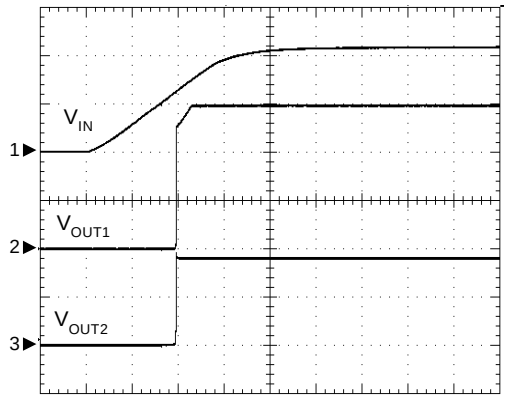
Noise



Operating Waveforms

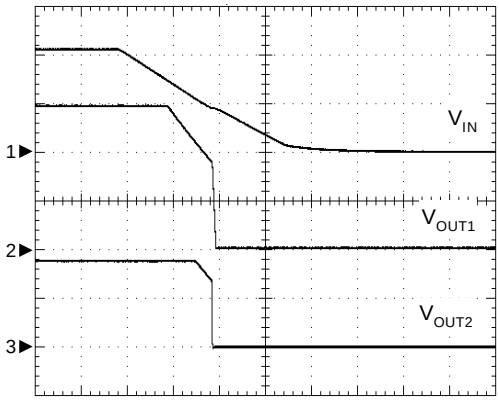
Refer to the typical application circuit. The test condition is V_{IN}=V_{EN}=4.2V, T_A= 25°C. Unless otherwise specified.

Power on



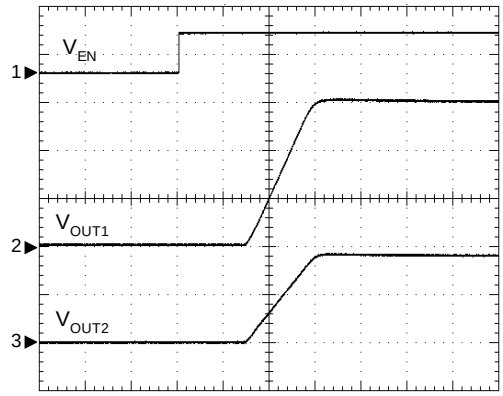
C_{IN}=C_{OUT}=1µF, I_{OUT1}=I_{OUT2}=10mA
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
TIME: 4ms/Div

Power off



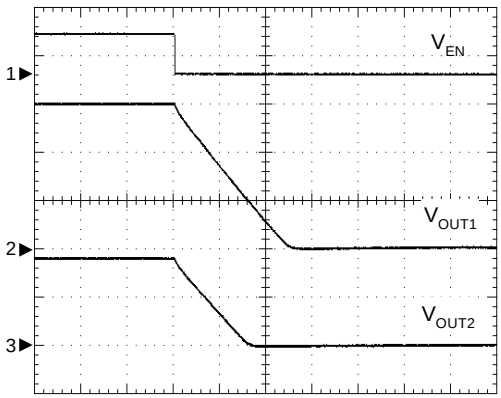
C_{IN}=C_{OUT}=1µF, I_{OUT1}=I_{OUT2}=10mA
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
TIME: 4ms/Div

Enable Response



C_{IN}=C_{OUT}=1µF, I_{OUT1}=I_{OUT2}=10mA
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
TIME: 40µs/Div

Disable Response



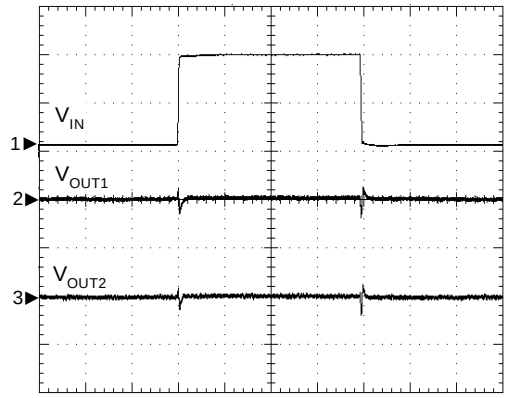
C_{IN}=C_{OUT}=1µF, I_{OUT1}=I_{OUT2}=50mA
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
TIME: 40µs/Div

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Operating Waveforms (Cont.)

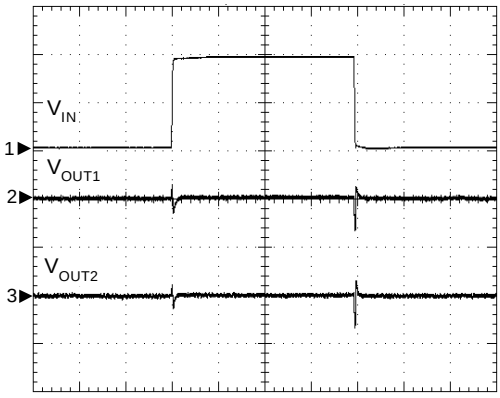
Refer to the typical application circuit. The test condition is V_{IN}=V_{EN}=4.2V, T_A= 25°C. Unless otherwise specified.

Line Transient Response



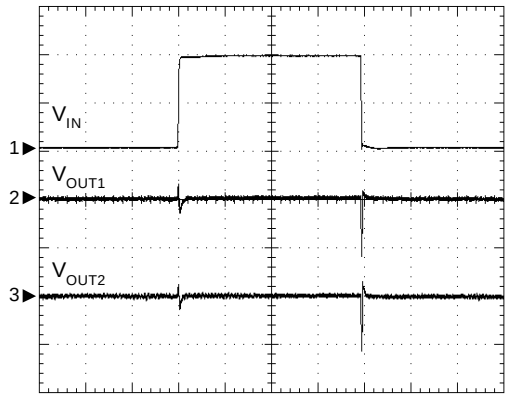
V_{IN}=3.8V to 4.8V to 3.8V (rise / fall time = 4μs)
C_{IN}=C_{OUT}=1μF, I_{OUT1}=I_{OUT2}=10mA
CH1: V_{IN}, 500mV/Div, DC, Offset=3.8V
CH2: V_{OUT1}, 20mV/Div, DC, Offset=3.0V
CH3: V_{OUT2}, 20mV/Div, DC, Offset=1.8V
TIME:100μs/Div

Line Transient Response



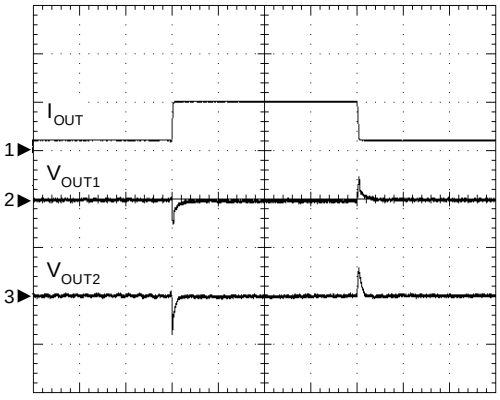
V_{IN}=3.8V to 4.8V to 3.8V (rise / fall time = 4μs)
C_{IN}=C_{OUT}=1μF, I_{OUT1}=I_{OUT2}=50mA
CH1: V_{IN}, 500mV/Div, DC, Offset=3.8V
CH2: V_{OUT1}, 20mV/Div, DC, Offset=3.0V
CH3: V_{OUT2}, 20mV/Div, DC, Offset=1.8V
TIME:100μs/Div

Line Transient Response



V_{IN}=3.8V to 4.8V to 3.8V (rise / fall time = 4μs)
C_{IN}=C_{OUT}=1μF, I_{OUT1}=I_{OUT2}=100mA
CH1: V_{IN}, 500mV/Div, DC, Offset=3.8V
CH2: V_{OUT1}, 20mV/Div, DC, Offset=3.0V
CH3: V_{OUT2}, 20mV/Div, DC, Offset=1.8V
TIME:100μs/Div

Load Transient Response



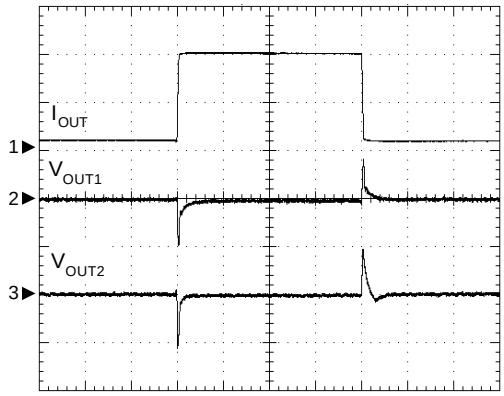
I_{OUT}=10mA to 50mA to 10mA (rise / fall time = 1μs)
C_{IN}=C_{OUT}=1μF, V_{IN}=V_{EN}=4.2V
CH1: I_{OUT}, 50mA/Div, DC
CH2: V_{OUT1}, 20mV/Div, DC, Offset=3.0V
CH3: V_{OUT2}, 20mV/Div, DC, Offset=1.8V
TIME:40μs/Div

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Operating Waveforms (Cont.)

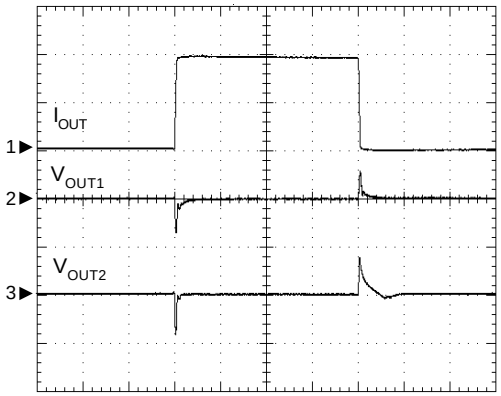
Refer to the typical application circuit. The test condition is V_{IN}=V_{EN}=4.2V, T_A= 25°C. Unless otherwise specified.

Load Transient Response



I_{OUT}=10mA to 100mA to 10mA (rise / fall time = 1µs)
C_{IN}=C_{OUT}=1µF, V_{IN}=V_{EN}=4.2V
CH1: I_{OUT}, 50mA/Div, DC
CH2: V_{OUT1}, 20mV/Div, DC, Offset=3.0V
CH3: V_{OUT2}, 20mV/Div, DC, Offset=1.8V
TIME:40µs/Div

Load Transient Response



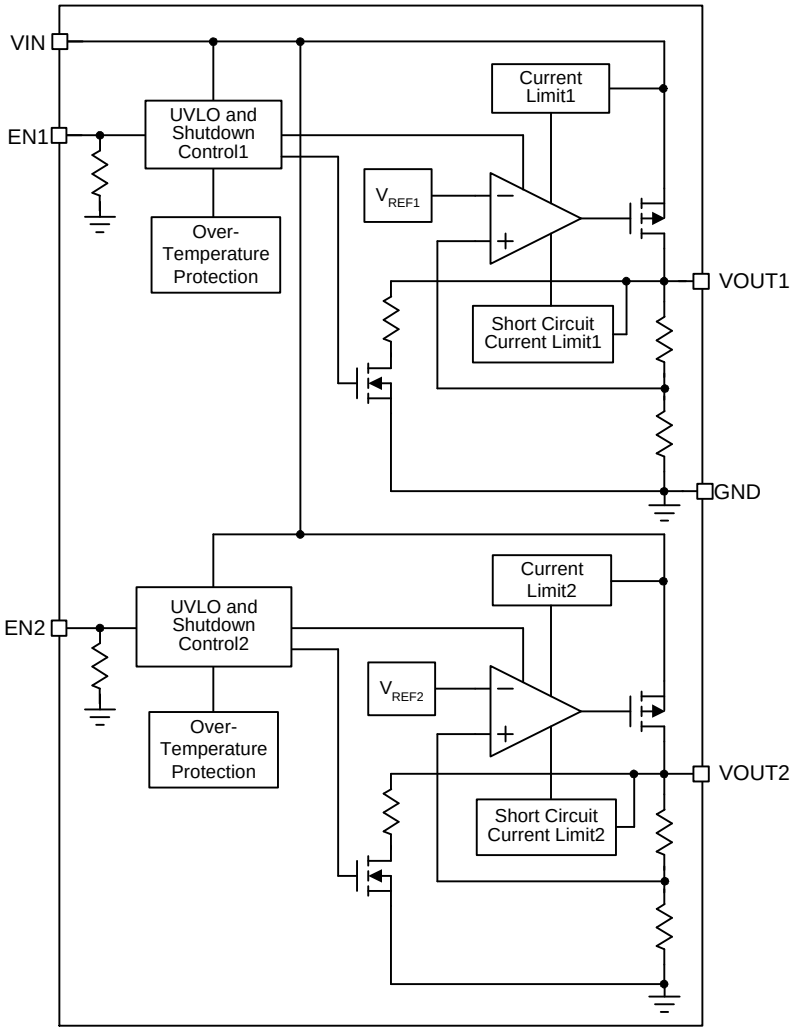
I_{OUT}=10mA to 200mA to 10mA (rise / fall time = 1µs)
C_{IN}=C_{OUT}=1µF, V_{IN}=V_{EN}=4.2V
CH1: I_{OUT}, 100mA/Div, DC
CH2: V_{OUT1}, 50mV/Div, DC, Offset=3.0V
CH3: V_{OUT2}, 50mV/Div, DC, Offset=1.8V
TIME:40µs/Div

Pin Description

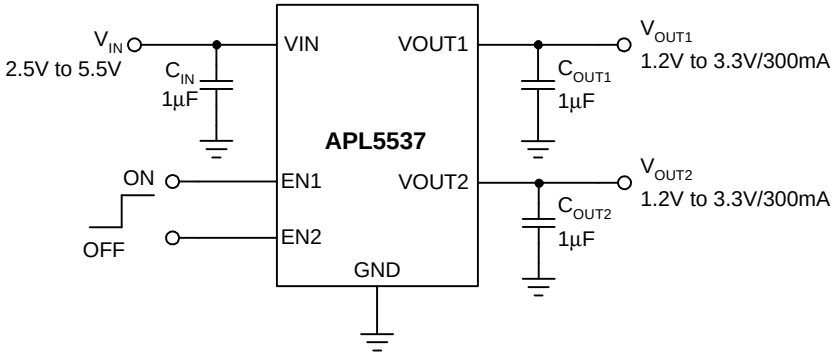
PIN		NAME	FUNCTION
NO.			
TSOT-23-6A	TDFN1.6x1.6-6		
5	1	VIN	Input Supply Pin. V_{IN} can range from 2.5V to 5.5V and should be bypassed with at least a 1µF capacitor.
4	2	EN1	Enable Input. Pulling the $V_{EN1/2}$ above 1.5V enables the respective regulator output; pulling $V_{EN1/2}$ below 0.4V disables the respective regulator output.
3	3	EN2	
2	4	GND	Ground.
1	5	VOUT2	Regulator Outputs. Sources up to 300mA. Bypass with at least a 1µF capacitor to the GND respectively.
6	6	VOUT1	
-	-	EP	Exposed Pad. Connect it to a large ground plane for heatsinking.

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Block Diagram



Typical Application Circuit



Function Description

VIN Under-Voltage Lockout (UVLO)

The APL5537 has a built-in under-voltage lockout circuit to keep the outputs shuting off until internal circuitry is operating properly. The UVLO circuit has a hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input.

Soft-Start (For Each Channel)

The APL5537 provides an internal soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The output voltage starts the soft-start at approximate 60μs after the VIN is over the UVLO threshold. The typical soft-start interval is about 60μs.

Current-Limit Protection (For Each Channel)

The APL5537 provides a current-limit protection function. During current limit, the device limits output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period.

Short-Circuit Current-Limit Protection (For Each Channel)

When the output voltage drops below 0.8V, which is caused by the over load or short circuit, the device limits the output current down to a safe level. The short circuit current limit is used to reduce the power dissipation during short circuit conditions. If the junction temperature is over the over-temperature threshold, the device will enter the thermal shutdown.

Enable/Disable (For Each Channel)

Pulling the $V_{EN1/2}$ above 1.5V enables the respective LDO output, and pulling $V_{EN1/2}$ below 0.4V disables the respective LDO output. When both the LDO outputs are disabled, the supply current is reduced to less than 1μA. EN1/2 pins are internally pulled low by resistors. If shutdown function is not used, connect EN1/2 to VIN for normal operation. The enable inputs are compatible with both TTL and CMOS logic levels.

Over-Temperature Protection

An over-temperature protection circuitry limits the junction temperature of APL5537. When the junction temperature exceeds +160°C, the over-temperature protection circuitry disables the LDO outputs, allowing the device to cool down. The LDO outputs are enabled again after the junction temperature cools down by 40°C, resulting in a pulsed output during continuous thermal overload conditions. Over-temperature protection is designed to protect the IC in the event of over temperature conditions. For reliable operation, the junction temperature cannot exceed T_J=+125°C

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Application Information

Input Capacitor

The APL5537 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limit the slew rate of the surge current, place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 1µF and a minimum ceramic capacitor of 1µF is necessary.

Output Capacitor

The APL5537 needs a proper output capacitor to maintain circuit stability and improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 1µF. With X5R and X7R dielectrics, 1µF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR, Figure 1. shows the curves of allowable ESR range as the function of load current for various output capacitor values.

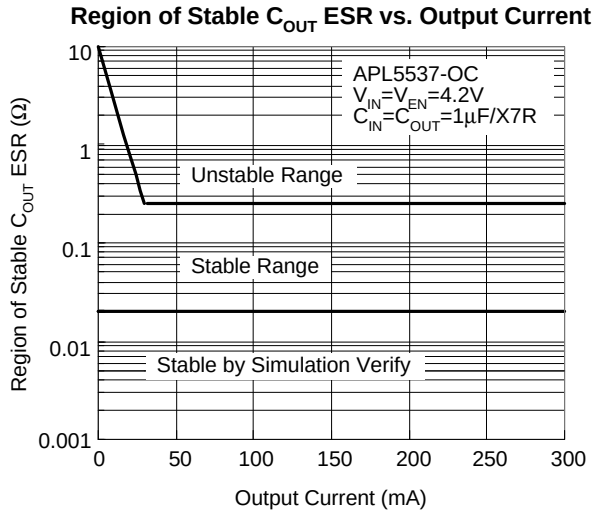


Figure1. Stable C_{OUT} ESR Range

Operation Region and Power Dissipation

The APL5537 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The TDFN1.6x 1.6-6 package power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. Assuming the T_A=25°C and maximum T_J=160°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

P_D(max)=(160-25)/165 = 0.82(W)

For normal operation, do not exceed the maximum junction temperature rating of T_J = 125°C. The calculated power dissipation should be less than:

P_D =(125-25)/165 = 0.61(W)

The GND provides an electrical connection to the ground and channels heat away. Connect the GND to the ground by using a large pad or a ground plane.

Layout Consideration

Figure 2 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Ceramic capacitors for load must be placed near the load as close as possible.
3. To place APL5537 and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 2, must have wide tracks.

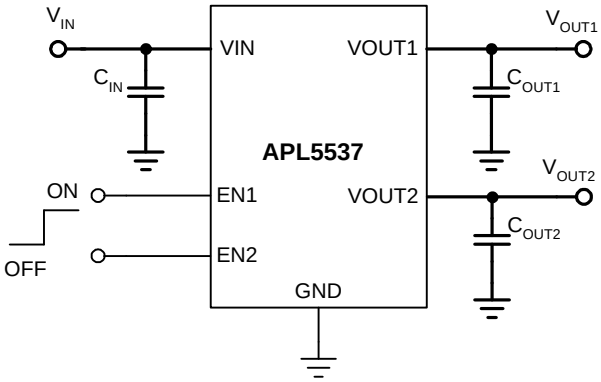
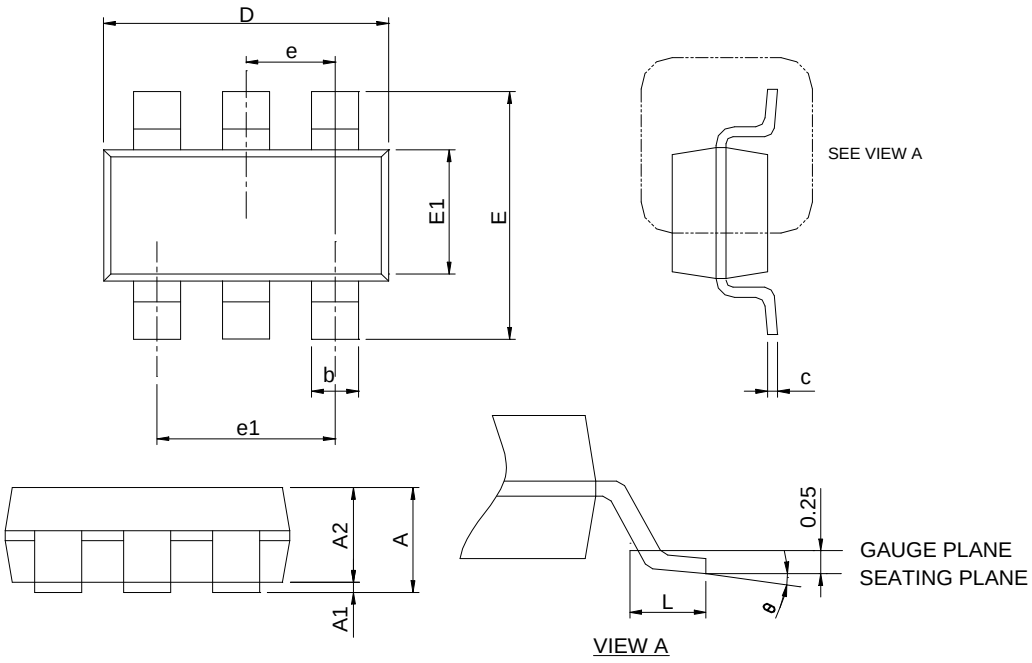


Figure2. Large Current Paths

Package Information

TSOT-23-6A



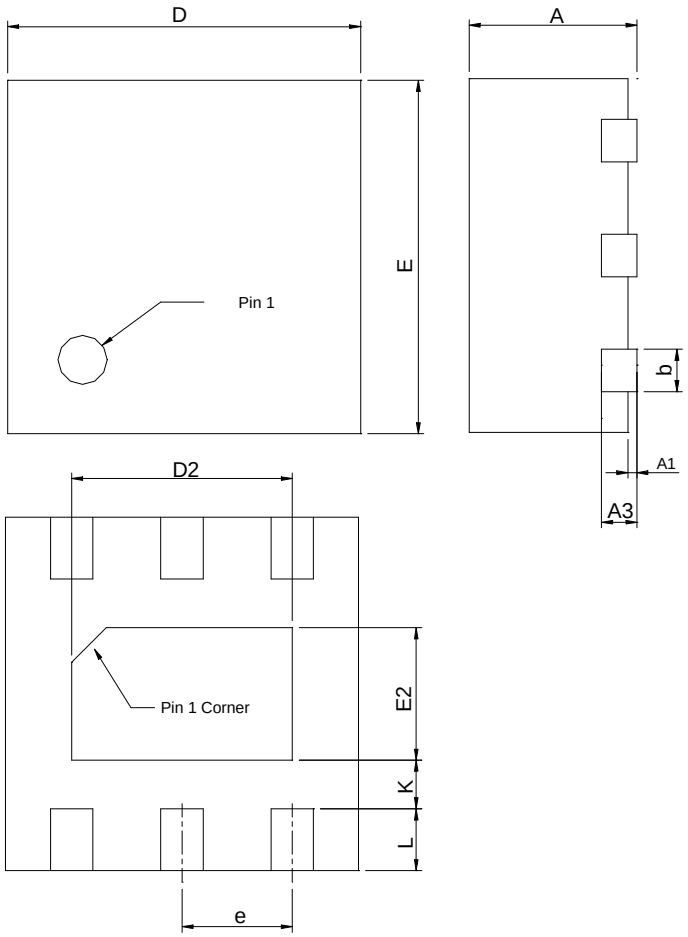
SYMBOL	TSOT-23-6A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

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Package Information (Cont.)

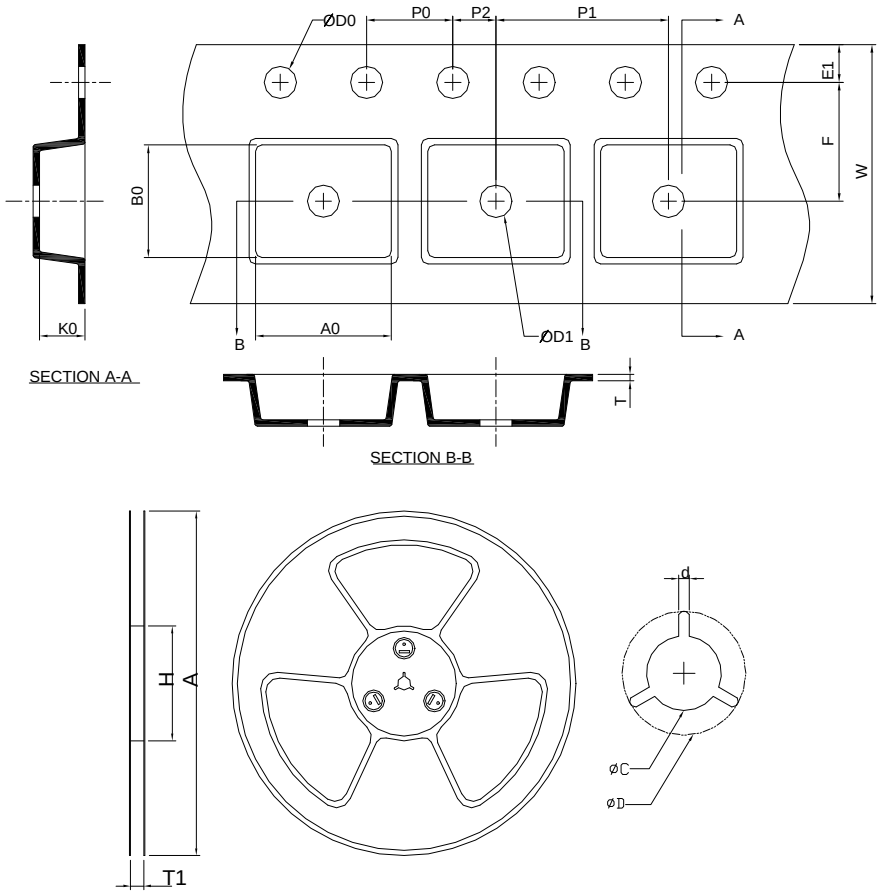
TDFN1.6x1.6-6



SYMBOL	TDFN1.6x1.6-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	1.55	1.65	0.061	0.065
D2	0.95	1.05	0.037	0.041
E	1.55	1.65	0.061	0.065
E2	0.55	0.65	0.022	0.026
e	0.50 BSC		0.020 BSC	
K	0.20	-	0.008	-
L	0.19	0.29	0.007	0.011

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSOT-23-6A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN1.6x1.6-6	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.90±0.20	1.90±0.20	1.30±0.20

(mm)

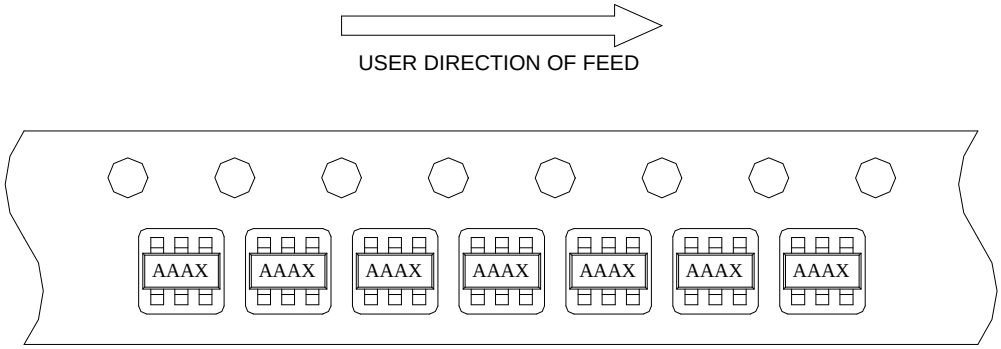
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Devices Per Unit

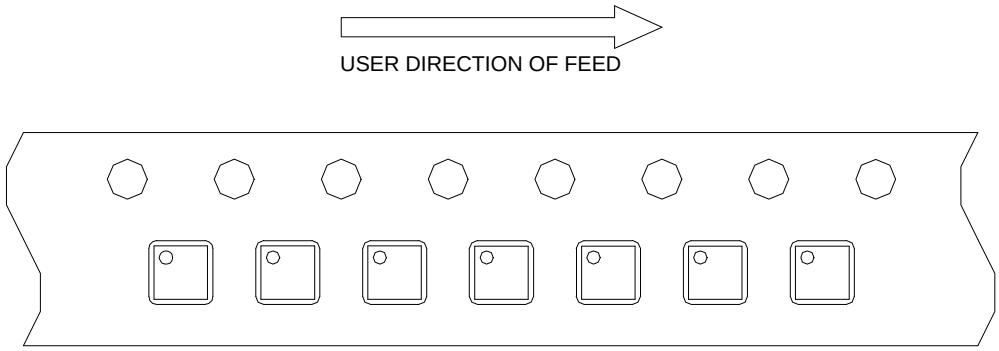
Package Type	Unit	Quantity
TSOT-23-6A	Tape & Reel	3000
TDFN1.6x1.6-6	Tape & Reel	3000

Taping Direction Information

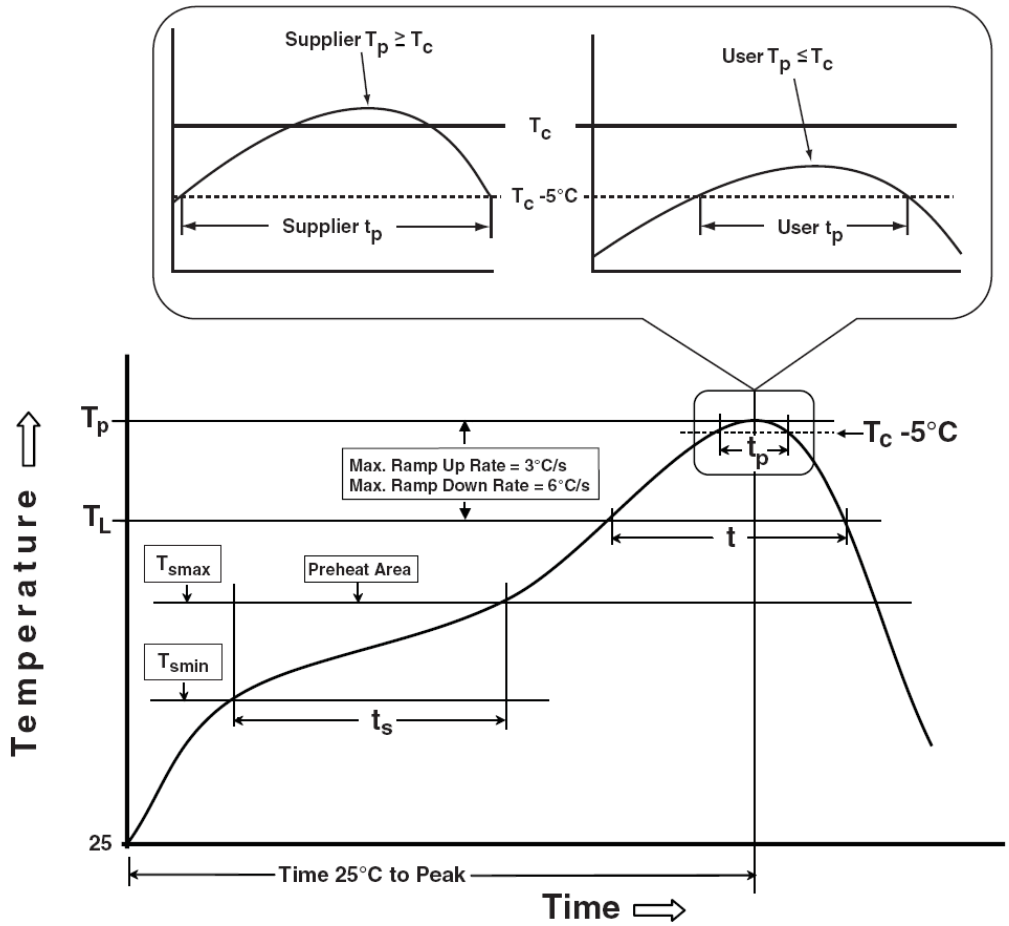
TSOT-23-6A



TDFN1.6x1.6-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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