Advanced Semiconductor Business Inc.

Plerow APL4500

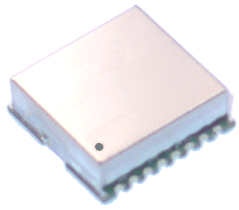
PLL Module

Features

- -4 dBm Output Level at 4500 MHz
- Channel Step Size : 1000 kHz
- 2nd Harmonic : < 0 dBc
- Spurious Level : < -70 dBc
- Lock Time : < 10 ms
- 25 mA Current Consumption

Description

The plerow™ PLL synthesizer module was designed for use in wireless and wireline systems in a wide range of frequency from 50 MHz to 6 GHz. ASB's PLL provides exceptionally low spurious and phase noise performance with fast locking time and low current consumption. All products are available in a surface-mount type package.



Specifications

Parameter	Unit	Min.	Typical	Max.
Frequency Range	MHz		4500	
Output Power	dBm	-5	-4	-3
Supply Voltage	V	4.7	5.0	5.3
Current Consumption	mA		25	35
Channel Step Size	kHz		1000	
2nd Harmonics	dBc		-4	0
Spurious Level	dBc		-78	-70
Lock Time	ms		3	10
Reference Frequency	MHz		10	
Reference Input Level	dBm	-5	0	5
Phase Noise (C / N)				
@ 10 kHz	dBc/Hz	-96	-93	-90
@ 100 kHz	dBc/Hz	-123	-120	-117
Output Impedance	Ω		50	
Operating Temp. Range	°C	-40	25	85
Package Type & Size	Mm	SMT, 19.0W×19.0L×5.8H		

1) Measurement conditions are as follows: T = 25°C, V_{CC} = 5 V, Freq. = 4500 MHz, 50 ohm system.

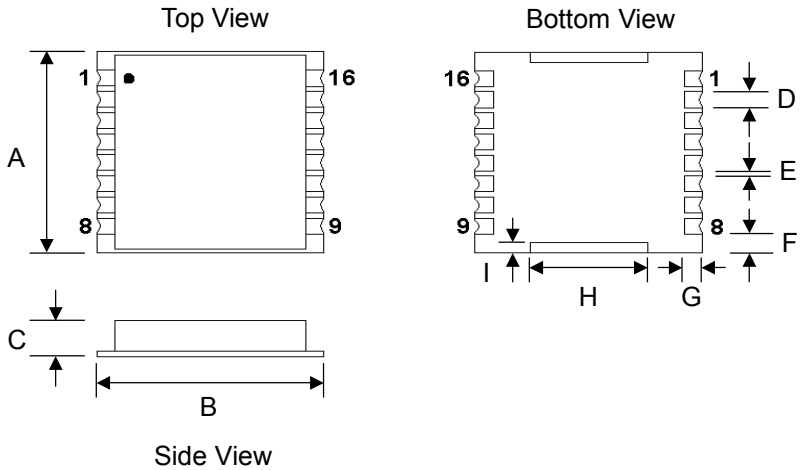
More Information

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Outline Drawing



Pin Configuration	
1	CLOCK
2	DATA
3	ENABLE
4	OSC IN
9	VCC (VCO)
13	RF OUT
15	VCP (PLL)
16	LOCK DETECT
Others	Ground

Dimension (mm)	
A	19.0
B	19.0
C	5.8
D	1.5
E	0.5
F	1.75
G	1.35
H	15.0
I	0.9
Tolerance: ± 0.2	