NEW PRODUCT

AP3591

SINGLE PHASE SYNCHRONOUS BUCK CONTROLLER

Description

The AP3591 is a synchronous adaptive on-time buck controller providing high efficiency, excellent transient response and high DC output accuracy for low voltage regulation in notebook application.

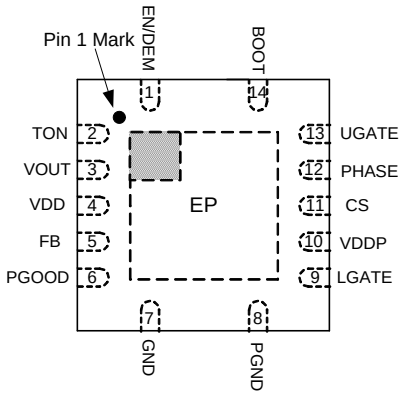
The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and features small external component count and fast transient response.

The operation mode is selectable by EN voltage. A Diode Emulation Mode (DEM) is activated for increasing efficiency at light loads, while PWM mode is activated only for low noise operation. The AP3591 also integrates internal Soft-start, UVLO, OVP, OTP, and programmable OCP to protect the circuit. A Power Good signal is employed to monitor the output voltage.

The AP3591 is available in U-QFN3535-14 package.

Pin Assignments

(Top View)



U-QFN3535-14

Features

- Fixed Frequency Constant On-time Control; Resistor Programmable Frequency Adjustable from 100kHz to 700kHz
- Good Stability Independent of the Output Capacitor ESR
- Quick Load Step Response
- Input Voltage Range: 4.5V to 26V
- Output Voltage Range: 0.75V to 5.5V
- CCM/DEM Mode Selection
- Integrated Bootstrap Diode
- Resistor Programmable Current Limit by Low-side R_{DS_ON} Sense
- Integrated Negative Over Current Limit
- Integrated OVP/UVP and Over Thermal Shutdown Function
- Power Good Indicator
- Internal Soft-start
- Integrate Output Discharge (Soft-stop)
- Safe Start-up into Pre-biased Loads
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3**)

Applications

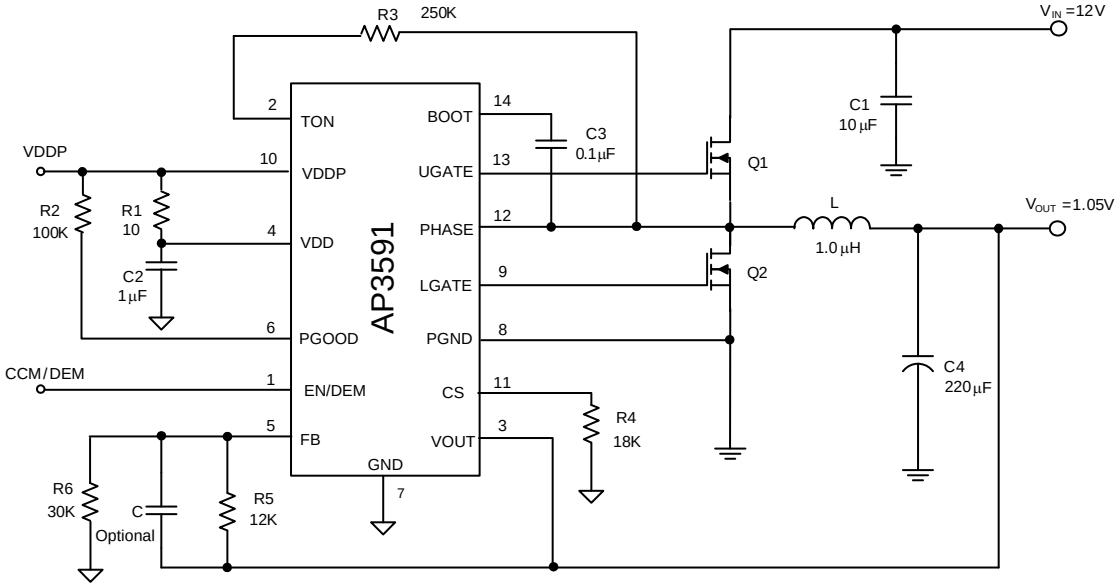
- Notebook Computer, AIO PC
- Low-voltage Distribute Power
- I/O Supplies

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit



BOM

Symbol	Value	Description	Manufacturer	Part Number
C1	10µF/25V	ESR < 4mΩ @400kHz	Murata	GRM31CR61E106KA12
C4	220µF/6.3V	ESR < 9mΩ @300kHz	Sanyo	6SVPE220M
L	1.0µH	DCR < 4mΩ, I_{MAX} = 24A	Vishay	IHLP5050CEER1R0M01
Q1	N-MOSFET	I_{DMAX} = 30A, $R_{DS(ON)}$ = 14mΩ	Infineon	BSC119N03S
Q2	N-MOSFET	I_{DMAX} = 30A, $R_{DS(ON)}$ = 14mΩ	Infineon	BSC119N03S

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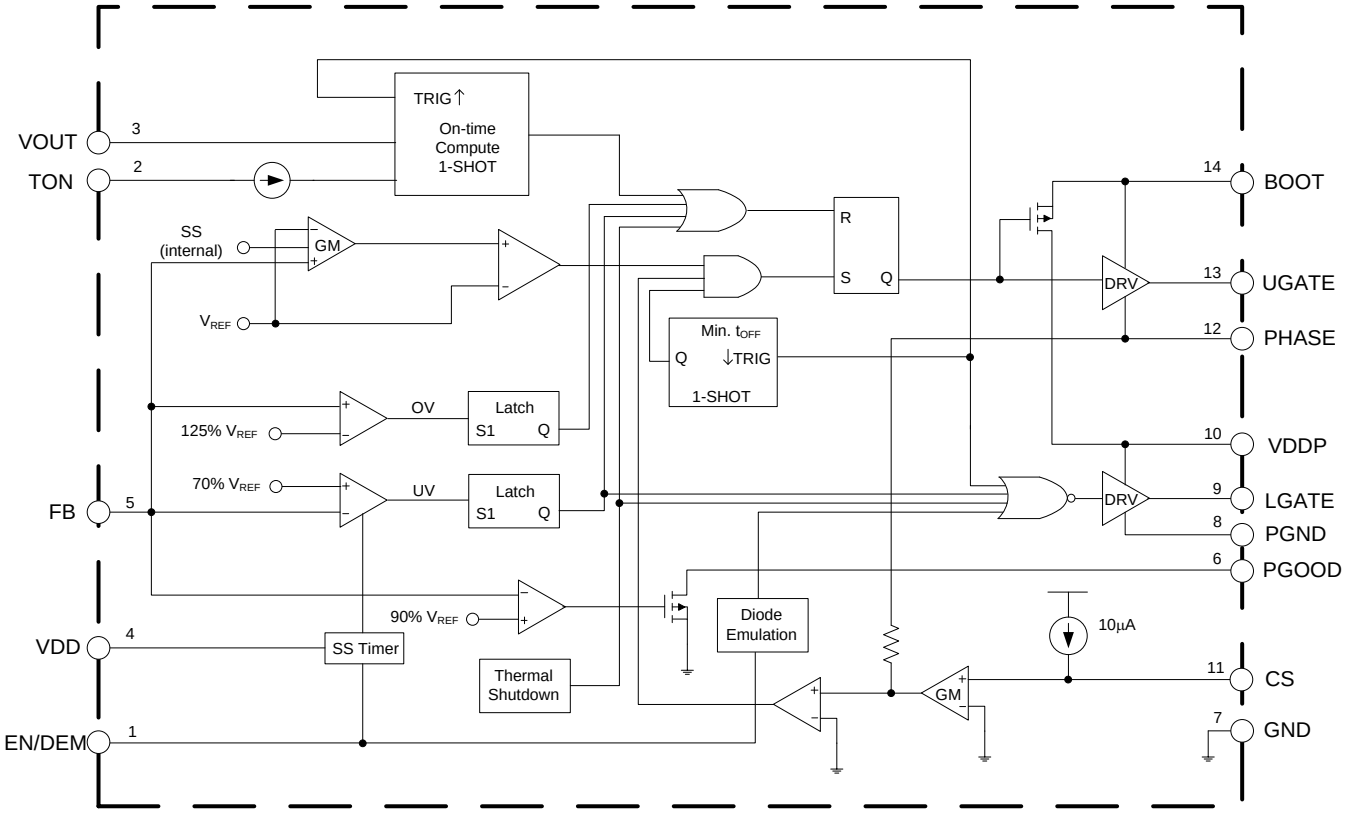
Pin Descriptions

Pin Number	Pin Name	Function
1	EN/DEM	Enable/Diode Emulation Mode control input. Connect to VDD for DEM mode; connect to GND for shutdown and float the pin for CCM mode
2	TON	On time/Frequency adjustment pin. Connect to PHASE through a resistor. TON is an input for the PWM controller
3	VOUT	Output voltage pin. Connect to the output of PWM converter. VOUT is an input for the PWM controller
4	VDD	Analog supply voltage input for the internal analog integrated circuit. Bypass to GND with a 1µF ceramic capacitor
5	FB	Feedback input pin. Connect FB pin to a resistor voltage divider from VOUT to GND to adjust V_{OUT} from 0.75V to 3.3V
6	PGOOD	Power good signal open-drain output for PWM converter. This pin will be pulled high when the output voltage is within the target range
7	GND	Analog Ground
8	PGND	Power Ground
9	LGATE	Low-side N-MOSFET gate driver output for the PWM converter. This pin swings between PGND and VDDP
10	VDDP	VDDP is the gate driver supply for external MOSFETs. Bypass to GND with a 1µF ceramic capacitor
11	CS	Over current trip point set input. Connect a resistor from this pin to signal ground to set threshold for both over current limit and negative over current limit
12	PHASE	The UGATE High-side gate driver return. Also serves as anode of over current comparator
13	UGATE	High-side N-MOSFET floating gate driver output for the PWM converter. This pin swings between PHASE and BOOT
14	BOOT	Bootstrap pin. A bootstrap capacitor is connected for PWM converter. Connect to an external ceramic capacitor to PHASE
–	Exposed Pad	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation

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Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{DD}, V_{DDP}	Supply Voltage	-0.3 to 6	V
V_{BS}	BOOT Pin Voltage	-0.3 to V_{PHASE}+6	V
V_{UGATE}	Voltage from UGATE to PHASE	-0.3 to 6	V
V_{LGATE}	Voltage from LGATE to GND	-0.3 to 6	V
V_{PHASE}	Voltage from PHASE to GND	-0.3 to 36	V
V_{PGND}	Voltage from PGND to GND	-0.3 to 0.3	V
–	Voltage from Other Pins to GND	-0.3 to 6	V
θ_{JA}	Thermal Resistance (Junction to Ambient)	60	°C/W
T_J	Operating Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10Secs)	+260	°C
V_{HBM}	ESD (Human Body Model)	2000	V
V_{MM}	ESD (Machine Model)	200	V

Note 4: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{DDP}	Supply Voltage	4.5	5.5	V
V_{IN}	Input Voltage	4.5	26	V
$V_{OUT(MAX)}$	Maximum Output Voltage	–	5.5	V
T_A	Operating Ambient Temperature	-40	+85	ºC

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Electrical Characteristics (V_{IN} = 12V, V_{DD} = V_{DDP} = 5V, V_{OUT} = 1.05V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY INPUT						
V_{IN}	Input Voltage	–	4.5	–	26	V
I_{Q-CCM}	Quiescent Current	VDD+VDDP current, CCM, EN floating, V_{FB} = 0.8V	–	500	800	μA
I_{Q-DEM}		V_{DD}+V_{DDP} current, DEM, V_{EN} = 5V, V_{FB} = 0.8V	–	500	800	μA
I_{SHDN}	Shutdown Current	V_{DD}+V_{DDP} current, DEM, V_{EN} = 0V	–	1	10	μA
ON-TIME TIMER, OSCILLATOR FREQUENCY AND SOFT START						
t_{ON}	On Time	V_{PHASE} = 12V, V_{OUT} = 2.5V, R_{ON} = 200kΩ	510	630	750	ns
		V_{PHASE} = 12V, V_{OUT} = 1.05V, R_{ON} = 200kΩ	190	260	330	
$t_{OFF-MIN}$	Min Off Time	–	250	400	580	ns
t_{SS}	Internal Soft Start Time	–	0.82	1.2	1.5	ms
PWM CONTROLLER GATE DRIVERS						
R_{U_PH}	Upper Gate Pull-up Resistance	V_{BOOT}-V_{PHASE} = 5V, 50mA source current	–	3.3	7	Ω
R_{U_GATE}	Upper Gate Sink Resistance	V_{BOOT}-V_{PHASE} = 5V, 50mA sink current	–	1	3	Ω
R_{L_PH}	Lower Gate Pull-up Resistance	–	–	1.8	4	Ω
R_{L_GATE}	Lower Gate Sink Resistance	V_{BOOT}-V_{PHASE} = 5V, 50mA source current	–	0.5	2	Ω
–	PHASE Falling to LGATE Rising Delay	V_{PHASE} < 1.2V to V_{LGATE} > 1.2V	–	30	–	ns
–	LGATE Falling to UGATE Rising Delay	V_{LGATE} < 1.2V to (V_{UGATE}-V_{PHASE}) > 1.2V	–	30	–	ns
V_{BOOT}	Boot Diode Forward Voltage	V_{DDP}-V_{BOOT}, I_{BOOT} = 10mA	0.5	0.83	1	V
I_{BSLK}	V_{BS} Leakage Current	V_{BOOT} = 34V, V_{PHASE} = 28V	–	0.1	1	μA
POWER GOOD						
–	PGOOD Threshold	PGOOD from low to high	92.5	95	97.5	%
–		PGOOD from high to low	102	105	107	%
–	PGOOD Lower Threshold Hysteresis	–	–	±5	–	%
V_{PG_L}	PGOOD Low Voltage	–	–	–	0.4	V
I_{PG_LEAK}	PGOOD Output Leakage Current	V_{PGOOD} = 5V	–	–	1	μA
t_{DELAY}	PGOOD Delay Time	Delay for PGOOD pin	16	22	36	μs

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Electrical Characteristics (Cont. V_{IN} = 12V, V_{DD} = V_{DDP} = 5V, V_{OUT} = 1.05V, T_A = +25°C, unless otherwise specified.)

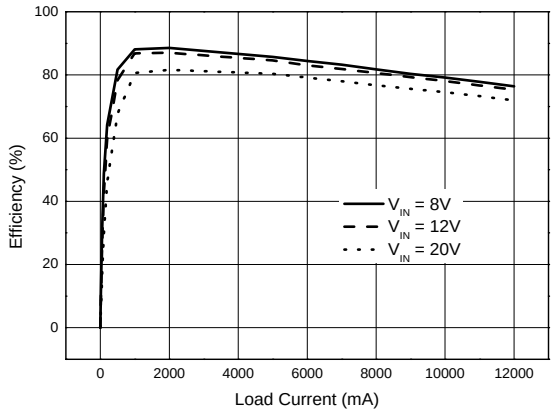
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOUT AND REFERENCE VOLTAGE						
V_{OUT}	Output Voltage	–	0.75	–	5.5	V
$R_{DISCHARGE}$	Output Discharge Resistance	V_{EN} = 0V	–	20	–	Ω
V_{FB}	Feedback Voltage	V_{DD} = 4.5V to 5.5V	0.742	0.75	0.758	V
I_{FB}	Feedback Bias Current	V_{FB} = 0.75V	-1	–	1	μA
PROTECTION						
I_{OC}	Current Limit Source Current	CS to GND	9	10	11	μA
–	I_{OC} Temperature Coefficient	–	–	4500	–	ppm/°C
V_{ILIM_SET}	Current Limit Setting Voltage Range	CS to GND	30	–	200	mV
V_{OCL_OFFSET}	Over Current Limit Comparator Offset Voltage	V_{CS} = 60mV, V_{CS-GND}-$V_{PGND-PHASE}$	-10	0	10	mV
V_{ZC_OFFSET}	Zero Crossing Comparator Offset Voltage	V_{PHASE} to GND, V_{EN} = 5V	-10	0	10	mV
V_{UCL_OFFSET}	Negative Over Current Limit Comparator Offset Voltage	EN floating, V_{CS} = 60mV, V_{CS-GND}-$V_{PHASE-PGND}$	-10	0	10	mV
V_{FBOV} /V_{FB}	Feedback Over Voltage Threshold	–	120	125	130	%
t_{FBOV_D}	Feedback Over Voltage Delay Time	–	–	33	–	μs
V_{FBUV} /V_{FB}	Feedback Under Voltage Threshold	–	65	70	75	%
t_{FBUV_D}	Feedback Under Voltage Protection Delay Time	–	–	28	–	μs
$t_{FBUV_EN_D}$	Feedback Under Voltage Protection Enable Delay Time	–	1.3	2	3.1	ms
V_{UVLO}	V_{DD} Under Voltage Lock Threshold	V_{DD} Rising	3.7	3.9	4.1	V
V_{HYS}	V_{DD} Under Voltage Lock Hysteresis	–	–	300	–	mV
T_{OTSD}	Thermal Shutdown	–	–	+160	–	°C
T_{HYS}	Thermal Shutdown Hysteresis	–	–	+20	–	°C
LOGIC THRESHOLD						
V_{ENH}	EN Control Logic Input Voltage	Setting DEM mode	2.4	2.65	2.9	V
$V_{ENH-HYS}$		Hysteresis	–	25	–	mV
V_{EN_FT}		Setting PWM-only mode	1.9	1.96	2	V
V_{ENL}		Shutdown Threshold	0.8	1.24	1.6	V
$V_{ENL-HYS}$		Hysteresis	–	65	–	mV
I_{EN_PH}	EN Pull_up Current	V_{EN} = 0V	–	1	–	μA

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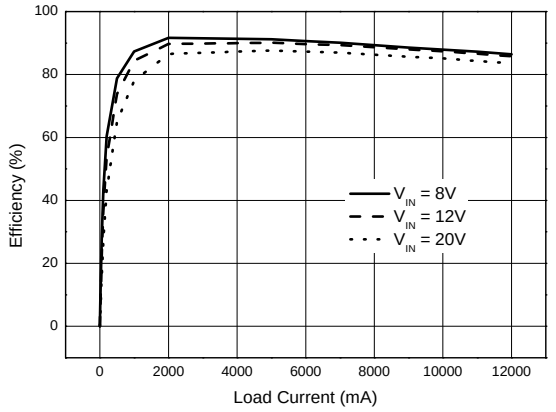
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Performance Characteristics

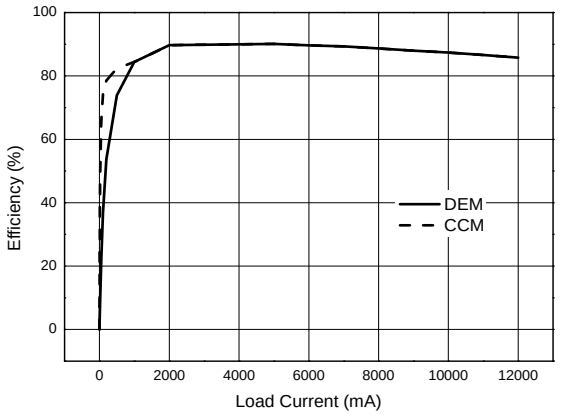
Efficiency vs. Load Current @V_{OUT} = 1.05V



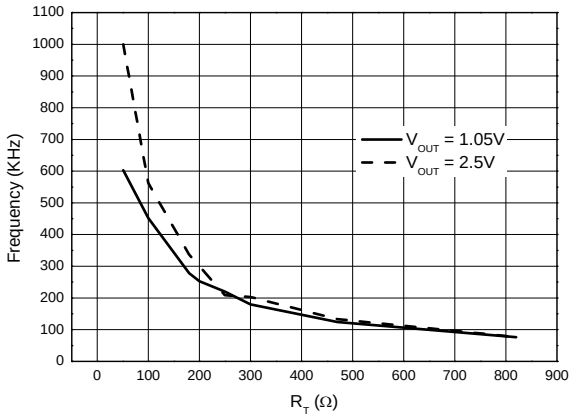
Efficiency vs. Load Current @V_{OUT} = 2.5V



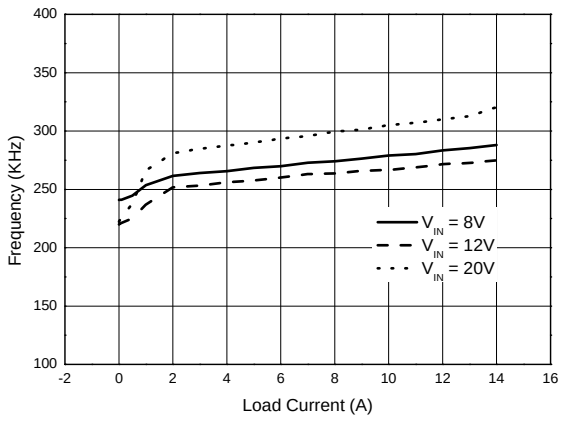
Efficiency vs. Load Current (CCM vs. DEM)



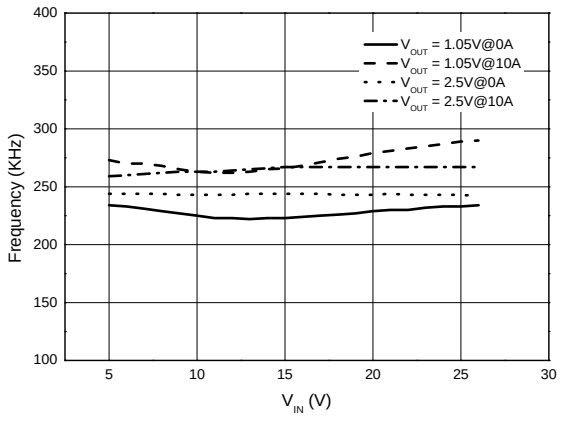
Frequency vs. R_T



Frequency vs. Load Current



Frequency vs. V_{IN}

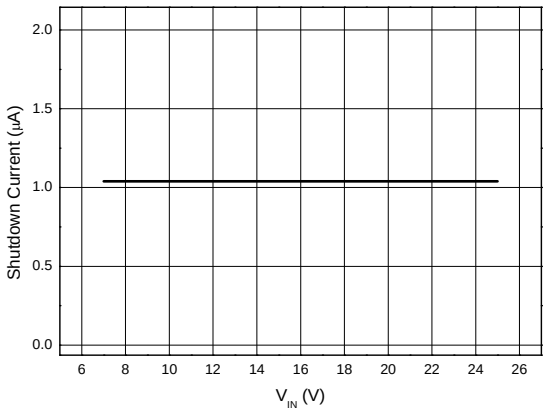


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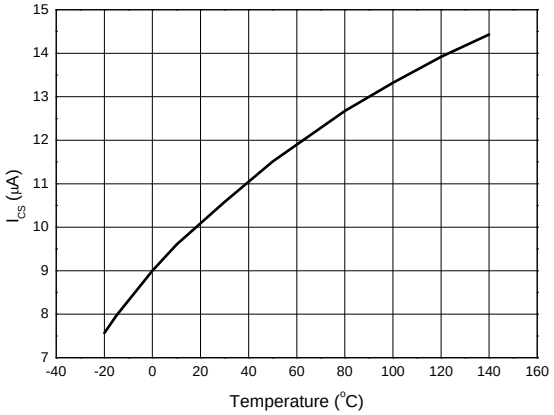
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Performance Characteristics (Cont.)

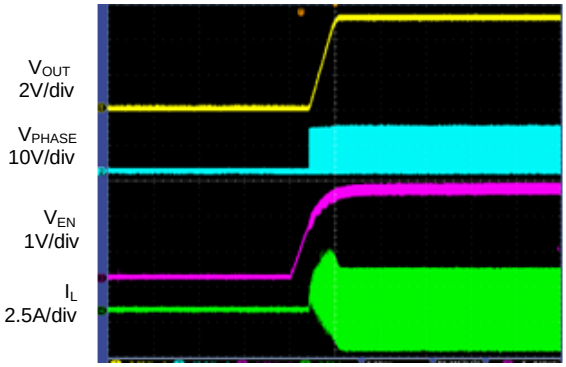
Shutdown Current vs. V_{IN}



I_{CS} vs. Temperature (°C)

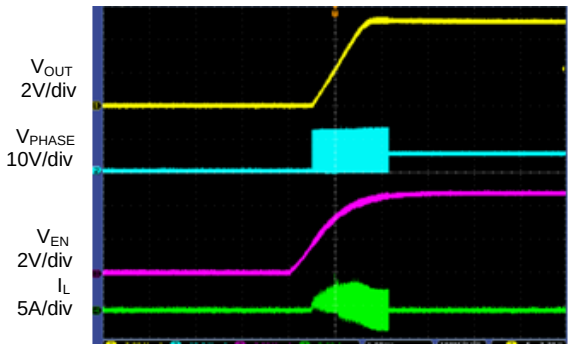


Power ON from EN @CCM



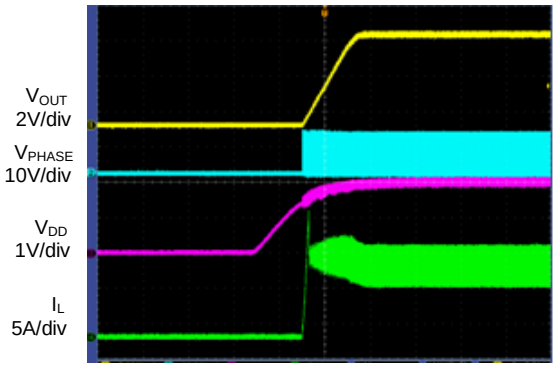
Time 2ms/div

Power ON from EN @DEM



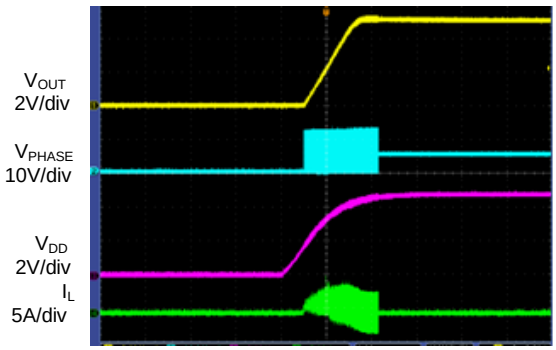
Time 1ms/div

Power ON from VDD @CCM



Time 1ms/div

Power ON from VDD @DEM



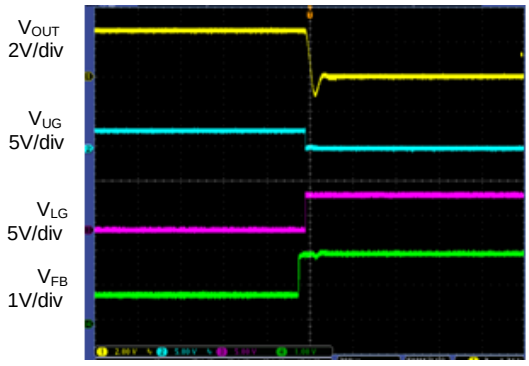
Time 1ms/div

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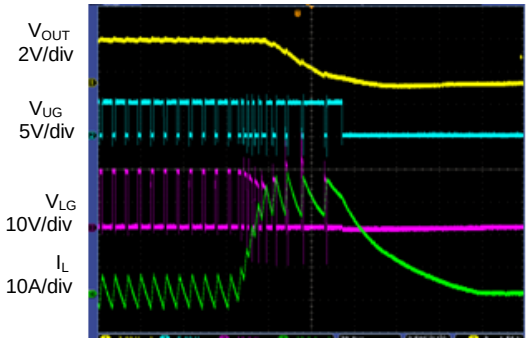
Performance Characteristics (Cont.)

OVP



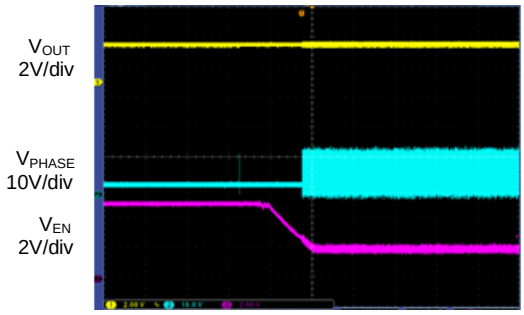
Time 200µs/div

UVP



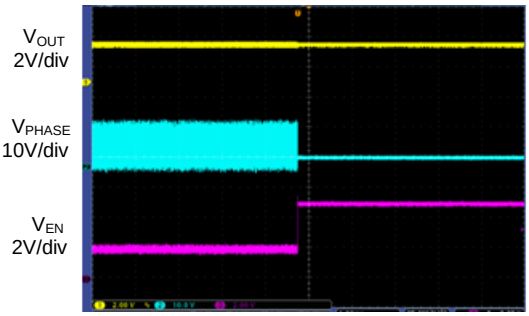
Time 20µs/div

MODE Transition DEM to CCM



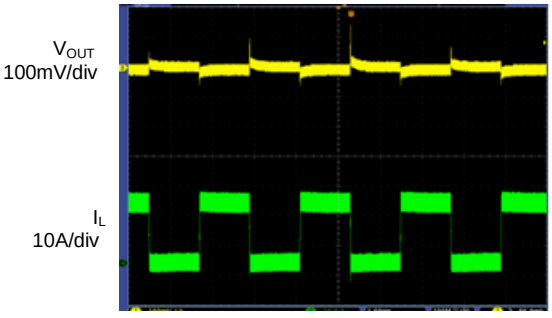
Time 4ms/div

MODE Transition CCM to DEM



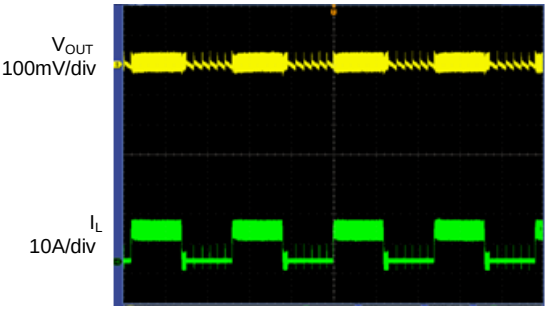
Time 4ms/div

Load Transient Response @ CCM



Time 1ms/div

Load Transient Response @ DEM



Time 1ms/div

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Application Information

1. Functional Description

The AP3591 is a synchronous step-down controller. Adaptive constant on time (COT) control is employed to provide fast transition response and easy loop stabilization. AP3591 does not have a dedicated in board oscillator. It runs with a pseudo-constant frequency which is set by R_{ON}. The output voltage variation is sensed by FB Pin. If V_{FB} is below 0.75V, the error comparator will trigger the control logic and generate an ON-time period, in which high side MOSFET is turned on and low side MOSFET is turned off. The ON-time period length is calculated using the following equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f}$$

V_{OUT} is the output voltage, V_{IN} is the input voltage, and f is the switching frequency.

The on-time is the time required for the voltage on this capacitor charging from zero volts to V_{OUT}, thereby the ON-time of the high side switch is directly proportional to the output voltage and inversely proportional to the input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

$$t_{ON} = 14.5p \times R_{TON} \times (V_{OUT}+0.1)/V_{IN}+50ns$$

After an ON-time period, the AP3591 goes into the OFF-time period. The OFF-time period length depends on V_{FB} in most case. It will end when V_{FB} decreases below 0.75V and then the ON-time period is triggered again. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is about 400ns typical.

2. Mode Selection Operation

AP3591 has two operation modes: Continuous Conduction Mode (CCM) and Diode Emulation Mode (DEM). When the EN/DEM pin voltage is higher than 2.9V, AP3591 will operate in DEM mode for high efficiency; when the EN/DEM pin is floating, AP3591 will operate in forced CCM mode to a certain frequency during a light load condition.

2.1 Diode Emulation Mode

If the DEM mode is selected, the AP3591 automatically reduces the switching frequency under a light load condition to get high efficiency. When the output current decreases and heavy load condition is formed, the inductor current decreases as well, and eventually comes close to zero current, which is the boundary between CCM and DEM. The low side MOSFET will turn off whenever the inductor current reaches zero level. The load is provided only by the output capacitor. When FB voltage is lower than 0.75V, the next ON cycle is beginning. The ON-time is kept the same as that in the heavy load condition. The switching frequency increases to keep V_{OUT} voltage when the output current increases from light to heavy load. The transition load point is calculated using the following equation:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

t_{ON} is the on-time.

2.2 Continuous Conduction Mode

When AP3591 operates in CCM mode, the duty cycle V_{OUT}/V_{IN} is not changed at light load condition. The low side MOSFET keeps on even when inductor current decreases to reverse. The benefit of CCM is to keep the switching frequency fairly constant to avoid a certain frequency during a light load condition.

3. Power On Reset and Soft-start

Power on reset occurs when V_{DD} rises above approximately 3.9V: the IC will reset the fault latch and prepare the PWM for operation. When V_{DD} is below 3.6V, the VDD under voltage lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from power supply input V_{IN} during turn on (referring to Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft-start voltage V_{SS} whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. V_{SS} internally ramps up to 95% of 0.75V in 1.2ms for AP3591 after the soft-start cycle is initiated.

Figure 1 shows a typical start-up interval for AP3591 when the EN/DEM pin has been released from a grounded (system shutdown) state.

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Application Information (Cont.)

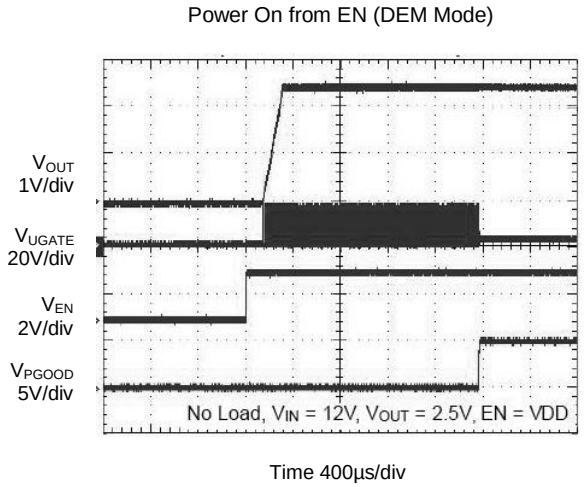


Figure 1. Start-up Behavior of AP3591

4. Power Good Output

The AP3591 features power good output to monitor the output voltage. It is an open-drain output and should be connected to a 5V power supply node through a resistor. The power good function is active after the soft start is finished. PGOOD signal becomes high if output voltage reaches ±5% of the target value after 64µs delay building into the PGOOD circuitry. It will become low immediately if the output voltage goes beyond ±10% of the target value.

5. Soft Stop

The AP3591 has a built in soft-stop circuitry. The output is discharged with an internal 20Ω transistor when EN/DEM is low or the device is in a fault condition including UVLO and OTP. The discharge time constant is determined by the output capacitance and resistance of the discharge transistor.

6. Pre-biased Output

Figure 2 shows the normal V_{OUT} start-up curve in blue; Initialization begins at T0, and output ramps between T1 and T2. If the output is pre-biased to a voltage less than the expected value, as shown by the magenta curve, the AP3591 will detect that condition. Neither MOSFET will turn on until the soft-start ramp voltage exceeds the output. V_{OUT} starts seamlessly ramping from there. If the output is pre-biased to a voltage above the expected value, as showed in the black curve, neither MOSFET will turn on until the output voltage is pulled down to the expected value through external load. Any resistive load connected to the output will help pull down the voltage.

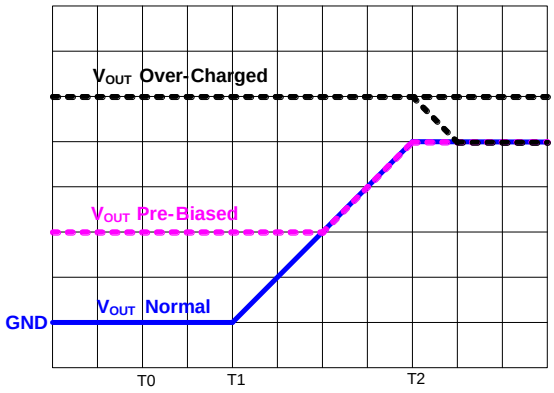


Figure 2. Start-up Behavior with Pre-biased Output Voltage

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Application Information (Cont.)

7. Over Current Protection (OCP)

Figure 3 shows the over current protection (OCP) scheme of AP3591. In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. When the voltage between PGND pin and PHASE pin is larger than the over current trip level, the OCP is triggered and the controller keeps the OFF state. Because the $R_{DS(ON)}$ of MOSFET increases with the temperature, I_{OC} has 4500ppm/ºC temperature coefficient to compensate this temperature dependency of $R_{DS(ON)}$.

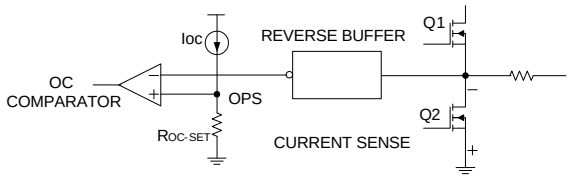


Figure 3. Over Current Scheme

A resistor $R_{OC\text{-}SET}$ should be connected from CS pin to GND. An internal current source I_{OC} (10µA typically), flowing through $R_{OC\text{-}SET}$ determines the OCP trip point I_{OCSET}, which can be calculated using the following equation:

$$V_{CS}(mV) = 10\mu A \times R_{OC\text{-}SET}(K\Omega)$$

The load current at over-current threshold (I_{O_OCSET}), can be calculated using the following equation:

$$I_{O_OCSET} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{\Delta I_{L(PP)}}{2}$$
$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

V_{OUT} is the output voltage, $\Delta I_{L(PP)}$ is the inductor current ripple peak to peak value and f is the switching frequency.

8. Negative Over Current Protection (NOCP)

The AP3591 supports cycle by cycle negative over current limiting in CCM mode. The over current limit value is the same absolute value as the positive over current limit. If the inductor reverse current is larger than NOCP current at OFF time, the LMOSFET is turned off. The reverse current will flows to VIN through the body diode of HMOSFET. After 400ns delay, LMOSFET is turned on again. If the NOCP is released, the HMOSFET is turned on and the device resumes normal operation.

9. Under Voltage Protection (UVP)

The output voltage is also monitored for under voltage protection. When the output voltage is less than 70% of the setting voltage threshold, under voltage protection is triggered after 28µs delay to prevent false transition. When UVP is triggered, UGATE and LGATE will get low, and the output is discharged with the internal 20Ω transistor. UVP is a latched protection; it can only be released by VDD or EN/DEM power-on reset. The UVP blanking time is 2ms during soft-start.

10. Under Voltage Lockout

The AP3591 provides an under voltage lockout circuit to prevent from undefined status at startup. The UVLO circuit shuts down the device when V_{DD} drops below 3.6V. The UVLO circuit has 300mV hysteresis, which means the device will start up again when V_{DD} rises to 3.9V.

11. Over Voltage Protection (OVP)

The feedback voltage is continuously monitored for over voltage protection. When OVP is triggered, LGATE will go high and UGATE will go low to discharge the output capacitor.

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Application Information (Cont.)

The AP3591 provides full-time over voltage protection whenever soft-start completes or not. The typical OVP threshold is 125% of the internal reference voltage V_{REF}. The AP3591 provides latched OVP and can only be released by VDD or EN/DEM power-on reset. There is 33µs delay built into the over voltage protection circuit to prevent false transitions.

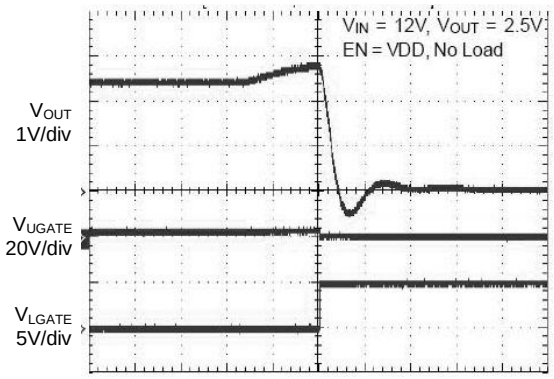


Figure 4. Over Voltage Protection

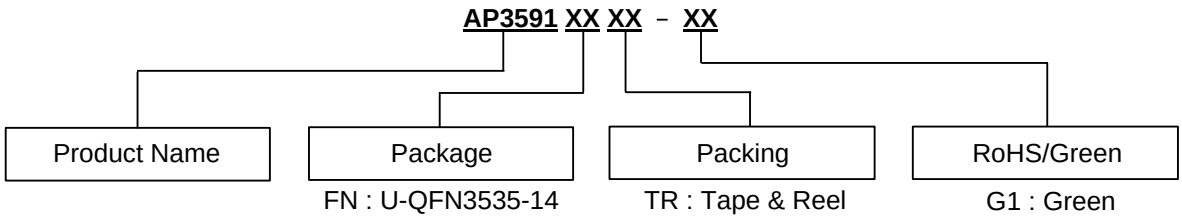
12. Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +160ºC, the AP3591 shuts itself off. Both UGATE and LGATE are driven low, turning off both MOSFETs. The output is discharged with the internal 20Ω transistor. When the junction temperature cools down to the required level (+140°C nominal), the device initiates soft-start as during a normal power-up cycle.

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Ordering Information



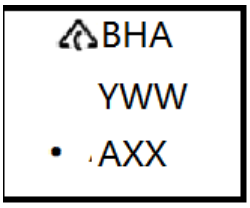
Diodes IC's Pb-free products with "G1" suffix in the part number, are RoHS compliant and green.

Package	Temperature Range	Part Number	Marking ID	Packing
U-QFN3535-14	-40 to +85°C	AP3591FNTR-G1	BHA	5000/Tape & Reel

Marking Information

(1) U-QFN3535-14

(Top View)



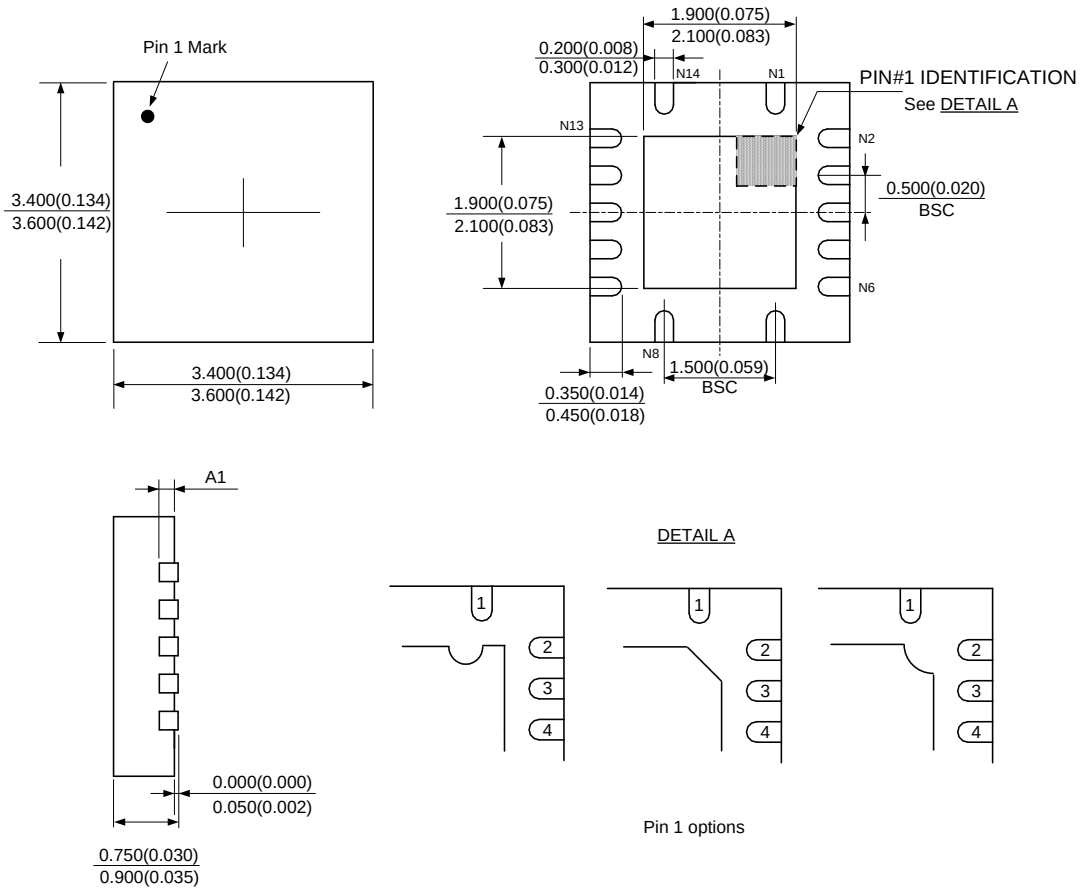
First Line: Logo and Marking ID
Second and Third Lines: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No.

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Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: U-QFN3535-14



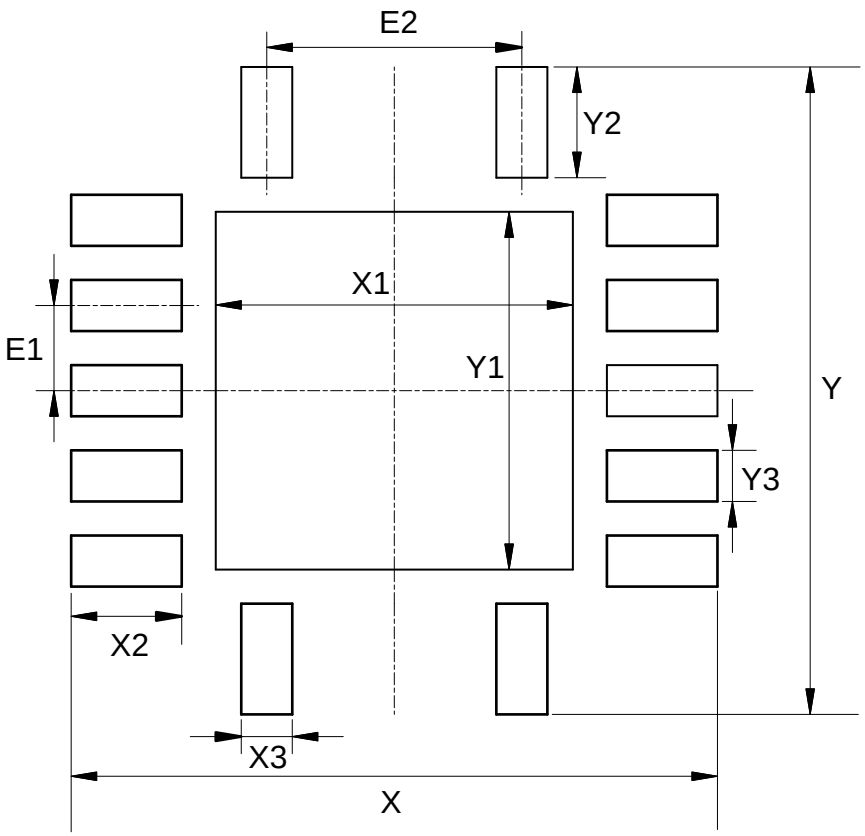
Symbol	A1			
	min(mm)	max(mm)	min(inch)	max(inch)
Option1	0.203(REF)		0.008(REF)	
Option2	0.150(REF)		0.006(REF)	

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Suggested Pad Layout

(1) Package Type: U-QFN3535-14



Dimensions	X=Y (mm)/(inch)	X1=Y1 (mm)/(inch)	X2=Y2 (mm)/(inch)	X3=Y3 (mm)/(inch)	E1 (mm)/(inch)	E2 (mm)/(inch)
Value	3.800/0.150	2.100/0.083	0.650/0.026	0.300/0.012	0.500/0.020	1.500/0.059

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