# AP2141/AP2151

## 0.5A SINGLE CHANNEL CURRENT-LIMITED POWER SWITCH

## Features

- Single USB port power switches
- Over-current and thermal protection
- 0.8A accurate current limiting
- Reverse Current Blocking
- 95mΩ on-resistance
- Input voltage range: 2.7V – 5.5V
- 0.6ms typical rise time
- Very low shutdown current: 1uA (max)
- Fault report (FLG) with blanking time (7ms typ)
- ESD protection: 4KV HBM, 400V MM
- Active high (AP2151) or active low (AP2141) enable
- Ambient temperature range -40ºC to 85°C
- SOT25, SOP-8L, MSOP-8L-EP (Exposed Pad), and DFN2018-6: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish / RoHS Compliant (Note 1)
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

## Description

The AP2141 and AP2151 are integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB 2.0 and available with both polarities of Enable input. They offer current and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

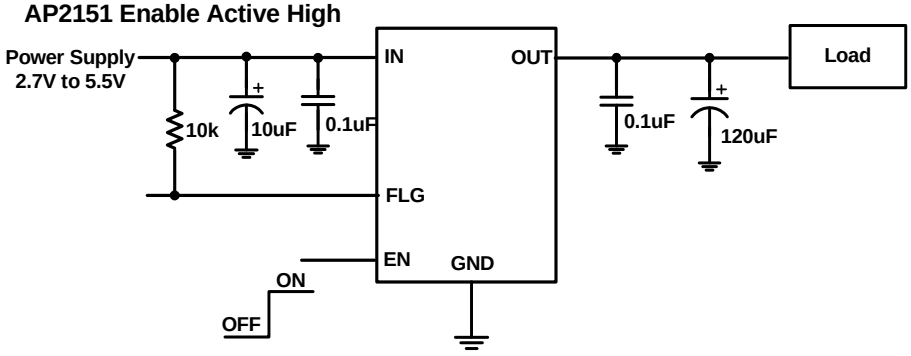
All devices are available in SOP-8L, MSOP-8L-EP, SOT25, and DFN2018-6 packages.

## Applications

- Consumer electronics – LCD TV & Monitor, Game Machines
- Communications – Set-Top-Box, GPS, Smartphone
- Computing – Laptop, Desktop, Servers, Printers, Docking Station, HUB

## Typical Application Circuit

**AP2151 Enable Active High**

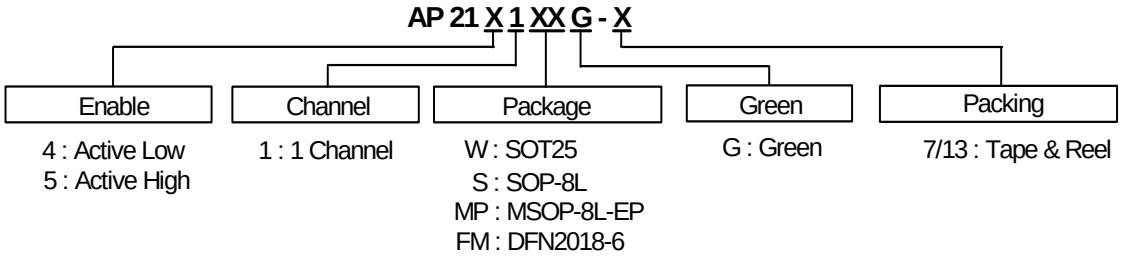



**Available Options**

| Part Number | Channel | Enable pin (EN) | Current limit (typical) | Recommended maximum continuous load current |
|---|---|---|---|---|
| AP2141 | 1 | Active Low | 0.8A | 0.5A |
| AP2151 | 1 | Active High | 0.8A | 0.5A |


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## Ordering Information



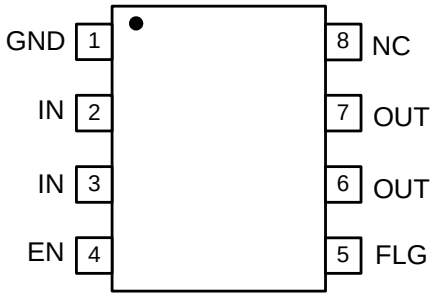

| Device | Package Code | Packaging (Note 2) | 7"/13" Tape and Reel | |
|---|---|---|---|---|
| | | | Quantity | Part Number Suffix |
| AP21X1WG-7 | W | SOT25 | 3000/Tape & Reel | -7 |
| AP21X1SG-13 | S | SOP-8L | 2500/Tape & Reel | -13 |
| AP21X1MPG-13 | MP | MSOP-8L-EP | 2500/Tape & Reel | -13 |
| AP21X1FMG-7 | FM | DFN2018-6 | 3000/Tape & Reel | -7 |

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html
2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.


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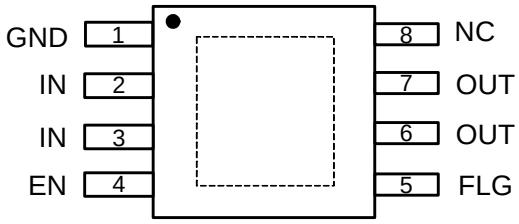
## Pin Assignment

( Top View )



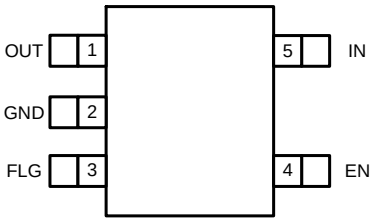

SOP-8L

( Top View )



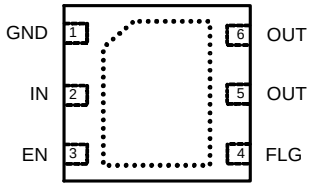

MSOP-8L-EP

( Top View )




SOT25

( Top View )




DFN2018-6

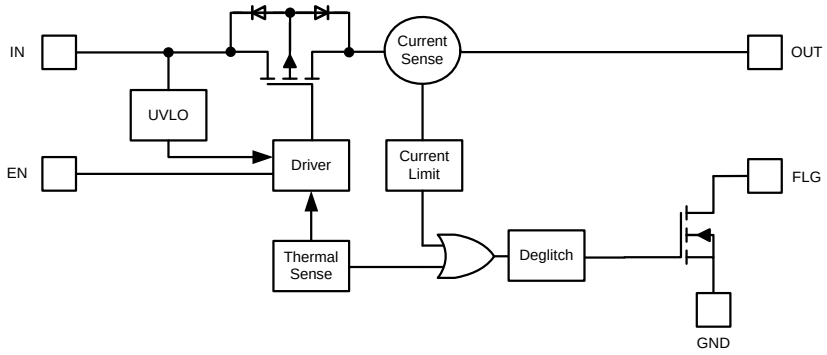
## Pin Descriptions

| Pin Name | Pin Number | | | Descriptions |
|---|---|---|---|---|
| | SOP-8L / MSOP-8L-EP | SOT25 | DFN2018-6 | |
| GND | 1 | 2 | 1 | Ground |
| IN | 2, 3 | 5 | 2 | Voltage input pin (all IN pins must be tied together externally) |
| EN | 4 | 4 | 3 | Enable input, active low (AP2141) or active high (AP2151) |
| FLG | 5 | 3 | 4 | Over-current and over-temperature fault report; open-drain flag is active low when triggered |
| OUT | 6, 7 | 1 | 5, 6 | Voltage output pin (all OUT pins must be tied together externally) |
| NC | 8 | N/A | N/A | No internal connection; recommend tie to OUT pins |


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## Functional Block Diagram

**AP2141, AP2151**




## Absolute Maximum Ratings

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| ESD HBM | Human Body Model ESD Protection | 4 | KV |
| ESD MM | Machine Model ESD Protection for MSOP-8L-EP, SOT25 packages | 400 | V |
| | Machine Model ESD Protection for DFN2018-6, SOP-8L packages | 300 | V |
| $V_{IN}$ | Input Voltage | 6.5 | V |
| $V_{OUT}$ | Output Voltage | $V_{IN}$ + 0.3 | V |
| $V_{EN}$ , $V_{FLG}$ | Enable Voltage | 6.5 | V |
| $I_{load}$ | Maximum Continuous Load Current | Internal Limited | A |
| $T_{Jmax}$ | Maximum Junction Temperature | 150 | °C |
| $T_{ST}$ | Storage Temperature Range (Note 3) | -65 to 150 | °C |

Notes: 3. UL Recognized Rating from -30°C to 70°C (Diodes qualified $T_{ST}$ from -65°C to 150°C)

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.7 | 5.5 | V |
| $I_{OUT}$ | Output Current | 0 | 500 | mA |
| $T_A$ | Operating Ambient Temperature | -40 | 85 | °C |


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## Electrical Characteristics

($T_A$ = 25°C, $V_{IN}$ = +5.0V, unless otherwise stated)

| Symbol | Parameter | Test Conditions | | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{UVLO}$ | Input UVLO | $R_{load}$=1kΩ | | | 1.6 | 1.9 | 2.5 | V |
| $I_{SHDN}$ | Input Shutdown Current | Disabled, $I_{OUT}$= 0 | | | | 0.5 | 1 | μA |
| $I_Q$ | Input Quiescent Current | Enabled, $I_{OUT}$= 0 | | | | 45 | 70 | μA |
| $I_{LEAK}$ | Input Leakage Current | Disabled, OUT grounded | | | | | 1 | μA |
| $I_{REV}$ | Reverse Leakage Current | Disabled, $V_{IN}$= 0V, $V_{OUT}$= 5V, $I_{REV}$ at $V_{IN}$ | | | | 1 | | μA |
| $R_{DS(ON)}$ | Switch on-resistance | $V_{IN}$ = 5V, $I_{OUT}$= 0.5A | $T_A$ = 25°C | SOT25, MSOP-8L-EP, SOP-8L | | 95 | 115 | mΩ |
| | | | | DFN2018-6 | | 90 | 110 | |
| | | | -40°C ≤ $T_A$ ≤ 85°C | | | | 140 | |
| | | $V_{IN}$ = 3.3V, $I_{OUT}$= 0.5A | $T_A$ = 25°C | | | 120 | 140 | |
| | | | -40°C ≤ $T_A$ ≤ 85°C | | | | 170 | |
| $I_{SHORT}$ | Short-Circuit Current Limit | Enabled into short circuit, $C_L$=22μF | | | | 0.6 | | A |
| $I_{LIMIT}$ | Over-Load Current Limit | $V_{IN}$= 5V, $V_{OUT}$= 4.8V, $C_L$=22μF, -40°C ≤ $T_A$ ≤85°C | | | 0.6 | 0.8 | 1.0 | A |
| $I_{Trig}$ | Current limiting trigger threshold | Output Current Slew rate (<100A/s) , $C_L$=22μF | | | | 1.0 | | A |
| $V_{IL}$ | EN Input Logic Low Voltage | $V_{IN}$ = 2.7V to 5.5V | | | | | 0.8 | V |
| $V_{IH}$ | EN Input Logic High Voltage | $V_{IN}$ = 2.7V to 5.5V | | | 2 | | | V |
| $I_{SINK}$ | EN Input leakage | $V_{EN}$ = 5V | | | | | 1 | μA |
| $T_{D(ON)}$ | Output turn-on delay time | $C_L$=1μF, $R_{load}$=10Ω | | | | 0.05 | | ms |
| $T_R$ | Output turn-on rise time | $C_L$=1μF, $R_{load}$=10Ω | | | | 0.6 | 1.5 | ms |
| $T_{D(OFF)}$ | Output turn-off delay time | $C_L$=1μF, $R_{load}$=10Ω | | | | 0.01 | | ms |
| $T_F$ | Output turn-off fall time | $C_L$=1μF, $R_{load}$=10Ω | | | | 0.05 | 0.1 | ms |
| $R_{FLG}$ | FLG output FET on-resistance | $I_{FLG}$ =10mA | | | | 20 | 40 | Ω |
| $T_{Blank}$ | FLG blanking time | $C_{IN}$=10uF, $C_L$=22μF | | | 4 | 7 | 15 | ms |
| $T_{SHDN}$ | Thermal Shutdown Threshold | Enabled, $R_{load}$=1kΩ | | | | 140 | | °C |
| $T_{HYS}$ | Thermal Shutdown Hysteresis | | | | | 25 | | °C |
| $\theta_{JA}$ | Thermal Resistance Junction-to-Ambient | SOP-8L (Note 4) | | | | 110 | | °C/W |
| | | MSOP-8L-EP (Note 5) | | | | 60 | | °C/W |
| | | SOT25 (Note 6) | | | | 157 | | °C/W |
| | | DFN2018-6 (Note 7) | | | | 70 | | °C/W |

Notes:
4. Test condition for SOP-8L: Device mounted on FR-4, 2oz copper, with minimum recommended pad layout.
5. Test condition for MSOP-8L-EP: Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
6. Test condition for SOT25: Device mounted on FR-4, 2oz copper, with minimum recommended pad layout.
7. Test condition for DFN2018-6: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer 1.0"x1.4" ground plane.


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## Typical Performance Characteristics

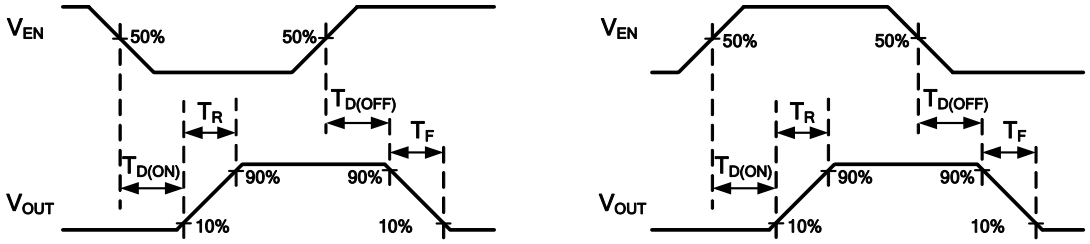
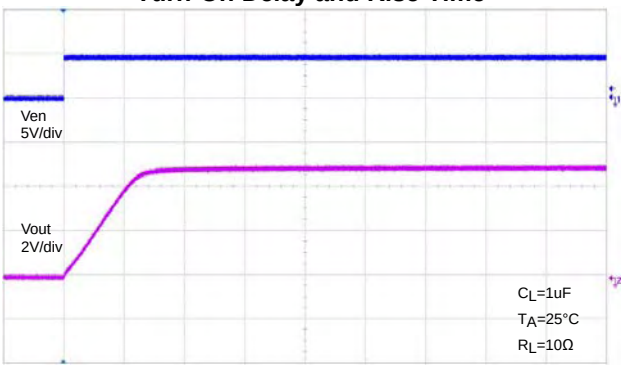



**Figure 1. Voltage Waveforms: AP2141 (left), AP2151 (right)**

**All Enable Plots are for AP2151 Active High**

**Turn-On Delay and Rise Time**



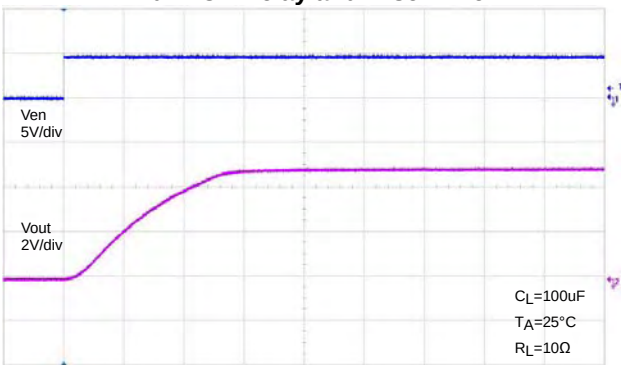

500us/div

**Turn-Off Delay and Fall Time**



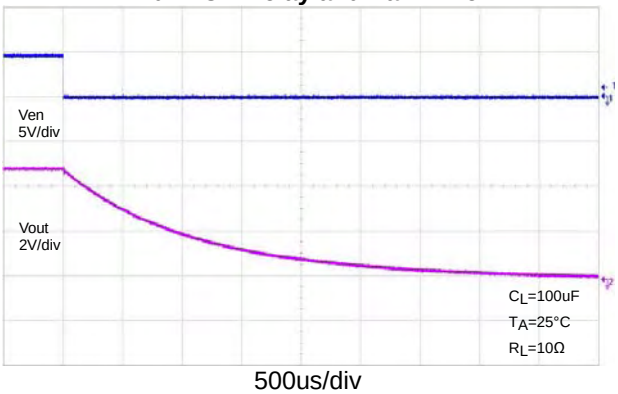

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**Turn-On Delay and Rise Time**




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**Turn-Off Delay and Fall Time**

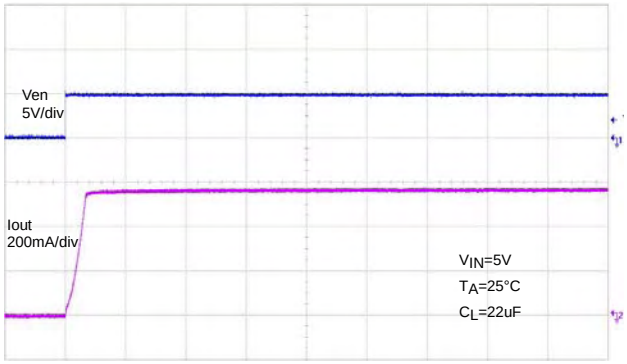



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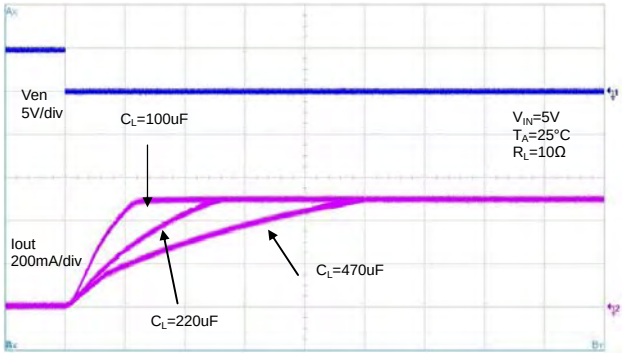
## Typical Performance Characteristics (Continued)

**Short Circuit Current, Device Enabled Into Short**



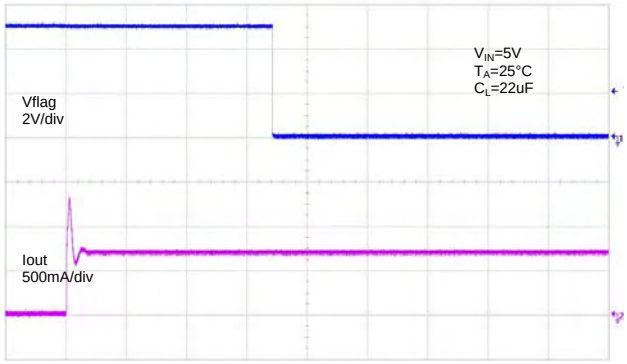

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**Inrush Current**



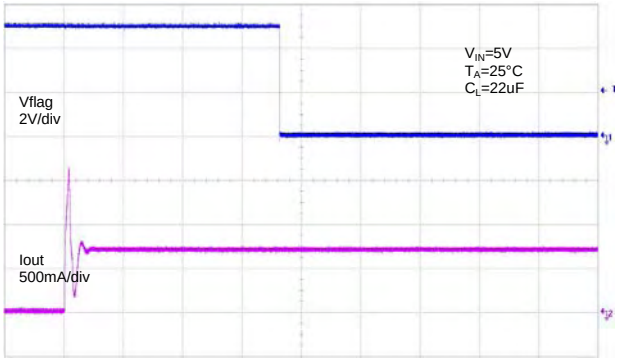

1ms/div

**3 Ω Load Connected to Enabled Device**




2ms/div

**2 Ω Load Connected to Enabled Device**



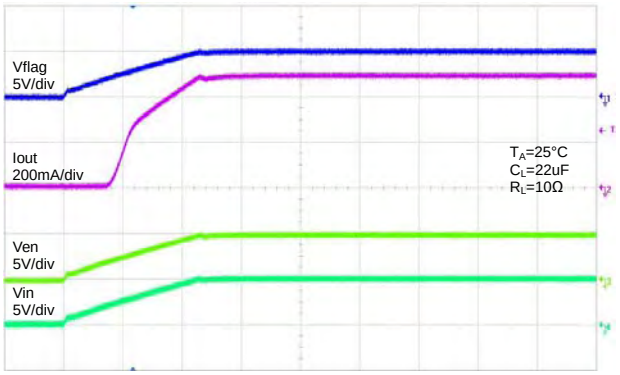

2ms/div

**Short Circuit with Blanking Time and Recovery**




20ms/div

**Power On**

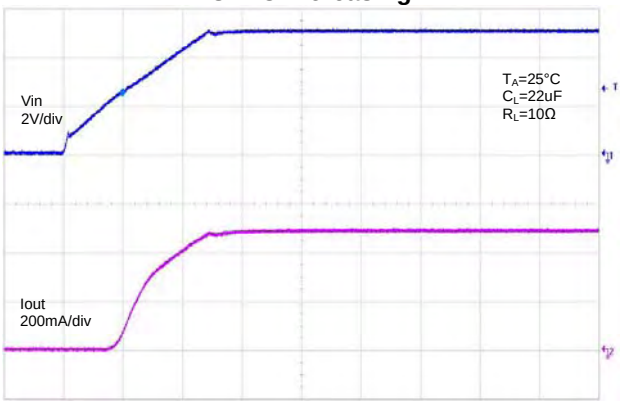



1ms/div


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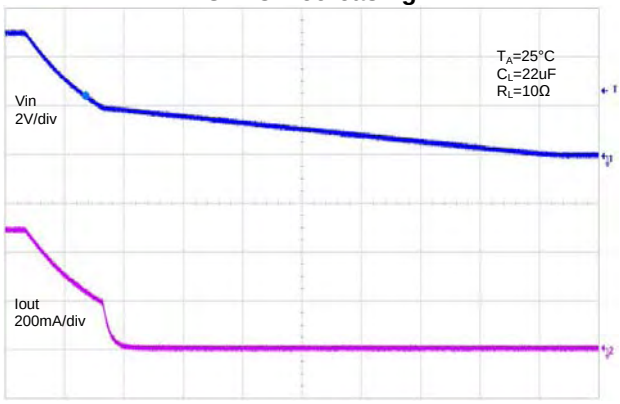
## Typical Performance Characteristics (Continued)

**UVLO Increasing**

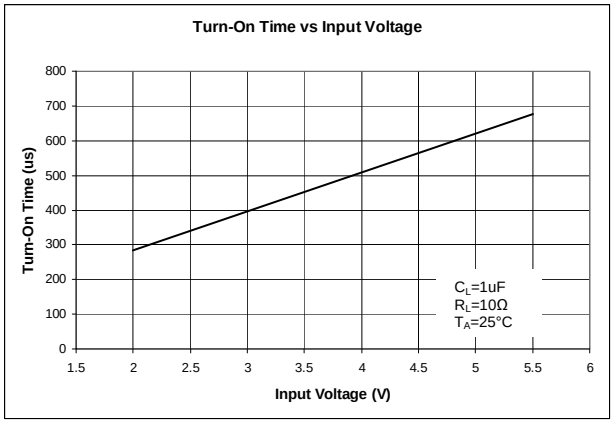


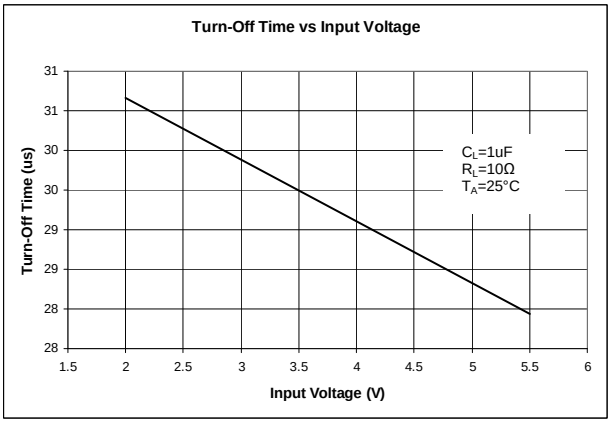

1ms/div

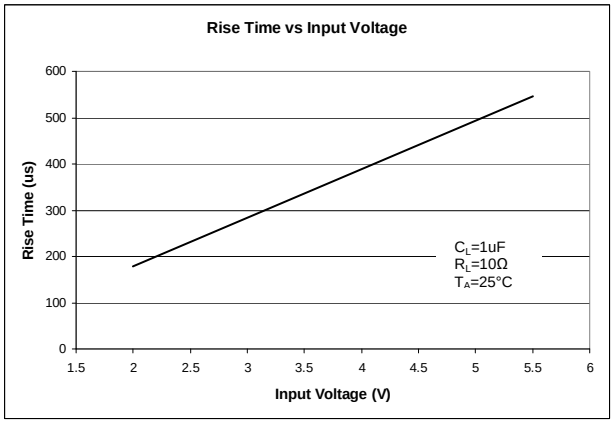
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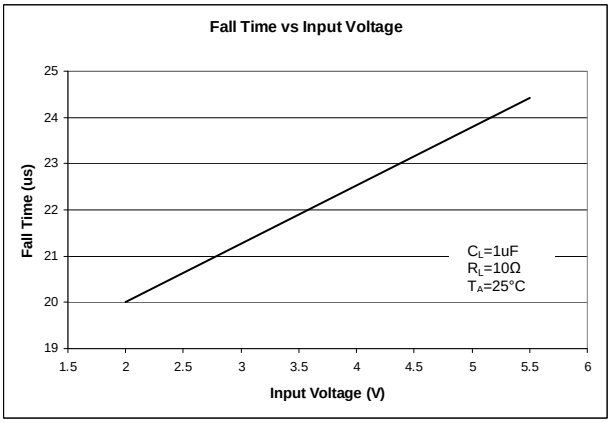



10ms/div



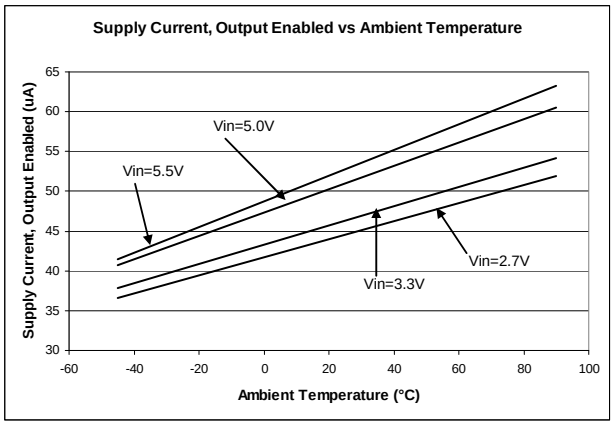



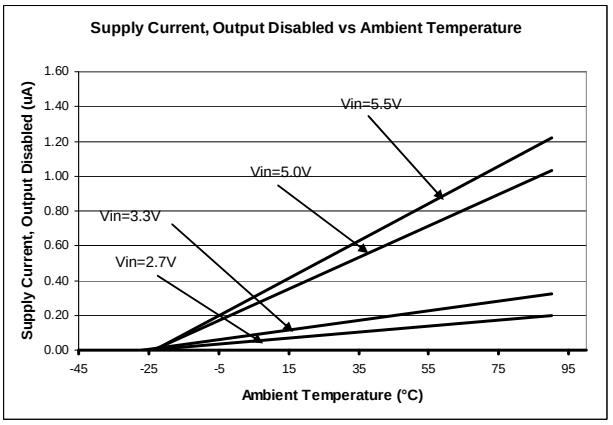



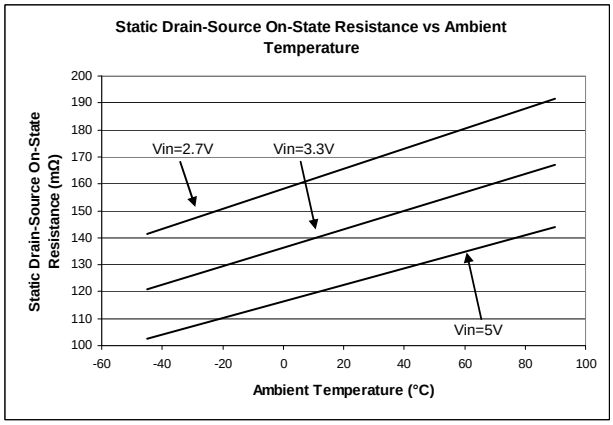


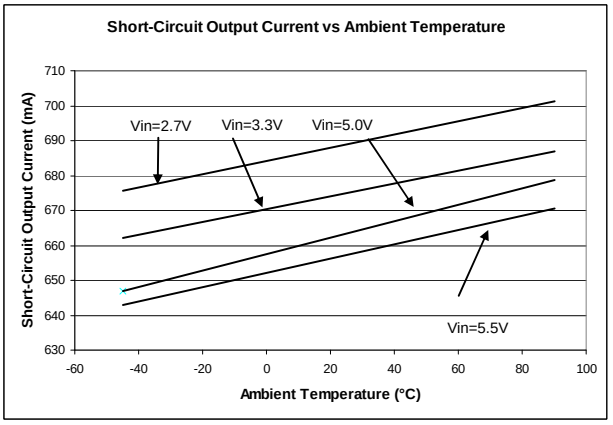
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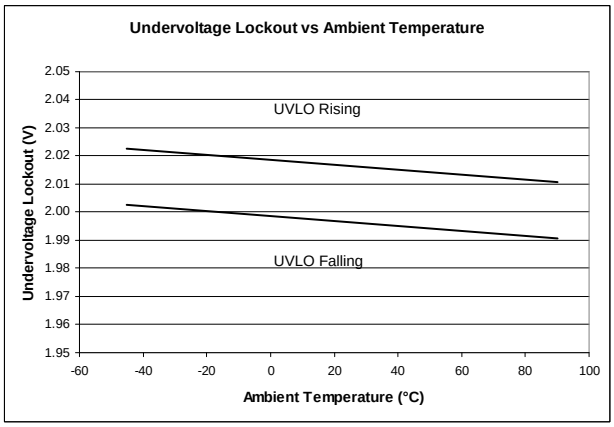
## Typical Performance Characteristics (Continued)

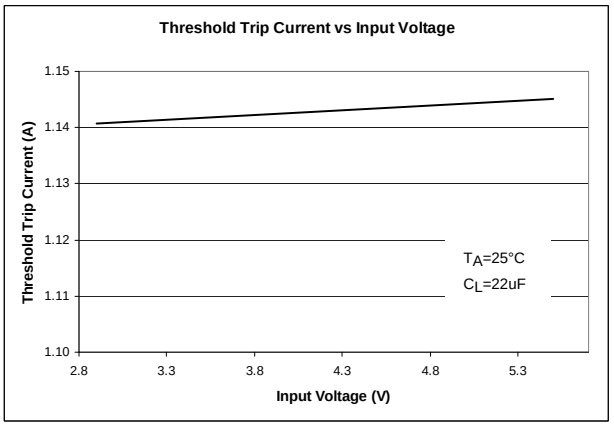


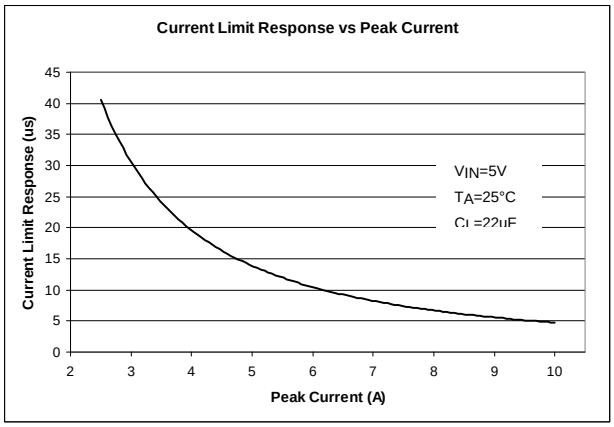





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## Typical Performance Characteristics (Continued)





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## Application Note

### Power Supply Considerations

A 0.01-µF to 0.1-µF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input (10-µF minimum) and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

### Over-current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before $V_{IN}$ has been applied. The AP2141/AP2151 senses the short circuit and immediately clamps output current to a certain safe level namely $I_{LIMIT}$.

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at $I_{LIMIT}$.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold ($I_{TRIG}$) is reached or until the thermal limit of the device is exceeded. The AP2141/AP2151 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at $I_{LIMIT}$.

Note that when the output has been shorted to GND at extremely low temperature (< -30°C), a minimum 120-µF electrolytic capacitor on the output pin is recommended. A correct capacitor type with capacitor voltage rating and temperature characteristics must be properly chosen so that capacitance value does not drop too low at the extremely low temperature operation. A recommended capacitor should have temperature characteristics of less than 10% variation of capacitance change when operated at extremely low temp. Our recommended aluminum electrolytic capacitor type is Panasonic FC series.

### FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7-ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The AP2141/AP2151 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.


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## Application Note (Continued)

### Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ($T_A$) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$= Ambient temperature °C
$R_{\theta JA}$ = Thermal resistance
$P_D$ = Total power dissipation

### Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2141/AP2151 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately 25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7-ms deglitch.

### Under-voltage Lockout (UVLO)

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 1.9V, even if the switch is enabled. Whenever the input voltage falls below approximately 1.9V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

### Host/Self-Powered HUBs

Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports (see Figure 2). This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

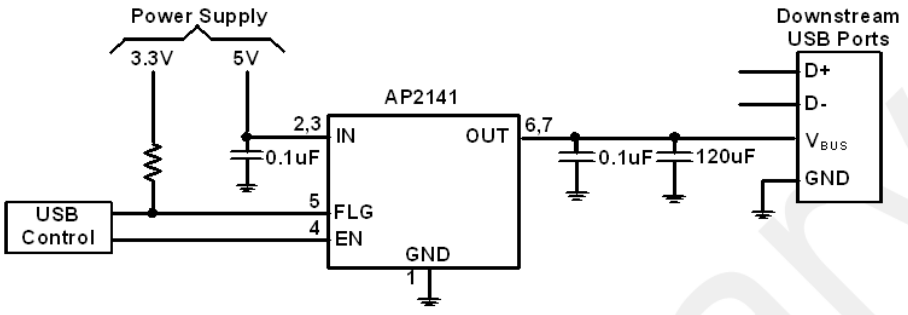



**Figure 2. Typical One-Port USB Host / Self-Powered Hub**


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## Application Note (Continued)

### Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the AP2141/AP2151, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2141/AP2151 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

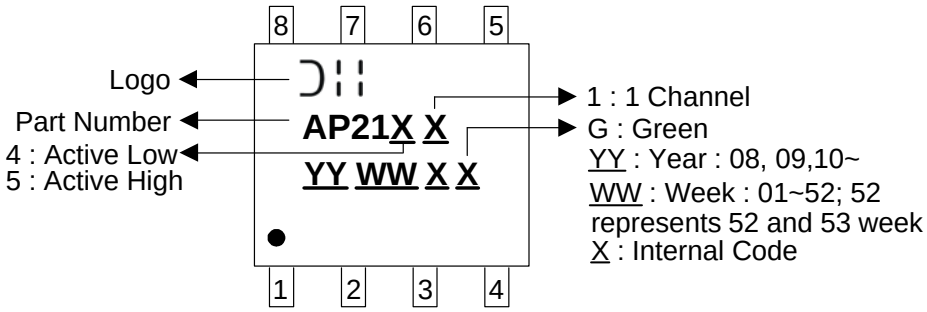
By placing the AP2141/AP2151 between the $V_{CC}$ input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.


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## Marking Information

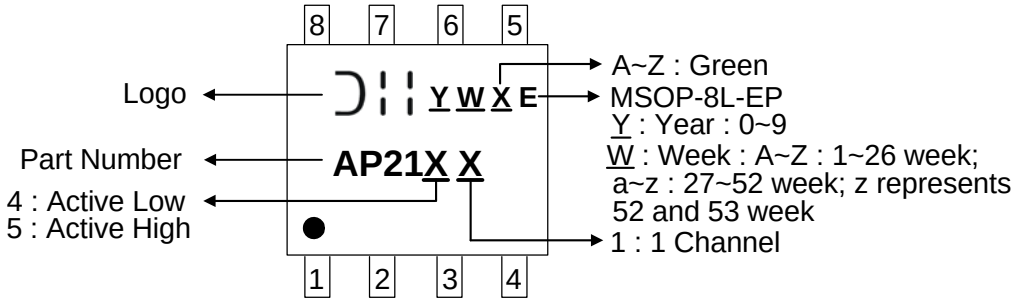
**(1) SOP-8L**

**( Top view )**



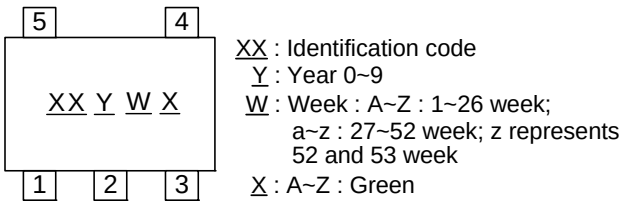

**(2) MSOP-8L-EP**

**( Top view )**




**(3) SOT25**

**( Top View )**



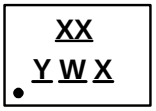

| Device | Package type | Identification Code |
|---|---|---|
| AP2141W | SOT25 | HR |
| AP2151W | SOT25 | HS |


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## Marking Information (Continued)

### (4) DFN2018-6

**(Top View)**

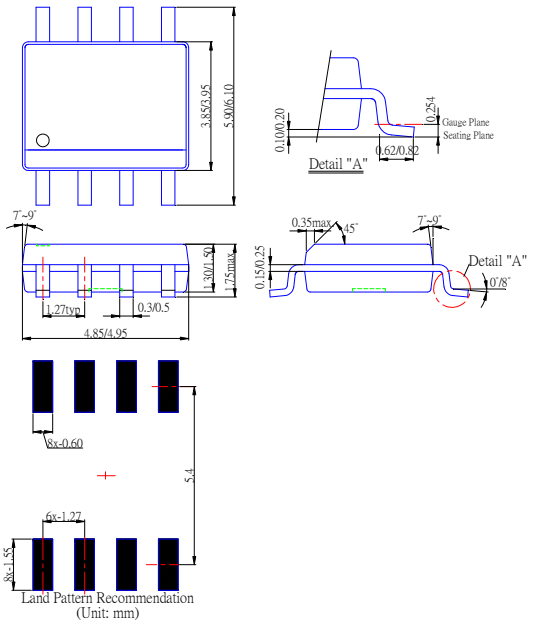



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Green

| Device | Package type | Identification Code |
|---|---|---|
| AP2141FM | DFN2018-6 | HR |
| AP2151FM | DFN2018-6 | HS |

## Package Information (All Dimensions in mm)

### (1) Package Type: SOP-8L

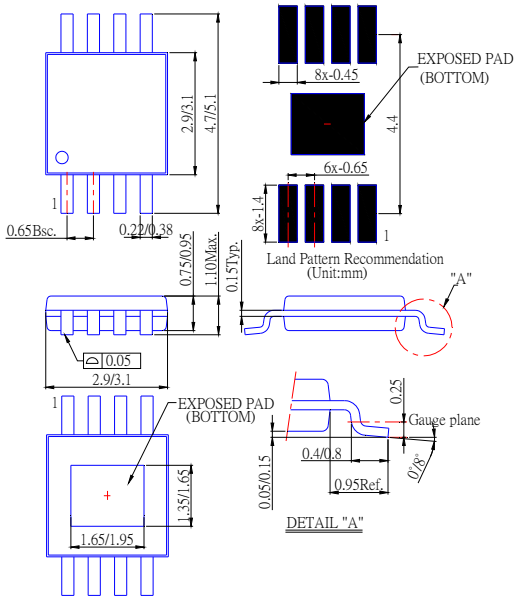




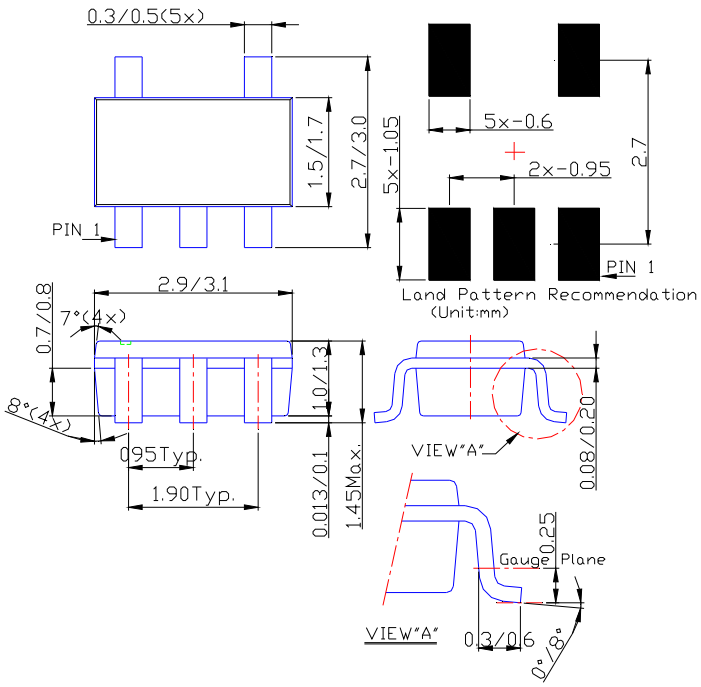
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## Package Information (Continued)

### (2) Package Type: MSOP-8L-EP




### (3) Package Type: SOT25

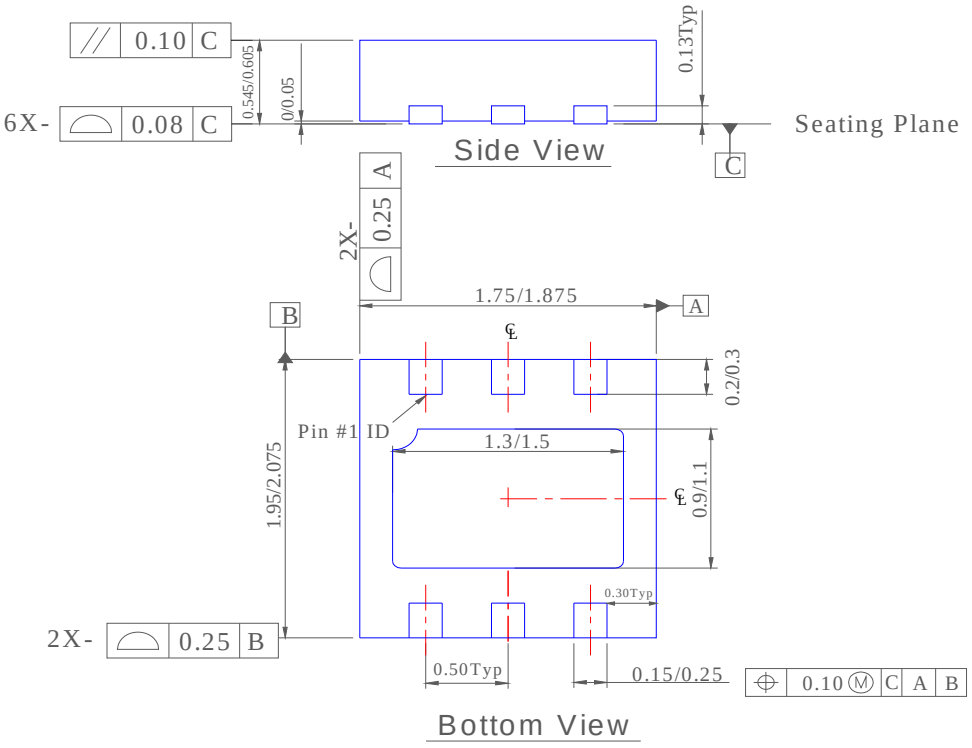




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## Package Information (Continued)

**(4) Package Type: DFN2018-6**

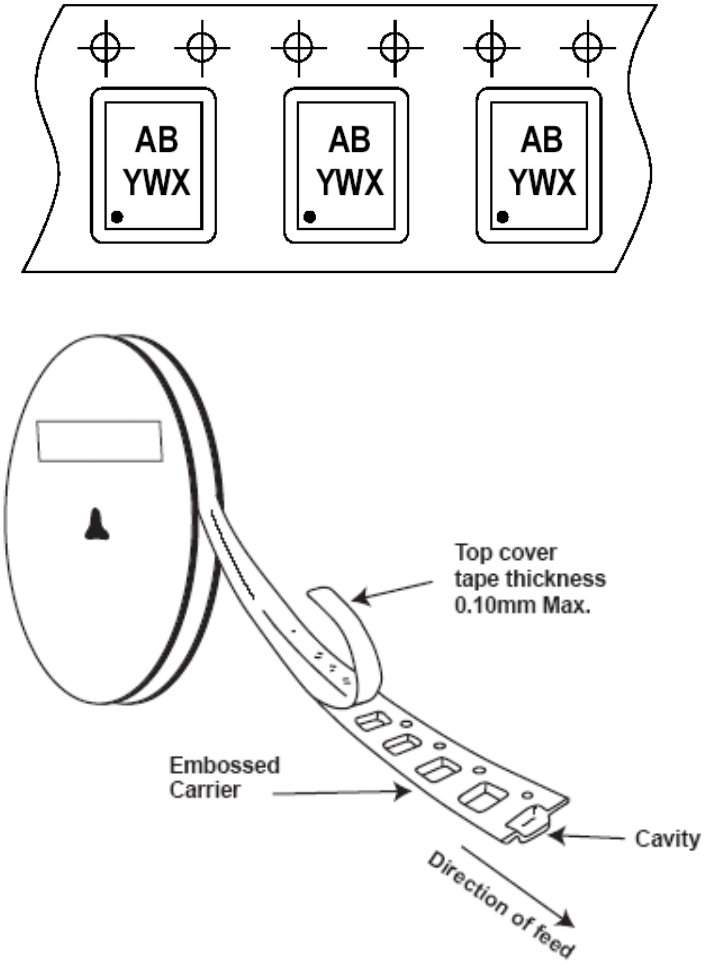




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## Taping Orientation

**For DFN2018-6**




Notes: 8. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf


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