AP1034

Stepper Motor Driver IC equipped with Active Decay Control

1. General Description

The AP1034 is driver for bipolar stepper motors. It supports 35V motor power supply and 2.0A constant current operation. The AP1034 can automatically control Decay setting (slow, fast, pre-fast) in the IC inside by AKM original "Active Decay Control". The AP1034 can achieve optimal current setting, therefore will reduce current ripple and bring the motor rotation operation of the high efficiency. The input interface is clock-in method and supports from 2 Phase (full step) to 2W1-2 Phase (1/8step) excitation. In addition, the AP1034 is built-in a regulator for control circuit and capable of driving a motor only by motor power supply voltage (VM), therefore can facilitate design for the application.
It is housed in a small QFN package with good heat dissipation performance, therefore the AP1034 is suitable for the stepping motor drive in a space-saving and high current.

2. Features

• Built-in PWM current control stepper motor driver	Active Decay Control
• Single Power Supply Operation	Built-in Regulator for control circuit
• Motor Operating Voltage	8.0 ~ 35.0V
• Max Output Current	2.0A
• On-Resistance (High+Low)	0.64Ω(typ.) @Ta=25℃
• Input Interface	Clock-in method
• Excitation Mode	2 Phase (Full step) 1-2 Phase (1/2 step) W1-2 Phase (1/4 step) 2W1-2 Phase (1/8 step)
• Selectable PWM chopper frequency	39kHz/77kHz
• Spike Noise Blanking Function	Without an external noise filter
• Power Saving Function	VM Power Consumption is less than10μA (Ta=25°C)
• Selectable Motor Rotation Direction	Forward/Reverse
• Corresponding to 3.3V/5V input signal	
• Built-in Charge Pump Circuit	
• Under Voltage Lockout Circuit(UVLO)	
• Thermal Shutdown Circuit (TSD)	
• Over Current Protection Circuit (OCP)	
• Operating Temperature Range	-30 °C ~ +85°C
• Package	AP1034AER: 24-pin QFN (4.0mm□) AP1034AEN: 32-pin QFN (5.0mm□)
• Pin Compatible Lineups	AP1035AER, AP1035AEN : 1.0A AP1037AER, AP1037AEN : 1.5A
• Applications	MFP/LBP, Scanner, Robotics ATM, Vending machines, Ticket machines, Moneychangers, Point of Sales System (POS) devices and etc.

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4. Block Diagram

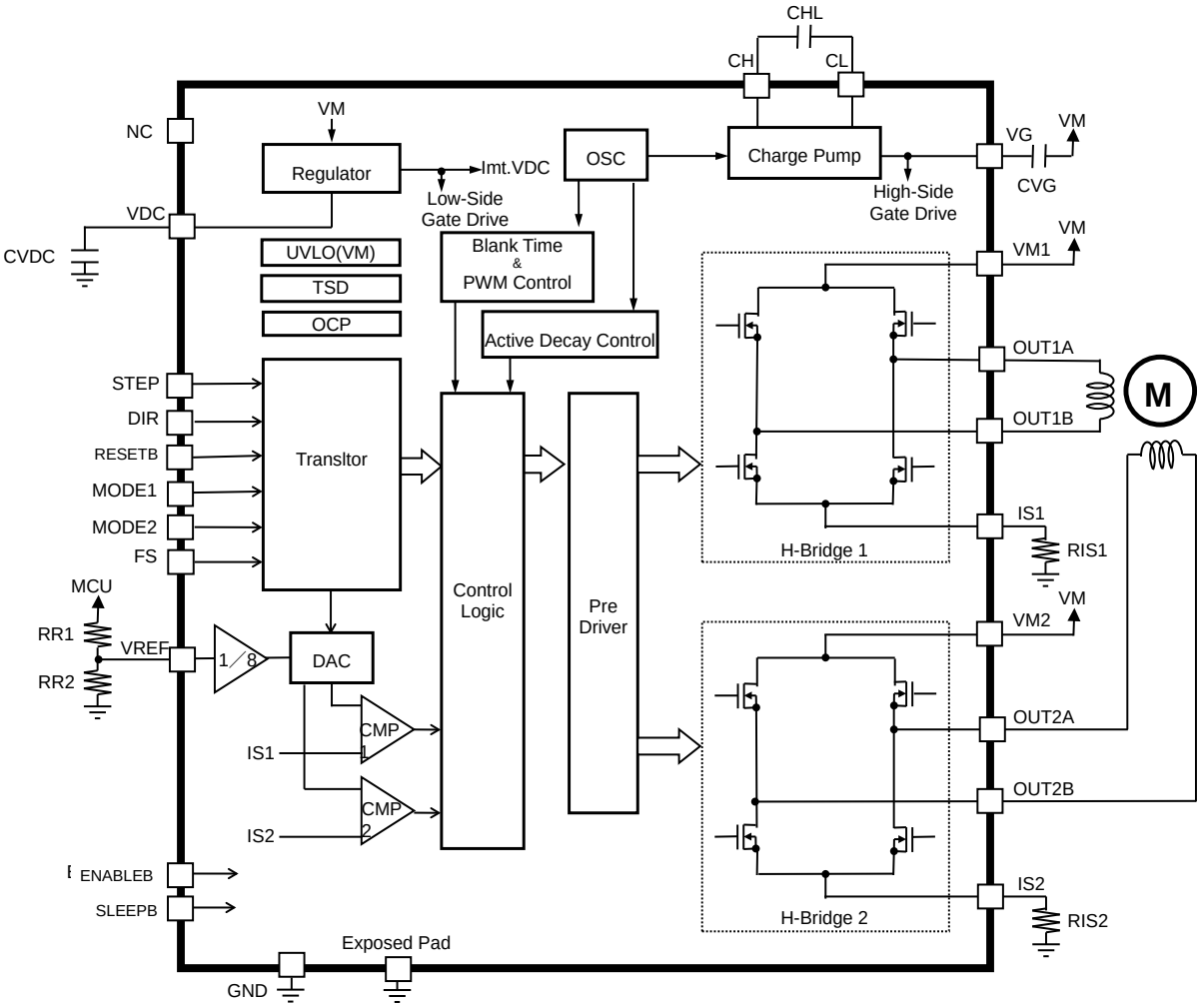


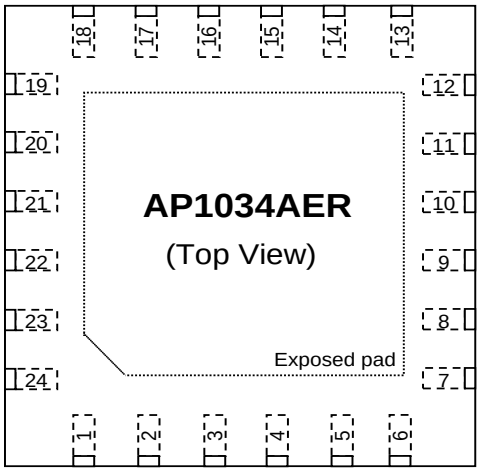
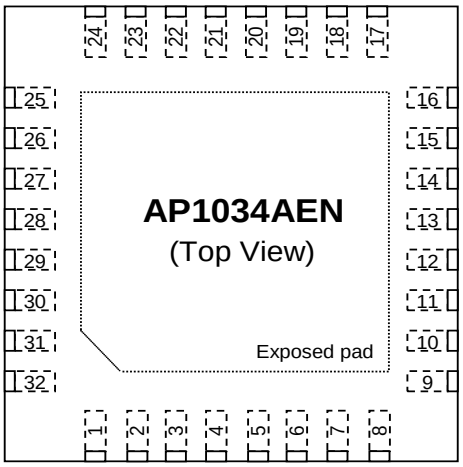
Figure 1. Block Diagram

5. Ordering Guide

AP1034AER	-30°C ~+85°C	24-pin QFN
AP1034AEN	-30°C ~+85°C	32-pin QFN

6. Pin Configurations and Function

■ Pin Configurations

AP1034AER: 24-pin QFN	AP1034AEN : 32-pin QFN
	

■ Functions

Pin Name	I/O	Pin Number		Function	Note
		24QFN	32QFN		
OUT2B	O	1	1	H-bridge 2 Output Terminal	
ENABLEB	I	2	5	Output Enable Terminal Please refer to Section10.1.	
GND	P	3,16	6,19	Ground Terminal	
CL	I	4	7	Connect Terminal for Charge Pump Capacitor	
CH	I	5	8	Connect Terminal for Charge Pump Capacitor	
VG	O	6	9	Connect Terminal for Stabilizing Capacitor	
VDC	O	7	10	Internal Regulator 4.5V Output Terminal	Not connect external node
MODE1	I	8	11	Motor Excitation Mode Setting Terminal Please refer to Section10.1.	Built-in 100kΩ pull-down
MODE2	I	9	12	Motor Excitation Mode Setting Terminal Please refer to Section10.1.	Built-in 50kΩ pull-down
RESETB	I	10	13	Reset Input Terminal Please refer to Section10.1.	Built-in 100kΩ pull-down
FS	I	11	14	Chopper Frequency Select Terminal Please refer to Section10.1.	Built-in 100kΩ pull-down
SLEEPB	I	12	15	Sleep Mode Input Terminal Please refer to Section10.1.	Built-in 100kΩ pull-down
STEP	I	14	17	Step Input Terminal Please refer to Section10.1.	
VREF	I	15	18	Input Terminal of Reference Voltage of PWM Constant Current Control	
DIR	I	17	20	Motor Rotate Direction Setting Terminal Please refer to Section10.1.	
OUT1B	O	18	24	H-bridge1 Output Terminal	
VM1	P	19	22	H-bridge1 Power Supply Terminal Please connect VM2 terminal in the system board.	
IS1	I	20	25	H-bridge1 Current Sense Terminal	
OUT1A	O	21	27	H-bridge1 Output Terminal	
OUT2A	O	22	30	H-bridge2 Output Terminal	
IS2	I	23	32	H-bridge2 Current Sense Terminal	
VM2	P	24	3	H-bridge2 Power Supply Terminal Please connect VM1 terminal in the system board.	
NC	-	13	2,4,16,21,23,26,28,29,31	No Connection Terminal	
Exposed Pad	-	-	-	Ground Terminal Please connect GND terminal in the system board.	For heat dissipation

Note 1. I (Input terminal), O (Output terminal), P (Power terminal)

7. Absolute Maximum Ratings

Parameter		Symbol	min	max	Unit	Condition
Motor Power Supply Voltage		VM	-0.5	35	V	
Digital Input/Output Terminal Voltage (STEP, DIR, RESETB, MODE1, MODE2, ENABLEB, SLEEPB, FS)		Vterm1	-0.5	5.5	V	
VM Level Terminal Voltage (OUT1A,OUT1B, OUT2A,OUT2B)		Vterm2	-0.5	VM	V	
VG,CH Terminal Voltage		Vterm3	VM -0.5	VM +5.5	V	The Min value must not exceed -0.5V.
VDC Terminal Voltage		VDC	-0.4	5.5	V	
V_{REF} Input Voltage		VREF	-0.5	VDC	V	
CL Terminal Voltage		VCL	-0.5	VDC	V	
IS1,IS2 Terminal Voltage		ISn	-0.5	1.5	V	
Output Current		Iload	-	2.5	A	(Note 3, Note 4)
Power Dissipation	32QFN	PD1	-	3.9	W	Ta=25°C (Note 4, Note 5)
			-	2.0	W	Ta=85°C (Note 4, Note 5)
	24QFN	PD2	-	3.1	W	Ta=25°C (Note 4, Note 5)
			-	1.6	W	Ta=85°C (Note 4, Note 5)
Junction Temperature		Tj	-	150	°C	
Storage Temperature		Tstg	-40	150	°C	

Note 2. All above voltages are with respect to GND. The each power supply of VC and VM is sequence-free.
Note 3. For Power Dissipation, the output current rating may be limited by duty cycle, Ta, and PCB board heat sinking design.
Note 4. Exposed Pad must be connected to GND.
Note 5. A 4-layer JEDEC51 compliant board is used.
If the temperature exceeds 25°C, be sure to derate at Figure 2.
24-pin QFN: R θ JA =40°C /W
32-pin QFN: R θ JA =32°C /W

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

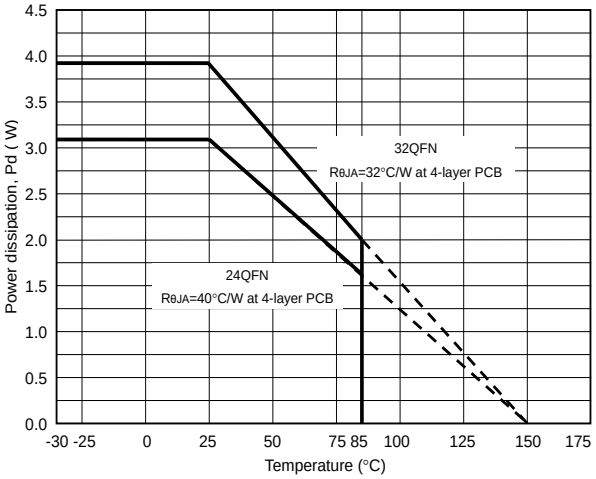


Figure 2. Maximum Power Dissipation

8. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Note
Motor Power Supply Voltage	VM	8.0	24.0	35.0	V	
Maximum Output Current (Continuous)	Iload	-	-	2.0	A	(Note 6)
Reference Voltage of PWM Constant Current Control	V_{REF}	0.0	-	3.6	V	Iload(100%)[A]=(V_{REF}/8)/R_{ISn}
Operating Temperature Range	Ta	-30	-	85	°C	

Note 6. Please have a thermal design so as not exceed Tj = 150 degrees and Power Dissipation.
Note 7. All voltages are with respect defined to GND (Exposed-Pad).

9. Electrical Characteristics

(Ta = 25°C, VM=24V, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Quiescent Current						
VM Quiescent Current	I_{VM}	ENABLEB="L"	-	-	12.0	mA
	I_{VMOFF}	ENABLEB="L" SLEEPB="H"	-	-	7.0	mA
	I_{VMPSV}	SLEEPB="L" SLEEP MODE	-	10	30	μA
H-bridge Circuit						
Driver On Resistance	R_{ON}	Iload = 1.5A	-	0.64	0.86	Ω
Body Diode Forward Voltage	V_F	I_F = 0.1A	-	0.8	1.2	V
Interface						
Input High Level Voltage	V_{IH}		2.0	-	-	V
Input Low Level Voltage	V_{IL}		-	-	0.8	V
Input Hysteresis (Note 9)	Vhys	STEP, DIR, RESETB, MODE1,MODE2,ENABLEB	0.2	0.4		V
Input Pulse Rise Time	t_R		-	-	1.0	μs
Input Pulse Fall Time	t_F		-	-	1.0	μs
Input High Level Current	I_{IH}	STEP,DIR, ENABLEB 5.5V applying	-	-	1.0	μA
Input Low Level Current	I_{IL}	0V applying	-1.0	-	-	μA
Reference Voltage						
VREF Input Voltage Range	V_{REF}		0	-	3.6	V
VREF Input Current	I_{VREF}	V_{REF}=2V	-3	-	3	μA

(Ta = 25°C, VM=24V, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Current Operation						
Blanking Time	t_B	FS="L"	1.3	2.6	5.2	µs
PWM Chopper Frequency	f_{CP1}	FS="L"	20	39	60	kHz
	f_{CP2}	FS="H"	40	77	120	kHz
Output Current Accuracy	$errI_{load}$	V_{REF}=2V, $\%I_{loadMAX}$=38%	-15	-	±15	%
		V_{REF}=2V, $\%I_{loadMAX}$=71%	-5	-	±5	%
		V_{REF}=2V, $\%I_{loadMAX}$=100%	-5	-	±5	%
Protection Circuit						
Overcurrent protection trip level	$I_{OCPTRIP}$		2.5	5.0	7.5	A
Overcurrent protection deglitch time	t_{OCPDET}		3.0	6.8	23.3	µs
Overcurrent protection deglitch voltage (Low side)	$VL_{OCPTRIP}$		0.5	-	1.1	V
Under Voltage Detect Voltage (UVLO)	VM_{UVLO}		5.7	6.35	7.0	V
Thermal Shut Down Temperature	T_{TSD}	(Note 9)	150	175	200	°C
Temperature Hysteresis	T_{TSDHYS}	(Note 9)	20	30	40	°C

Note 8. All above voltages are with respect to GND.
Note 9. Not tested in production.

(Ta = 25°C, VM=24V, unless otherwise specified.)

Parameter	Symbol	min	typ	max	Unit
STEP Signal "H" Level Time	$t_{WH(STEP)}$	1.0	-	-	µs
STEP Signal "L" Level Time	$t_{WL(STEP)}$	1.0	-	-	µs
DIR, MODEx Signal Setup Time	$t_{S(STEP)}$	200	-	-	ns
DIR, MODEx Signal Hold Time	$t_{H(STEP)}$	200	-	-	ns

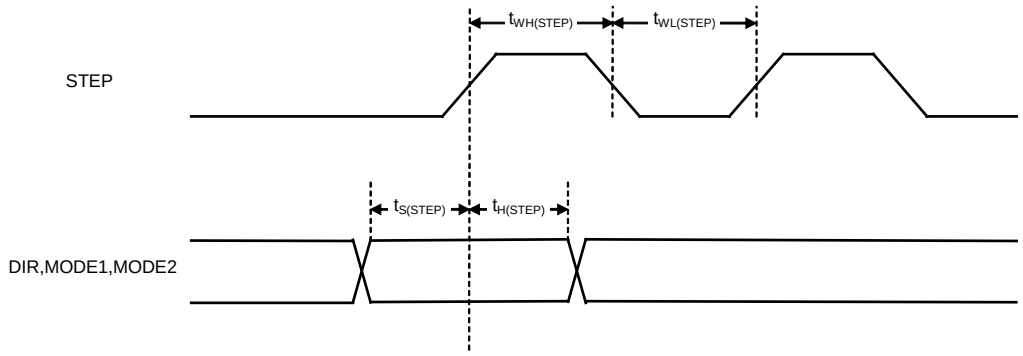


Figure 3. Timing Chart

10. Functional Descriptions

10.1 Input and Output of Terminal

■ Truth Table

Table 1. Output state against SLEEPB and ENABLEB settings

SLEEPB	ENABLEB	OUT1A OUT2A	OUT1B OUT2B	Condition
L	X	Output OFF (Hi-Z)	Output OFF (Hi-Z)	Sleep mode Internal control circuit : OFF
H	H	Output OFF (Hi-Z)	Output OFF (Hi-Z)	Disable mode Internal control circuit : ON
H	L	Output On	Output On	Enable mode DIR="H" : CW DIR="L" : CCW

Note 10. X : Don't Care

■ ENABLEB : Output Enable Terminal

When the input is "H", this pin turns off all the H-bridge outputs (motor output becomes Hi-Z). When the input is "L", all H-bridge outputs become enable. At that time, the input of sequencer (STEP,DIR,MODE1,MODE2) is independent of the logic of enable. ENABLEB input is the function of making H-Bridge output off. During output is off, the input of sequencer (STEP,DIR,MODE1,MODE2) is hold. Refer to Figure 4.

Table 2. Settings of output enable terminal

ENABLEB	Condition
L	Operating mode
H	Output Hi-Z (Electrical angle hold)

■ SLEEPB : Sleep Mode Setting Terminal

When the input is "L", this pin sets the IC in sleep mode, and turns off all the H-bridge outputs, internal regulator, and charge pump circuit (motor output becomes Hi-Z). Control circuit is reset. If the "H" is input, the sleep mode is canceled. After the sleep mode is canceled, it restarts from the home position (Table 9). STEP input cannot be input during 3msec(max) after the sleep mode is canceled, to wait for the stable operation of internal charge pump. Refer to Figure 5. Please input "L" to SLEEPB terminal when turning on power.

Table 3. Settings of sleep mode terminal

SLEEPB	Condition
L	SLEEP mode (Output : Hi-Z)
H	Operating mode

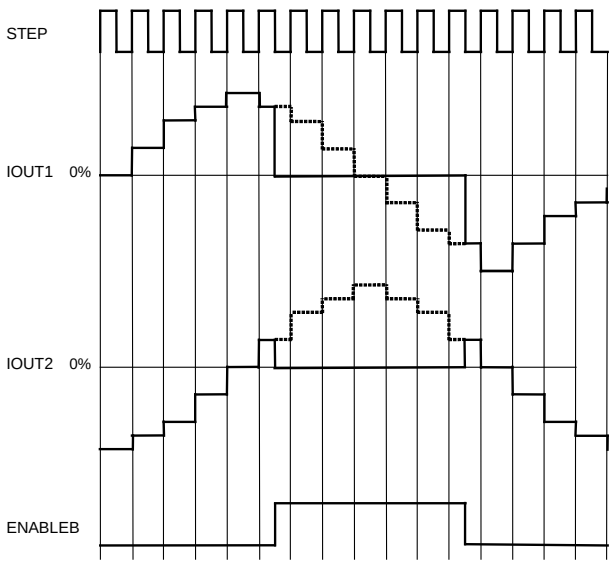


Figure 4. ENABLEB signal Timing Chart (W1-2 phase)

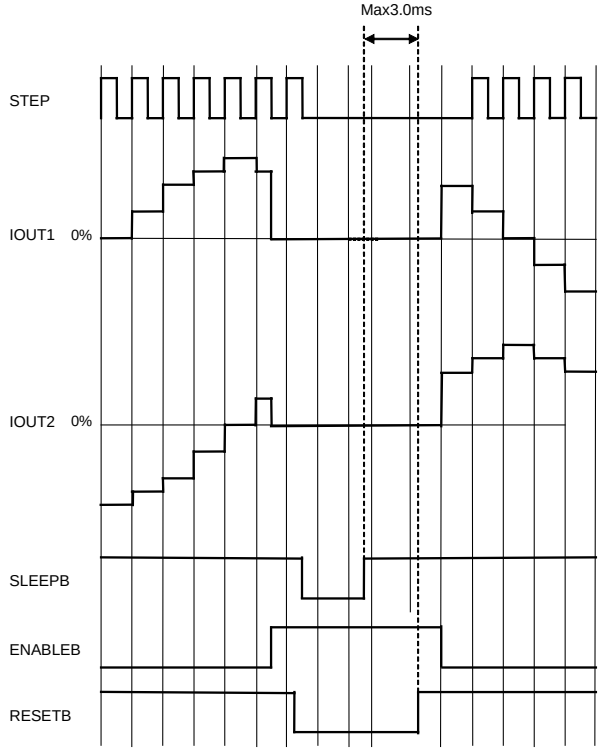


Figure 5. Sleep Mode Cancel Timing Chart (W1-2 phase)

■ MODE1,MODE2 : Motor Excitation Mode Setting Terminal

The MODE1 and MODE2 terminals are used to configure stepping format as shown below.

Table 4. Settings of MODE terminals that excite motor

MODE1	MODE2	Excitation mode
L	L	2 phase (Full step)
H	L	1-2 phase (1/2step)
L	H	W1-2 phase (1/4step)
H	H	2W1-2phase (1/8step)

■ STEP : Step Input Terminal

The sequencer operates at the rising edge of the STEP input, electrical angle will proceed one at each step. Please design the pattern such that there is no jump of noise in STEP input terminal.

Table 5. Step excitation state against STEP input

STEP	Condition
Rising Edge	Sends excitation step
Falling Edge	Hold excitation step

■ DIR : Motor Rotation Direction Setting Terminal

This pin sets the direction of motor rotation. When changing the direction, a new setting is reflected on a rising edge of the CLK pin. Refer to Figure 6.

・CCW : H-bridge2 current is output by shifting 90deree ahead against the H-bridge1 current.

・CW : H-bridge2 current is output by shifting 90degree behind against the H-bridge1 current.

Table 6. Settings of rotate direction of motor

DIR	Condition
L	CCW (Reverse)
H	CW (Forward)

■ RESETB : Home Position Setting Terminal

When the RESETB input is “H”, the sequencer is set at home position, and all the H-bridge outputs become off (motor output becomes Hi-Z). In this case, STEP input is ignored until “H” is input to the RESETB terminal. The internal circuits are in enable state. Refer to Figure 7.

Table 7. Settings of home position terminal

RESETB	Condition
L	Output : Hi-Z (Home Position)
H	Operating mode

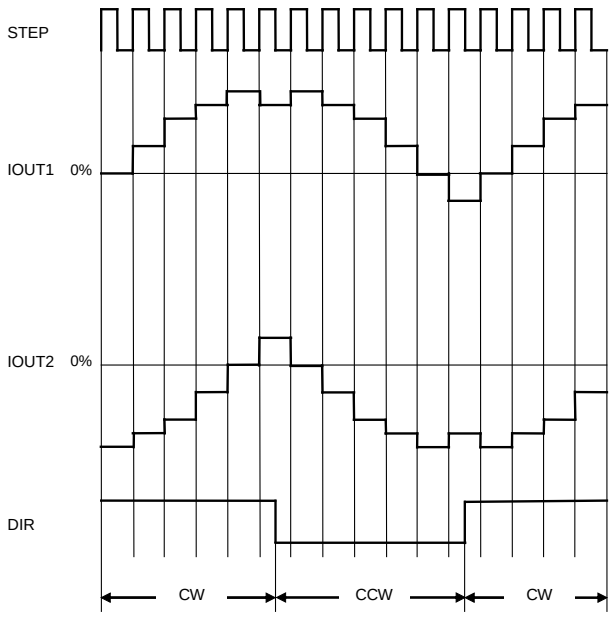


Figure 6. DIR signal Timing Chart (W1-2 phase)

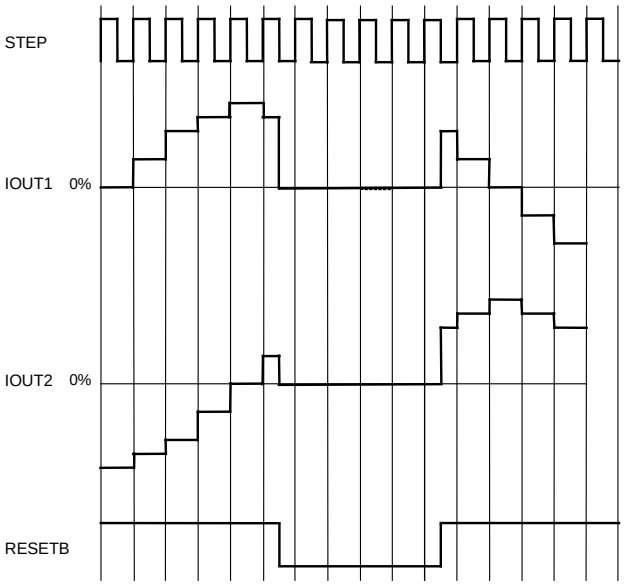


Figure 7. RESETB signal Timing Chart (W1-2 phase)

■ FS : PWM Chopper Frequency Select Terminal
By inputting “H” to the FS input, it is possible to drive the PWM chopper frequency in 77kHz (typ). By inputting “L” or connecting GND, PWM chopper frequency becomes 39kHz (typ).
Please decide the setting of the FS input “50us” before than the ENABLEB input is set to "L".

Table 8. Settings of PWM chopper frequency select terminal

FS	Condition
L	f_{CP}=39kHz(typ)
H	f_{CP}=77kHz(typ)

10.2 PWM Constant Current Control

■ Setting of the Output Current

The frequency of the internal OSC circuit is used to drive a stepper motor in PWM constant current controlling. The maximum current value (Setting Current = Trip Current) is determined by a sense resistance (R_{IS}) for sensing current and the input voltage to the VREF pin (V_{REF}).

Iload (100%) [A]= (V_{REF} /8) / R_{IS}
VREF : PWM constant current setting voltage
RIS : H-Bridge sense resistor
VREF damping ratio : 1/8

Calculation example1 : VREF=2.5V, RIS=0.2ohm
Iload (100%)[A] = (2.5 / 8) / 0.2ohm = 1.56A

In the figure below, area shaded in gray is the range of recommended sense resistance value.

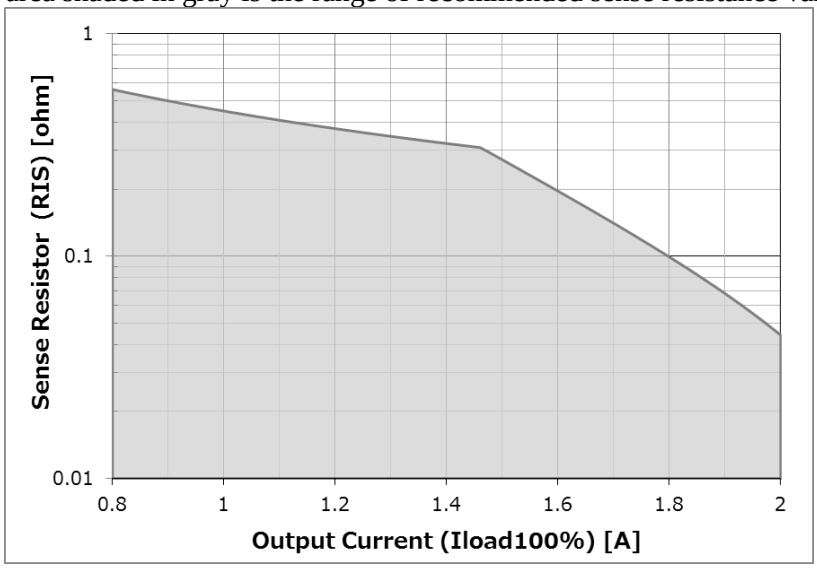


Figure 8. Recommended Sense Resistor

■ Active Decay Mode Current Waveform

The AP1034 selects the decay mode automatically for better current follower performance. Usually, it operates in slow decay mode but changes to fast decay mode when switching the step during current decreasing period.

Also There is Pre fast decay mode before Charge mode. Therefore if in the low target current, it is possible to reduce the current distortion.

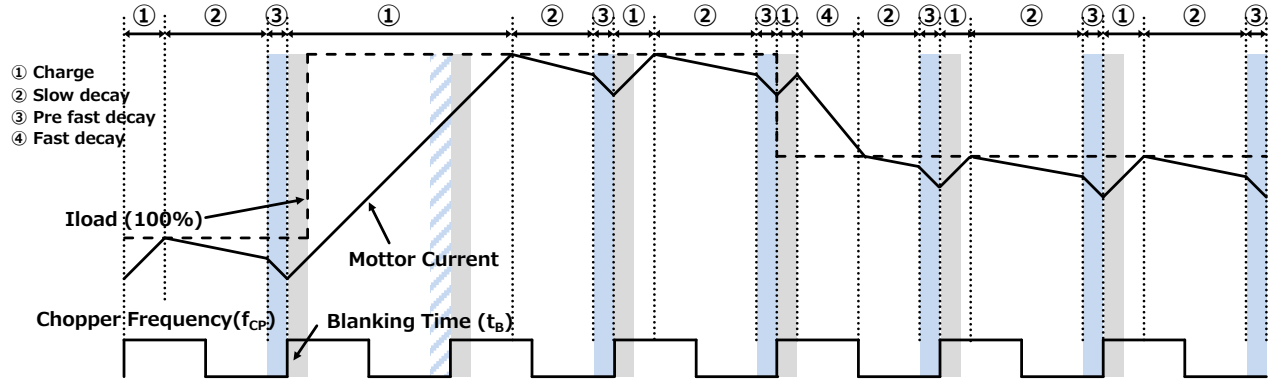


Figure 9. Active Decay Mode Current Waveform

■ Blanking Time

Recovery current of parasitic diode arises when the decay mode changes charge mode during PWM constant current operation. It can flow into current sense resistor, and the noise of current sense terminal (IS1,IS2) cause the malfunction of internal comparator (CMP1,CMP2) . To prevent malfunction, the detection of current sense comparator is blanking during Charge mode. The blanking time of the IC is 2.6us fixed at FS=L, 1.3us fixed at FS=H.

■ Output Transistor Operating Mode

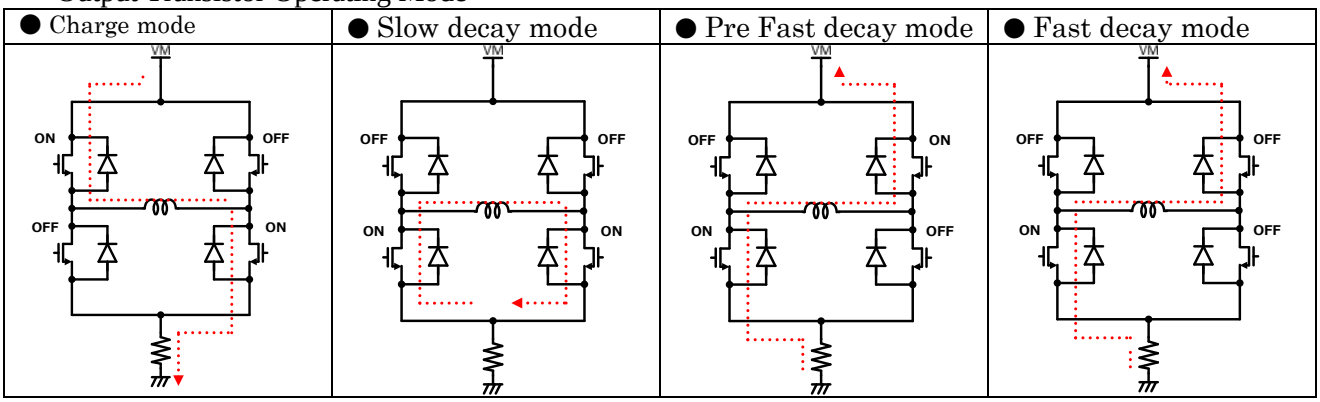


Figure 10. Current Flow of Mixed Decay Mode

10.3 Micro-Step Function

■ Step Sequence

Table 9. Setting Current Comparison of Excitation Modes

2 phase (Full step)	1-2 phase (1/2step)	W1-2 phase (1/4step)	2W1-2 phase (1/8step)	Phase1 Current [%$I_{loadmax}$]	Phase2 Current [%$I_{loadmax}$]	Step Angle [°]
	1	1	1	100	0	0.00
			2	98	20	11.25
		2	3	92	38	22.50
			4	83	56	33.75
1	2	3	5	71	71	45.00
			6	56	83	56.25
		4	7	38	92	67.50
			8	20	98	78.75
	3	5	9	0	100	90.00
			10	-20	98	101.25
		6	11	-38	92	112.50
			12	-56	83	123.75
2	4	7	13	-71	71	135.00
			14	-83	56	146.25
		8	15	-92	38	157.50
			16	-98	20	168.75
	5	9	17	-100	0	180.00
			18	-98	-20	191.25
		10	19	-92	-38	202.50
			20	-83	-56	213.75
3	6	11	21	-71	-71	225.00
			22	-56	-83	236.25
		12	23	-38	-92	247.50
			24	-20	-98	258.75
	7	13	25	0	-100	270.00
			26	20	-98	281.25
		14	27	38	-92	292.50
			28	56	-83	303.75
4	8	15	29	71	-71	315.00
			30	83	-56	326.25
		16	31	92	-38	337.50
			32	98	-20	348.75

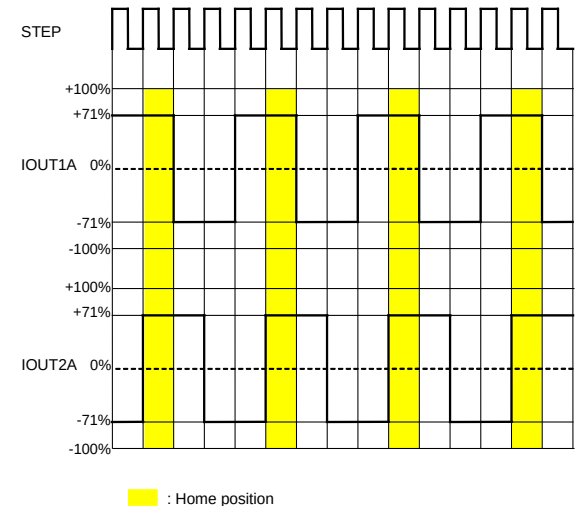
: Home micro-step position at Step Angle 45°

Note 11. When the excitation mode is changed to a coarser mode, it is set to the closest position in the rotate direction set by DIR signal. However, the motor could step-out or misstep depends on the operation state of motor during switching time. The changing sequence of the excitation mode should be determined by adequate evaluation.

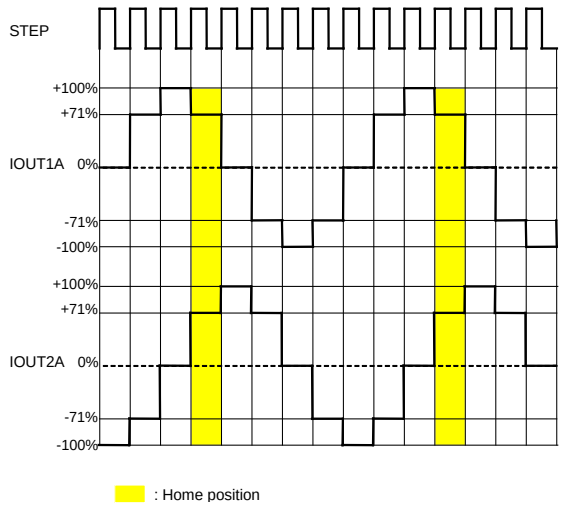
Table 10. When changing to 2phase excitation mode at eighth position from 2W1-2phase excitation mode

DIR	Before	After
	2W1-2	2phase(4step)
H	8step position	2step position
L	8step position	1step position

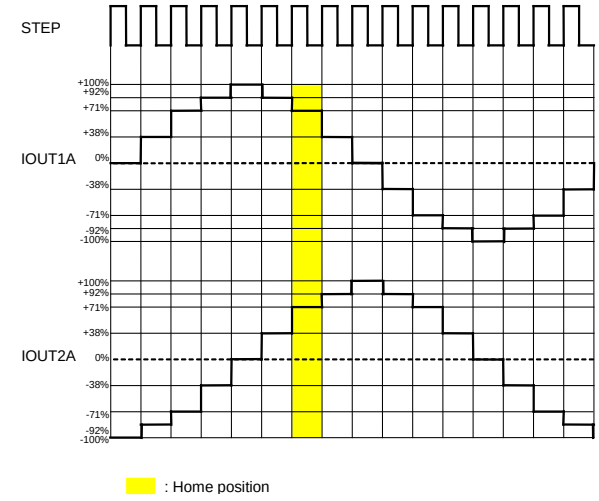
■ Example of Current Waveforms in Each Excitation Mode



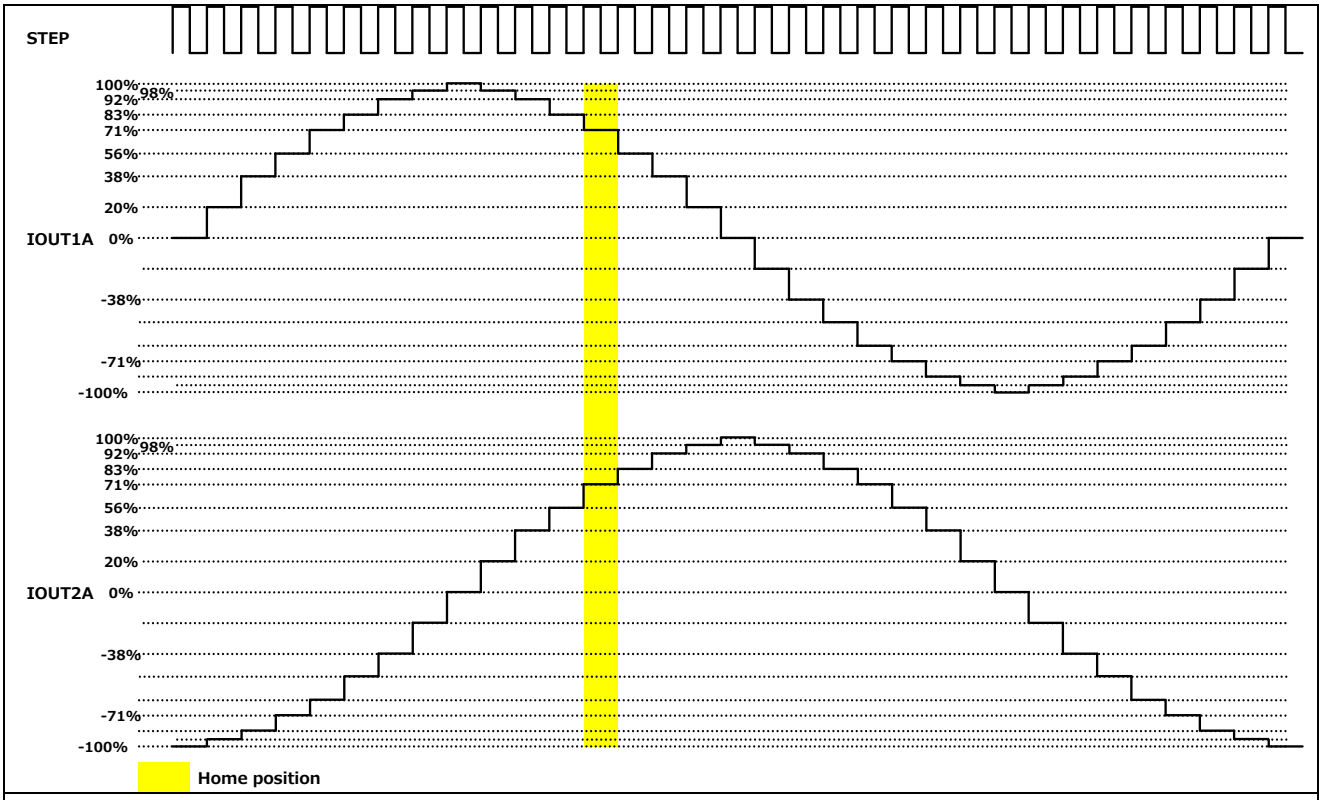
2 phase (CW mode : DIR=”H”)



1-2 phase (CW mode : DIR=”H”)



W1-2 phase (CW mode : DIR=”H”)



2W1-2 phase (CW mode : DIR="H")

Note 12. "+" means the current is flowing through the OUT1B from OUT1A and the OUT2B from OUT2A.

10.4 Protection Functions

Table 11. Recovery type and the output state of the protection circuit

Protection Circuit		H-Bridge Outputs	Recovery type
Thermal Shutdown (TSD)		Hi-Z	Automatic
Under Voltage Lockout (UVLO)		Hi-Z	Automatic
Over Current Protection (OCP)	Shorted-Load	Hi-Z	Latch off
	Shorted-to-Ground		
	Shorted-to-Power		

■ Thermal Shutdown Circuit (TSD)

If the internal temperature of the IC (Tj) reaches 175 °C (typ), the H-Bridge outputs Hi-Z. In addition, it will automatically return to the normal operation when it becomes less than 145 °C (typ).

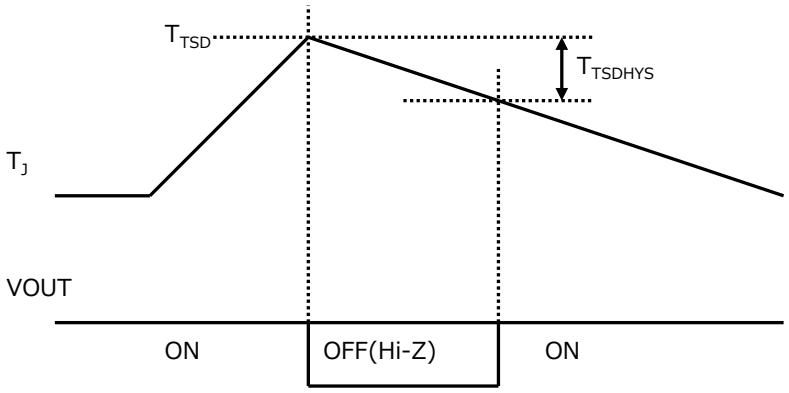


Figure 11. TSD Timing Chart

■ Under Voltage Lock Output Circuit (UVLO)

When VM voltage is lower than 6.35V (typ), the H-Bridge output is the Hi-Z. Please note that this circuit does not operate during sleep mode. When UVLO operates, internal circuits which includes H-Bridge output, internal regulator, charge pump circuit become disable, and also the control circuit is reset (initialize). If VM voltage goes up than the specified voltage, UVLO is released. After the UVLO released, it restarts from the home position. STEP input cannot be input during 3msec after the UVLO is canceled, to wait for the stable operation of internal charge pump.

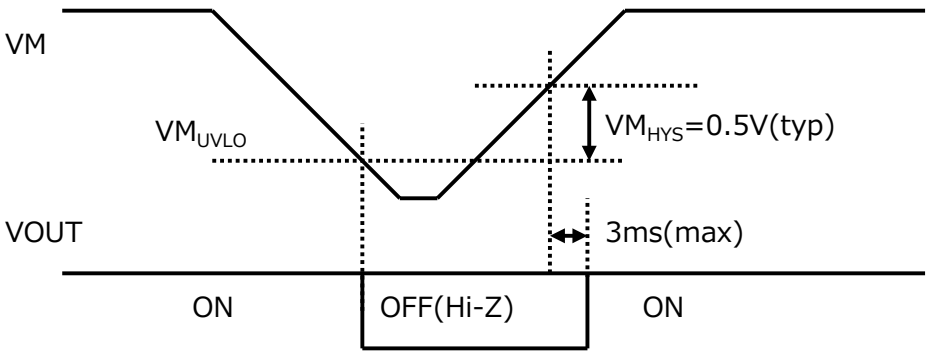


Figure 12. UVLO Timing Chart

■ Over Current Protection Circuit (OCP)

The IC has over current protection circuit to prevent breakdown of H-Bridge drivers. If the specified current flows, H-Bridge outputs of all channel becomes latch off. It recovers by re-input of the motor power supply voltage (VM) or input of SLEEPB or RESETB.

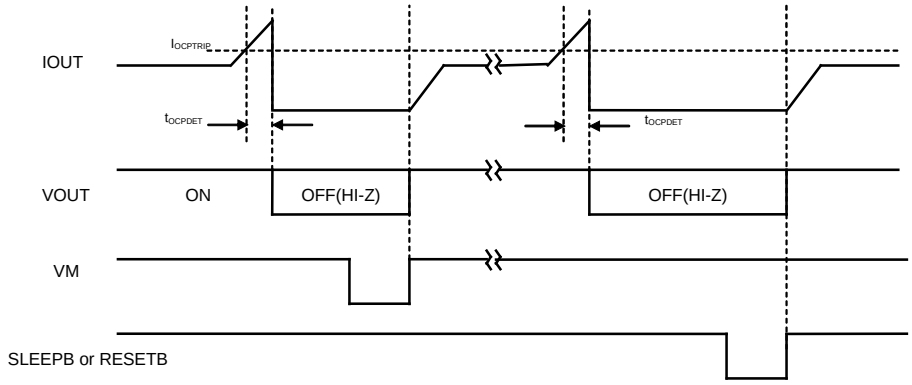


Figure 13. OCP Timing Chart

Note13. If latch is released under the abnormal condition after OCP operation, the IC may repeat the operation(latch → return → latch) . This will be the cause of heat generation and deterioration of the IC. Also, chattering noise on SLEEPB or RESETB pin may cause a malfunction of OCP and it will result in damage to the device.

Note14. When the Shorted-Load or the Shorted-to-Power occurs, the current comparison comparator works. After the blanking time, the IC becomes slow decay mode and repeats normal operation every chopper cycle.

Note15. If the current sense resistors(R_{IS}) are shorted, the OCP operates before the current comparator comparison works in all conditions, so that the output of all channels will be Hi-Z.

11. Recommended External Circuit

■ Recommended External Circuit

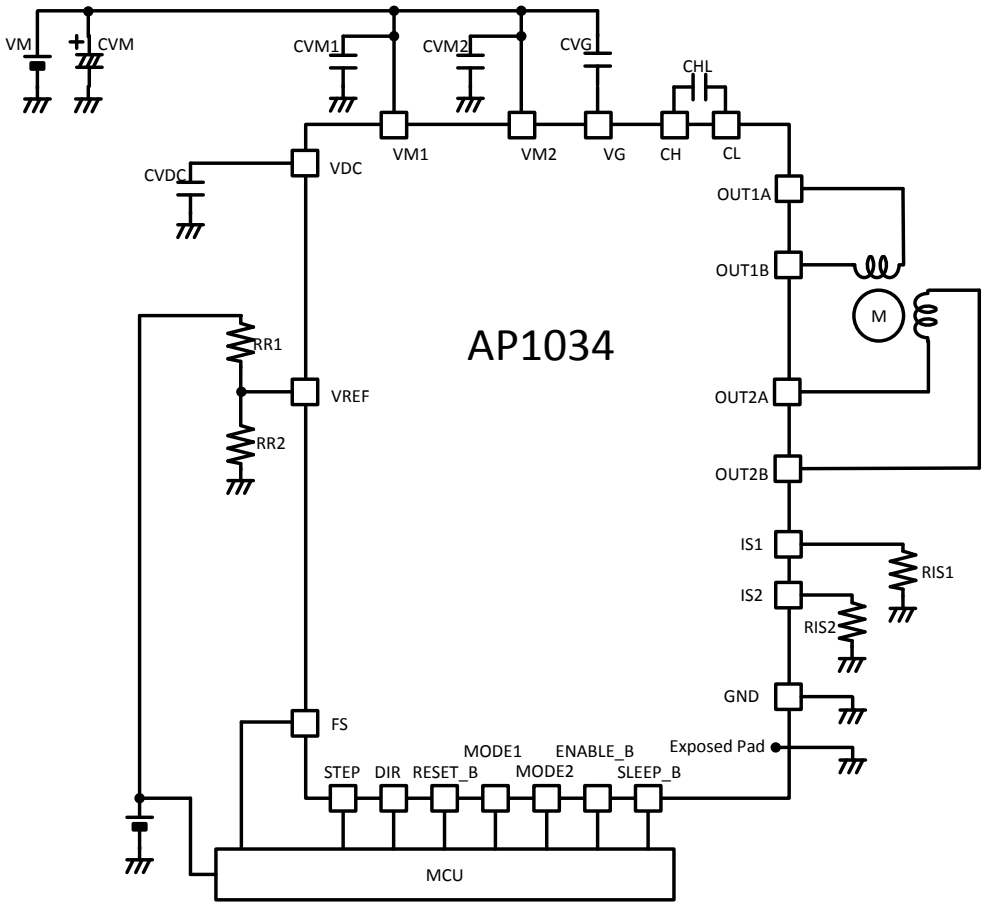


Figure 14. Recommended External Circuit

Table 12. Recommended External Components

Items	typ	Unit	Remark
CVM	100	μF	Electrolytic Capacitor
CVM1	0.22	μF	Ceramic Capacitor
CVM2	0.22	μF	Ceramic Capacitor
CHL	0.01	μF	Ceramic Capacitor
CVG	0.1	μF	Ceramic Capacitor
CVDC	0.22	μF	Ceramic Capacitor
RIS1	0.2	Ω	At 1.56[A]setting (@VREF=2.5V)
RIS2	0.2	Ω	At 1.56[A]setting (@VREF=2.5V)
RR1	30	kΩ	At VREF=2.5V setting (@VC=5.0V)
RR2	30	kΩ	At VREF=2.5V setting (@VC=5.0V)

Note 16. Above values are examples. Please choose appropriate external components for your system board.
Note 17. Capacitance of CVM and CVC should be determined in consideration of the load current profile, the load capacitance, the line resistance and etc. of the actual system board.

■ Recommended Layout

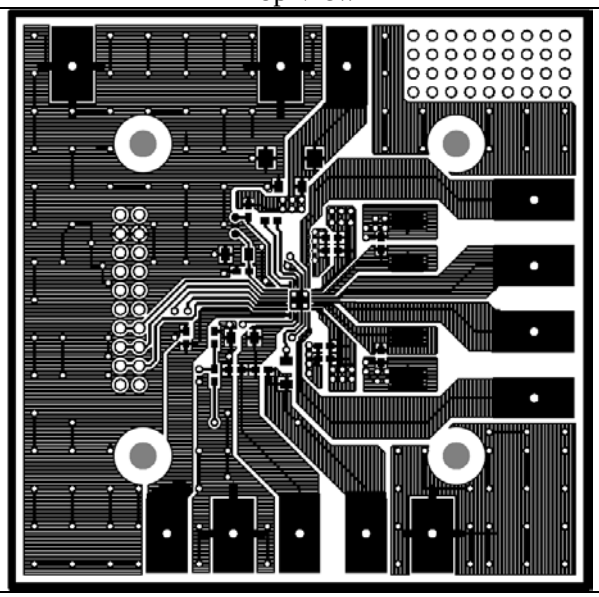
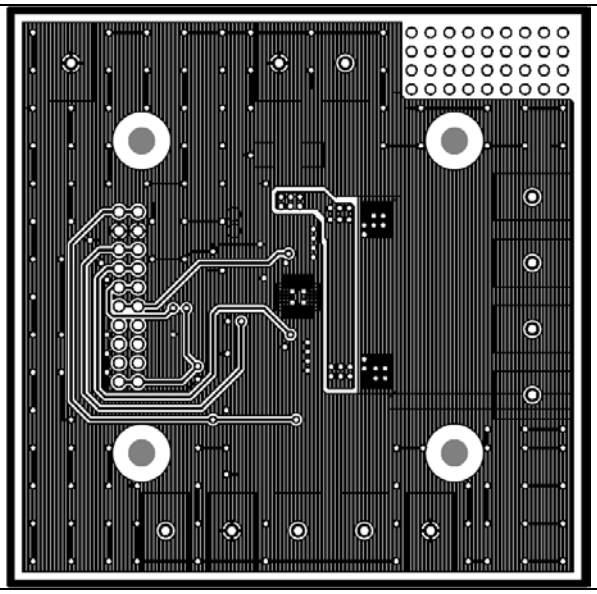
Top View	Bottom View
	

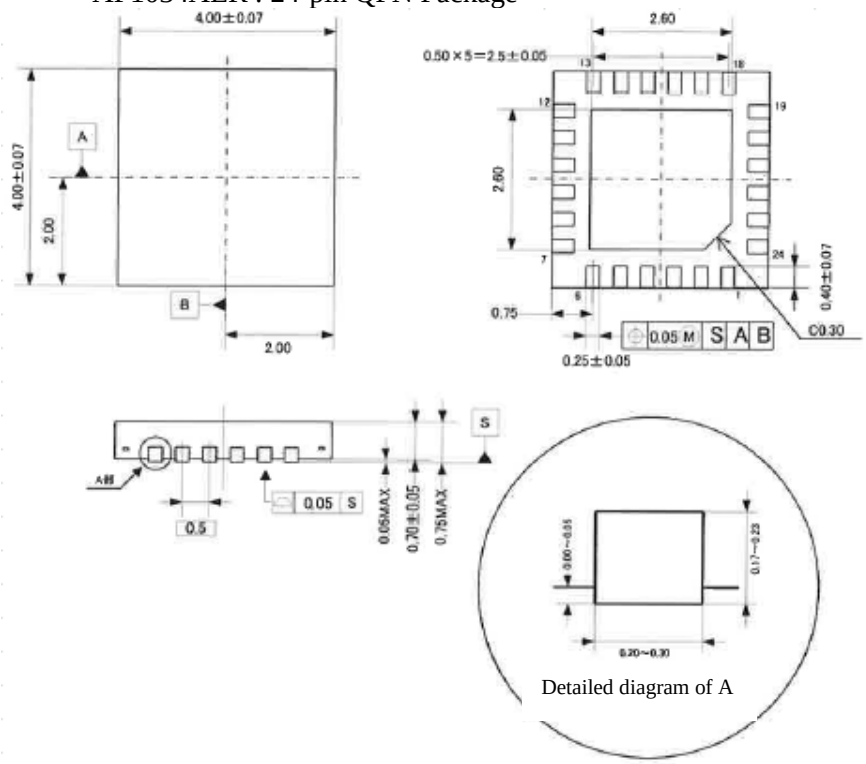
Figure 15. Recommended Layout Pattern

Note 18. Please layout the large ground plane on the PCB.
Note 19. Exposed Pad (heat sink) is common to the ground terminal. Please connect it to the ground of the PCB.
Note 20. The ground via of the PCB back side under IC mounted area is effective for heat radiation to each layer of the PCB.

12. Package

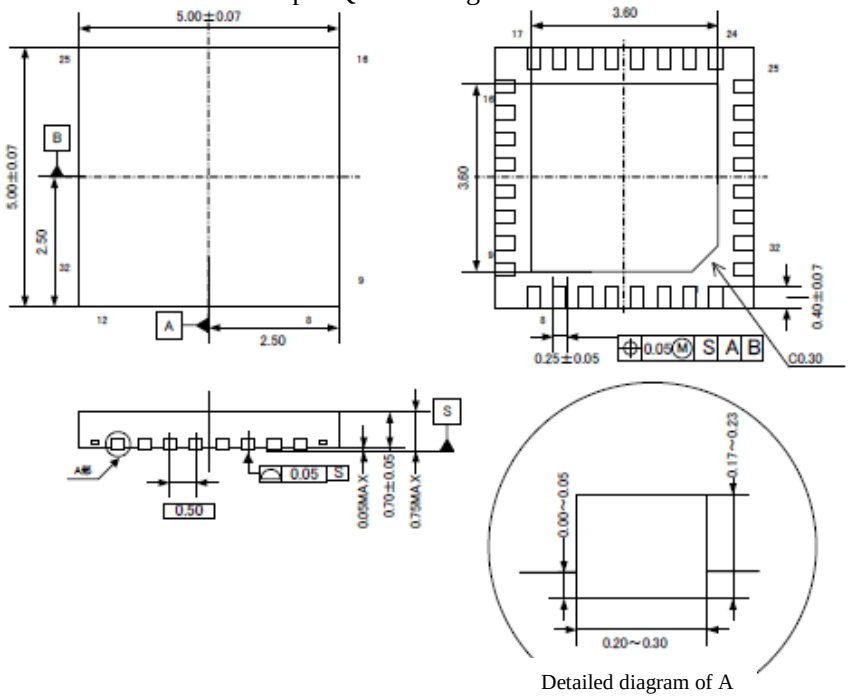
■ Outline Dimensions

● AP1034AER : 24-pin QFN Package



Unit : mm

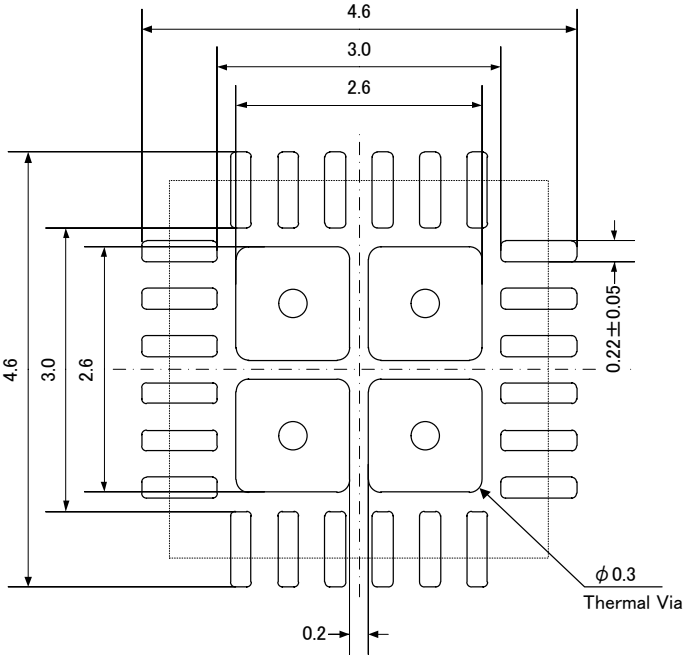
● AP1034AEN : 32-pin QFN Package



Unit : mm

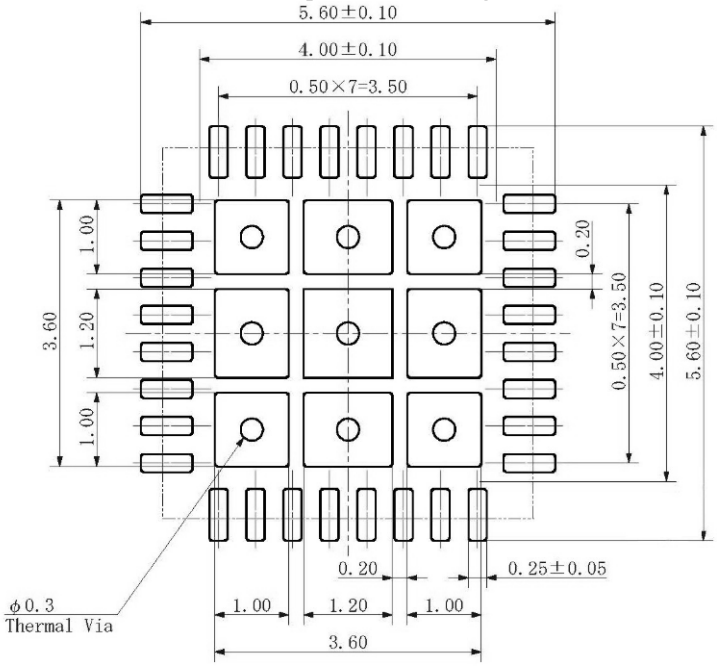
■ **Recommended Land Pattern**

- AP1034AER ： 24-pin QFN Package



【unit : mm】

- AP1034AEN ： 32-pin QFN Package

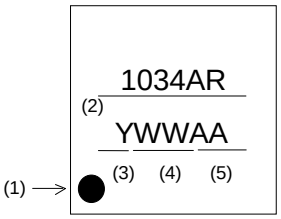


【unit: mm】

∗The most suitable dimensions of the mount pad change by a substrate material, solder paste materials, a soldering method, device precision. It is therefore recommended that customers contact the actual design should be optimized according to the situation.

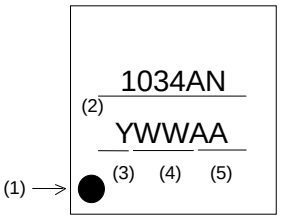
■ Marking

● AP1034AER



(1) 1pin Indication
(2) Market No.
(3) Year code (last 1 digit)
(4) Week code
(5) Management code

● AP1034AEN



(1) 1pin Indication
(2) Market No.
(3) Year code (last 1 digit)
(4) Week code
(5) Management code

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
16/04/20	00	-	First Edition
16/06/28	01	12	<Add >: Figure8
		18	<Add> In addition, please do not make chattering noise for SLEEPB or RESETB signal because it causes the malfunction of the OCP circuit and may let an IC damage.
		19	<Modify>: Table 13. Recommended External Components

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