*RoHS Compliant*

# SATA Disk Module

***Specification of SDM // M1***

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*Version 1.3*

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# Features:

- **Standard Serial ATA 2.6 (Gen. 2)**
  - Serial ATA 2.6 (Gen. 2)
  - SATA II, 3.0 Gbps
  - ATA-compatible command set
- **Capacities**
  - 4, 8, 16 GB
- **Performance**
  - Burst read/write: 300 MB/sec
  - Sustained read: up to 100 MB/sec
  - Sustained write: up to 88 MB/sec
- **Intelligent endurance design**
  - Built-in hardware BCH ECC, correcting 8-bit or 15-bit error per 512-byte data sector
  - Global wear-leveling scheme together with dynamical block allocation to significantly increase the lifetime of a flash device and optimize the disk performance
  - Flash bad-block management
  - Power Failure management
  - Quick Erase
  - S.M.A.R.T.
- **NAND Flash Type: SLC**
- **Data integrity under power-cycling**
  - No battery required for data storage
- **Temperature**
  - 0℃ to 70℃ for operating
  - -40℃ to 100℃ for storage
- **Supply voltage**
  - 3.3 V ± 5%
- **Low power consumption**
  - Active mode: 260 mA
  - Idle mode: 130 mA
- **Form Factor**
  - Mini PCIe form factor
- **Connector**
  - mSATA
- **RoHS compliant**


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# Table of Contents

1. Product Description ..... 3
1.1 Introduction ..... 3
1.2 Functional Block Diagram ..... 3
1.3 ATA Mode Support ..... 4
1.4 Capacity Specification ..... 4
1.5 Performance ..... 4
1.6 Pin Assignment ..... 5
2. Software Interface ..... 6
2.1 Command Set ..... 6
3. Flash Management ..... 8
3.1 Error Correction/Detection ..... 8
3.2 Bad Block Management ..... 8
3.3 Wear Leveling ..... 8
3.4 Power Failure Management ..... 8
3.5 Quick Erase ..... 8
3.6 S.M.A.R.T. ..... 9
4. Environmental Specifications ..... 10
4.1 Environments ..... 10
4.2 Mean Time Between Failures (MTBF) ..... 10
4.3 Certification and Compliance ..... 10
5. Electrical Characteristics ..... 11
5.1 Operating Voltage ..... 11
6. Physical Characteristics ..... 12
7. Product Ordering Information ..... 13
7.1 Product Code Designations ..... 13
7.2 Valid Combinations ..... 14


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# 1. Product Description

## 1.1 Introduction

Apacer's SDM II M1 is a solid-state disk (SSD) drive that contains a controller, embedded firmware, and flash media along with a male connector. Using NAND flash memory devices, the SAFD drive interfaces with the host allowing data to be seamlessly transferred between the host and the flash devices.

The SDM II M1 drive is designed with a single-chip controller, offering capacities of up to 16 gigabytes and providing full support for the SATA II high-speed interface standard. It can operate at sustained access rates of up to 100 megabytes per second, which is much faster than any other solid-state or traditional SATA drive currently available on the market.

In addition to buffer management through dynamical allocation, the SDM II M1 adopts the Apacer-specific global wear-leveling scheme to allow uniform use of all storage blocks, ensuring that the lifetime of a flash media can be significantly increased and the disk performance is optimized as well. The SDM II M1 provides the S.M.A.R.T. feature that follows the SATA Rev. 2.6, ATA/ATAPI-7 specifications and uses the standard SMART command B0h to read data from the drive. This feature protects the user from unscheduled downtime by monitoring and storing critical drive performance.

## 1.2 Functional Block Diagram

The SDM M1 drive includes a single-chip SATA II Controller and the flash media, as well as the SATA standard interface. The controller integrates the flash management unit with the controller itself to support multi-channel, multi-bank flash arrays. Figure 1-1 shows the functional block diagram.

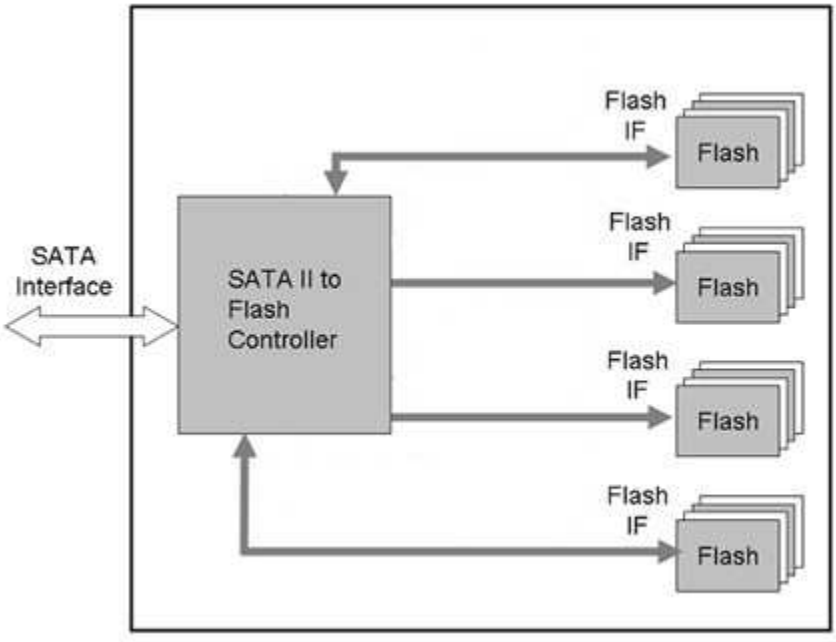



**Figure 1-1** Apacer SDM M1 block diagram


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## 1.3 ATA Mode Support

The SDM II M1 provides ATA mode support as follows:

- Up to PIO mode-4
- Up to Multiword DMA mode-2
- Up to UDMA mode-5

## 1.4 Capacity Specification

Capacity specification of the SDM II M1 product family is available as shown in Table 1-1. It lists the specific capacity, the default numbers of logical cylinders and heads, and the number of logical sectors per track for each product line.

**Table 1-1** Capacity specification

| Capacity | Total Bytes | Cylinders | Heads | Sectors | Max LBA |
|---|---|---|---|---|---|
| 4 GB | 4,021,936,128 | 7,793 | 16 | 63 | 7,855,344 |
| 8 GB | 8,061,419,520 | 15,620 | 16 | 63 | 15,744,960 |
| 16 GB | 16,139,681,792 | 16,383 | 16 | 63 | 31,522,816* |

*Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.

## 1.5 Performance

Performance of the SDM II M1 is shown in Table 1-2.

**Table 1-2** Performance specification

| Capacity / Performance | 4 GB | 8 GB | 16GB |
|---|---|---|---|
| Sustained Read (MB/s) | 100 | 100 | 100 |
| Sustained Write (MB/s) | 46 | 88 | 88 |

Note: Performances vary from flash configurations.


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## 1.6 Pin Assignment

Pin assignment of the SDM II M1 is shown in Figure 1-2 and described in Table 1-3.

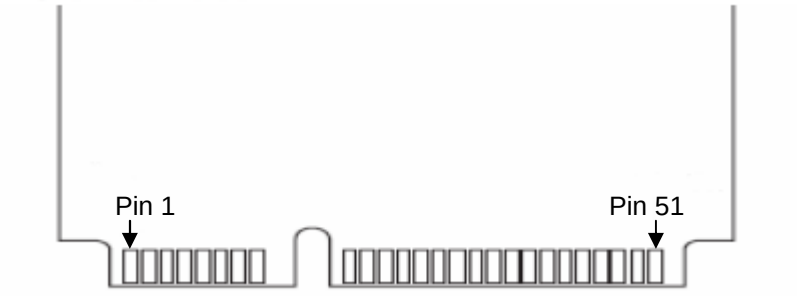



**Figure 1-2** Apacer SDM M1 pin assignment

**Table 1-3** Pin Assignment Description

| Pin # | Assignment | Description | Pin # | Assignment | Description |
|---|---|---|---|---|---|
| 1 | N/A | N/A | 27 | GND | Return Current Path |
| 2 | +3.3V | 3.3V source | 28 | N/A | N/A |
| 3 | N/A | N/A | 29 | GND | Return Current Path |
| 4 | GND | Return Current Path | 30 | N/A | N/A |
| 5 | N/A | N/A | 31 | Rx- | SATA Differential |
| 6 | N/A | N/A | 32 | N/A | N/A |
| 7 | N/A | N/A | 33 | Rx+ | SATA Differential |
| 8 | N/A | N/A | 34 | GND | Return Current Path |
| 9 | GND | Return Current Path | 35 | GND | Return Current Path |
| 10 | N/A | N/A | 36 | Reserved | No Connect |
| 11 | N/A | N/A | 37 | GND | Return Current Path |
| 12 | N/A | N/A | 38 | Reserved | No Connect |
| 13 | N/A | N/A | 39 | +3.3V | 3.3V source |
| 14 | N/A | N/A | 40 | GND | Return Current Path |
| 15 | GND | Return Current Path | 41 | +3.3V | 3.3V source |
| 16 | N/A | N/A | 42 | N/A | N/A |
| 17 | N/A | N/A | 43 | GND | Return Current Path |
| 18 | GND | Return Current Path | 44 | N/A | N/A |
| 19 | N/A | N/A | 45 | Reserved | N/A |
| 20 | N/A | N/A | 46 | N/A | N/A |
| 21 | GND | Return Current Path | 47 | Reserved | N/A |
| 22 | N/A | N/A | 48 | N/A | N/A |
| 23 | Tx+ | SATA Differential | 49 | DA/DSS | Device Activity / Disable Staggered Spin Up |
| 24 | +3.3V | 3.3V source | 50 | GND | Return Current Path |
| 25 | Tx- | SATA Differential | 51 | Presence Detection | Shall be pulled to GND by device |
| 26 | GND | Return Current Path | 52 | +3.3V | 3.3V source |


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# 2. Software Interface

## 2.1 Command Set

Table 2-1 summarizes the ATA commands supported by the SDM II M1.

**Table 2-1:** Command set (1 of 2)

| Command | Code | FR[1] | SC[2] | SN[3] | CY[4] | DH[5] | LBA[6] |
|---|---|---|---|---|---|---|---|
| Check-Power-Mode | E5H | - | - | - | - | D[8] | - |
| Execute-Drive-Diagnostic | 90H | - | - | - | - | D | - |
| Flush-Cache | E7H | - | - | - | - | D | - |
| Identify-Drive | ECH | - | - | - | - | D | - |
| Idle | E3H | - | Y | - | - | D | - |
| Idle-Immediate | E1H | - | - | - | - | D | - |
| Initialize-Drive-Parameters | 91H | - | Y | - | - | Y | - |
| Read-DMA | C8H or C9H | - | Y | Y | Y | Y | Y |
| Read-Multiple | C4H | - | Y | Y | Y | Y | Y |
| Read-Sector(s) | 20H or 21H | - | Y | Y | Y | Y | Y |
| Read-Verify-Sector(s) | 40H or 41H | - | Y | Y | Y | Y | Y |
| Recalibrate | 10H | - | - | - | - | D | - |
| Security-Disable-Password | F6H | - | - | - | - | D | - |
| Security-Erase-Prepare | F3H | - | - | - | - | D | - |
| Security-Erase-Unit | F4H | - | - | - | - | D | - |
| Security-Freeze-Lock | F5H | - | - | - | - | D | - |
| Security-Set-Password | F1H | - | - | - | - | D | - |
| Security-Unlock | F2H | - | - | - | - | D | - |
| Seek | 7XH | - | - |  | Y | Y |  |
| Set-Features | EFH | Y[7] | - | - | - | D | - |


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**Table 2-1:** Command set (2 of 2)

| Command | Code | FR[1] | SC[2] | SN[3] | CY[4] | DH[5] | LBA[6] |
|---|---|---|---|---|---|---|---|
| Set-Multiple-Mode | C6H | - | Y | - | - | D | - |
| Sleep | E6H | - | - | - | - | D | - |
| SMART | B0H | Y | Y | Y | Y | D | |
| Standby | E2H | - | - | - | - | D | - |
| Standby-Immediate | E0H | - | - | - | - | D | - |
| Write-DMA | CAH | - | Y | Y | Y | Y | Y |
| Write-Multiple | C5H | - | Y | Y | Y | Y | Y |
| Write-Sector(s) | 30H | - | Y | Y | Y | Y | Y |

**1.** FR - Features register
**2.** SC - Sector Count register
**3.** SN - Sector Number register
**4.** CY - Cylinder registers
**5.** DH - Drive/Head register
**6.** LBA - Logical Block Address mode supported (see command descriptions for use)
**7.** Y - The register contains a valid parameter for this command.
**8.** For the Drive/Head register:
Y means both the SDM and Head parameters are used
D means only the SDM parameter is valid and not the Head parameter


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# 3. Flash Management

## 3.1 Error Correction/Detection

The SDM II M1 implements a hardware ECC scheme, based on the BCH algorithm, to achieve up to 8/15 bit correction per 512 bytes.

## 3.2 Bad Block Management

Although bad blocks on the flash media are already identified by the flash manufacturer, they can also be accumulated over time during operation. The SDM II M1's controller maintains a table that lists those normal blocks with disk data, the free blocks for wear leveling, and bad blocks with errors. When a normal block is detected broken, it is replaced with a free block and listed as a bad block. When a free block is detected broken, it is then removed from the free block list and marked as a bad block.

During device operation, this ensures that newly accumulated bad blocks are transparent to the host. The device will stop file write service once there are only two free blocks left such that the read function is still available for copying the files from the disk into another.

## 3.3 Wear Leveling

The NAND flash devices are limited by a certain number of write cycles. When using a FAT-based file system, frequent FAT table updates are required. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole SSD, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. This scheme is called wear leveling.

Apacer's wear-leveling scheme is achieved both via buffer management and Apacer-specific global wear leveling. They both ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

## 3.4 Power Failure Management

The Low Power Detection on the controller initiates cached data saving before the power supply to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected blackout. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

## 3.5 Quick Erase

Accomplished by the Secure Erase (SE) command, which added to the open ANSI standards that control disk drives, "Quick Erase" is built into the disk drive itself and thus far less susceptible to malicious software attacks than external software utilities. It is a positive easy-to-use data destroy command, amounting to electronic data shredding. Executing the command causes a drive to internally completely erase all possible user data. This command is carried out within disk drives, so no additional software is required. Once executed, neither data nor the erase counter on the device would be recoverable, which blurs the accuracy of


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device lifespan. The process to erase will not be stopped until finished while encountering power failure, and will be continued when power is back on.

## 3.6 S.M.A.R.T.

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

Apacer SMART feature follows the SATA Rev. 2.6, ATA/ATAPI-7 specifications, using the standard SMART command B0h to read data from the drive. And based on the SFF-8035i Rev. 2.0 specifications, Apacer SMART defines 3 vendor-specified SMART Attribute IDs (E5h, E8h-EFh, and F3h) in the SDM II M1. They represent Flash ID, good block count, free-list block count, maximum erase count, average erase count, and firmware version information. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the SDM II M1 is in critical condition.


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# 4. Environmental Specifications

## 4.1 Environments

The SDM II M1 environmental specifications follow the US Military Standard MIL-STD-810F, as shown in Table 4-1.

**Table 4-1** SDM M1 environmental specifications

| Environment | Specification |
|---|---|
| Temperature | 0℃ to 70℃ (Operating) |
| | -40℃ to 100℃ (Non-operating) |
| Humidity | 5% to 95% RH (Non-condensing) |
| Vibration | Sine wave: 5~55~5 Hz (X, Y, Z)<br>Random: 10-2000 Hz, 16.3 G (X, Y, Z) |
| Shock - Operating | Acceleration: 1,500 G, 0.5 ms<br>Peak acceleration: 50 G, 11 ms |
| Altitude | 80,000 ft |

## 4.2 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in the SAFD drive. Although many component MTBFs are given in databases and often these values are not really accurate, the prediction result for the SDM II M1 is more than 2,000,000 hours.

## 4.3 Certification and Compliance

The SDM II M1 complies with the following standards:

- CE – EN55022/55024
- FCC 47CFR Part15 Class B
- RoHS
- MIL-STD-810F
- SATA II (SATA Rev. 2.6)
- Up to ATA/ATAPI-7 ( including S.M.A.R.T.)


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# 5. Electrical Characteristics

## 5.1 Operating Voltage

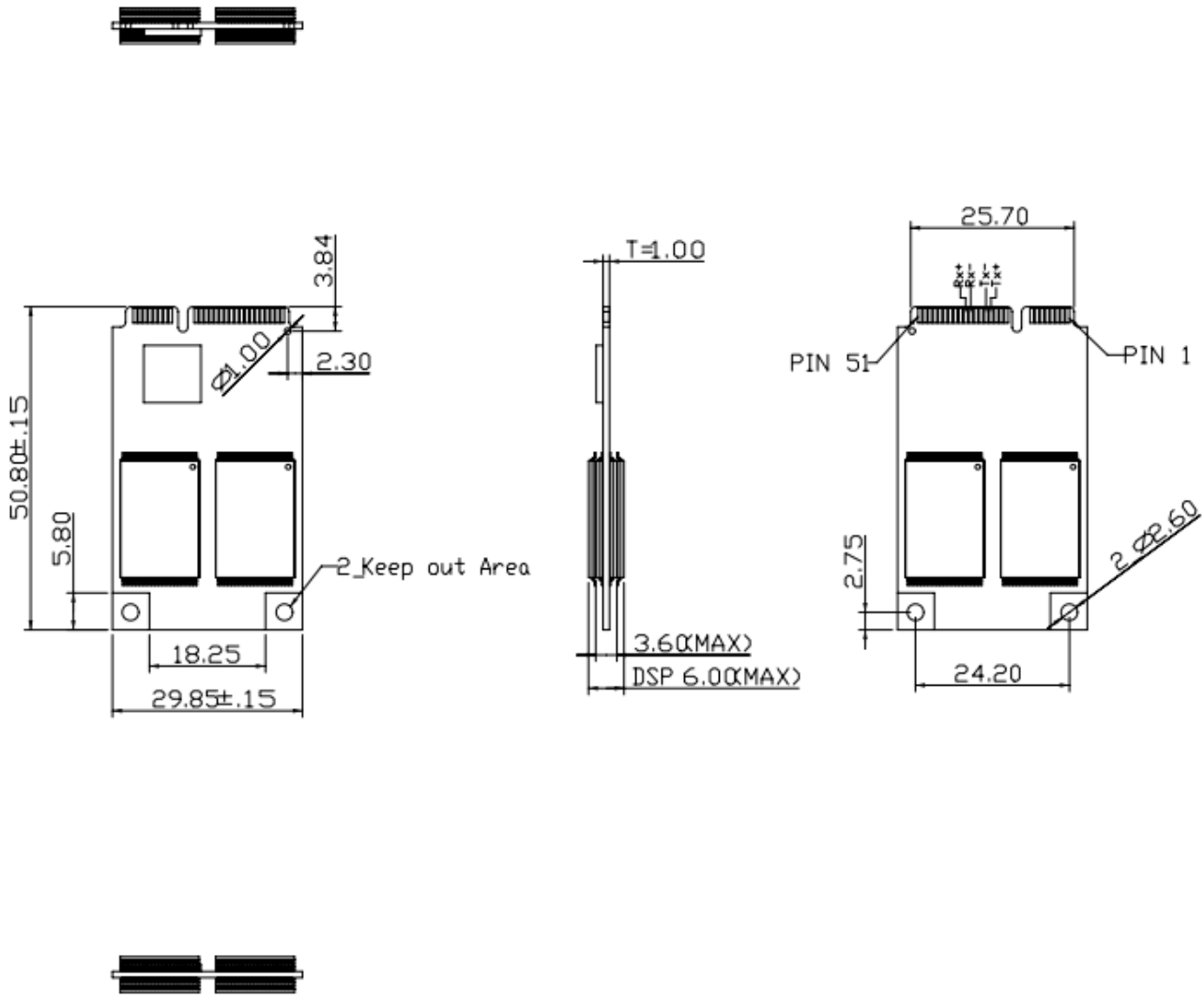
Table 5-1 lists the supply voltage for SDM II M1.

**Table 5-1** SDM II M1 operating voltage

| Parameter | Conditions |
|---|---|
| Supply voltage | 3.3V ±5% ( 3.135V~3.465 V) |


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# 6. Physical Characteristics

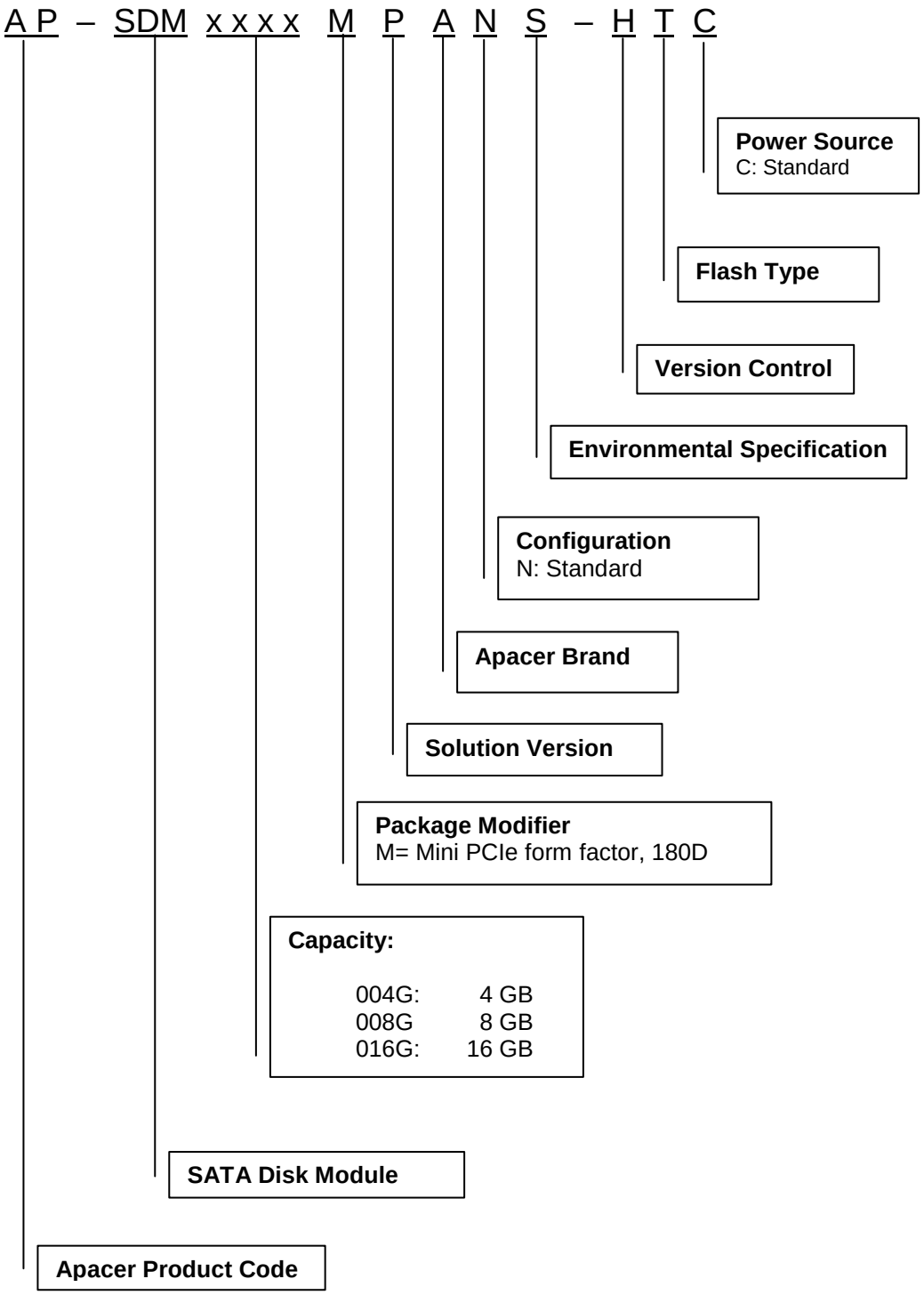



Unit: mm
Tolerance: ± 0.2


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# 7. Product Ordering Information

## 7.1 Product Code Designations





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## 7.2 Valid Combinations

| Capacity | Standard |
|---|---|
| 4 GB | AP-SDM004GMPANS-HTC |
| 8 GB | AP-SDM008GMPANS-HTC |
| 16 GB | AP-SDM016GMPANS-HTC |


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# Revision History

| Revision | Description | Date |
|---|---|---|
| 0.1 | Preliminary release | 11/13/2009 |
| 1.0 | Official release | 01/06/2010 |
| 1.1 | Updated Product Ordering Information | 01/28/2010 |
| 1.2 | Updated drawings | 03/09/2010 |
| 1.3 | Updated Product Ordering Information | 01/18/2011 |


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