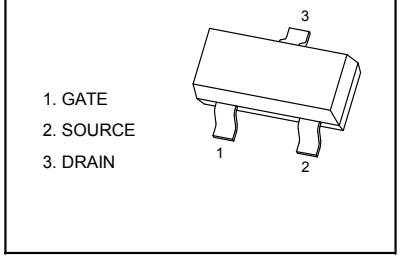
AO3415

SOT-23 Plastic-Encapsulate MOSFETS

20V P-Channel MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$Typ	I_D Max
-20V	37mΩ@ -4.5V	-4.8A
	43mΩ@ -3.3V	

SOT-23



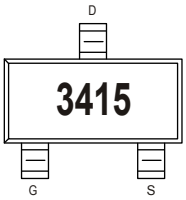
FEATURE

- Excellent $R_{DS(ON)}$, low gate charge,low gate voltages

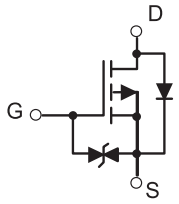
APPLICATION

- Load switch and in PWM applicatopns

MARKING



Equivalent circuit



PACKAGE SPECIFICATIONS

Package	Reel Size	Reel DIA. (mm)	Q'TY/Reel (pcs)	Box Size (mm)	QTY/Box (pcs)	Carton Size (mm)	Q'TY/Carton (pcs)
SOT-23	7'	178	3000	203×203×195	45000	438×438×220	180000

Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{(BR)DSS}$	-20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current	T_A= 25°C	I_D	-4.8	A
	T_A= 70°C		-3.6	
Pulsed Drain Current [1]		I_{DM}	-30	A
Maximum Power Dissipation [2]	T_A= 25°C	P_D	1.5	W
	T_A= 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-50 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		R_{thJA}	80	°C/W

Notes
1) Pulse width limited by maximum junction temperature.
2) Surface Mounted on FR4 Board, t ≤ 5 sec.

The above data are for reference only.

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25℃ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Static Parameters						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-20			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.4	-0.7	-1.2	
Zero gate voltage drain current	I_{DSS}	V_{DS} =20V, V_{GS} =0V (TA=25℃)			-1	μA
		V_{DS} =16V, V_{GS} =0V (TA=125℃)			-100	
Gate-body leakage current	I_{GSS}	V_{DS} =0V, V_{GS} =±8V			±10	
Drain-source on-state resistance(note1)	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-4A		37	45	mΩ
		V_{GS} =-3.3V, I_D =-3A		43	55	
		V_{GS} =-2.5V, I_D =-2A		52	65	
Forward transconductance(note2)	g_{FS}	V_{DS} =-5V, I_D =-4A	8			S
Dynamic Parameters (note3)						
Input capacitance	C_{iss}	V_{DS} =-10V,V_{GS} =0V,f =1MHz		675		pF
Output capacitance	C_{oss}			120		
Reverse transfer capacitance	C_{rss}			85		
Gate resistance	R_g	V_{DS} =0V,V_{GS} =0V,f =1MHz		6.5		Ω
Switching Parameters						
Total gate charge	Q_g	V_{DS} =-10V,V_{GS} =-4.5V,I_D =-4A		14.2		nC
Gate-Source charge	Q_{gs}			3.2		
Gate-drain charge	Q_{gd}			5.8		
Turn-on delay time (note3)	$t_{d(on)}$	V_{DS}=-10V, V_{GS}=-4.5V R_{GEN} =3Ω, R_L=2.5Ω,		15		ns
Turn-on rise time(note3)	t_r			11		
Turn-off delay time(note3)	$t_{d(off)}$			22		
Turn-off fall time(note3)	t_f			35		
Drain-source body diode characteristics						
Continuous source-drain diode current	I_S	T_C=25℃			-2.0	A
Body diode voltage (note 2)	V_{SD}	I_S=-2A,VGS =0V		-0.83	-1.2	V

Notes:

1) PRepetitive rating,pulse width limited by junction temperature.
2) Pulse test: pulse width ≤ 300us, duty cycle≤ 2%.
3) These parameters have no way to verify.

Typical Characteristics

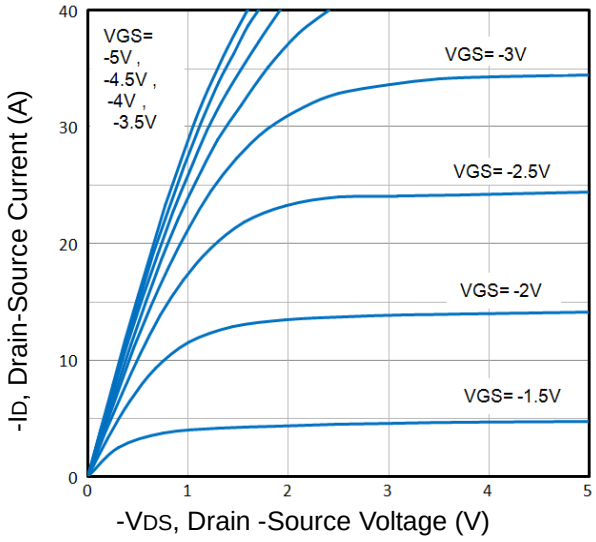


Fig1. Typical Output Characteristics

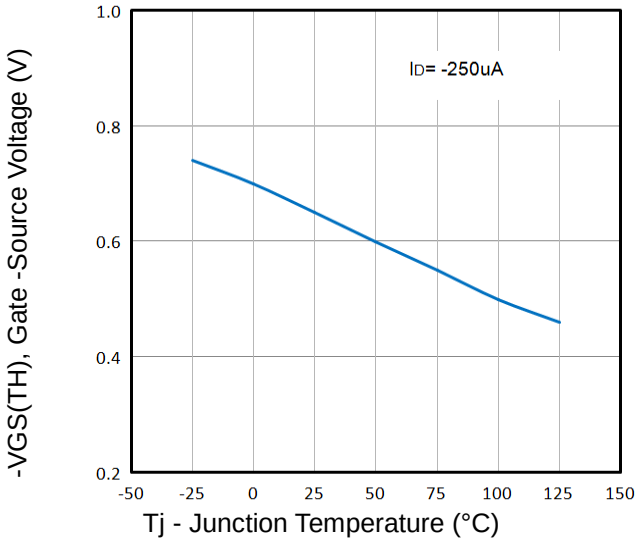


Fig2. Normalized Threshold Voltage Vs. Temperature

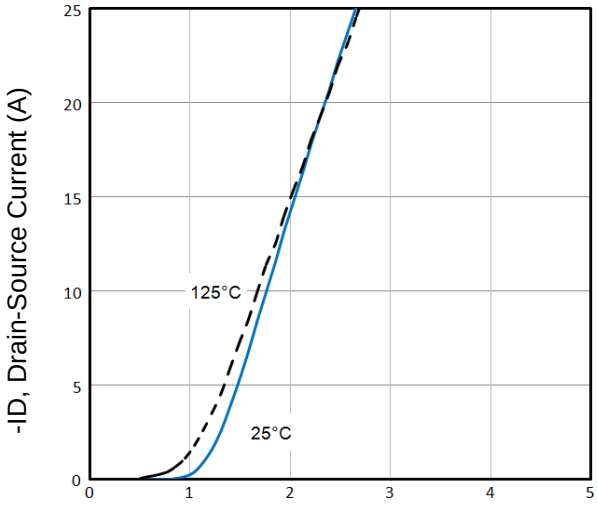


Fig3. Typical Transfer Characteristics

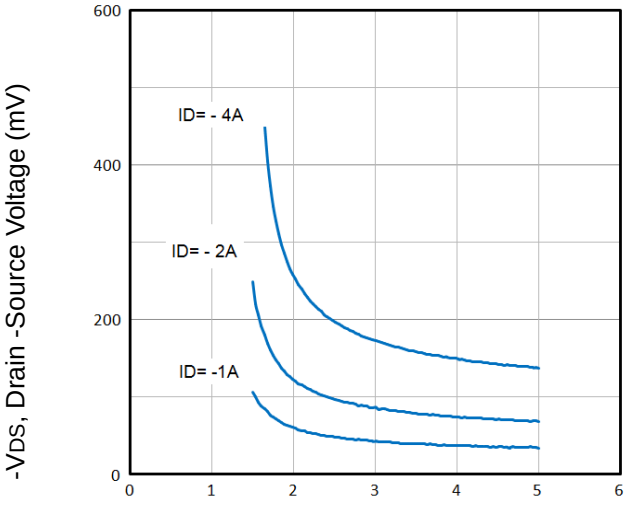


Fig4. Drain -Source Voltage vs Gate -Source Voltage

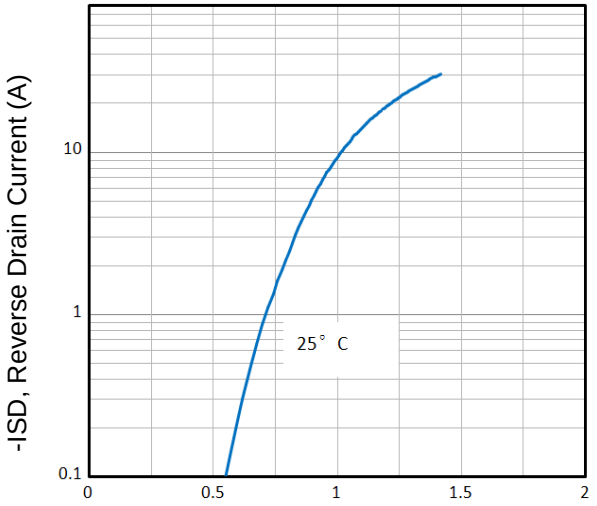


Fig5. Typical Source-Drain Diode Forward Voltage

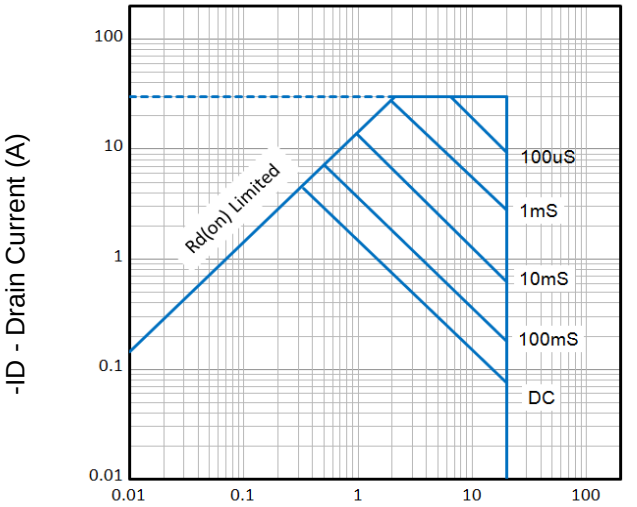


Fig6. Maximum Safe Operating Area

Typical Characteristics

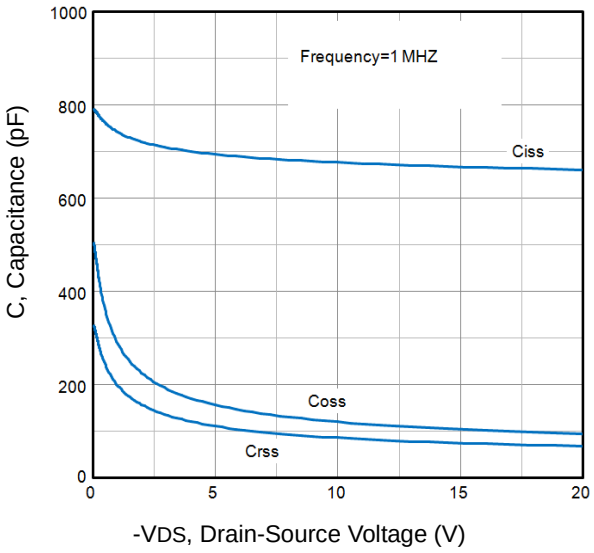


Fig7. Typical Capacitance Vs. Drain-Source Voltage

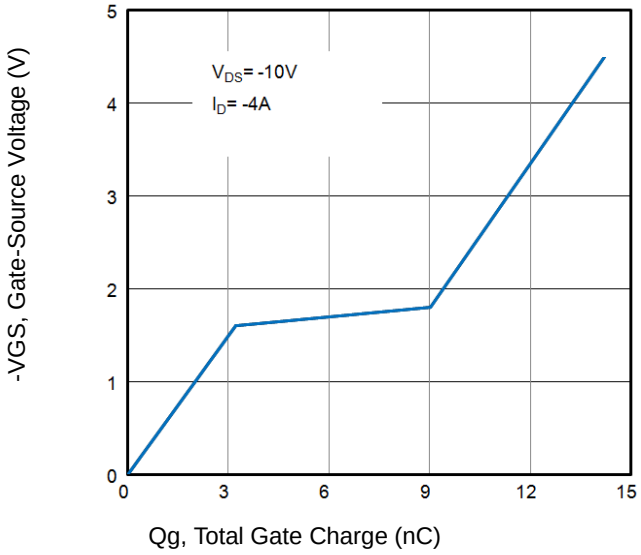


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

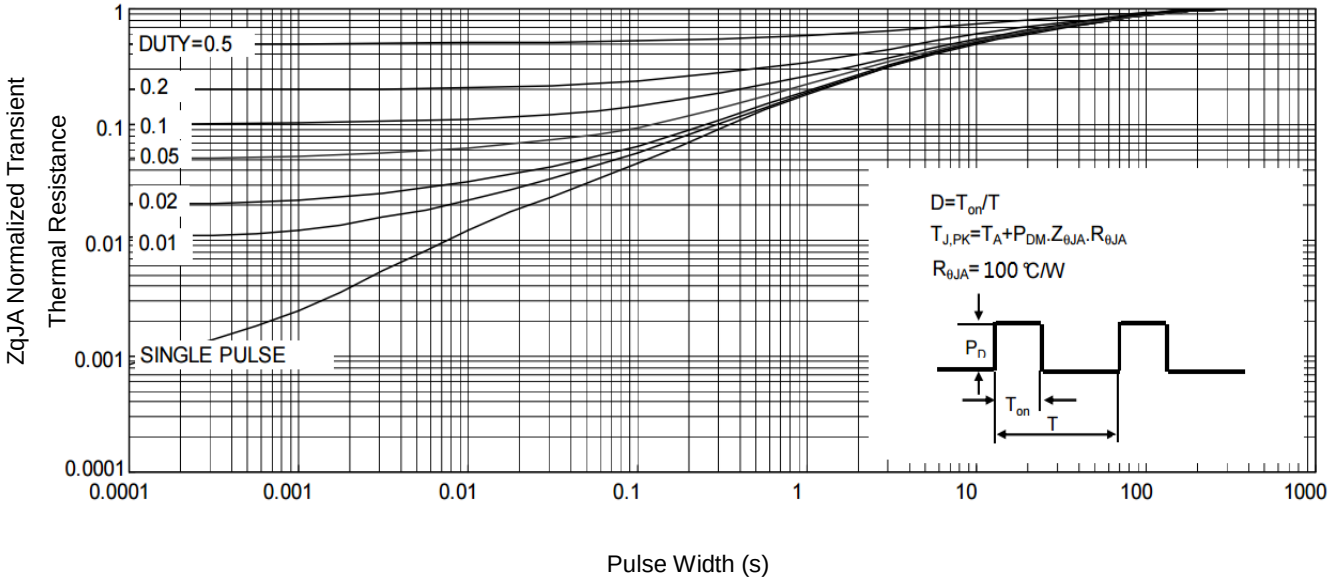


Fig9. Normalized Maximum Transient Thermal Impedance

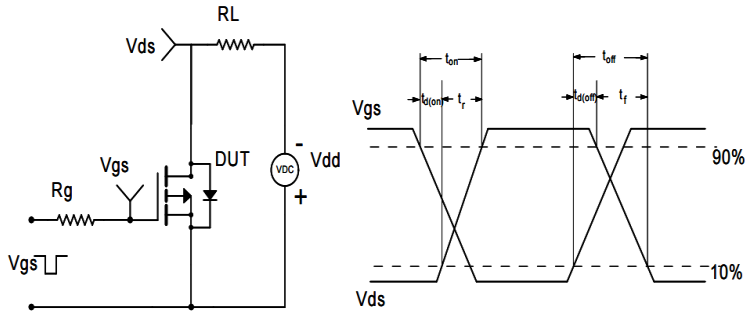
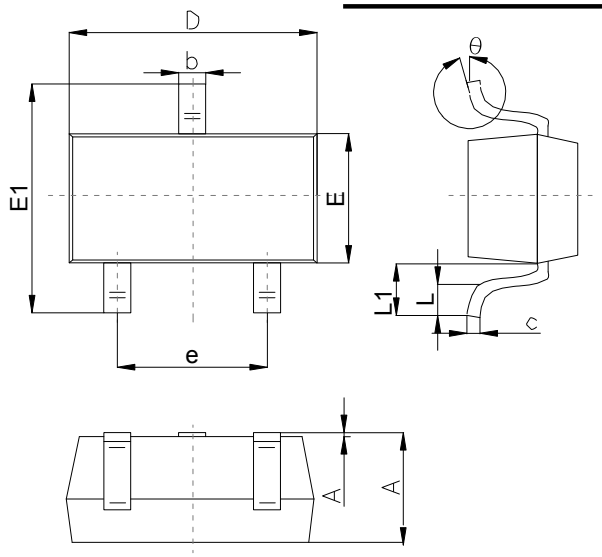


Fig10. Switching Time Test Circuit and waveforms

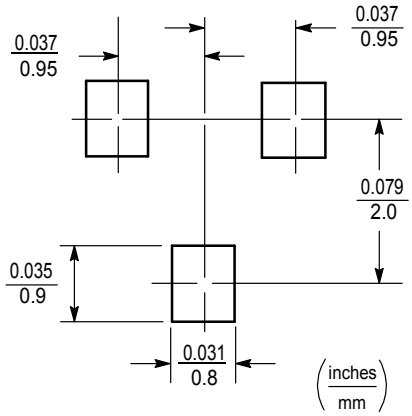
Outlitne Drawing

SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.90		1.40
A1	0.00		0.10
b	0.30		0.50
c	0.08		0.20
D	2.80	2.90	3.10
E	1.20		1.60
E1	2.25		2.80
e	1.80	1.90	2.00
L	0.10		0.50
L1	0.4		0.55
θ	0°		10°

Suggested Pad Layout



Note:
1. Controlling dimension:in/millimeters. 2.General tolerance: ±0.05mm.
3.The pad layout is for reference purposes only.