AND8039/D

The One-Transistor Forward Converter

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APPLICATION NOTE

INTRODUCTION

The one–transistor forward converter is the most elementary form of transformer–isolated buck converter. It is typically used in off–line applications in the 100–300 watt region. This application note illustrates the approach one would take to design a high DC input voltage, one–transistor forward converter. With additional modifications, it could be made work as a 110 VAC off–line power supply.

Description of Operation

A simplified schematic of a one–transistor forward converter can be seen in Figure 1.

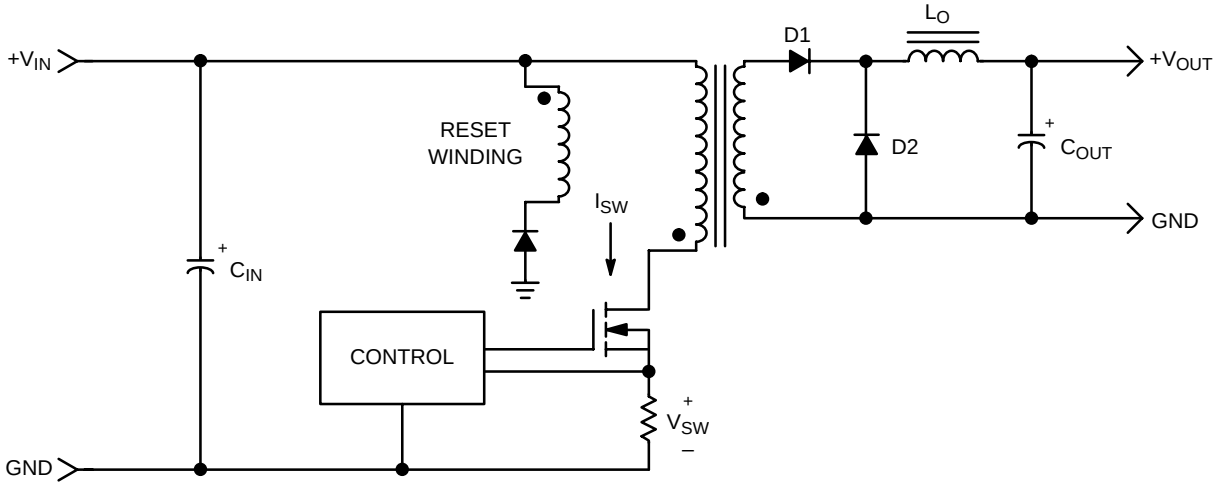


Figure 1. Simplified Schematic of a One Transistor Forward Converter

One can see a transformer has been placed between the input voltage and a buck converter output stage. The power switch (SW) is used to create a rectangular voltage waveform whose amplitude is the input voltage and its duty cycle is the controllable variable. The transformer provides both a step–up or down function and a safety dielectric isolation between the input line and the output load.

The major restriction of this topology is the maximum duty cycle must be about 50 percent. Whenever a core is driven in a unidirectional fashion, that is, current only being driven from one direction into the primary, the core must be *reset*. *Magnetization energy* which serves only to reorient the magnetic domains within the core must be emptied, or else the core will “walk–up” to *saturation* after a few cycles. To do this, one needs to *reset* the core. Resetting is done by drawing current from a winding during the period when the transformer is unloaded, that is, when the power switch and rectifiers are not conducting. Any winding can provide the reset function, but the higher the voltage on the winding, the quicker the core will reset. Typically, this is the primary winding or a separate reset winding of equal turns to the primary. Current from the reset winding can then be returned to the input capacitor and reused during the next cycle of operation.

The typical switch voltage and current can be seen in Figure 2. When the power switch is ON, the switch sees the output filter inductor’s current reflected by through the transformer. The amplitude of the primary current is the output rectifier current times turns ratio of the transformer (N1/N2) plus a small amount of magnetization current. During the power switch OFF time, the switch voltage “flys” up to about twice the input voltage. During this time, the reset winding begins to output magnetization current back to the input capacitor.

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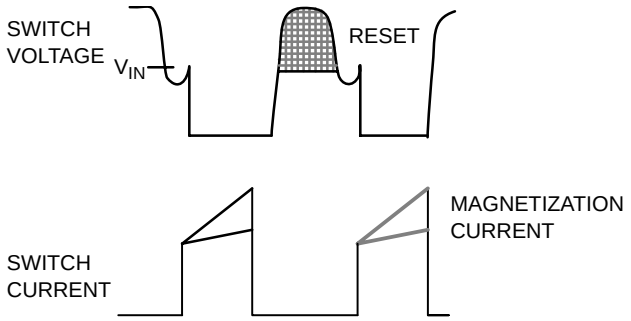


Figure 2. Power Switch Waveforms

The output rectification and filter section works identically to the buck converter. The voltage waveform of secondary looks like an inverted primary winding waveform except the zero voltage point is the input voltage point on the primary waveform. The waveform goes positive when the power switch is conducting. The output rectifier also conducts during this time. This presents a unipolar, PWM rectangular voltage signal to the inductor, just as found in a typical buck converter. The catch diode then operates when the power switch and the output rectifier are OFF. Continuous current is then maintained through the output filter inductor.

Design of the One–Transistor Forward Converter

Please refer to the schematic in Figure 5 when Component designations are mentioned.

Design Specifications:
Input Voltage Range: +140–+200 VDC
Output Voltage: +28 VDC
Output Current: 0.5 A–4.0 A
Max. Output Ripple Voltage: 30 mV

Predesign Estimates:
Output Power:
$P_{out(max)} = (V_{out})(I_{out(max)}) = 112$ Watts
Peak Input Current:
$I_{pk} \approx 2.8\ P_{out}/V_{in(min)} = 2.24$ Amps
Average Input Currents:
$I_{av(low)} = P_{out}/\text{eff}(V_{in(max)}) = 0.66$ Amps
$I_{av(hi)} = P_{out}/\text{eff}(V_{in(min)}) = 0.94$ Amps

Design of the Transformer

One begins with the transformer for every switching power supply design. All of the needed parameters are now known and it serves as the backbone for the remainder of the design.

One must first select a core family that will house the transformer. This is done first by reviewing various core styles and their attributes. The most common off–line core is the E–E core, for which there are several variations. The standard E–E core is based upon the old 50–60 Hz lamination core styles, which are very adequate for most applications. There are some low–profile styles such as the Philips EFD family which yields a very trim, low profile appearance, but can cost slightly more for the basic core–bobbin sets. Selecting an approximate core size is done by appreciating that first the core must have a sufficient core crossectional area to contain the needed flux density to transport the power from the primary to the secondary winding(s). Secondly, there must be enough winding area to contain the required turns of the needed wire gauges. Thirdly, for off–line transformers, the core family must have the ability to meet the minimum creepage and clearance dimensions of the safety agencies after the transformer is finished. To begin, one would use an equation like equation 1 which is an artificial quantity derived from the product of the core crossectional area ($A_{c)}$ times the winding area(W_a).

$$W_aA_c \approx 0.7\ (P_{out}\ W_{d(pri)} \times 10^8)/fB_{max}\ (USA) \quad \text{(eq. 1A)}$$

where: $W_{d(pri)}$ is the average wire diameter needed to carry the primary current in cm.
B_{max} is the maximum operating flux density in Gauss (Webers/cm^2)

In the MKS system (Europe and the rest of the world)

$$W_aA_c \approx 0.7\ (P_{out}\ W_{d(pri)})/fB_{max} \quad \text{(eq. 1B)}$$

where: $W_{d(pri)}$ is the average wire diameter needed to carry the primary current in meters (m).
B_{max} is the maximum operating flux density in Teslas (Webers/m^2)

The result is in cm^4 (eq. 1A) or m^4 (eq. 1B). The core manufacturers usually provide the W_aA_c for each core size. The core size can then be chosen and should be as large or larger than this result. For off–line applications, of which this is not, one should increase the result by about 20 percent to accommodate the added insulating tape needed for an IEC–qualified transformer. Also, a core and bobbin set must be used that has sufficient creepage (distance over a surface) and clearance (distance through air) dimensions. For 110–220 VAC applications, this is 3.2 mm between phases, and 8.0 mm between the input and output circuits. This may be difficult determining the off–line–suitability of a core and bobbin from its data sheet.

In one–transistor forward converters, the operating flux density (B_{max}) dictates how much magnetization energy, which is not used, must be released by the core prior to the next power switch conduction cycle. This is a point of tradeoff, if B_{max} is set too low, then there will be many turns on the transformer, thus making the transformer larger than it needs to be. Setting B_{max} too high, makes the transformer smaller, but increases the losses related to the core reset function. A good point of compromise is to set B_{max} at about 25 percent of B_{sat} at 100 kHz. This level should be reduced by a factor of 0.04 per 100 kHz above this frequency. One can then calculate the turns by:

$$N_{pri} \approx (V_{in(nom)} \times 10^8)/4fB_{max}\ A_c\ (US) \quad \text{(eq. 2A)}$$

where: B_{max} is in Gauss (webers/cm^2)
A_c is the core crossectional area in cm^2

In the MKS system (Europe and elsewhere)

$$N_{pri} \approx (V_{in(nom)})/4fB_{max}\ A_c \quad \text{(eq. 2B)}$$

where: B_{max} is in Teslas (webers/m^2)
A_c is the core crossectional area in m^2

This should be viewed as a nominal–minimum turns–count since adding more turns lowers the operating flux density, which may be counter–intuitive the average electric–based engineer.

The reset winding is identical in turns to the primary winding and usually about 3–4 wire gauges smaller than that of the primary winding. It is phased oppositely from the primary so that it can discharge the magnetization energy when the power switch is off.

The secondary turns needed for this application is found by realizing that the secondary voltage must provide an output waveform that will have a volt–time average that will create the proper output voltage when presented to the L–C filter. In other words, ($DC_{max}V_{out(min)}$) plus the forward voltage drop of the output rectifier must be greater than the DC output voltage. This can be done by:

$$N_{sec} \approx 1.1\ N_{pri}\ (V_{out} + V_{fwd})/V_{in(min)}\ DC_{max} \quad \text{(eq. 3)}$$

where: DC_{max} is the maximum duty cycle of the system (<0.5)
V_{fwd} is the nominal forward voltage drop of the rectifier.

The 1.1 factor provides a 10 percent margin in the supply's low voltage dropout point and also provides margin for other variations in the circuit. This secondary should be the main output which would then serve as the reference winding for all of the other secondary windings. One should round the result up to the next integer turn.

When determining any additional secondary winding, one must account for each of the forward voltage drops of their respective rectifiers. This can be done by:

$$N_{sec(n)} \approx N_{sec(1)}\ (V_{out(n)} + V_{fwd(n)})/(V_{sec(1)} + V_{fwd(1)}) \quad \text{(eq. 4)}$$

The accuracy of each of the output voltages must now be considered. Some variation can be gotten by changing the output rectifier technology, otherwise the turns can be adjusted by raising the reference secondary winding by a turn and adjusting the other windings. This is an iterative process done until the output voltages are within an acceptable tolerance and all of the windings are integer turns.

This design example only has one output voltage. The auxiliary winding which provides power to the control IC, need not be regulated or accurate. It needs to only exceed the low voltage inhibit limit of the UC3845 which is 8.0 V at the low input voltage. Peak rectifying the auxiliary winding in the forward conduction mode, yields a winding with 3.5 turns. Lets round up to 4 and add a series resistor (about 100 ohms) and a 18 V zener diode across the auxiliary voltage filter capacitor to limit the maximum voltage. This will protect the gate of the power MOSFET.

In this example, an EFD25 core will be used. The primary turns were calculated to be 41 turns of a #24 AWG. The reset winding will be 41T of #28 AWG. The secondary is 21 turns of 2 stands of #22 AWG. The auxiliary winding will be 4 turns of #28 AWG. The primary and reset windings will be wound first onto the bobbin. Next the auxiliary winding is wound on top of these windings. Three layers of mylar tape are applied to provide some degree of dielectric isolation (not quite IEC), then the secondary winding will be applied last. A last layer of tape is added to provide some protection to the outer winding.

A cautious note must be now conveyed, this design example is a non–isolated, high–voltage input power supply. It is for example only and cannot be built for sale because it does not meet the IEC (UL CSA or other) specifications for dielectric isolation and for creepage (the distance along a surface). To make this an off–line one transistor forward converter, the input rectifier bridge, EMI filter, an opto–isolated feedback circuit, an opto–isolated feedback circuit and the transformer would have to be built to IEC specifications.

Selection of the Power Semiconductors

Power Switch

In one–transistor forward converters, the power switch will see twice the maximum input voltage plus any spikes caused winding leakage inductance, and rectifier forward and reverse characteristics. So the minimum V_{DSS} rating for the power MOSFET is about:

$$V_{DSS(min)} = 2\ (V_{in(max)}) + V_{clamp(est)} = 450\ V$$

The minimum drain current rating should be greater than just slightly less than slightly less than the maximum peak current. This is 2.24 A.

Another major consideration, especially for surface mount components, is the heat generated by the device. The $R_{DS(ON)}$ and the drive circuit have the greatest influence on this. By over–rating the drain current, some reduction in heat can be realized. This lessens the amount of PCB area needed to keep the junction temperature of the MOSFET at a reasonable temperature (about +40–+60°C). A reasonable estimation of the maximum $R_{DS(on)}$ assuming a heatsink area of twice the minimum footprint area is:

$$R_{DS(on)(max)} = 3.3\ (\Delta T)/(I_{in(av)})^2(Theta\ (jA)) \quad \text{(eq. 6)}$$

This results in a maximum $R_{DS(ON)}$ of 3.5 ohms. So a summary of the MOSFET ratings are:
$V_{DSS} > 450$ V
$I_D > 2.24$ A
$R_{DS(on)} < 3.5$ ohms

To further reduce the heat, an MTB8N50E was chosen.

Output Rectifier

The output rectifier will also be a surface mount D2PAK. This efficiently couples the heat to the copper pad on the PCB.

The maximum reverse voltage is:

$$V_{r(min)} = V_{in(max)}(N_{sec}/N_{pri}) > 102 \text{ V}$$

The Peak output current is:

$$I_{out(pk)} = 2.8\, I_{out(max)} \text{ or } 11.2 \text{ A}$$

The selected rectifier is the MURB1620CT.

Design of the Output Filter Section

As in all forward–mode converters, the output is converted back to DC by the use of an L–C filter. A two–stage filter is going to be used which is a much more efficient output filter than a single stage filter. The abbreviated schematic is shown in Figure 3.

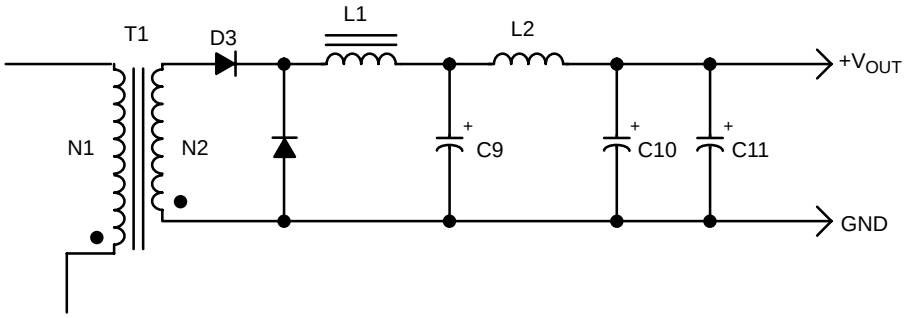


Figure 3. Schematic of the Two–Stage Output Filter

Below the voltage feedback crossover frequency ($f_{xo} \approx$ about 8.0 kHz) all of the output capacitors appear to be essentially in parallel (i.e., C9, C10 and C11). The first stage inductor should be calculated such that it does not enter the discontinuous–mode at light load. The second–stage filter has its corner frequency at about 22 kHz and provides an additional 15–20 dB of ripple attenuation with little additional phase lag and no additional output capacitance.

The first stage inductor should be sized to allow 20 percent of the AC ripple current through to the capacitor. This is a little more than is typically allowed, but the existence of the second filter provides a more pronounced effect, thus allowing the first filter to be smaller.

$$L_o \approx (V_{sec(min)} - V_{out})\, t_{off(min)}/1.4\, I_{out(min)} \qquad \text{(eq. 4)}$$

where: $V_{sec(min)}$ is 1.1 $V_{in(min)}(N_s/N_{pri})$

The resulting minimum inductance is 88 uH. Lets round this up to 100 uH which will give us a more standard value off–the–shelf inductor and extend the minimum current capabilities of the supply. Now one must choose an inductor whose core can be driven with 4+ amps on its winding without the fear of core saturation. Coiltronics P/N CTX100–2–52.

Next the output filter capacitor is calculated. In forward–mode converters, the roles of the output capacitor are transient hold–up voltage and output ripple reduction. The output filter inductor greatly reduces the RMS ripple current to the output capacitor(s) thus relaxing their ratings somewhat. The transient load hold–up function is typically shared with other filter capacitors outside of the power supply. So the common method of calculating the value of the output filter capacitance is by the ripple–reduction function. Assuming a very benign load (resistor) and so that only the ripple is considered, one then calculates:

$$C_o = I_{out(max)}\,(1 - DC_{max})/V_{ripple} \qquad \text{(eq. 5)}$$

where: V_{ripple} is the desired p–p ripple voltage on the output.

This results in a total output capacitance of 533 uF. If one allocates about one–third of this value to the first–stage filter and two–thirds to the output, and rounding–up to the next standard value, one gets C9, C10 and C11 as 220 uF, 50 VDC or Nichicon Part number EVR2E470MPA which has a 430 mA_{rms} ripple current rating.

The second–stage filter inductance is determined by setting its pole above the crossover frequency of the closed feedback loop so that it will not contribute significant additional phase shift, but will further reduce the ripple voltage. If we set the output filter's filter pole at no more than 25 percent of the switching frequency and at least three times the filter pole of the first–stage filter, then the nominal corner frequency of the second–stage filter is around 20–25 kHz. The second–stage filter inductor can then be found by:

$$L_{o(2)} = (2\pi f_p)^2/(C10 + C11) \qquad \text{(eq. 6)}$$

Setting the second–stage filter pole at 22 kHz, the resulting second–stage inductor value is 0.1 uH. This can easily be done as an air–core inductor or a spiral PCB inductor, which is what I will do.

Design of the Primary Current Sensing Network

The UC3845, current–mode control IC is being used. Its current sensing input has a maximum trip voltage of 1.0 volt when the current–mode circuit is just starting–up. To minimize the losses associated with the current sensing resistance, one should use about a trip voltage of between 0.3 and 0.4 V. This results in a current sensing resistor of:

$$Rsc\ (R8) < V_{trip}/I_{pk(max)} = 0.3/2.24\ A = 0.13\ ohms$$

make this value 0.1 ohms for a convenient off–the–shelf value.

A spike filter should be placed between the current sensing resistor (R8) and the IC. The time constant of this R–C filter, if set too long, will enter a pulse–skipping mode at light loads. If its time constant is made too short, then some spikes may still enter the current comparator and produce erratic pulsewidths. A time constant of 300 nS is a good time.

One must first select one of the values. By making the R larger, one can provide some series protection between the power switch and the input pin of the IC. I will assign a value of 1.0 K to R7. The capacitor then becomes:

$$C7 = 300\ nS/1.0\ K\Omega = 300\ pF$$

Design of the Bootstrap Start–Up Circuit

The purpose of this circuit is to initially start the control circuit up from a turned–off state. The control circuit then would draw its power directly from the transformer. The most efficient circuit cuts off its start–up current after the power supply has begun steady–state operation. This reduces an unnecessary loss.

The circuit seen in the schematic (Figure 5) is essentially a current–limited, high–voltage, linear regulator. When the auxiliary power supply from the transformer is less than 10 V, the start–up circuit is operational. When the auxiliary supply exceeds 10 V, it cuts off its collector current, which is about 1.0 mA. A 10 uF or greater capacitor (C2) must be placed on the auxiliary bus to store enough energy to actually start the supply, since the IC will draw about 10 mA in the operate mode.

R1 = (Vin(min)–Vz)/1.0 mA = (140–12)/1.0 mA
= 128 K Make 120 K

R2 = (Vin(min)–Vz)/2.0 mA
= 64 K Make 62 K

The zener diode (Z1) is a 500 mW 12 V, 1N5242

The selection of high voltage bipolar small signal transistors is limited. An MPSW42 works nicely for Q1. The purpose of D1 is to avoid stressing the base–emitter junction in the reverse direction, if the auxiliary voltage goes far above the +12 V base voltage. The typical reverse breakdown voltage ($V_{(BR)EBO}$) is between 3.0–6.0 V. A 1N4148 is going to be used for D1.

Design of the Voltage Feedback and Compensation

Design of the Resistor Divider

The UC3845 has a 2.5 volt reference. One should set the value of the top resistor of the resistor divider (R11) between 2.0 k to 15 k ohms. This then makes the other values in the compensation network reasonable values. This can be done by selecting the sense current, that is the current allowed to flow through the resistor divider. As an estimate one can first calculate:

$$Isense = (28\ V - 2.5\ V)/7.0\ Kohms = 3.65\ mA$$

Using that sense current the lower resistor (R5) then becomes:

$$R5 = 2.5\ V/3.65\ mA = 684\ ohms$$
– closest resistance 680 ohms

The upper resistor is then:

$$R11 = (28.0\ V - 2.5\ V)/3.65\ mA) = 6986\ ohms$$
or 6.98 kohms 1%

Design of the Feedback Loop Compensation

This is a current–mode controlled, forward converter where only a 1–pole, 1–zero method of compensation is required (2 poles if the op amp compensation is considered). This provides maximum of +90 degrees phase boost, which helps in avoiding unstable operation.

Determining the Control–to–Output Characteristic

The gain at DC for this topology is:

$$A_{DC} = \left[(V_{in} - V_{out})^2/V_{in}V_e\right](N_{sec}/N_{pri}) = 13.5$$

$$G_{DC} = 20\ Log\ (A_{DC}) = 22.6\ dB$$

The output filter pole is:

$$f_{fp} = 1/(2\pi R_L C_o)$$
$$= 4.3\ Hz\ (light\ load\ (0.5\ A))$$
$$= 34.5\ Hz\ (rated\ load\ (4.0\ A))$$

where: R_L is the equivalent resistance of the load (V_{out}/I_{out})
C_o is the net value of the output capacitance (C9+C10+C11)

The ESR zero of the net output capacitance is:

$$f_{z(esr)} = 1/(2\pi R_{esr} C_o)$$
$$= 1/(2\pi(50\ m\ ohms)\ (660\ \mu F))$$
$$= 4822\ Hz$$

where: R_{esr} is all of the ESR resistances in parallel.

Calculating the Compensation Elements

Locating the compensating breakpoints:

$$f_{ez} = f_{fp(light\ load)} = 4.3\ Hz$$
$$f_{ep} = f_{p(esr)} = 4.8\ kHz$$

The crossover frequency will be set at about 8.0 kHz. To accomplish this, one assumes that the eventual closed loop bode gain response of the system will be –20 dB/decade continuous slope. Then one can calculate the amount of mid–band gain that the error amplifier must provide to "push–up" or "lower" the gain function so that the crossover frequency is set at 8.0 kHz. This is done by:

$$G_{xo} = 20\ \mathrm{Log}(f_{xo}/f_{fp}) + G_{DC} = +18.2\ \mathrm{dB}$$

converting this value to absolute gain for later use:

$$A_{xo} = 10[G_{xo}/20] = +8.13$$

Now one can begin to calculate the actual error amplifier feedback component values.

$$C5 = 1/2\pi f_{xo}A_{xo}R11 = 360\ \mathrm{pF}$$
$$R4 = A_{xo}R11 = 56\ \mathrm{K\ ohms}$$
$$C6 = 1/2\pi f_{ez}R4 = 0.56\ \mu\mathrm{F}$$

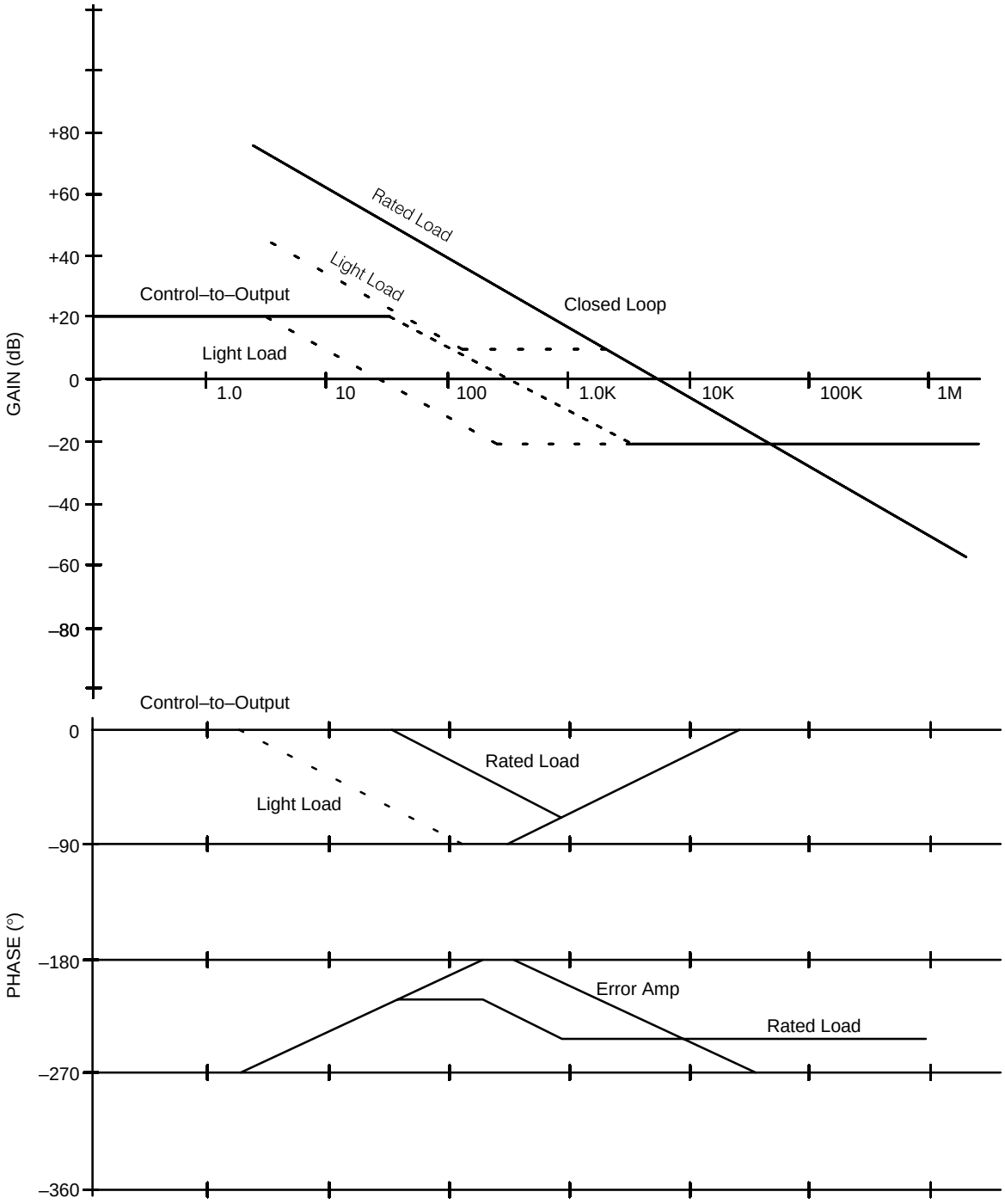


Figure 4. Compensation Bode Plots for the Example

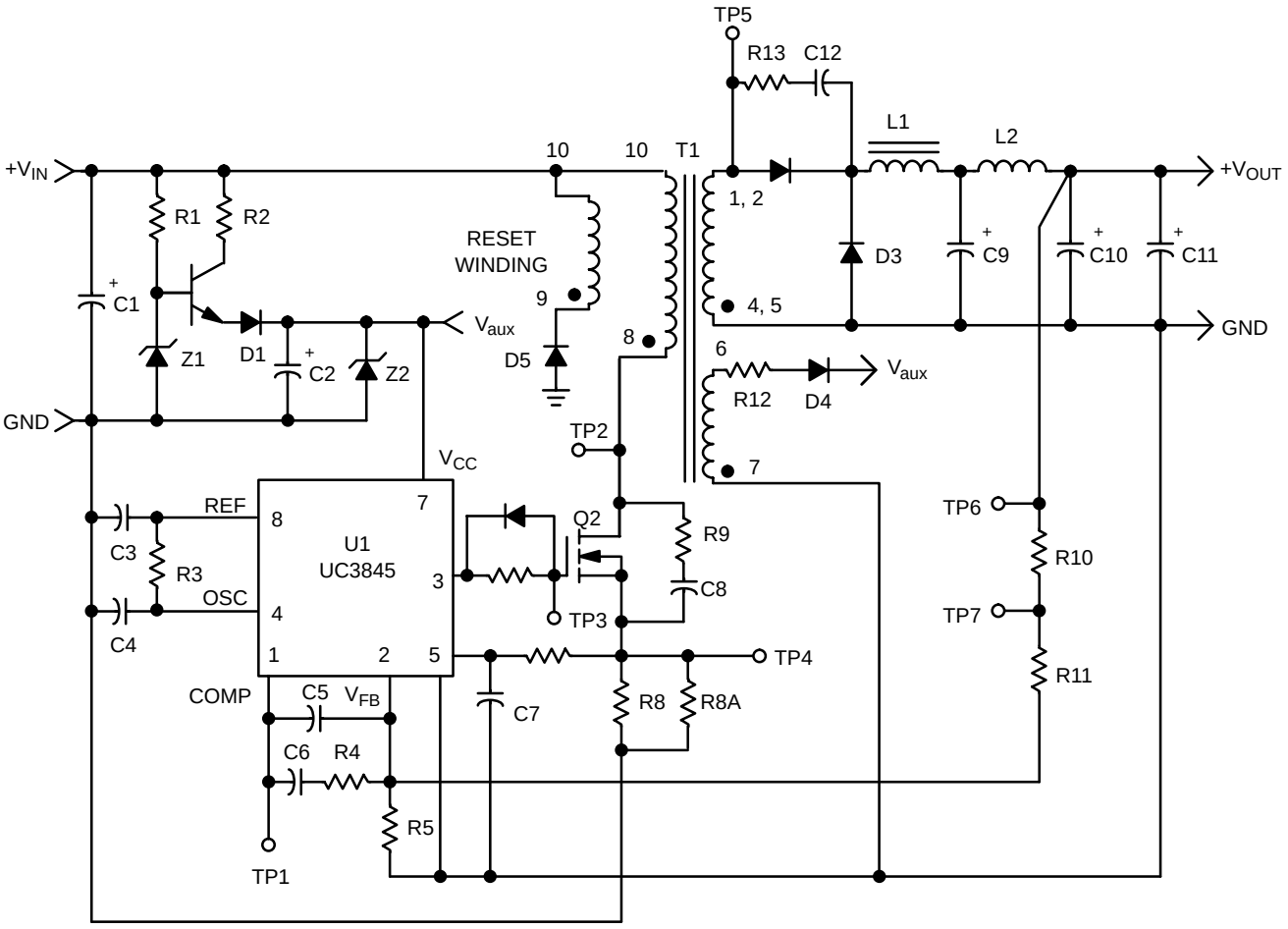


Figure 5. 112 Watt, One–Transisitor Forward Converter

Conclusion

This application note illustrated the design steps needed to complete a one–transistor forward converter. This demonstration unit is only for instruction and to complete a design for the “real world” one should also include: dielectric isolation from the input to output, an input rectification and filter section and some additional methods of protection.

Bill of Material

Designator	Part Number	Manufacturer	Ratings	Description
C1	UVR2E470MPA	Nichicon	250 V	47 μF. Electrolytic
C2*	UMA1E100MDA	Nichicon	25 V	10 μF, Tantalum
C3	MR055C105JAA	AVX	50 V	0.1 μF, Ceramic
C4	MR055C102JAA	AVX	50 V	1000 pF, Ceramic
C5	MR055C361JAA	AVX	50 V	360 pF, Ceramic
C6	MR055C564JAA	AVX	50 V	0.56 μF, Ceramic
C7	MR055C301JAA	AVX	50 V	300 pF, Ceramic
C8*	68Q101MDAAA	AVX	500 V	100 pF Ceramic
C9	UVR1H221MPA	Nichicon	50 V	220 μF, Electrolytic
C10	UVR1H221MPA	Nichicon	50 V	220 μF, Electrolytic
C11*	UVR1H221MPA	Nichicon	50 V	220 μF, Electrolytic
C12	68Q101MDAAA	AVX	500 V	100 pF Ceramic
D1*	1N4148	ON Semiconductor	200 V, 0.1 A	Signal Diode
D2	1N4148	ON Semiconductor	200 V, 0.1 A	Signal Diode
D3*	MURB1620CT	ON Semiconductor	200 V, 16 A	Dual Ultrafast Rectifier
D4	1N4148	ON Semiconductor	200 V, 0.1 A	Signal Diode
J1*	570–500	Deltron		Banana Socket–Black
J2	570–500	Deltron		Banana Socket–Red
J3*	570–500	Deltron		Banana Socket–Black
J4	570–500	Deltron		Banana Socket–Red
L1	CTX100–5–52	CoilTronics	100 uH, 6 A	Inductor
Q1	MPSW42	ON Semiconductor	300 V, 0.1 A	Small Signal Bipolar
Q2	MTB8N50E	ON Semiconductor	500 V, 8 A	HV Power MOSFET
R1*	OK1245R52	Ohmite	120 K	Resistor, 1/4 W
R2*	OK6235R52	Ohmite	62 K	Resistor, 1/4 W
R3	OK1535R52	Ohmite	15 KΩ	Resistor, 1/4 W
R4	OK5635R52	Ohmite	56 KΩ	Resistor, 1/4 W
R5	OK6815R52	Ohmite	680 Ω	Resistor, 1/4 W
R6	OK1015R52	Ohmite	100 Ω	Resistor, 1/4 W
R7	OK1015R52	Ohmite	100 Ω	Resistor, 1/4W
R8*	RWR100	Ohmite	0.1 Ω	Resistor, Wirewound
R9	OK1560R52	Ohmite	56 Ω	Resistor, 1/4 W
R10	OK2005R52	Ohmite	20 Ω	Resistor, 1/4 W
R11*	MK6981F	Ohmite	6.98 KΩ	Resistor, 1/4 W, 1%
R12	OK1015R52	Ohmite	100 Ω	Resistor, 1/4 W
R13	OK1015R52	Ohmite	100 Ω	Resistor, 1/4 W
T1*	N34356	Cramer Magnetics		Transformer–Custom
U1	UC3845BN	ON Semiconductor		Controller IC
Z1	1N5242B	ON Semiconductor	12 V, 500 mW	Zener Diode
Z2	1N5248B	ON Semiconductor	18 V, 500 mW	Zener Diode

* Snubber components – values to be assigned at prototyping

Notes

Notes

Notes

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