AN4142
Application note

STM32W108xx datasheet bit and register naming migration

Introduction

The purpose of this application note is to explain the compatibility guideline between revisions 13 and 14 of datasheet STM32W108xx. To that aim, this document does not provide detailed information on the two datasheet versions, but it highlights for each peripheral the bit and register naming between them.

Regarding the hardware, revisions 13 and 14 of the STM32W108xx datasheet are identical. Revision 14 differs from revision 13 version in terms of documentation level.

However, the details of the migration guideline between the HAL and StdLib are documented in separate documents. Please refer to AN4141 *Migration and compatibility guideline for STM32W108xx microcontroller applications based on the HAL*.

This application note applies to the products listed in *Table 1*.

Table 1. Applicable products

Type	Part numbers
Microcontrollers	STM32W108xx

Table 2. Color coding

Color	Meaning
	Old name
	New name
	Reserved
	New register added
	Register removed

Contents

1 Why migrate from revision 13 to revision 14 of datasheet STM32W108xx? 5

2 Embedded memory 6

2.1 Flash memory 6

2.1.1 STM32W108xx FLASH bit and register overview 6

2.2 Memory controller 8

2.2.1 STM32W108xx MEM bits and registers overview 8

3 System modules 9

3.1 Resets 9

3.1.1 STM32W108xx RST bits and registers overview 9

3.2 Clocks 10

3.2.1 STM32W108xx CLK oscillators overview 10

3.2.2 STM32W108xx CLK bits and registers overview 10

3.3 System timers 12

3.3.1 STM32W108xx watchdog timer overview 12

3.3.2 STM32W108xx Sleep timer Overview 12

3.3.3 STM32W108xx MAC Timer Overview 15

3.4 Power management 15

3.4.1 STM32W108xx Power Overview 15

4 General-purpose input/outputs 18

4.1 Standard General-purpose input/output 18

4.1.1 STM32W108xx GPIO Overview 18

4.2 External interupt 19

4.2.1 STM32W108xx EXTI Overview 19

4.3 Debug management 21

4.3.1 STM32W108xx DBG Overview 21

5 Serial interfaces 22

5.1 STM32W108xx Serial control Overview 22

6 General-purpose timers 28

6.1 STM32W108xx Timers Overview 28

7 Analog-to-digital converter 32

7.1 STM32W108xx ADC Overview 32

8 Interrupts 34

8.1 STM32W108xx NVIC Overview 34

8.2 Management interrupt 36

9 Revision history 37

List of tables

Table 1. Applicable products . . . 1
Table 2. Color coding . . . 1
Table 3. FLASH memory bits and registers overview . . . 6
Table 4. Memory controller bits and registers overview . . . 8
Table 5. RST bits and registers overview . . . 9
Table 6. CLK bits and registers overview . . . 11
Table 7. WDG bits and registers overview . . . 12
Table 8. SLPTMR bits and registers overview . . . 13
Table 9. WDG bits and registers overview . . . 15
Table 10. Power bits and registers overview . . . 16
Table 11. GPIO bits and registers overview . . . 18
Table 12. EXTI bits and registers overview . . . 19
Table 13. WDG bits and registers overview . . . 21
Table 14. SC bits and registers overview . . . 22
Table 15. TIM bits and registers overview . . . 28
Table 16. ADC bits and registers overview . . . 32
Table 17. NVIC bits and registers overview . . . 34
Table 18. MGMT bits and registers overview . . . 36
Table 19. Document revision history . . . 37

1 Why migrate from revision 13 to revision 14 of datasheet STM32W108xx?

The revision 14 of the STM32W108xx datasheet is an updated version of revision 13 of the datasheet that supports the standard naming (clocks oscillators, bits, registers...) used inside the STM32Fxx standard microcontrollers documentations.

This revision 14 of the STM32W108xx is an aligned version with the available firmware STM32W108xx_StdPeriph_Lib_V1.0.0.

In this version, the missing registers that are used in the old HAL and not documented in the revision 13 of the datasheet are added. In addition the structures for the available registers are re-organized to be compatible with the StdLib and the memory mapping is added for each peripheral.

2 Embedded memory

This section describes the embedded memory peripherals (FLASH, MEM) bits and registers migration from revision 13 to revision 14 of the STM32W108xx datasheet.

2.1 Flash memory

The Flash memory interface is the same IP on STM32F microcontrollers families, so almost all of the bits and registers are already aligned with the standard naming except for the FLASH control registers (FPEC_CLK_REQ and FPEC_CLK_STAT registers).

2.1.1 STM32W108xx FLASH bit and register overview

Table 3 gives the list of the changes (renaming) made in the FLASH bits and registers.

Table 3. FLASH memory bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx FLASH bits/registers naming overview																
0x8000	FLASH_ACR	Reserved											PRFTBS	PRFTBE	HLFCYA	LATENCY		
	FLASH_ACR	Reserved											PRFTBS	PRFTBE	HLFCYA	LATENCY		
0x8004	FLASH_KEYR	FKEYR[31:16]	FKEYR[15:0]															
	FLASH_KEYR	FKEYR[31:16]	FKEYR[15:0]															
0x8008	FLASH_OPTKEYR	OPTKEYR[31:16]	OPTKEYR[15:0]															
	FLASH_OPTKEYR	OPTKEYR[31:16]	OPTKEYR[15:0]															
0x800C	FLASH_SR	Reserved											EOP	WRPRTERR	Res.	PGERR	Res.	BSY
	FLASH_SR	Reserved											EOP	WRPRTERR	Res.	PGERR	Res.	BSY

Table 3. FLASH memory bits and registers overview (continued)

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx FLASH bits/registers naming overview																
0x8010	FLASH_CR	Reserved				EOPIE	Res	ERRIE	OPTWRE	Res	LOCK	STRT	OPTER	OPTPG	Res.	MER	PER	PG
0x8010	FLASH_CR	Reserved				EOPIE	Res	ERRIE	OPTWRE	Res	LOCK	STRT	OPTER	OPTPG	Res.	MER	PER	PG
0x8014	FLASH_AR	FAR[31:16]	FAR[15:0]															
0x8014	FLASH_AR	FAR[31:16]	FAR[15:0]															
0x801C	FLASH_OBR	Reserved															RDPRT	OPTERR
0x801C	FLASH_OBR	Reserved															RDPRT	OPTERR
0x8020	FLASH_WRPR	WRP[31:16]	WRP[15:0]															
0x8020	FLASH_WRPR	WRP[31:16]	WRP[15:0]															
0x402C	FPEC_CLK_REQ	Reserved																FPEC_CLK_REQ
0x402C	FLASH_CLKER	Reserved																EN
0x4030	FPEC_CLK_STAT	Reserved															FPEC_BSY	FPEC_CLK_ACK
0x4030	FLASH_CLKSR	Reserved															BSY	ACK

2.2 Memory controller

The memory controller is a set of registers to control the RAM and DMA memories, these registers are required for low power mode, however before entering in low power modes the user needs to save the context for all the memory controller registers and restore these configurations after the wake up from the low power modes. In revision 13 of the datasheet, the memory controller is not documented.

2.2.1 STM32W108xx MEM bits and registers overview

Table 4 gives the memory controller bits and registers naming.

Table 4. Memory controller bits and registers overview

Offset	Register	Bit 31-16	Bit15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx MEM Controller bits/registers naming overview																
0x5000	RAM_PROTR1	[31:0]																
0x5004	RAM_PROTR2	[31:0]																
0x5008	RAM_PROTR3	[31:0]																
0x500C	RAM_PROTR4	[31:0]																
0x5010	RAM_PROTR5	[31:0]																
0x5014	RAM_PROTR6	[31:0]																
0x5018	RAM_PROTR7	[31:0]																
0x501C	RAM_PROTR8	[31:0]																
0x5020	DMA_PROTR1	OFFSET							ADDRESS									
0x5024	DMA_PROTR2	Reserved														CHANNEL		
0x5028	RAM_CR	Reserved														WEN	Reserved	

3 System modules

This section describes the system module peripherals (RST, CLK, System timers, PWR) bits and registers migration from revision 13 to revision 14 of the STM32W108xx datasheet.

3.1 Resets

For the RST IP, there are no updates in term for structure but the only updates are related to the bits and registers naming.

3.1.1 STM32W108xx RST bits and registers overview

Table 5 gives the list of the changes (renaming) made in the RST bits and registers.

Table 5. RST bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx RST bits/registers naming overview																
0X002C	RESET_EVENT	Reserved									CPU_LOCKUP	OPT_BYTE_FAIL	WAKE_UP_DSLEEP	SW_RST	W_DOG	RSTB_PIN	POWER_LV	POWER_HV
	RST_SR										LKUP	OBFAIL	WKUP	SWRST	WDG	PIN	PWRLV	PWRHV

3.2 Clocks

The clock IP is completely updated in term of clock oscillators naming and in term of bits and registers naming.

3.2.1 STM32W108xx CLK oscillators overview

The STM32W108xx integrates four oscillators and to be in line with STM32F families the clocks oscillators naming convention is updated as follows:

- The High frequency RC oscillator (12MHz RC) is renamed by the High Speed Internal clock (HSI).
- The 24 MHz crystal oscillator (24MHz XTAL) is renamed by the High Speed External clock (HSE)
- The 10 KHz RC oscillator (10kHz RC) is renamed by the Low Speed Internal 10 KHz clock (LSI10K)
- The 32.768 KHz crystal oscillator(32kHz XTAL) is renamed by the Low Speed External clock (LSE)

Note: The CLK1K clock is generated from the 10 KHz RC oscillator, so this clock is renamed by Low Speed Internal 1 KHz clock (LSI1K).

3.2.2 STM32W108xx CLK bits and registers overview

In the revision 13 of the STM32W108xx datasheet, the clock peripheral is not fully documented:

- The LSI10KCR, LSI1KCR, HSICR, PERIODCR and PERIODSR registers are required to calibrate the internal clocks (HSI and LSI) are missing.
- The HSECR1 register is required to configure the bias trim, the value should be reset to full bias at power up.
- The HSECOMPR register is required to check the 24MHz oscillator comparator outputs status.
- The DITHERCR register is required to enable disable the clock dither.
- The PCTRACECR register is required to select the PC_TRACE source.
- The new name for the SLEEPTMR_CLKEN register is SLEEPCR register; this register is removed from the sleep timer section and added in the clock section.

Table 6 gives the list of the changes made in the CLK bits and registers naming.

Table 6. CLK bits and registers overview

Offset	Register	Bit 31-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx CLK bits/registers naming overview																
0x0008	SLEEPTMR_CLKEN	Reserved															SLEEPTMR_CLK10KEN	SLEEPTMR_CLK32KEN
	CLK_SLEEPCR	Reserved															LSI10KEN	LSEEN
0x000C	CLK_LSI10KCR	Reserved															TUNE	
0x0010	CLK_LSI1KCR	Res.	CALINT						CLKFRAC									
0x0014 - 0x4000	Reserved																	
0x4004	CLK_HSECR1	Reserved															BIASTRIM	
0x4008	CLK_HSICR	Reserved															TUNE	
0x400C	CLK_HSECOMPR	Reserved															HLEVEL	LLEVEL
0x4010	CLK_PERIODCR	Reserved															MODE	
0x4014	CLK_PERIODSR	Res.	PERIOD															
0x4018	CLK_DITHERCR	Reserved																DIS
0x401C	OSC24M_CTRL	Reserved															OSC24M_EN	OSC24M_SEL
	CLK_HSECR2	Reserved															EN	SW1
0x4020	CPU_CLK_SEL	Reserved																CPU_CLK_SEL
	CLK_CPUCR	Reserved																SW2

3.3 System timers

This sub-section describes the System Timers peripherals (WDG, SLPTMR, MACTMR) bits and registers migration from revision 13 to revision 14 of the STM32W108xx datasheet.

3.3.1 STM32W108xx watchdog timer overview

There are no major updates on the WDG IP. The only updates are related to the bit and register naming. *Table 7* gives the list of the changes made in the WDG bits and registers naming.

Table 7. WDG bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx WDG bits/registers naming overview																
0x6000	WDOG_CFG	Reserved															WDOG_DIS	WDOG_EN
	WDG_CR	Reserved															WDGDIS	WDGEN
0x6004	WDOG_CTRL	Reserved	WDOG_CTRL															
	WDG_KR	Reserved	KEY[15:0]															
0x6008	WDOG_RESTART	Reserved	WDOG_RESTART															
	WDG_KICKSR	Reserved	KS[15:0]															

3.3.2 STM32W108xx Sleep timer Overview

The sleep Timer IP has two levels of changes: the first one is related to the IP structure and to the low power modes requirement and the second one is related to the bits and registers naming.

- The sleep timer force register SLPTMR_IFR is required in low power modes: if the dedicated sleep timer interrupt (WRAP, CMPA or CMPB) is enabled and configured as wake event, in this case the interrupt will not be generated when the CPU

wakes up from low power mode, so the user should check in the power wake up status register PWR_WAKESR which flag is used to wake up the CPU then force the dedicated interrupt in the sleep timer force register SLPTMR_IFR.

- The Sleep timer clock enables register SLEEPTMR_CLKEN is renamed by the sleep control register CLK_SLEEPCR and moved to the clock section.

Table 8 gives the list of the changes made in the Sleep Timer bits and registers.

Table 8. SLPTMR bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108 SleepTimer bits/registers naming overview																
0x600C	SLEEPTMR_CFG	Reserved				SLEEPTMR_REVERSE	SLEEPTMR_ENABLE	SLEEPTMR_DBGPAUSE	Res.		SLEEPTMR_CLKDIV				Reserved		SLEEPTMR_CLKSEL
	SLPTMR_CR	Reserved				REVERSE	EN	DBGP	Res.		PSC				Reserved		CLKSEL
0x6010	SLEEPTMR_CNTH	Res.	SLEEPTMR_CNTH															
	SLPTMR_CNTH	Res.	CNTH															
0x6014	SLEEPTMR_CNTL	Res.	SLEEPTMR_CNTL															
	SLPTMR_CNTL	Res.	CNTL															
0x6018	SLEEPTMR_CMPAH	Res.	SLEEPTMR_CMPAH															
	SLPTMR_CMPAH	Res.	CMPAH															

Table 8. SLPTMR bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108 SleepTimer bits/registers naming overview																
0x601C	SLEEPTMR_CMPAL	Res.	SLEEPTMR_CMPAL															
	SLPTMR_CMPAL	Res.	CMPAL															
0x6020	SLEEPTMR_CMPBH	Res.	SLEEPTMR_CMPBH															
	SLPTMR_CMPBH	Res.	CMPBH															
0x6024	SLEEPTMR_CMPBL	Res.	SLEEPTMR_CMPBL															
	SLPTMR_CMPBL	Res.	CMPBL															
0xA014	INT_SLEEPTMRFLAG	Reserved														INT_SLEEPTMRCMPB	INT_SLEEPTMRCMPA	INT_SLEEPTMRWRAP
	SLPTMR_ISR	Reserved														CMPB	CMPA	WRAP
0xA020	SLPTMR_IFR	Reserved														CMPB	CMPA	WRAP
0xA054	INT_SLEEPTMRCFG	Reserved														INT_SLEEPTMRCMPB	INT_SLEEPTMRCMPA	INT_SLEEPTMRWRAP
	SLPTMR_IER	Reserved														CMPB	CMPA	WRAP
0x0008	SLEEPTMR_CLKEN	Reserved															SLEEPTMR_CLK10KEN	SLEEPTMR_CLK32KEN

3.3.3 STM32W108xx MAC Timer Overview

The MAC Timer IP can be used to measure the timing, this timer is not documented in the revision 13 of datasheet STM32W108xx. *Table 9* gives the MAC timer bits and registers mapping.

Table 9. WDG bits and registers overview

Offset	Register	Bit[31:21]	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx MAC Timer bits/registers naming overview																					
0x2038	MACTMR_CNTR	Reserved	CNT[20:0]																				
0x2040-2088	Reserved																						
0x208C	MACTMR_CR	Reserved																				RST	EN

3.4 Power management

The Low power IP is used to configure the Low power wake up event sources and to control the wake up status, the registers descriptions for this IP are missing in the revision 13 of the STM32W108xx datasheet.

3.4.1 STM32W108xx Power Overview

Table 10 gives the list of the power bits and registers mapping.

Table 10. Power bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx PWR bits/registers naming overview																
0x0004	PWR_DSLEEPCR1	Reserved															LVFREEZE	Reserved
0x008-0x0010	Reserved																	
0x0014	PWR_DSLEEPCR2	Reserved																MODE
0x0018	PWR_VREGCR	Reserved					1V8EN	Res.	1V8TRIM				Res.		1V2EN	Res.	1V2TRIM	
0x001C	Reserved																	
0x0020	PWR_WAKECR1	Reserved							CSYSPWRUPREQ	CPWRRUPREQ	CORE	WRAP	COMPB	COMPA	IRQD	SC2	SC1	WAKEEN
0x0024	PWR_WAKECR2	Reserved											COREWAKE	Reserved				
0x0028	PWR_WAKESR	Reserved							CSYSPWRUPREQ	CPWRRUPREQ	CORE	WRAP	COMPB	COMPA	IRQD	SC2	SC1	GPIOPIN
0x002C-0x0030	Reserved																	
0x0034	PWR_CPWRUPREQSR	Reserved																REQ
0x0038	PWR_CSYSPWRUPREQSR	Reserved																REQ
0x003C	PWR_CSYSPWRUPACKSR	Reserved																ACK
0x0040	PWR_CSYSPWRUPACKCR	Reserved																INHIBIT
0x0044 - 0xBC04	Reserved																	

Table 10. Power bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx PWR bits/registers naming overview																
0xBC08	PWR_ WAKEPAR	Reserved									PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
0xBC0C	PWR_ WAKEPBR	Reserved									PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0xBC10	PWR_ WAKEPCR	Reserved									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0xBC14- 0xBC18	Reserved																	
0xBC1C	PWR_ WAKEFILTR	Reserved													IRQD	SC2	SC1	GPIOPIN

4 General-purpose input/outputs

The General-purpose input/output IP presented in the revision 13 of the STM32W108xx datasheet is split into three main parts:

- Standard General-purpose input/output : GPIO
- External interrupt: EXTI
- Debug management: DBG

The GPIO_PAWAKE, GPIO_PBWAKE, GPIO_PCWAKE and GPIO_WAKEFILT registers are renamed respectively PWR_WAKEPAR, PWR_WAKEPBR, PWR_WAKEPCR and PWR_WAKEFILTR registers. These registers are required to manage the GPIO wake up resources from low power modes and will be presented in the low power mode section.

4.1 Standard General-purpose input/output

This part will contain only the GPIO configurations and status registers.

4.1.1 STM32W108xx GPIO Overview

Table 11 gives the list of the changes (renaming) made in the GPIO bits and registers.

Table 11. GPIO bits and registers overview

Offset (GPIOA/ GPIOB/ GPIOC)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx GPIO bits/registers naming overview																
0x00	GPIO_PxCFGL	Res	Px3_CFG				Px2_CFG				Px1_CFG				Px0_CFG			
	GPIOx_CRL	Res	CNFMODE3[3:0]				CNFMODE2[3:0]				CNFMODE1[3:0]				CNFMODE0[3:0]			
0x04	GPIO_PxCFGH	Res	Px7_CFG				Px6_CFG				Px5_CFG				Px4_CFG			
	GPIOx_CRH	Res	CNFMODE7[3:0]				CNFMODE6[3:0]				CNFMODE5[3:0]				CNFMODE4[3:0]			
0x08	GPIO_PxIN	Reserved									Px7	Px6	Px5	Px4	Px3	Px2	Px1	Px0
	GPIOx_IDR	Reserved									IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0

Table 11. GPIO bits and registers overview

Offset (GPIOA/ GPIOB/ GPIOC)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx GPIO bits/registers naming overview																
0x0C	GPIO_PxOUT	Reserved									Px7	Px6	Px5	Px4	Px3	Px2	Px1	Px0
	GPIOx_ODR	Reserved									ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
0x10	GPIO_PxSET	Reserved									Px7	Px6	Px5	Px4	Px3	Px2	Px1	Px0
	GPIOx_BSR	Reserved									BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0
0x14	GPIO_PxCLR	Reserved									Px7	Px6	Px5	Px4	Px3	Px2	Px1	Px0
	GPIOx_BRR	Reserved									BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

4.2 External interupt

This part will contain the GPIO external interrupts configurations and status registers.

4.2.1 STM32W108xx EXTI Overview

Table 12 gives the list of the changes (renaming) made in the EXTI bits and registers.

Table 12. EXTI bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0xA814	INT_GPIOFLAG	Reserved													INT_ IRQDFLAG	INT_ IRQCFLAG	INT_ IRQBFLAG	INT_ IRQAFLAG
	EXTI_PR	Reserved													IRQDP	IRQCP	IRQBP	IRQAP
0xA818-0xA85C	Reserved																	

Table 12. EXTI bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0xA860	GPIO_INTCFGA	Reserved								GPIO_INTFILT	GPIO_INTMOD			Reserved				
	EXTIA_TSR	Reserved								FILTEN	INTMOD			Reserved				
0xA864	GPIO_INTCFGB	Reserved								GPIO_INTFILT	GPIO_INTMOD			Reserved				
	EXTIB_TSR	Reserved								FILTEN	INTMOD			Reserved				
0xA868	GPIO_INTCFGC	Reserved								GPIO_INTFILT	GPIO_INTMOD			Reserved				
	EXTIC_TSR	Reserved								FILTEN	INTMOD			Reserved				
0xA86C	GPIO_INTCFGD	Reserved								GPIO_INTFILT	GPIO_INTMOD			Reserved				
	EXTID_TSR	Reserved								FILTEN	INTMOD			Reserved				
0xA870-0xBC10	Reserved																	
0xBC18	GPIO_IRQCSEL	Reserved													GPIO_SEL			
	EXTIC_CR	res	Reserved												GPIO_SEL[4:0]			
0xBC14	GPIO_IRQDSEL	Reserved													GPIO_SEL			
	EXTID_CR	res	Reserved												GPIO_SEL[4:0]			

4.3 Debug management

This part will contain the required registers for the debug mode.

4.3.1 STM32W108xx DBG Overview

The GPIO PC trace control register GPIO_PCTRACECR is added to selects PC trace source on baseband debug GPIO pins.

Table 13 gives the list of the changes (renaming) made in the DBG bits and registers.

Table 13. WDG bits and registers overview

Address (DBG)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0x4028	GPIO_PCTRACECR	Reserved																SEL
0x402C-0xBBFC	Reserved																	
0xBC00	GPIO_DBGCFG	Reserved											GPIO_DEBUGDIS	GPIO_EXTREGEN	Reserved			
	GPIO_DBGCR	Reserved											DBGDIS	EXTREGEN	Reserved			
0xBC04	GPIO_DBGSTAT	Reserved													GPIO_BOOTMODE	Reserved	GPIO_FORCEDBG	GPIO_SWEN
	GPIO_DBGSR	Reserved													BOOTMODE	Reserved	FORCEDBG	SWEN

5 Serial interfaces

The STM32W108 has two serial controllers: SC1 and SC2, the register organization in the Datasheet Rev 14 for these IP are presented as following:

- Serial Controller common registers
- Serial peripheral interface registers
- Inter-Integrated circuit registers
- Universal Asynchronous Receiver/Transmitter registers (available for SC1 only)
- Direct memory access registers

5.1 STM32W108xx Serial control Overview

Table 14 gives the list of the changes (renaming) made in the SC bits and registers.

Table 14. SC bits and registers overview

Offset (SC1/ SC2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
Serial Controller (Common registers)																		
0xA808 0xA80C	INT_ SCxFLAG	Res.		INT_SC1PARERR	INT_SC1FRMERR	INT_SCTXULDB	INT_SCTXULDA	INT_SCRXULDB	INT_SCRXULDA	INT_SCNAK	INT_SCCMDFIN	INT_SCTXFIN	INT_SCRXFIN	INT_SCTXUND	INT_SCRXOVF	INT_SCTXIDLE	INT_SCTXFREE	INT_SCRXVAL
	SCx_ISR	Res.		PE	FE	TXULODB	TXULODA	RXULODB	RXULODA	NACK	CMDFIN	BTF	BRF	UDR	OVR	IDLE	TXE	RXNE

Table 14. SC bits and registers overview

Offset (SC1/ SC2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0xA848 0xA84C	INT_ SCxCFG	Res.		INT_SC1PARERR	INT_SC1FRMERR	INT_SCTXULDB	INT_SCTXULDA	INT_SCRXULDB	INT_SCRXULDA	INT_SCNAK	INT_SCCMDFIN	INT_SCTXFIN	INT_SCRXFIN	INT_SCTXUND	INT_SCRXOVF	INT_SCTXIDLE	INT_SCTXFREE	INT_SCRXVAL
	SCx_ IER	Res.		PEIE	FEIE	TXULODRIE	TXULODAIE	RXULODBIE	RXULODAIE	NACKIE	CMDFINIE	BTFIE	BRFIE	UDRIE	OVRIE	IDLEIE	TXEIE	RXNEIE
0xA854 0xA858	SCx_ INTMODE	Reserved														SC_TXIDL ELEVEL	SC_TXFRE ELEVEL	SC_RXVA LLEVEL
	SCx_ICR	Reserved														IDLELEVEL	TXELEVEL	RXNELEV EL
0xC854 0xC054	SCx_ MODE	Reserved															SC_MODE	
	SCx_CR	Reserved															MODE[1:0]	
0xC83C 0xC03C	SCx_DATA	Reserved									SC_DATA							
	SCx_DR	Reserved									DR[7:0]							
0xC860 0xC060	SCx_ RATELIN	Reserved													SC_RATELIN			
	SCx_CRR1	Reserved													LIN[3:0]			
0xC864 0xC064	SCx_ RATEEXP	Reserved													SC_RATEEXP			
	SCx_CRR2	Reserved													EXP[3:0]			
Serial Controller (Serial peripheral interface registers)																		
0xC840 0xC040	SCx_ SPISTAT	Reserved													SC_SPIT XIDLE	SC_SPITX FREE	SC_ SPIRXVAL	SC_SPIR XOVF
	SCx_ SPISR	Reserved													IDLE	TXE	RXNE	OVF

Table 14. SC bits and registers overview

Offset (SC1/ SC2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0xC858 0xC058	SCx_ SPICFG	Reserved											SC_SPIR XDRV	SC_ SPIMST	SC_ SPIRPT	SC_ SPIORD	SC_ SPIPHA	AC_ SPIPOL
	SCx_ SPICR	Reserved											RXMODE	MSTR	RPTEN	LSBFIRST	CPHA	CPOL
Serial Controller (Inter-Integrated circuit registers)																		
0xC844 0xC044	SCx_ TWISTAT	Reserved													SC_TWIC MDFIN	SC_ TWIRXFIN	SC_ TWITXFIN	SC_TWIR XNAK
	SCx_I2CSR	Reserved													CMDFIN	BRF	BTF	NACK
0xC84C 0xC04C	SCx_ TWICTRL1	Reserved													SC_ TWISTOP	SC_ TWISTART	SC_ TWISEND	SC_TWIR ECV
	SCx_ I2CCR1	Reserved													STOP	START	BTE	BRE
0xC850 0xC050	SCx_ TWICTRL2	Reserved																SC_ TWIACK
	SCx_ I2CCR2	Reserved																ACK
0xC848 0xC848	SC1_ UARTSTAT	Reserved										SC_UAR TTXIDL E	SC_UAR TPARER R	SC_UA RTFRM ERR	SC_UART RXOVR	SC_ UARTTXFR EE	SC_UARTR XVAL	SC_ UARTCTS
	SC1_ UARTSR	Reserved										IDLE	PE	FE	OVR	TXE	RXNE	CTS
0xC85C 0xC85C	SC1_ UARTCFG	Reserved										SC_ UARTAU TO	SC_ UARTFL OW	SC_ UARTO DD	SC_ UARTPAR	SC_ UART2STP	SC_ UART8BIT	SC_ UARTRTS
	SC1_ UARTCR	Reserved										AHFCE	HFCE	PS	PCE	STOP	M	nRTS
0xC868 0xC868	SC1_ UARTPER	Res	SC_UARTPER															
	SC1_ UARTBRR1	Res	N[15:0]															

Table 14. SC bits and registers overview

Offset (SC1/ SC2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0xC86C 0xC86C	SC1_ UARTFRAC	Reserved																SC_UART FRAC
	SC1_ UARTBRR2	Reserved																F
Serial Controller (Direct memory access registers)																		
0xC800 0xC000	SCx_ RXBEGA	Reserved							SC_RXBEGA									
	SCx_ DMARXBEG ADDAR	Reserved							ADD[12:0]									
0xC804 0xC004	SCx_ RXENDA	Reserved							SC_RXENDA									
	SCx_ DMARXEND ADDAR	Reserved							ADD[12:0]									
0xC808 0xC008	SCx_ RXBEGB	Reserved							SC_RXBEGB									
	SCx_ DMARXBEG ADDBR	Reserved							ADD[12:0]									
0xC80C 0xC00C	SCx_ RXENDB	Reserved							SC_RXENDB									
	SCx_ DMARXEND ADDBR	Reserved							ADD[12:0]									
0xC810 0xC010	SCx_ TXBEGA	Reserved							SC_TXBEGA									
	SCx_ DMATXBEG ADDAR	Reserved							ADD[12:0]									

Table 14. SC bits and registers overview

Offset (SC1/ SC2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0xC814 0xC014	SCx_ TXENDA	Reserved	SC_TXENDA															
	SCx_ DMATXENDADDAR	Reserved	ADD[12:0]															
0xC818 0xC018	SCx_ TXBEGB	Reserved	SC_TXBEGB															
	SCx_ DMATXBEGADDBR	Reserved	ADD[12:0]															
0xC81C 0xC01C	SCx_ TXENDB	Reserved	SC_TXENDB															
	SCx_ DMATXENDADDBR	Reserved	ADD[12:0]															
0xC820 0xC020	SCx_ RXCNTA	Reserved	SC_RXCNTA															
	SCx_ DMARXCNTAR	Reserved	CNT[12:0]															
0xC824 0xC024	SCx_ RXCNTB	Reserved	SC_RXCNTB															
	SCx_ DMARXCNTBR	Reserved	CNT[12:0]															
0xC828 0xC028	SCx_ TXCNT	Reserved	SC_TXCNT															
	SCx_ DMATXCNTR	Reserved	CNT[12:0]															

Table 14. SC bits and registers overview

Offset (SC1/ SC2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx EXTI bits/registers naming overview																
0xC82C 0xC02C	SCx_ DMASTAT	Reserved				SC_ RXSSEL			SC_RX FRMB	SC_RX FRMA	SC_ RXPARB	SC_RXP ARA	SC_ RXOVRB	SC_RX OVRA	SC_ TXACTB	SC_ TXACTA	SC_ RXACTB	SC_ RXACTA
	SCx_ DMASR	Reserved				NSSS			FEB	FEA	PEB	PEA	OVRB	OVRA	TXBACK	TXAACK	RXBACK	RXAACK
0xC830 0xC030	SCx_ DMACTRL	Reserved											SC_TXD MARST	SC_ RXDMA RST	SC_ TXLODB	SC_ TXLODA	SC_ RXLODB	SC_ RXLODA
	SCx_ DMACR	Reserved											TXRST	RXRST	TXLODB	TXLODA	RXLODB	RXLODA
0xC834 0xC034	SCx_ RXERRA	Reserved				SC_RXERRA												
	SCx_DMAR XERRAR	Reserved				ADD[12:0]												
0xC838 0xC038	SCx_ RXERRB	Reserved				SC_RXERRB												
	SCx_ DMARXERR BR	Reserved				ADD[12:0]												
0xC870 0xC070	SCx_RXCNT SAVED	Reserved				SC_RXCNTSAVED												
	SCx_ DMARXCNT SAVEDR	Reserved				CNT[12:0]												

6 General-purpose timers

In addition to the flash memory interface the timer IP is the same as the one used in the STM32Fxx microcontroller's families, so almost of the bits and registers are already aligned with the standard naming except the registers that are used to manage the timer interrupts (INT_TIMxCFG, INT_TIMxFLAG and INT_TIMxMISS registers).

6.1 STM32W108xx Timers Overview

Table 15. TIM bits and registers overview

Offset (TIM1/ TIM2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx GPTimer bits/registers naming overview																
0xE000 0xF000	TIMx_ CR1	Reserved									TIM_ ARBE	TIM_ CMS		TIM_ DIR	TIM_ OPM	TIM_ URS	TIM_ UDIS	TIM_ CEN
	TIMx_ CR1	Reserved									ARPE	CMS		DIR	OPM	URS	UDIS	CEN
0xE004 0xF004	TIMx_ CR2	Reserved									TIM_ TI1S	TIM_MMS			Reserved			
	TIMx_ CR2	Reserved									TI1S	MMS			Reserved			
0xE008 0xF008	TIMx_ SMCR	Res	TIM_ ETP	TIM_ ECE	TIM_ETPS		TIM_ETF				TIM_ MSM	TIM_TS			Res.	TIM_SMS		
	TIMx_ SMCR	Res	ETP	ECE	ETPS		ETF				MSM	TS			Res.	SMS		
0xE014 0xF014	TIMx_ EGR	Reserved										TIM_TG	Res	TIM_ CC4G	TIM_ CC3G	TIM_ CC2G	TIM_ CC1G	TIM_ UG
	TIMx_ EGR	Reserved										TG	Res	CC4G	CC3G	CC2G	CC1G	UG

Table 15. TIM bits and registers overview

Offset (TIM1/ TIM2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx GPTimer bits/registers naming overview																
0xE018 0xF018	TIMx_ CCMR1	Res.		TIM_OC2M			TIM_ OC2BE	TIM_ OC2FE	TIM_CC2S		Res.	TIM_OC1M			TIM_ OC1BE	TIM_ OC1FE	TIM_CC1S	
		Res	TIM_IC2F				TIM_IC2PSC				TIM_IC1F				TIM_IC1PSC			
	TIMx_ CCMR1	Res.		OC2M			OC2PE	OC2FE	CC2S		Res.	OC1M			OC1PE	OC1FE	CC1S	
		Res	IC2F				IC2PSC				IC1F				IC1PSC			
0xE01C 0xF01C	TIMx_ CCMR2	Res;		TIM_OC4M			TIM_ OC4BE	TIM_ OC4FE	TIM_CC4S		Res.	TIM_OC3M			TIM_ OC3BE	TIM_ OC3FE	TIM_CC3S	
		Res	TIM_IC4F				TIM_IC4PSC				TIM_IC3F				TIM_IC3PSC			
	TIMx_ CCMR2	Res.		OC4M			OC4PE	OC4FE	CC4S		Res.	OC3M			OC3PE	OC3FE	CC3S	
		Res	IC4F				IC4PSC				IC3F				IC3PSC			
0xE020 0xF020	TIMx_ CCER	Reserved			TIM_ CC4P	TIM_ CC4E	Res.		TIM_ CC3P	TIM_ CC3E	Res.		TIM_ CC2P	TIM_ CC2E	Reserved		TIM_ CC1P	TIM_ CC1E
	TIMx_ CCER	Reserved			CC4P	CC4E	Res.		CC3P	CC3E	Res.		CC2P	CC2E	Reserved		CC1P	CC1E
0xE024 0xF024	TIMx_ CTN	Res	TIM_CTN															
	TIMx_ CTN	Res	CTN[15:0]															
0xE028 0xF028	TIMx_ PSC	Res	TIM_PSC															
	TIMx_ PSC	Res	PSC[15:0]															
0xE02C 0xF02C	TIMx_ ARR	Res	TIM_ARR															
	TIMx_ ARR	Res	ARR[15:0]															

Table 15. TIM bits and registers overview

Offset (TIM1/ TIM2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx GPTimer bits/registers naming overview																
0xE034 0xF034	TIMx_ CCR1	Res	TIM_CCR															
	TIMx_ CCR1	Res	CCR[15:0]															
0xE038 0xF038	TIMx_ CCR2	Res	TIM_CCR															
	TIMx_ CCR2	Res	CCR[15:0]															
0xE03C 0xF03C	TIMx_ CCR3	Res	TIM_CCR															
	TIMx_ CCR3	Res	CCR[15:0]															
0xE040 0xF040	TIMx_ CCR4	Res	TIM_CCR															
	TIMx_ CCR4	Res	CCR[15:0]															
0xE050	TIM1_ OR	Reserved													TIM_ ORRSVD	TIM_ CLKMSK EN	TIM1_ EXTRIGSEL	
	TIM1_ OR	Reserved													ORRSVD	CLKMSK EN	EXTRIGSEL	
0xF050	TIM2_ OR	Reserved									TIM_ REMAP C4	TIM_RE MAPC3	TIM_ REMA PC2	TIM_ REMAP C1	TIM_ ORRSVD	TIM_ CLKMSK EN	TIM1_ EXTRIGSEL	
	TIM2_ OR	Reserved									REMAP C4	REMAPC 3	REMA PC2	REMAP C1	ORRSVD	CLKMSK EN	EXTRIGSEL	

Table 15. TIM bits and registers overview

Offset (TIM1/ TIM2)	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx GPTimer bits/registers naming overview																
0xA840	INT_TIMxCFG	Reserved										INT_TIMTIF	Res	INT_TIMCC4IF	INT_TIMCC3IF	INT_TIMCC2IF	INT_TIMCC1IF	INT_TIMUIF
0xA844	TIMx_IER	Reserved										TIE	Res	CC4IE	CC3IE	CC2IE	CC1IE	UIE
0xA800	INT_TIMxFLAG	Reserved				INT_TIMRSVD				Res.		INT_TIMTIF	Res	INT_TIMCC4IF	INT_TIMCC3IF	INT_TIMCC2IF	INT_TIMCC1IF	INT_TIMUIF
0xA804	TIMx_ISR	Reserved				RSVD				Res.		TIP	Res	CC4IP	CC3IP	CC2IP	CC1IP	UIP
0xA818	INT_TIMxMISS	Reserved				INT_TIMMISSCC4IF	INT_TIMMISSCC3IF	INT_TIMMISSCC2IF	INT_TIMMISSCC1IF	Res.		INT_TIMMISSRSVD						
0xA81C	TIMx_MISSR	Reserved				CC4IM	CC3IM	CC2IM	CC1IM	Res.		RSVD						

7 Analog-to-digital converter

For the ADC IP, there are no updates in term for structure but the only updates are related to the bits and registers naming.

7.1 STM32W108xx ADC Overview

Table 16 gives the list of the changes (renaming) made in the ADC bits and registers.

Table 16. ADC bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx ADC bits/registers naming overview																
0xD004	ADC_CFG	Res	ADC_ PERIOD			ADC_ HVSELP	ADC_ HVSELN	ADC_MUXP			ADC_MUXN					ADC_ 1MHZCLK	Reserved	ADC_ ENABLE
	ADC_CR	Res	SMP[2:0]			HVSELP	HVSELN	CHSELP[3:0]			CHSELN[3:0]					CLK	Reserved	ADON
0xD008	ADC_ OFFSET	Res	ADC_OFFSET_FIELD															
	ADC_ OFFSETR	Res	OFFSET[15:0]															
0xD00C	ADC_GAIN	Res	ADC_GAIN_FIELD															
	ADC_ GAINR	Res	GAIN[15:0]															
0xD010	ADC_ DMACFG	Reserved												ADC_ DMARST	Reserved		ADC_DMAAUT OWRAP	ADC_ DMALOAD
	ADC_ DMACR	Reserved												RST	Reserved		AUTOWRAP	LOAD
0xD014	ADC_ DMASTAT	Reserved															ADC_ DMAOVF	ADC_ DMAACT
	ADC_ DMASR	Reserved															OVF	ACT

Table 16. ADC bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx ADC bits/registers naming overview																
0xD018	ADC_ DMABEG	Reserved				ADC_DMABEG												
	ADC_ DMAMSAR	Reserved				MSA[13:0]												
0xD01C	ADC_ DMASIZE	Reserved				ADC_DMASIZE_FIELD												
	ADC_ DMANDTR	Reserved				NDT[12:0]												
0xD020	ADC_ DMACUR	Reserved				ADC_DMACUR_FIELD												Reserved
	ADC_ DMAMNAR	Reserved				MNA[13:0]												Reserved
0xD024	ADC_ DMACNT	Reserved				ADC_DMACNT_FIELD												
	ADC_ DMACNDTR	Reserved				CNDT[12:0]												
0xA810	INT_ ADCFLAG	Reserved												INT_ ADCOVF	INT_ ADCSAT	INT_ ADCULDFULL	INT_ ADCULDHALF	Reserved
	ADC_ISR	Reserved												DMAOVF	SAT	DMABF		Reserved
0xA850	INT_ ADCCFG	Reserved												INT_ ADCOVF	INT_ ADCSAT	INT_ ADCULDFULL	INT_ ADCULDHALF	Reserved
	ADC_IER	Reserved												DMAOVFIE	SATIE	DMABFIE		Reserved

8 Interrupts

The STM32W108xx microcontrollers are based on the core Cortex-M3, so the nested vectored interrupt controller (NVIC) registers section is removed from the datasheet and a reference to the Cortex-M3 programming manual.pdf (PM0056) is added to make the library compliant with the Cortex™ microcontroller software interface standard (CMSIS)

8.1 STM32W108xx NVIC Overview

Table 17 gives the compatibility guideline between the NVIC registers section presented in datasheet Rev13 and the equivalent one in the Cortex-M3 programming manual.

The bits and registers definitions for the Cortex-M3 Core Peripheral Access Layer are provided in the CMSIS library under: CMSIS\Include\core_cm3.h file

Table 17. NVIC bits and registers overview

Offset	0xA820		0xE100		0xE180		0xE200		0xE280		0xE300		0xED3C	
Register	INT_ MISS	Res	INT_ CFGSET	NVIC_ ISER	INT_CFG CLR	NVIC_ ICER	INT_PEN DSET	NVIC_ ISPR	INT_PEN DCLR	NVIC_ ICPR	INT_ ACTIVE	NVIC_ IABR	SCS_ AFSR	SCB_ AFSR
Bit 31-17	Reserved		Reserved										Reserved	
Bit 16	INT_ DEBUG		INT_ DEBUG	DEBUG	INT_ DEBUG	DEBUG	INT_ DEBUG	DEBUG	INT_ DEBUG	DEBUG	INT_ DEBUG	DEBUG		
Bit 15	INT_ IRQD		INT_ IRQD	IRQD	INT_ IRQD	IRQD	INT_ IRQD	IRQD	INT_ IRQD	IRQD	INT_ IRQD	IRQD		
Bit 14	INT_ IRQC		INT_ IRQC	IRQC	INT_ IRQC	IRQC	INT_ IRQC	IRQC	INT_ IRQC	IRQC	INT_ IRQC	IRQC		
Bit 13	INT_ IRQB		INT_ IRQB	IRQB	INT_ IRQB	IRQB	INT_ IRQB	IRQB	INT_ IRQB	IRQB	INT_ IRQB	IRQB		
Bit 12	INT_ IRQA		INT_ IRQA	IRQA	INT_ IRQA	IRQA	INT_ IRQA	IRQA	INT_IRQA	IRQA	INT_I RQA	IRQA		
Bit 11	INT_ADC		INT_ ADC	ADC	INT_ ADC	ADC	INT_ ADC	ADC	INT_ ADC	ADC	INT_ADC	ADC		

Table 17. NVIC bits and registers overview

Bit 10	INT_ MACRX	Res	INT_ MACRX	Res.	INT_ MACRX	Res.	INT_ MACRX	Res.	INT_ MACRX	Res.	INT_ MACRX	Res.	Res.		
Bit 9	INT_ MACTX		INT_ MACTX		INT_ MACTX		INT_ MACTX		INT_ MACTX						
Bit 8	INT_ MACTMR		INT_MAC TMR	MACTMR	INT_MAC TMR	MACTMR	INT_MAC TMR	MACTMR	INT_MAC TMR	MACTMR	INT_ MACTMR	MACTMR			
Bit 7	INT_SEC		INT_ SEC	Res.	INT_ SEC	Res.	INT_ SEC	Res.	INT_ SEC	Res.	INT_SEC	Res.			
Bit 6	INT_SC2		INT_ SC2	SC2	INT_SC2	SC2	INT_SC2	SC2	INT_SC2	SC2	INT_SC2	SC2			
Bit 5	INT_SC1		INT_ SC1	SC1	INT_SC1	SC1	INT_SC1	SC1	INT_SC1	SC1	INT_SC1	SC1			
Bit 4	INT_SLEE PTMR		INT_SLEE PTMR	SLEEPTM R	INT_SLEE PTMR	SLEEPT MR	INT_SLEE PTMR	SLEEPT MR	INT_SLEE PTMR	SLEEPT MR	INT_SLEE PTMR	SLEEPTM R			
Bit 3	INT_BB		INT_BB	Res	INT_BB	Res	INT_BB	Res	INT_BB	Res	INT_BB	Res	WRONGS IZE	WRONGS IZE	
Bit 2	INT_ MGMT		INT_ MGMT	MGMT	INT_ MGMT	MGMT	INT_ MGMT	MGMT	INT_ MGMT	MGMT	INT_ MGMT	MGMT	PROTEC TED	PROTEC TED	
Bit 1	INT_TIM2		INT_ TIM2	TIM2	INT_ TIM2	TIM2	INT_ TIM2	TIM2	INT_ TIM2	TIM2	INT_TIM2	TIM2	Reserved		
Bit 0	INT_TIM1		INT_ TIM1	TIM1	INT_ TIM1	TIM1	INT_ TIM1	TIM1	INT_ TIM1	TIM1	INT_TIM1	TIM1	MISSED	MISSED	

8.2 Management interrupt

The HSE COMP high level and HSE COMP low level interrupts can be managed separately using the management interrupt IP . *Table 18* gives the MGMT bits and registers mapping.

Table 18. MGMT bits and registers overview

Offset	Register	Bit[31:16]	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		STM32W108xx PWR bits/registers naming overview																
0xA018	MGMT_ISR	Reserved															HSECOMPHLIF	HSECOMPLLIF
0xA01C -0xA054	Reserved																	
0xA058	MGMT_IER	Reserved															HSECOMPHLIE	HSECOMPLLIE

9 Revision history

Table 19. Document revision history

Date	Revision	Changes
23-Aug-2012	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com