AN3321
Application note

How to enable remote reset from JTAG on EVALSPEAr310 board rev 2.0

Introduction

This application note provides information on how to modify the evaluation board for SPEAr310 (EVALSPEAr310) rev 2.0 to enable remote system reset through the JTAG interface.

Remote reset is a feature not available by default on EVALSPEAr310 board, but it can help during software debug activity.

1 How to enable the remote system reset from JTAG

The EVALSPEAr310 board (EVB) has a standard "Multi-ICE JTAG Interface" connector, named J26. Through J26, it is possible to connect a JTAG adapter (refer to Appendix F of the reference document [1.]). The connector supports separate reset signals for JTAG-TAP (nTRST pin) and for the board system (nSRST pin).

On the EVB rev 2.0, the actual circuit for system reset is not able to receive a remote reset from the JTAG connector. This can affect the debugging activity, forcing the developer to reset manually by pressing the on-board reset button.

Note: 1 All the modifications listed below are mandatory.

2 A basic skill on soldering tools is required.



This is an ESD sensitive device, improper handling can cause permanent damage to the on-board components.

Here below you can find the list of all the modifications required on the EVB to enable remote system reset through JTAG.

Before starting, you need the following components:

- one device P/N STM6315SDW13F
- one resistor in package 0603, value 0 ohm. It can be replaced with a short wire connection.

Connecting the nSRST pin of the JTAG connector

The EVB default assembly configuration has one resistor (R329) missing, isolating nSRST pin. To connect nSRST pin:

- Mount the R329 resistor, 0 ohm. It is located close to the JTAG connector on the bottom layer.

Joining all reset signals in a single wire

On the revision 2.0 of the board, the reset is distributed through the unidirectional device U12. By design, U12 blocks nSRST signals to go from JTAG to system reset, and prevents JTAG to reset all on-board components. To connect the nSRST signal to the system reset, modify the top layer of the board as follows (see *Figure 1: EVB top layer*):

1. Remove U12, located near the JTAG connector.
2. Solder together pins 7, 8 and 9 of U12.
3. Solder together pins 11, 12, 13, 14, 15, 16, 17 and 18 of U12.

Figure 3 shows the area of U12 after these modifications.

Creating a "wired AND" reset

To comply with JTAG specifications, the reset wire has to be a "wired AND" of "open drain" devices with a common pull-up resistor. The actual reset chip U11 does not have any "open drain" output. To make this feature available:

- Replace the reset chip U11 with a STM6315SDW13F.

  U11 is located close to JTAG connector on the bottom layer (see *Figure 2: EVB bottom layer*). Passive pull-up is already available (R242).

Cleaning-up reset wire

On the actual revision of the board, some optional delay circuits are installed adding high load to reset wire. This is not compliant with JTAG specifications. To solve this issue modify the top layer of the board as follows (see *Figure 1: EVB top layer*):

1. Remove R137 and C57, located near the SMII PHY U18
2. Remove R172 and C75, located near the SMII PHY U19
3. Remove R207 and C90, located near the SMII PHY U20
4. Remove C236, located near the SMII PHY U21. Be careful NOT to remove R242

Figure 1. EVB top layer

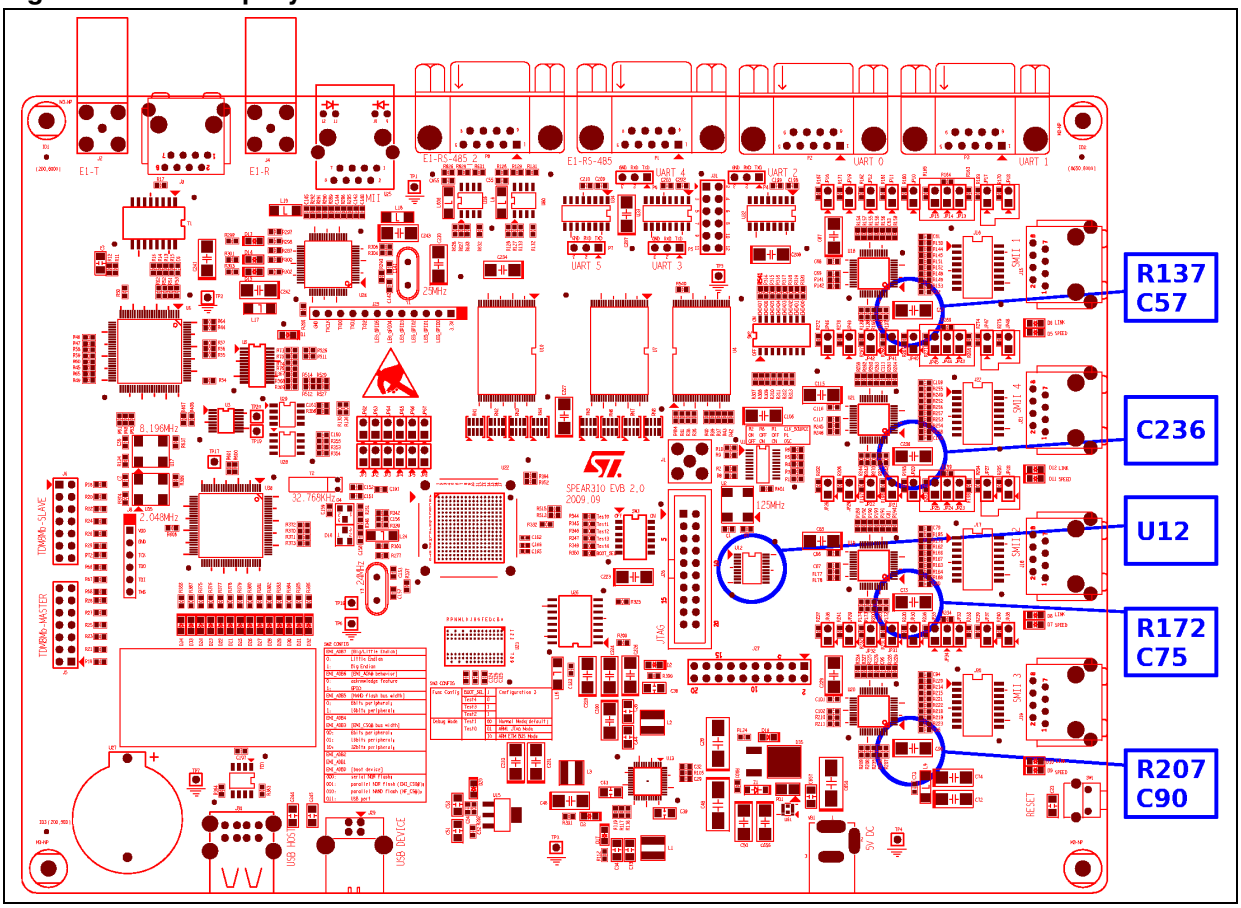


Figure 2. EVB bottom layer

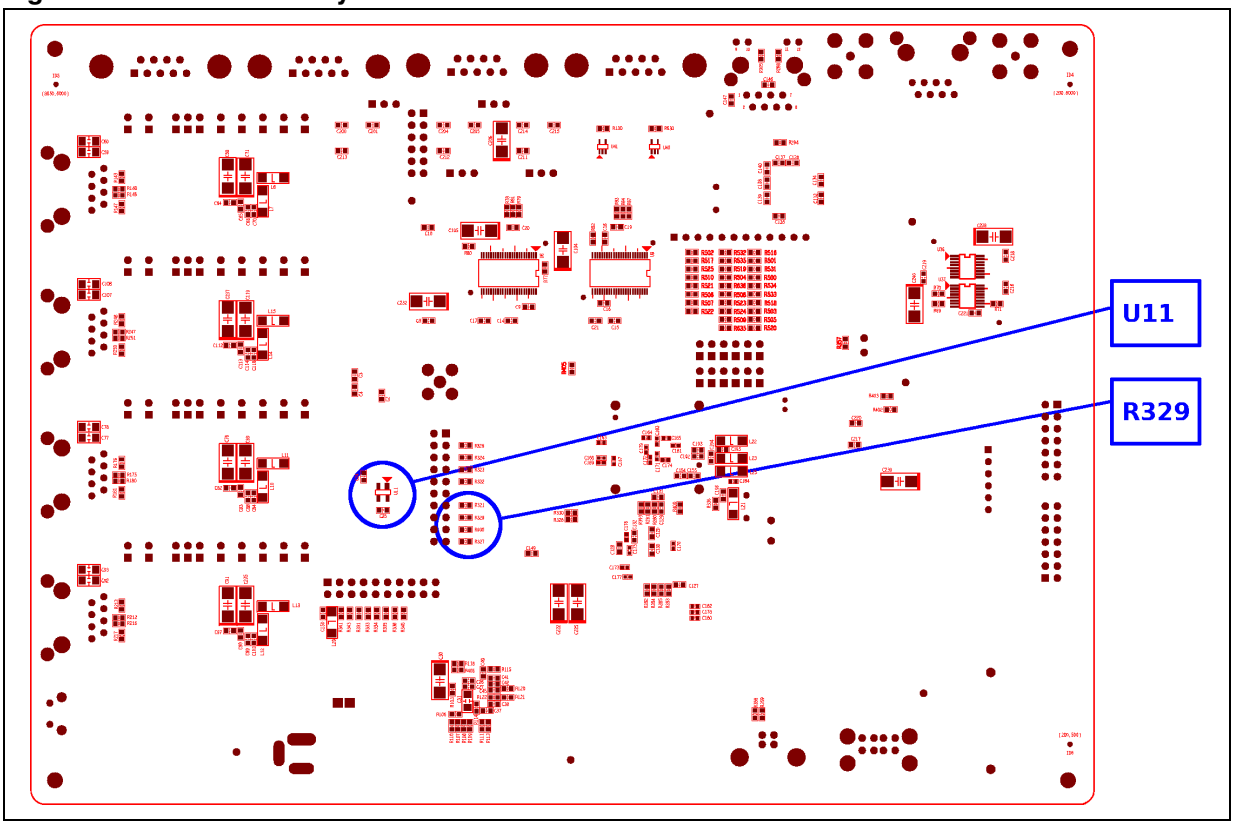
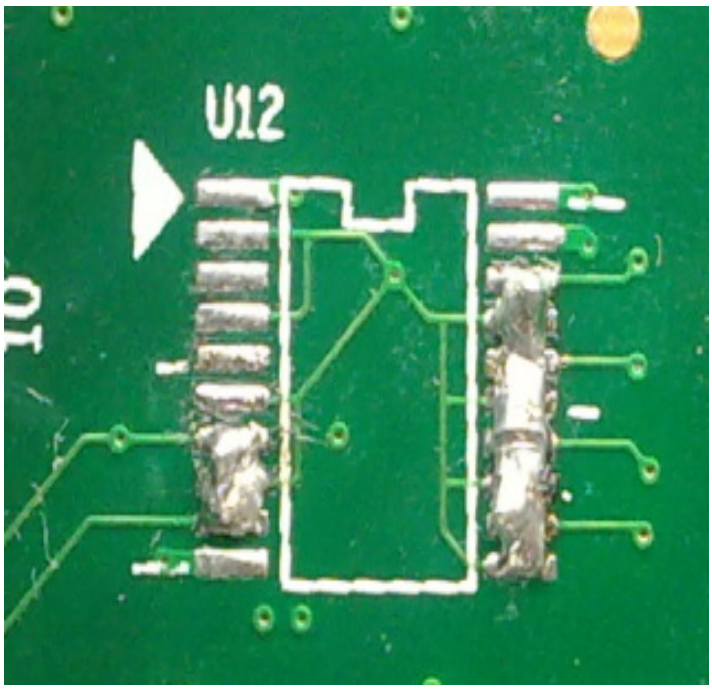


Figure 3. Connections replacing U12



2 References

1. ARM, DUI 0048 F, User manual "Multi-ICE" Version 2.2
   http://infocenter.arm.com/help/topic/com.arm.doc.dui0048f/dui0048.pdf
2. STMicroelectronics, "EVALSPEAr310 Board UM - Rev. 2" User manual (UM0843)
   http://www.st.com/stonline/products/literature/um/16543.pdf

3 Revision history

Table 1. Document revision history

Date	Revision	Changes
25-Nov-2010	1	Initial release.

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