AN3009
Application note

How to design a transition mode PFC pre-regulator using the L6564

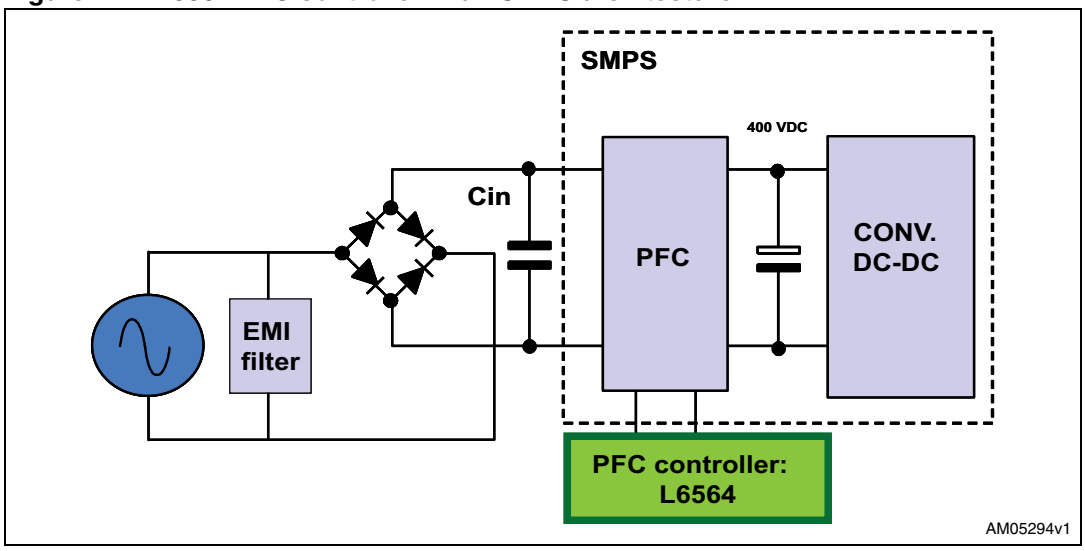
Introduction

The transition mode (TM) technique is widely used for power factor correction in low and medium power applications, such as lamp ballasts, high-end adapters, flatscreen TVs, monitors and PC power supplies, and all switched-mode power supplies that must meet harmonics reduction regulations.

The L6564 is the latest proposal from STMicroelectronics for these types of applications, which may require a low-cost power factor correction solution.

The L6564 is a current-mode power factor correction (PFC) controller that operates in transition mode and embeds all the functions needed to control and properly protect a high-performance PFC converter into a very compact 10-pin SSOP-10 package.

Figure 1. L6564 PFC controller in an SMPS architecture



Contents

1 Introduction to the power factor correction (PFC) 4

2 Operating the transition mode PFC (boost topology) 6

3 Designing a transition mode PFC 8

3.1 Input specification 8

3.2 Operating conditions 10

3.3 Designing the power section 11

3.3.1 Rectifier bridge 11

3.3.2 Input capacitor 11

3.3.3 Output capacitor 12

3.3.4 Boost inductor 13

3.3.5 Power MOSFET selection and dissipation 15

3.3.6 Boost diode selection 18

3.4 L6564 biasing circuitry 19

4 Design example using the L6564-TM PFC Excel spreadsheet 30

5 EVL6564-100W demonstration board 33

6 References 34

7 Revision history 35

List of figures

Figure 1. L6564 PFC controller in an SMPS architecture . . . 1
Figure 2. Boost converter circuit . . . 6
Figure 3. Inductor current waveform and MOSFET timing. . . . 7
Figure 4. Switching frequency fixing the line voltage . . . 14
Figure 5. θ_1 and θ_2 depending on input voltage. . . . 17
Figure 6. Representation of capacitive losses . . . 17
Figure 7. Conduction losses and total losses in the STF7NM50N MOSFET for the L6564 TM PFC 18
Figure 8. L6564 internal schematic . . . 19
Figure 9. Open-loop transfer function bode plot . . . 23
Figure 10. Phase . . . 23
Figure 11. Multiplier characteristics for V_{FF} =1 V . . . 24
Figure 12. Multiplier characteristics for V_{FF} = 3 V . . . 24
Figure 13. Optimum MOSFET activation . . . 28
Figure 14. Excel spreadsheet design specification input table . . . 30
Figure 15. Other design data . . . 30
Figure 16. Excel spreadsheet TM PFC schematic. . . . 31
Figure 17. Excel spreadsheet BOM - 100 W TM PFC based on L6564 . . . 32
Figure 18. Wide-range 100 W demonstration board electrical circuit (EVL6564-100W) . . . 33

1 Introduction to the power factor correction (PFC)

The front-end stage of conventional offline converters, typically consisting of a full-wave rectifier bridge with a capacitor filter, has an unregulated DC bus from the AC mains. The filter capacitor must be large enough to have a relatively low ripple superimposed on the DC level. This means that the instantaneous line voltage is below the voltage on the capacitor most of the time, thus the rectifiers conduct only for a small portion of each line's half-cycle.

The current drawn from the mains then becomes a series of narrow pulses whose amplitude is five to ten times higher than the resulting DC value. Many drawbacks result, such as a much higher peak and RMS current down from the line, distortion of the AC line voltage, overcurrents in the neutral line of the three-phase systems and, consequently, poor utilization of the power system's energy capability. This can be measured in terms of either total harmonic distortion (THD), as norms provide for, or power factor (PF), intended as the ratio between the real power (the one transferred to the output) and the apparent power (RMS line voltage times RMS line current) drawn from the mains, which is more immediate. A traditional input stage with capacitive filter has a low PF (0.5-0.7) and a high THD (>100%).

By using switching techniques, a power factor correction (PFC) pre-regulator, located between the rectifier bridge and the filter capacitor, allows drawing a quasi-sinusoidal current from the mains, in phase with the line voltage. The power factor becomes very close to 1 (more than 0.99 is possible) and the previously mentioned drawbacks are eliminated. Theoretically, any switching topology can be used to achieve a high power factor but, in practice, the boost topology has become the most popular thanks to the advantages it offers.

- Primarily because the circuit requires the fewest external parts (low-cost solution).
- The boost inductor located between the bridge and the switch causes the input di/dt to be low, thus minimizing the noise generated at the input and, therefore, the requirements on the input EMI filter.
- The switch is source-grounded, therefore easy to drive.

However, a boost topology requires the DC output voltage to be higher than the maximum expected line peak voltage (400 VDC is a typical value for 230 V or wide-range mains applications). In addition, there is no isolation between the input and output, thus any line voltage surge is passed on to the output. Two methods of controlling a PFC pre-regulator are currently widely used: the fixed-frequency average current mode pulse-width modulation (FF PWM) and the transition mode pulse-width modulation (TM PWM), the latter having a fixed ON time and variable frequency. The first method needs a complex control that requires a sophisticated controller IC (ST's L4981A, with the variant of the frequency modulation offered by the L4981B) and a considerable component count. The second method requires a simpler control (implemented by ST's L6564), fewer external parts and is therefore much more economical. With the first method, the boost inductor works in continuous conduction mode, while the transition mode makes the inductor work on the boundary between continuous and discontinuous mode by definition. For a given throughput power, transition mode operation involves higher peak currents. This, also consistently with cost considerations, suggests its use in a lower power range (typically up to 250 W), while the former is recommended for higher power levels. To conclude, FF PWM is not the only alternative when continuous current mode (CCM) operation is desired. FF PWM modulates both switch ON and OFF times (their sum is constant by definition), and a given converter operates in either CCM or DCM (discontinuous current mode), depending on the input voltage and the load conditions.

Exactly the same result can be achieved if the ON time only is modulated and the OFF time is kept constant, in which case, however, the switching frequency is no longer fixed. This is referred to as “fixed off time” (FOT) control. Peak current-mode control can still be used. This application note focuses on transition mode.

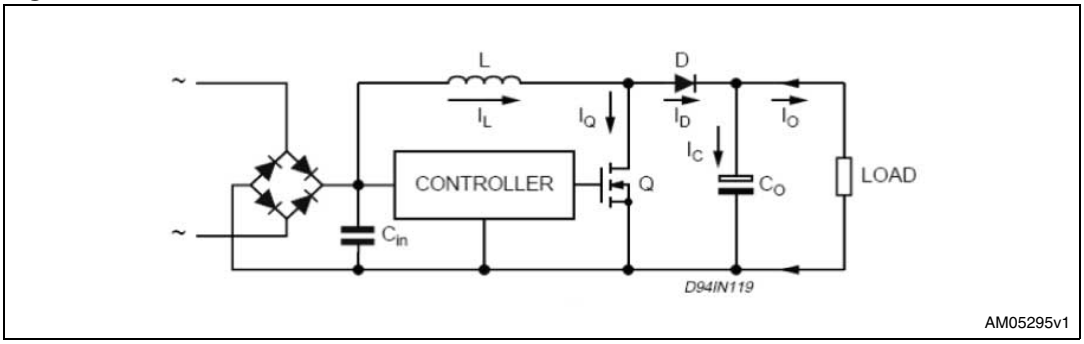
2 Operating the transition mode PFC (boost topology)

The operation of the PFC transition mode controlled boost converter can be summarized as follows.

The AC mains voltage is rectified by a bridge and this rectified voltage is delivered to the boost converter. This boost converter, using a switching technique, boosts the rectified input voltage to a regulated DC output voltage (Vo).

The boost converter consists of a boost inductor (L), a controlled power switch (Q), a catch diode (D), an output capacitor (Co) and, obviously, a control circuitry (*Figure 2*). The goal is to shape the input current in a sinusoidal fashion, in phase with the input sinusoidal voltage. To do this, the L6564 uses the transition mode technique.

Figure 2. Boost converter circuit



The error amplifier compares a partition of the output voltage of the boost converter with an internal reference, generating an error signal proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (below 20 Hz), the error signal is a DC value over a given half-cycle.

The error signal is fed into the multiplier block and multiplied by a partition of the rectified mains voltage. The result is a rectified sinusoid whose peak amplitude depends on the mains peak voltage and the value of the error signal.

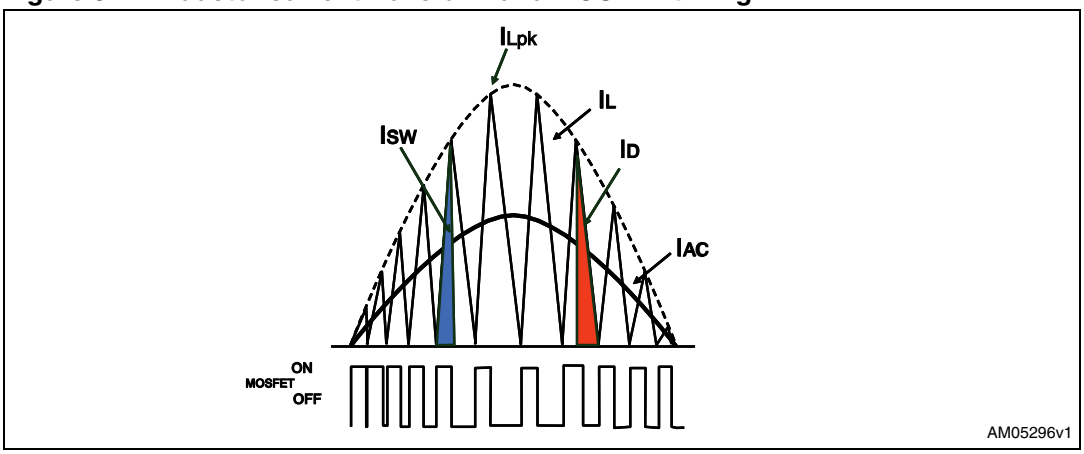
The output of the multiplier is in turn fed into the (+) input of the current comparator, thus it represents a sinusoidal reference for the PWM. In fact, when the voltage on the current sense pin (instantaneous inductor current times the sense resistor) equals the value on the (+) of the current comparator, the conduction of the MOSFET is terminated. As a consequence, the peak inductor current is enveloped by a rectified sinusoid. As demonstrated in *Section 3.3.4*, transition mode control causes a constant ON time operation over each line half-cycle.

After the MOSFET has been turned off, the boost inductor discharges its energy into the load until its current goes to zero. The boost inductor has now run out of energy, the drain node is floating and the inductor resonates with the total capacitance of the drain. The drain voltage drops rapidly below the instantaneous line voltage and the signal on the zero current detector (ZCD) drives the MOSFET on again and another conversion cycle starts.

This low voltage across the MOSFET upon its activation reduces both the switching losses and the total drain capacitance energy that is dissipated inside the MOSFET.

The resulting inductor current and the timing intervals of the MOSFET are shown in *Figure 3*, where it can be observed that, by geometric relationships, the average input current (the one drawn from the mains) is just one half of the peak inductor current waveform.

Figure 3. Inductor current waveform and MOSFET timing



The system operates not exactly on, but very close to, the boundary between continuous and discontinuous current mode and that is why this system is called a transition mode PFC. Besides the simplicity and the few external parts required, this system minimizes the inductor's size due to the low inductance value needed. On the other hand, the high current ripple on the inductor involves high RMS current and high noise on the rectified mains bus, which needs a heavier EMI filter to be rejected. These drawbacks limit the use of the TM PFC to lower power range applications.

3 Designing a transition mode PFC

3.1 Input specification

This sections describes a possible design flowchart referred to as a transition mode PFC, using the L6564. The first part is a detailed specification of the operating conditions of the circuit that is needed for the following calculation. In this example, a L6564 wide input range mains PFC circuit has been considered. Some design criteria is also provided.

- Mains voltage range (Vac rms): $VAC_{min} = 90Vac \quad VAC_{max} = 265Vac$ (1)

- Minimum mains frequency $f_l = 47\,Hz$ (2)

- Rated output power (W): $P_{out} = 100\,W$ (3)

Because the PFC has a boost topology, the regulated output voltage depends strongly on the maximum AC input voltage. In fact, for correct operation of the boost mechanism the output voltage must always be higher than the input. As a result, because Vin max is 265.1.414 = 374.7 Vpk, the typical value of the output has been set to 400 Vdc. If the input voltage is higher, as is typical in ballast applications, the output voltage must be increased accordingly. As a rule of thumb, the output voltage must be 6 or 7% higher than the maximum input voltage peak.

- Regulated DC output voltage (Vdc): $V_{out} = 400\,V$ (4)

The target efficiency and power factor are set here to the minimum input voltage and maximum load. They are used for the following operating condition calculation of the PFC. Of course, at high input voltages the efficiency is higher.

- Expected efficiency (%): $\eta = 94\%$ (5)

- Expected power factor: $PF = 0.99$ (6)

Because of the narrow-loop voltage bandwidth, the PFC output can face overvoltages at start-up or when load transients occur.

To avoid excessive output voltages that might overstress the output components and the load, the L6564 incorporates a device pin (PFC_OK, pin #6) dedicated to monitoring the output voltage with a separate resistor divider, selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (V_{OVP}), usually larger than the maximum Vout that can be expected (including worst-case load/line transients).

- Maximum output voltage (Vdc): $V_{OVP} = 430$ V (7)

The mains frequency generates a 2 f_L voltage ripple on the output voltage at full load. The ripple amplitude determines the current flowing into the output capacitor and the ESR.

Additionally, a request for a certain hold-up capability can be sent to the PFC in case mains dips occur, in which case the output capacitor also has to be dimensioned taking into account the required minimum voltage value (Vout min) after the hold-up time (t_{Hold}) has elapsed.

- Maximum output low frequency ripple: $\Delta V_{out} = 20$ V (8)

- Minimum output voltage after line drop (Vdc): $V_{outmin} = 300$ V (9)

- Holdup capability (ms): $t_{Hold} = 10$ ms (10)

The PFC's minimum switching frequency is one of the main parameters used to dimension the boost inductor; here the switching frequency is considered at low mains at the peak of the sinusoid and at full load conditions. As a rule of thumb, the switching frequency must be higher than the audio bandwidth to prevent audible noise. Additionally, it must not interfere with the L6564's minimum internal starter period (reported in the datasheet). On the other hand, if the minimum frequency is too high, the circuit shows excessive losses at a higher input voltage and probably skips switching cycles not only at light loads. The typical minimum frequency range is 20 - 50 kHz for wide-range operation.

- Minimum switching frequency (kHz): $f_{swmin} = 40$ kHz (11)

To properly select the power components of the PFC and dimension the heatsinks if they are needed, the maximum operating ambient temperature around the PFC circuitry must be known. Note that this is not the maximum external operating temperature of the entire equipment, but rather the local temperature at which the PFC components are working.

- Maximum ambient temperature (°C): $T_{ambx} = 50°C$ (12)

3.2 Operating conditions

The first step is to define the main parameters of the circuit, using the specification points defined in the previous section.

- Rated DC output current

Equation 1

$$I_{out} = \frac{P_{out}}{V_{out}} \qquad I_{out} = \frac{100\ W}{400\ V} = 0.25\ A$$

- Maximum input power

Equation 2

$$P_{in} = \frac{P_{out}}{\eta} \qquad P_{in} = \frac{100\ W}{94} \cdot 100 = 106.38\ W$$

- RMS input current

Equation 3

$$I_{in} = \frac{P_{in}}{VAC_{min} \cdot PF} \qquad I_{in} = \frac{106.38\ W}{90Vac \cdot 0.99} = 1.19\ A$$

- Peak inductor current

Equation 4

$$IL_{pk} = 2 \cdot \sqrt{2} \cdot I_{in} \qquad IL_{pk} = 2 \cdot \sqrt{2} \cdot 1.19\ A = 3.38\ A$$

As shown in *Figure 3 on page 7*, the inductor current is of a triangular shape at the switching frequency, and the peak of the triangle is twice its average value. The average value of the inductor current is exactly the peak of the input sinewave current, and therefore can be easily calculated as its RMS value can be obtained from *Equation 3*. To write a complete inductor specification for the inductor manufacturer, one also must provide the RMS and AC current, which can both be calculated from *Equation 5* and *Equation 6*, respectively.

- RMS inductor current

Equation 5

$$IL_{rms} = \frac{2}{\sqrt{3}} \cdot I_{in} \qquad IL_{rms} = \frac{2}{\sqrt{3}} \cdot 1.19\ A = 1.38\ A$$

- AC inductor current

Equation 6

$$IL_{ac} = \sqrt{IL_{rms}^2 - I_{in}^2} \qquad IL_{ac} = \sqrt{(1.38)^2 - (1.19\ A)^2} = 0.69\ A$$

The current flowing in the inductor can be split into two parts, depending on the instant of conduction: during the ON time, the current increases from zero up to the peak value and circulates into the switch, while during the following OFF time, the current decreases from the peak down to zero and circulates into the diode. Therefore, a current with a triangular wave flows into these two components with a peak value equal to the inductor value. It is also possible, therefore, to calculate the RMS current flowing into the switch and into the diode, which is necessary to calculate the losses of these two elements.

- RMS switch current

Equation 7

$$ISW_{rms} = IL_{pk} \cdot \sqrt{\frac{1}{6} - \frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{VAC_{min}}{V_{out}}} \qquad ISW_{rms} = 3.38\ A \cdot \sqrt{\frac{1}{6} - \frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{90Vac}{400\ V}} = 1.18\ A$$

- RMS diode current

Equation 8

$$ID_{rms} = IL_{pk} \cdot \sqrt{\frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{VAC_{min}}{V_{out}}} \qquad ID_{rms} = 3.38\ A \cdot \sqrt{\frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{90Vac}{400\ V}} = 0.72\ A$$

3.3 Designing the power section

3.3.1 Rectifier bridge

The input rectifier bridge can use any standard, slow recovery, low-cost device. A 600 V device is normally used to obtain enough margin against mains surges. A negative temperature coefficient (NTC) resistor limiting the current at turn-on is required to prevent any overstress on the diode bridge.

The power dissipation of the rectifier bridge can be calculated using *Equation 9*, *Equation 10* and *Equation 11*. The threshold voltage and dynamic resistance of a single diode of the bridge can be found in the component datasheet.

Equation 9

$$\bar{I}_{inrms} = \frac{\sqrt{2} \cdot I_{in}}{2} = \frac{\sqrt{2} \cdot 1.19\ A}{2} = 0.84\ A$$

Equation 10

$$\bar{I}_{in_avg} = \frac{\sqrt{2} \cdot I_{in}}{\pi} = \frac{\sqrt{2} \cdot 1.19\ A}{\pi} = 0.54\ A$$

For this application, a GBU4J rectifier bridge has been used. The power dissipated by the bridge is:

Equation 11

$$P_{bridge} = 4 \cdot R_{diode} \cdot \bar{I}^2_{inrms} + 4 \cdot V_{th} \cdot \bar{I}_{in_avg}$$

$$P_{bridge} = 4 \cdot 0.04\ \Omega \cdot (0.84\ A)^2 + 4 \cdot 0.7\ V \cdot 0.54\ A = 1.62\ W$$

3.3.2 Input capacitor

The input high-frequency filter capacitor (Cin) has to attenuate the switching noise due to the high-frequency inductor current ripple (twice the average line current, as shown in *Figure 3*). The worst conditions occur on the peak of the minimum rated input voltage. The maximum high-frequency voltage ripple across Cin is usually imposed between 5% and 20% of the minimum rated input voltage. This is expressed by a coefficient r (= 0.05, 0.2) as an input design parameter.

- Ripple voltage coefficient (%): r= 0.15 (13)

Equation 12

$$C_{in} = \frac{I_{in}}{2\pi \cdot f_{sw\,min} \cdot r \cdot VAC_{min}} \qquad C_{in} = \frac{1.19A}{2\pi \cdot 40\,kHz \cdot 0.15 \cdot 90Vac} = 0.359\,\mu F$$

In real conditions, the input capacitance must be designed taking into account the EMI filter and a tolerance on the component of about 5% to 10% (typical for polyester capacitors).

A commercial value of Cin = 0.47 µF has been selected. Of course, a larger capacitor provides a benefit from an EMI point-of-view, but does not benefit the THD, especially at high mains. Therefore, a compromise must be found between these two parameters. A good-quality film capacitor for this component must be selected to provide effective filtering.

3.3.3 Output capacitor

The selection of the output bulk capacitor (Co) depends on the DC output voltage *(4)*, the allowed maximum output voltage *(7)* and the converter's output power *(3)*.

The 100/120 Hz (twice the mains frequency) voltage ripple (ΔVout = peak-to-peak ripple value) is a function of the capacitor impedance and the peak capacitor current.

Equation 13

$$\Delta V_{out} = 2 \cdot I_{out} \cdot \sqrt{\frac{1}{(2\pi \cdot 2f_l \cdot C_O)^2} + ESR^2}$$

With a low ESR capacitor the capacitive reactance is dominant, therefore:

Equation 14

$$C_O \geq \frac{I_{out}}{2\pi \cdot f_l \cdot \Delta V_{out}} = \frac{P_{out}}{2\pi \cdot f_l \cdot V_{out} \cdot \Delta V_{out}} \qquad C_O \geq \frac{100\ W}{2\,\pi \cdot 47\ Hz \cdot 400\ V \cdot 20\ V} = 42.5\,\mu F$$

ΔVout is usually selected in the range of 1.5% of the output voltage. Although ESR does not normally affect the output ripple, it should be taken into account to calculate the power losses. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

Equation 15

$$I_{Crms} = \sqrt{ID^2_{rms} - I^2_{out}} \qquad I_{Crms} = \sqrt{(0.72\ A)^2 - (0.25\ A)^2} = 0.67\ A$$

If the PFC stage has to guarantee a specified hold-up time, the selection criterion of the capacitance changes: Co has to deliver the output power for a certain time (t_{Hold}) with a specified maximum dropout voltage ($V_{out\,min}$), that is, the minimum output voltage value (which takes load regulation and output ripple into account) and is the minimum output operating voltage before the 'power fail' detection and consequent stopping by the downstream system supplied by the PFC.

Equation 16

$$C_O = \frac{2 \cdot P_{out} \cdot t_{Hold}}{\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2} \qquad C_O = \frac{2 \cdot 100\ W \cdot 10\ ms}{(400\ V - 20\ V)^2 - (300\ V)^2} = 36.7\ \mu F$$

A 20% tolerance on the electrolytic capacitors has to be considered to obtain the correct dimensioning. As per *Equation 14*, we have selected for this application a capacitor Co equal to 47 µF (450 V) so as to maintain a hold-up capability for 12 ms. The actual output voltage ripple with this capacitor is also calculated. In detail:

Equation 17

$$t_{hold} = \frac{C_O \cdot \left[\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2\right]}{2 \cdot P_{out}} \qquad t_{hold} = \frac{47\ \mu F \cdot \left[(400\ V - 20\ V)^2 - (300\ V)^2\right]}{2 \cdot 100\ W} = 14.78\ ms$$

As expected the ripple variation on the output is:

Equation 18

$$\Delta V_{out} = \frac{I_{out}}{2 \cdot \pi \cdot f_l \cdot C_O} \qquad \Delta V_{out} = \frac{0.25\ A}{2 \cdot \pi \cdot 47\ Hz \cdot 47\ \mu F} = 18.02\ V$$

3.3.4 Boost inductor

The boost inductor determines the working frequency of the converter, thus it is usually calculated so that the minimum switching frequency is greater than the maximum frequency of the L6564's internal starter (typically 150 µs) to ensure correct transition mode operation. Assuming a unity power factor, it is possible to write:

Equation 19

$$t_{on}(VAC, \vartheta) = \frac{L \cdot IL_{pk} \cdot \sin(\vartheta)}{\sqrt{2} \cdot VAC \cdot \sin(\vartheta)} = \frac{L \cdot IL_{pk}}{\sqrt{2} \cdot VAC}$$

Equation 19 shows that the ON time does not depend on the angle of the mains phase, but is constant over the entire mains cycle.

Equation 20

$$t_{off}(VAC, \vartheta) = \frac{L \cdot IL_{pk} \cdot \sin(\vartheta)}{V_{out} - \sqrt{2} \cdot VAC \cdot \sin(\vartheta)}$$

ton and toff are the power MOSFET's ON and OFF times respectively, IL_{pk} the maximum peak inductor current in a line cycle and θ the instantaneous line phase in the interval $[0,\Pi]$). Note that the ON time is constant over a line cycle.

As previously said, IL_{pk} is twice the line-frequency peak current (*Equation 4*), which is related to the input power and input mains voltage. By substituting this relationship in the expressions of ton and toff, it is possible to find the instantaneous switching frequency along a given line cycle.

Equation 21

$$f_{sw}(VAC,\theta) = \frac{1}{T_{on}+T_{off}} = \frac{1}{2 \cdot L \cdot P_{in}} \cdot \frac{VAC^2 \cdot \left(V_{out} - \sqrt{2} \cdot VAC \cdot \sin(\theta)\right)}{V_{out}}$$

The switching frequency is minimal at the top of the sinusoid ($\theta = \Pi/2$ ==> $\sin\theta = 1$), maximal at the zero crossings of the line voltage ($\theta = 1$ or Π ==> $\sin\theta = 0$), where toff = 0.

The absolute minimum frequency fswmin can occur at either the maximum VAC_{max} or the minimum mains voltage VAC_{min}. The inductor value is therefore defined by the formula:

Equation 22

$$L(VAC) = \frac{VAC^2 \cdot (V_{out} - \sqrt{2} \cdot VAC)}{2 \cdot f_{sw\,min} \cdot P_{in} \cdot V_{out}}$$

After calculating the values of the inductor at low and high mains – $L(VAC_{min})$ and $L(VAC_{max})$ – the minimum value must be taken into account. It becomes the maximum inductance value for dimensioning the PFC.

Equation 23

$$L(VAC_{min}) = \frac{(90Vac)^2 \cdot (400\ V - \sqrt{2} \cdot 90Vac)}{2 \cdot 40\ \ kHz \cdot 106.38\ W \cdot 400\ V} = 0.642\ mH$$

$$L(VAC_{max}) = \frac{(265Vac)^2 \cdot (400\ V - \sqrt{2} \cdot 265Vac)}{2 \cdot 40\ kHz \cdot 106.38\ W \cdot 400\ V} = 0.515\ mH$$

For this application, a 0.52 mH boost inductance has been selected.

Figure 4. Switching frequency fixing the line voltage

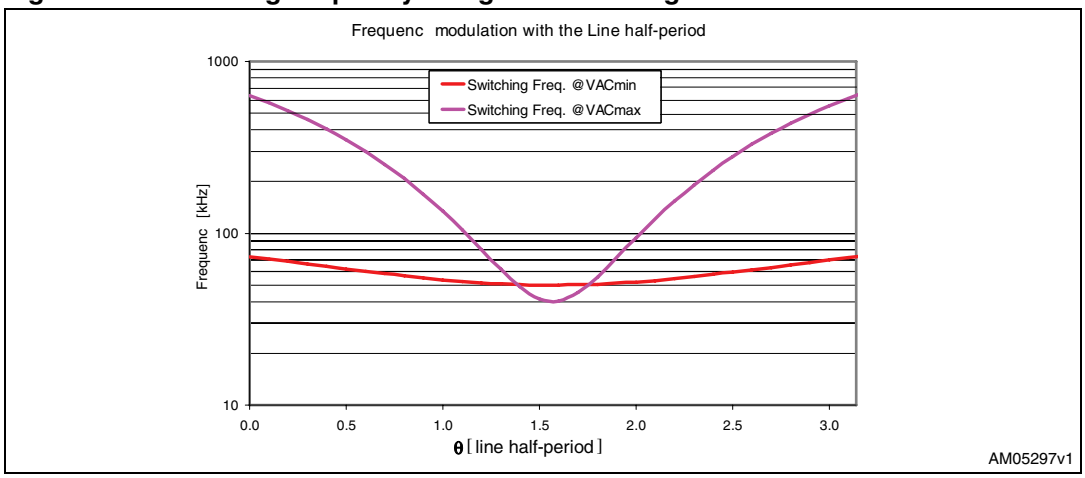


Figure 4 shows the switching frequency versus the θ angle calculated with *Equation 22*, a 0.52 mH boost inductance and the line voltage fixed at the minimum and maximum values. The minimum switching frequency can be recalculated for the selected inductance value by inverting *Equation 22* to become:

Equation 24

$$f_{sw\,min}(VAC) = \frac{VAC^2 \cdot (V_{out} - \sqrt{2} \cdot VAC)}{2 \cdot L \cdot P_{in} \cdot V_{out}}$$

When one compares fswmin(VAC_{min}) and fswmin(VAC_{max}) with L = 0.52 mH, the actual calculated minimum switching frequency is 40.13 kHz, as expected.

The core size is determined by assuming a peak flux density Bx ≅ 0.25 T (depending on the ferrite grade selected and relevant specific losses) and by calculating the maximum current according to *Equation 45*, as a function of the maximum clamping voltage of the current sense pin and the value of the sense resistor.

DC and AC copper losses and ferrite losses must also be calculated to determine the maximum temperature rise of the inductor.

3.3.5 Power MOSFET selection and dissipation

The MOSFET selection involves mainly its $R_{DS(on)}$, which depends on the output power *(3)*, since the breakdown voltage is fixed by the output voltage only *(4)*, plus the overvoltage allowed *(7)* and a safety margin (20%). Therefore, a voltage rating of 500 V (1.2 · Vout = 480 V) has been selected. With regard to its current rating, as a rule of thumb, one can select a device with approximately three times the RMS switch current (*Equation 7*) but, in any case, the calculation of the power dissipation provides the final confirmation that the selected device is the right one for the circuit. The heatsink dimensions must also be taken into consideration. For this L6564 TM PFC application, we have selected a STF7NM50 MOSFET. The MOSFET's power dissipation depends on the conduction, switching and capacitive losses.

The conduction losses at maximum load and minimum input voltage are calculated by:

Equation 25

$$P_{cond}(VAC) = R_{DS(on)} \cdot (ISW_{rms}(VAC))^2$$

Since in datasheets the $R_{DS(on)}$ is normally given at ambient temperature (25 °C), to correctly calculate the conduction losses at 100°C (typical MOSFET junction working temperature), a factor of 1.75-2 should be applied. The correct factor can be found in the device datasheet.

The conduction losses referred to a 1 Ω $R_{DS(on)}$ at ambient temperature as a function of the input power (p_{in}) and Vac can now be calculated by combining *Equation 25* and *Equation 7*.

Equation 26

$$P'_{cond}(VAC) = 2 \cdot (ISW_{rms}(VAC))^2 = 2 \cdot \left(\frac{P_{in}}{\sqrt{2} \cdot VAC \cdot PF} \cdot \sqrt{2 - \frac{16}{3\pi} \cdot \frac{\sqrt{2} \cdot VAC}{V_{out}}} \right)^2$$

The switching losses in the MOSFET occur only at turn-off because of the TM operation, and can be basically expressed by:

Equation 27

$$P_{switch}(VAC) = V_{MOS} \cdot I_{MOS} \cdot t_{fall} \cdot f_{sw}(VAC)$$

Equation 27 represents the crossing between the MOSFET current that decreases linearly during the fall time and the voltage on the MOSFET drain that increases. In fact, during the fall time, the current of the boost inductor flows into the parasitic capacitance of the MOSFET charging it.

For this reason, switching losses also depend on the total drain capacitance. Because the switching frequency depends on the input line voltage and the phase angle on the sinusoidal waveform, using *Equation 27* the switching losses per 1 µs of current fall time and 1 nF of total drain capacitance can be written as:

Equation 28

$$P'_{switch}(VAC) = IL_{pk} \cdot V_{out} \cdot \frac{1}{\pi}\int_{0}^{\pi}(\sin\vartheta)^2 \cdot f_{sw}(VAC,\theta)\cdot d\vartheta$$

Refer to the MOSFET datasheet to find the value of tfall at turn-off.

At turn-on, the losses are due to the discharge of the total drain capacitance inside the power MOSFET itself. In general, the capacitive losses are given by:

Equation 29

$$P_{cap}(VAC) = \frac{1}{2}\cdot C_d \cdot V^2{}_{MOS} \cdot f_{sw}(VAC)$$

where Cd is the total drain capacitance including the MOSFET and any other parasitic capacitances such as the inductor at the drain node, and where V_{MOS} is the drain voltage at the MOSFET's turn-on.

Taking into account the frequency variation with the input line voltage and the phase angle similar to *Equation 29*, a detailed description of the capacitive losses per 1 nF of total drain capacitance can be calculated as:

Equation 30

$$P'_{cap}(VAC) = \frac{1}{2}\cdot\frac{1}{\pi}\int_{\vartheta_1}^{\vartheta 2}\left(2\sqrt{2}VAC - V_{out}\right)^2 f_{sw}(VAC,\vartheta)\cdot d\vartheta$$

θ and θ_2 depend on the input voltage and are defined below.

Equation 31

$$\vartheta_1 = \arcsin\left(\frac{V_{out}}{2\sqrt{2}VAC}\right)$$

Equation 32

$$\vartheta_2 = \pi - \vartheta_1$$

Figure 5. θ_1 and θ_2 depending on input voltage

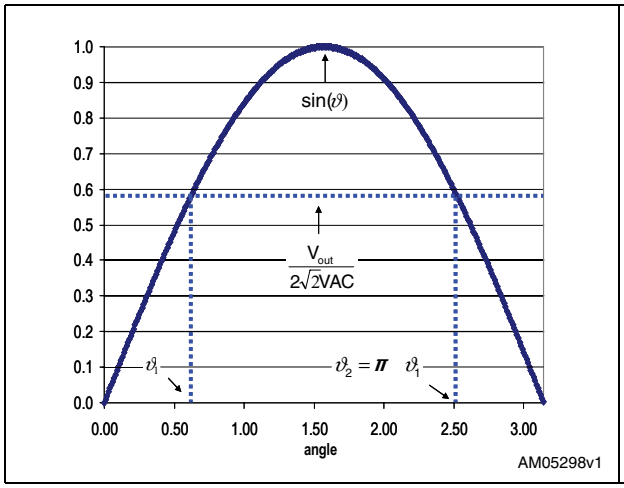


Figure 6. Representation of capacitive losses

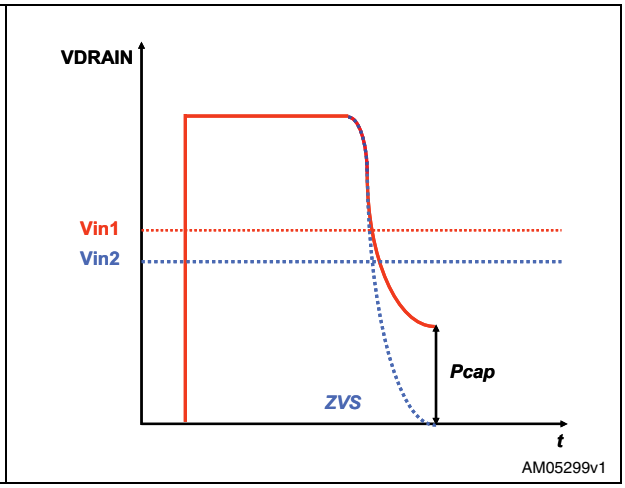


Figure 5 shows the relationship between θ_1 and θ_2 depending on the input voltage. *Figure 6* represents a waveform of the drain voltage. The MOSFET's activation occurs exactly on the valley because the inductor has run out of energy and therefore can resonate with the drain capacitance. Details are provided in the section on the ZCD pin (pin #7). It is clear that for an input voltage theoretically lower than half of the output voltage, the resonance should ideally reach zero, achieving a zero voltage operation and therefore avoiding any losses on this edge. An input voltage corresponding to a positive value of the valley generates capacitive losses. However, activation of the MOSFET always occurs at the minimum voltage of the resonance and therefore the losses are minimized.

In practice, it is possible to estimate the total switching and capacitive losses by solving the integral of the switching frequency depending on sin(θ) on the half-line cycle.

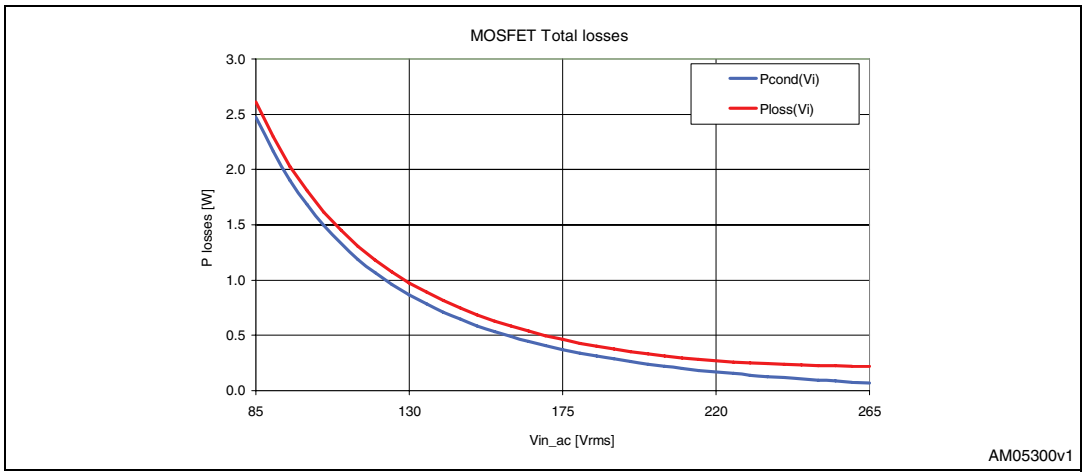
The total losses function of the input mains voltage is the sum of the three previous losses' functions (*Equation 26*, *Equation 28* and *Equation 30* respectively) multiplied by the MOSFET parameters.

Equation 33

$$P_{loss}(VAC) = R_{DS(on)} \cdot P'_{cond}(VAC) + \frac{t_{fall}^2}{C_d} \cdot P'_{sw}(VAC) + C_d \cdot P'_{cap}(VAC)$$

Figure 7 shows the trend of the total losses (derived from *Equation 33*) as a function of the input mains voltage for the selected MOSFET STF7NM50N. Capacitive losses are dominant at high mains voltages and are essentially caused by conduction losses at low and medium mains voltages.

Figure 7. Conduction losses and total losses in the STF7NM50N MOSFET for the L6564 TM PFC



From *Equation 33* and by using the data relevant to the selected MOSFET and calculating the losses at VAC_{min} and VAC_{max}, one can observe that the maximum total losses occur at VAC_{min}. From this number and the maximum ambient temperature *(12)*, the total maximum thermal resistance required to keep the junction temperature below 125 °C is:

Equation 34

$$R_{th} = \frac{125\ °C - T_{ambx}}{P_{loss}(VAC)} \qquad R_{th} = \frac{125\ °C - 50\ °C}{2.58\ W} = 29\frac{°C}{W}$$

If the result of *Equation 34* is lower than the junction-to-ambient thermal resistance given in the MOSFET datasheet for the selected device package, a heatsink must be used.

The STF7NM50N junction-to-ambient thermal resistance in free-air is 62 °C/W, therefore a heatsink is necessary.

3.3.6 Boost diode selection

Following a similar criterion to the one for the MOSFET, the output rectifier can also be selected. A minimum breakdown voltage of 1.2·(Vout + ΔV_{OVP}) and current rating higher than 3·Iout (*Equation 1*) can be chosen for a rough initial selection of the rectifier. The correct choice is then confirmed by the thermal calculation: if the diode junction temperature works within 125 °C, the device has been selected correctly, otherwise a bigger device must be selected.

For this 100 W application, we have selected a STTH2L06 (600 V, 2 A).

The current values of the rectifier AVG (*Equation 1*) and RMS (*Equation 8*), and the parameter Vth (rectifier threshold voltage) and R_d (dynamic resistance) given in the datasheet allow the rectifier losses to be calculated.

From the STTH2L06 datasheet the Vth is 0.89 V and R_d is 0.08 Ω

Equation 35

$$P_{diode} = V_{th} \cdot I_{out} + R_d \cdot ID^2_{rms} \qquad P_{diode} = 0.89\ V \cdot 0.25\ A + 0.08\ \Omega \cdot (0.72\ A)^2 = 0.26\ W$$

From *(12)* and *Equation 35*, the maximum thermal resistance to keep the junction temperature below 125 °C is:

Equation 36

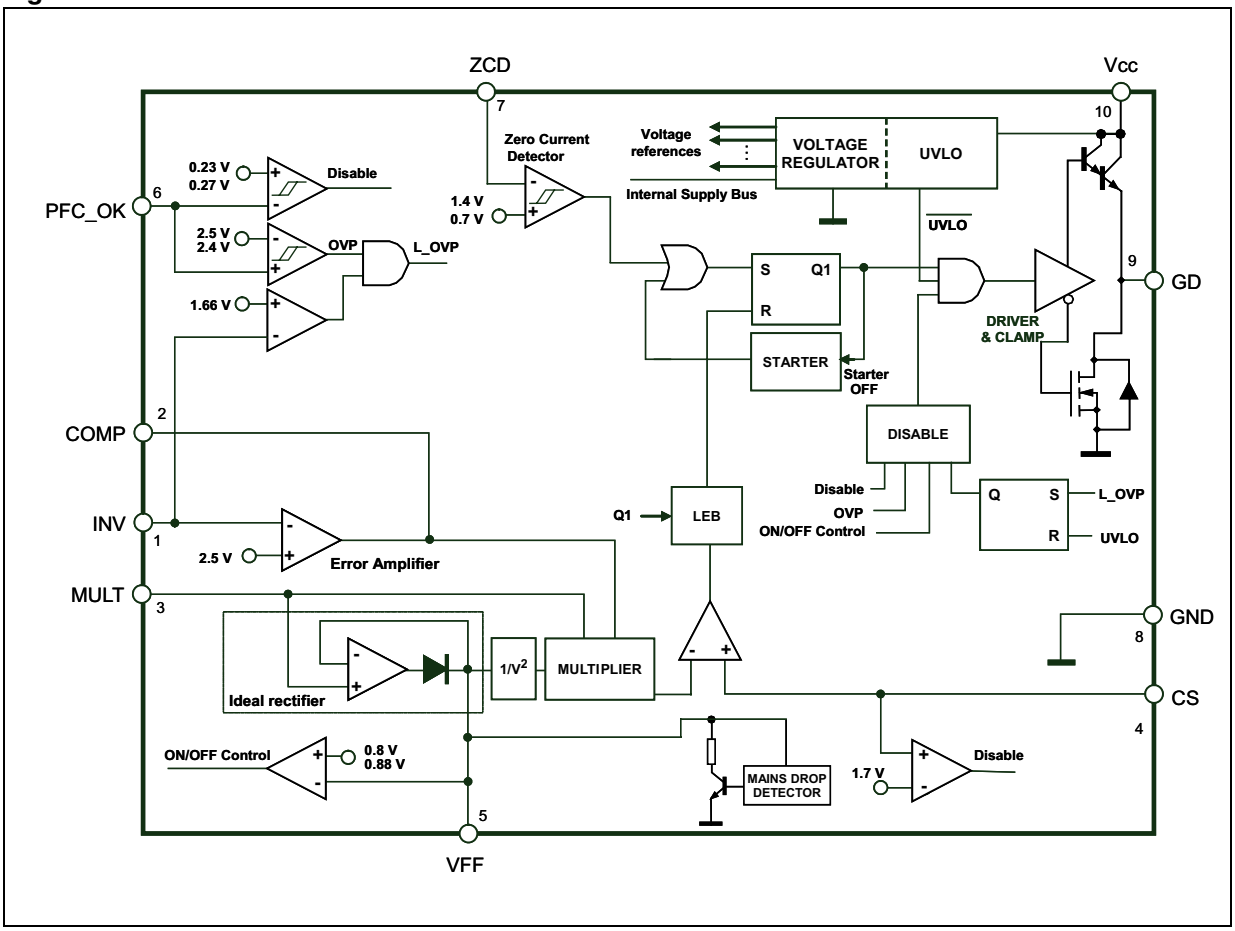
$$R_{th} = \frac{125\ °C - T_{ambx}}{P_{diode}} \qquad R_{th} = \frac{125\ °C - 50\ °C}{0.26\ W} = 284\frac{°C}{W}$$

Because the calculated R_{th} is higher than the STTH2L06 junction-to-ambient thermal resistance, a heatsink is not needed to properly dissipate the heat.

3.4 L6564 biasing circuitry

This section describes the biasing circuitry of the L6564. *Figure 8* represents the L6564's internal schematic. For more information on the device's internal functions, refer to the datasheet.

Figure 8. L6564 internal schematic



Pin 1 (INV): this pin is connected both to the inverting input of the E/A and to the OVP circuitry. A resistive divider has to be connected between the regulated output voltage of the boost and this pin. The internal reference on the E/A non-inverting input is 2.5 V (typ.). The PFC output voltage (Vout) is set at its nominal value by the resistor ratio of the feedback output divider. R_{outH} and R_{outL} can then be selected by considering the nominal output

voltage *(4)* and the desired output power dissipated on the output divider. Following is an example with a power dissipation of 50 mW.

Equation 37

$$R_{outH} = \frac{(V_{OUT} - 2.5V)^2}{50\ mW} \qquad R_{outH} = \frac{(400\ V - 2.5\ V)^2}{50\ mW} = 3.160\ M\Omega$$

By selecting a commercial value of R_{outH} equal to 3 MΩ, we get:

Equation 38

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5\ V} - 1 \qquad \frac{R_{outH}}{R_{outL}} = \frac{400\ V}{2.5\ V} - 1 = 159$$

Equation 39

$$R_{outL} = \frac{R_{outH}}{159} \qquad R_{outL} = \frac{3\ M\Omega}{159} = 18.8\ k\Omega$$

We have selected R_{outL} = 62 kΩ in parallel to 27 kΩ Note that for R_{outH} a resistor with a suitable voltage rating (>400 V) is needed, or else additional in-series resistors must be used.

Also note that the maximum value of the resistor divider is limited by the L6564's INV pin input bias current given in the datasheet. To guarantee correct output voltage regulation, the current flowing in the resistor divider must be significantly higher than the current flowing into the pin.

Pin 6 (PFC_OK - feedback failure protection): the PFC_OK pin is dedicated to monitoring the output voltage by a separate resistor divider. This divider is selected so that the voltage at the pin reaches 2.5 V (typ.) if the output voltage exceeds a preset value V_{OVP} *(7)*, usually larger than the maximum Vout that can be expected, and also including worst-case load/line transients. For a maximum output voltage V_{OVP} of 430 V and imposing a 50 µA current flowing into the divider, we obtain:

Equation 40

$$R_L = \frac{V_{REF_PFC_OK}}{I_{divider}} \qquad R_L = \frac{2.5\ V}{50\ \mu A} = 50\ k\Omega$$

By selecting a commercial value of 51 kΩ, we then get:

Equation 41

$$R_H = R_L \cdot \left(\frac{V_{OVP}}{V_{REF_PFC_OK}} - 1 \right) \qquad R_H = 51\ k\Omega \cdot \left(\frac{430\ V}{2.5\ V} - 1 \right) = 8.721\ M\Omega$$

By connecting in series two 3.3 MΩ and one 2.2 MΩ resistors, a total value of 8.8 MΩ is obtained.

Note that both feedback dividers connected to the L6564's pin #1 (INV) and pin #6 (PFC_OK) can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus, which needs to be significantly higher than the current biasing the error amplifier and PFC_OK comparator.

The OVP function described above can handle "normal" overvoltage conditions, that is, those resulting from an abrupt load/line change or occurring at start-up. If the overvoltage is generated by a feedback disconnection for instance, when one of the upper resistors of the output divider fails to open, an additional circuitry detects the voltage drop of pin INV. If the voltage on pin INV is lower than 1.66 V (typ.) and at same time the OVP is active, a feedback failure is assumed.

Thus, the activity of the gate driver is immediately stopped, the device is shut down, its quiescent consumption is reduced to less than 180 µA and the condition is latched for as long as the supply voltage of the IC remains above the UVLO threshold. To restart the system, it is necessary to recycle the input power so that the V_{CC} voltage of the L6564 goes below 6 V and that one of the PWM controllers goes below its UVLO threshold. Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also a failure of the protection itself. If either one of the PFC_OK dividers fails to short or open, or a PFC_OK pin is floating, the IC is shut down and the pre-regulator stopped. Moreover, the PFC_OK pin doubles its function as a not-latched IC disable: a voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart the IC, simply let the voltage at the pin go above 0.27 V.

Pin 2 (COMP): this pin is the output of the E/A that is fed into one of the two inputs of the multiplier. A feedback compensation network is placed between this pin and INV (pin #1). It has to be designed with a narrow bandwidth to prevent the system from rejecting the output voltage ripple (100 Hz) that would result in a high distortion of the input current waveform.

A simple way of defining the capacitance value is to set the bandwidth (BW) from 20 to 30 Hz. The compensation network can be a simple capacitor, providing a low-frequency pole as well as a high DC gain. A more complex network, typically a type-II CRC network providing two poles and a zero, is more suitable for constant power loads like a downstream converter.

If a single capacitor is used it can be dimensioned using the following formulas.

Equation 42

$$BW = \frac{1}{2\pi \cdot (R_{outH} // R_{outL}) \cdot C_{Compensation}}$$

Equation 43

$$C_{Compensation} = \frac{1}{2\pi \cdot (R_{outH} // R_{outL}) \cdot BW}$$

For a more complex compensation network calculation refer to [2] and [3] in *Chapter 6: References*.

For this 100 W TM PFC, a CRC network providing two poles and a zero has been implemented with the following values.

$$C_{compP} = 68\ nF \quad C_{compS} = 680\ nF \quad R_{compS} = 82\ k\Omega \qquad (14)$$

The relevant open-loop transfer function and its phase function are reported in *Figure 9* and *Figure 10*.

Figure 9. Open-loop transfer function bode plot

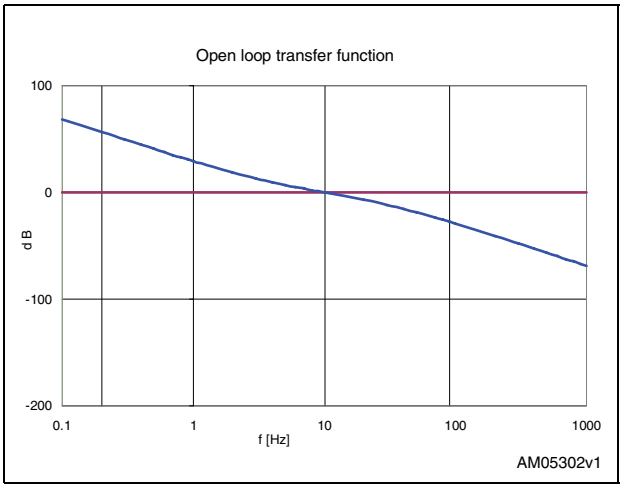
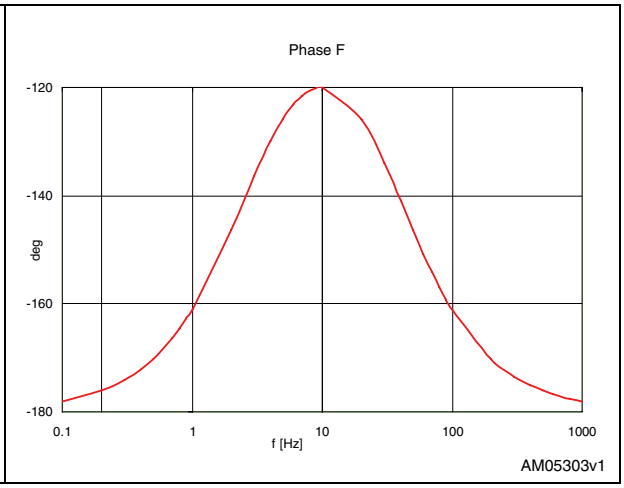


Figure 10. Phase



The two bode plot charts refer to the PFC operating at 265 Vac and full load. In these conditions, the crossover frequency is 11.55 Hz and the phase margin is 55 °C. The third harmonic distortion introduced by the E/A 100 Hz residual ripple is below 3%.

Pin 4 (CS): this pin is the inverting input of the current sense comparator. The L6564 receives the information on the instantaneous inductor current through this pin, provided by an external sense resistor (R_s) via an RC filter. As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The MOSFET stays in the off state until the PWM latch is set again by the ZCD signal. The pin is equipped with 150 ns leading-edge blanking to improve noise immunity.

For a 100 W PFC, the sense resistor value (R_s) can be calculated as follows.

Equation 44

$$R_s < \frac{Vcs_{min}}{IL_{pk}} \qquad R_s < \frac{1.0\ V}{3.38\ A} = 0.296\ \Omega$$

Where:

- ILpk is the maximum peak current in the inductor, calculated as shown in *Equation 4*.
- Vcsmin equals 1.0 V and is the minimum voltage admitted on the L6564's current sense (as per the datasheet).

Because the internal current sense clamping sets the maximum current that can flow in the inductor, the maximum peak of the inductor current is calculated considering the maximum voltage Vcsmax admitted on the L6564 (as per the datasheet).

Equation 45

$$IL_{pkx} = \frac{Vcs_{max}}{R_s} \qquad IL_{pkx} = \frac{1.16\ V}{0.27\ \Omega} = 4.30\ A$$

The calculated ILpkx is the value at which the boost inductor is not saturated and is used to calculate the inductor's number of turns and air gap length.

If the boost inductor gets saturated, a second comparison level at 1.7 V detects the abnormal current value and activates a safety procedure that temporarily stops the converter and limits the stress of the power components.

The power dissipated in R_s is given by:

Equation 46

$$P_s = R_s \cdot ISW_{rms}^2 \quad P_s = 0.27\ \Omega \cdot (1.18\ A)^2 = 0.37\ W$$

According to the results of *Equation 45* and *Equation 46*, two resistors of 0.47 Ω and 0.68 Ω, each with a power rating of 0.25 W, have been selected.

Pin 3 (MULT): this pin is the second multiplier input. It is connected through a resistive divider to the rectified mains to obtain a sinusoidal voltage reference. The multiplier can be described by the relationship:

Equation 47

$$V_{CS} = V_{CS_OFFSET} + k_m \cdot \frac{(V_{COMP} - 2.5\ V) \cdot V_{MULT}}{V_{FF}^2}$$

Where:

- V_{CS} (multiplier output) is the reference for the current sense (V_{CS_OFFSET} is its offset).
- k = 0.45 (typ.) is the multiplier gain.
- V_{COMP} is the voltage on pin #2 (E/A output).
- V_{MULT} is the voltage on pin #3.
- V_{FF} is the second input to the multiplier for $1/V^2$ function. It compensates the control loop gain dependence on the mains voltage. The voltage at this pin is a DC level equal to the peak voltage on the MULT pin (pin #3).

Figure 11. Multiplier characteristics for V_{FF} =1 V

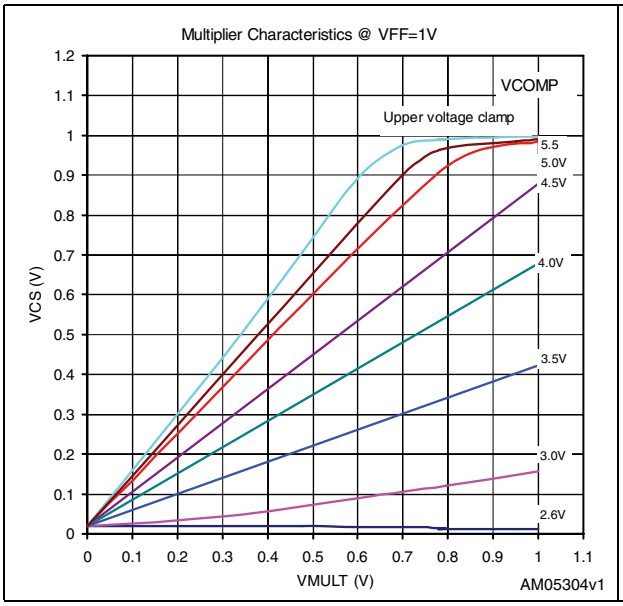


Figure 12. Multiplier characteristics for V_{FF} = 3 V

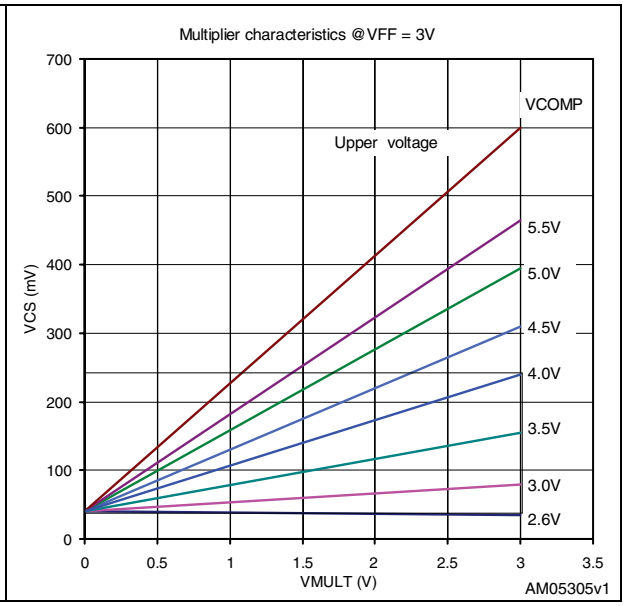


Figure 11 and *Figure 12* show the typical multiplier characteristics.

The linear operation of the multiplier is guaranteed within the range 0 to 3 V of V_{MULT} and the range 0 to 1.16 V (typ.) of Vcs, while the minimum guaranteed value of the maximum slope of the characteristics family (typ.) is given in *Equation 48*.

Equation 48

$$\frac{dV_{CS}}{dV_{MULT}} = 1.66\frac{V}{V}$$

The voltage on the MULT pin is also used to derive the information on the RMS mains voltage for the V_{FF} compensation. The multiplier divider should be calculated by taking into account the relation with the V_{FF} pin so that the description of the V_{FF} pin comes before the dimensioning formula.

Pin 5 (voltage feed-forward): the power-stage gain of the PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get fc = 20 Hz at 264 Vac means having an fc of about 4 Hz at 88 Vac, resulting in sluggish control dynamics. Additionally, the slow control loop causes large transient current flows during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when the sense resistor is selected to let the full load power pass under the minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power inputs at high lines, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

The voltage feed-forward can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop.

In this way, a change in the line voltage causes an inversely proportional change of the half sine amplitude at the amplifier's output (if the line voltage doubles, the amplitude of the multiplier output is halved and vice-versa), so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which significantly improves dynamic behavior at low lines and simplifies loop design.

Actually, with other PFCs embedding the voltage feed-forward function, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small, the voltage generated is affected by a considerable amount of ripple at twice the mains frequency, which causes distortion of the current reference (resulting in high THD and poor PF); if it is too large, there is a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off is required.

The L6564 realizes an innovative voltage feed-forward which, with a technique that makes use of just two external parts, overcomes this time constant trade-off issue whichever voltage change occurs on the mains, both surges and drops. A capacitor C_{FF} and a resistor R_{FF}, both connected from the pin V_{FF} (pin #5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on the MULT pin (pin #3). In this case, the following value has been selected.

$$C_{FF} = 1\,\mu F \quad R_{FF} = 1\,M\Omega \tag{15}$$

In this way, if a sudden rise occurs in the line voltage, C_{FF} is rapidly charged through the low impedance of the internal diode; if a drop occurs in the line voltage, an internal "mains drop" detector enables a low impedance switch that suddenly discharges C_{FF}, thus avoiding a long settling time before reaching the new voltage level. Consequently, an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the pre-regulator's output, like in systems with no feed-forward compensation. This pin is internally connected to a comparator in order to provide the brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (does not latch) the IC and brings its consumption to a considerably lower level. The IC restarts when the voltage at the pin goes above 0.88 V. This information has to be taken into account when the MULT divider is selected.

The procedure to properly set the operating point of the multiplier is described hereafter. First, the maximum peak value for VMULT, ($VMULT_{max}$) is selected. This value, which occurs at the maximum mains voltage, should be 3 V or nearly so in wide-range mains, and less in case of single mains. The sense resistor selected is R_s = 0.27 Ω as described in the pin #4 paragraph. According to the L6564 datasheet and the linearity setting of the pin, the maximum voltage accepted on the multiplier input is:

$$VMULT_{max} = 3\ V \tag{16}$$

From *(16)* the maximum required divider ratio is calculated as:

Equation 49

$$k_p = \frac{V_{MULT\,max}}{\sqrt{2}\cdot VAC_{max}} = \frac{3.00\ V}{\sqrt{2}\cdot 265 Vac} = 8\cdot 10^{-3}$$

Assuming a 60 µA current is flowing into the multiplier divider, the lower resistor value can be calculated as:

Equation 50

$$R_{multL} = \frac{V_{MULT\,max}}{60\ \mu A} = \frac{3.00\ V}{60\ \mu A} = 50\ k\Omega$$

A commercial value of 51 kΩ for the lower resistor has been selected. The upper resistor value can now be calculated as:

Equation 51

$$R_{multH} = \frac{1-k_p}{k_p} R_{multL} = \frac{1-8\cdot 10^{-3}}{8\cdot 10^{-3}} 51\,k\Omega = 6.319\,M\Omega$$

For this application, we have selected R_{multH} = 6.9 MΩ and R_{multL} = 51 kΩ. Note that for R_{multH} a resistor with a suitable voltage rating (>400 V) is needed, otherwise more in-series resistors must be used.

The voltage on the multiplier pin with the selected component values is re-calculated when the minimum line voltage is 0.93 V and the maximum line voltage is 2.74 V. The multiplier works correctly within its linear region.

Because the MULT divider also determines the mains input voltage at which the PFC starts and stops (brownout function), these values are calculated using the actual divider ratio.

Equation 52

$$V_{START} = \frac{0.88\ V}{\sqrt{2}} \cdot \frac{R_{multH} + R_{multL}}{R_{multL}} \qquad V_{START} = \frac{0.88\ V}{\sqrt{2}} \cdot \frac{6.9\ M\Omega + 51\ k\Omega}{51\ k\Omega} = 84.4\ V$$

As well as the stop voltage:

Equation 53

$$V_{STOP} = \frac{0.80\ V}{\sqrt{2}} \cdot \frac{R_{multH} + R_{multL}}{R_{multL}} \qquad V_{STOP} = \frac{0.80\ V}{\sqrt{2}} \cdot \frac{6.9\ M\Omega + 51\ k\Omega}{51\ k\Omega} = 77.1\ V$$

The start and stop PFC mains voltages are compatible with the input mains voltage range *(1)*.

In order to obtain the required start-up and shut-down voltage, a reiteration might be required, done by selecting the MULT resistors and checking the actual PFC start and stop mains voltages.

Pin 7 (ZCD): pin #7 is the input of the zero current detector circuit. In transition mode PFC, the ZCD pin is connected through a limiting resistor to the auxiliary winding of the boost inductor. The ZCD circuit is triggered by the negative-going edge: when the voltage on the pin falls below 0.7 V, it sets the PWM latch and thus the MOSFET is turned on. However, to do so, the circuit must first be armed: prior to falling below 0.7 V, the voltage on pin #7 must experience a positive-going edge that exceeds 1.4 V (due to the MOSFET's turn-off). The maximum main-to-auxiliary winding turn ratio (nmax) must ensure that the voltage delivered to the pin during the MOSFET's OFF time is sufficient to arm the ZCD circuit. A safe margin of 15% has been added.

Equation 54

$$nmax = \frac{n_{primary}}{n_{auxiliary}} = \frac{V_{out} - \sqrt{2} \cdot VAC_{max}}{1.4\ V \cdot 1.15} \qquad nmax = \frac{400\ V - \sqrt{2} \cdot 265 Vac}{1.4\ V \cdot 1.15} = 15.71$$

If the winding is also used to supply the IC, the above criteria may not be compatible with the V_{CC} voltage range. To solve this incompatibility, the self-supply network shown in *Figure 18* can be used.

The minimum value of the limiting resistor can be found considering the maximum voltage across the auxiliary winding with a selected turn ratio equal to 10 and assuming a 0.6 mA current through the pin.

Equation 55

$$R_1 = \frac{\frac{V_{out}}{n_{aux}} - V_{ZCDH}}{0.6\ mA} \qquad R_1 = \frac{\frac{400\ V}{10} - 5.7\ V}{0.6\ mA} = 57.16\ k\Omega$$

Equation 56

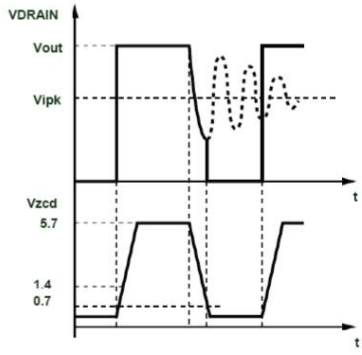
$$R_2 = \frac{\frac{\sqrt{2} \cdot VAC_{max}}{n_{aux}} - V_{ZCDL}}{0.6\ mA} \qquad R_2 = \frac{\frac{\sqrt{2} \cdot 265 Vac}{10} - 0\ V}{0.6\ mA} = 62.4\ k\Omega$$

V_{ZCDH} at 5.7 V and V_{ZCDL} at 0 V are the upper and lower ZCD clamp voltages of the L6564.

Considering the highest value of the two calculations, an RZCD equal to 68 kΩ has been selected as the limiting resistor.

The actual value can then be tuned by trying to make the activation of the MOSFET occur right on the valley of the drain voltage (which is resonating because the boost inductor has run out of energy – as shown in *Figure 13*).This minimizes the power dissipation at turn-on.

Figure 13. Optimum MOSFET activation



Pin 8 (GND): this pin acts as the current return for both the signal's internal circuitry and for the gate drive current. When layouting the printed circuit board, these two paths should run separately.

Pin 9 (GD): this pin is the output of the driver. It can drive an external MOSFET with a 600 mA source and a 800 mA sink capability.

The high-level voltage of this pin is clamped at about 12 V so as to avoid excessive gate voltages in case the pin is supplied with a high Vcc. To avoid undesired switch-ons of the external MOSFET because of some leakage current when the supply of the L6564 is below the UVLO threshold, an internal pull-down circuit holds the pin low. The circuit guarantees 1.1 V maximum on the pin (when Isink = 2 mA), with Vcc > VCC_ON. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET used for this purpose.

Pin 10 (Vcc): this pin is the supply of the device. It is externally connected to the start-up circuit (normally, one resistor is connected to the rectified mains) and to the self-supply circuit.

Whatever the configuration of the self-supply system, a capacitor must be connected between this pin and ground.

To start the L6564, the voltage must exceed the start-up threshold (12 V typ.). Below this value the device does not work and consumes less than 90 µA (typ.) from Vcc. This allows the use of high-value start-up resistors (in the hundred kΩ), which reduces power consumption and optimizes system efficiency at low loads, especially in wide-range mains applications.

When operating, the current consumption (of the device only, not of the gate drive) rises to a value that depends on the operating conditions but never exceeds 6 mA.

The device keeps on working as long as the supply voltage is over the UVLO threshold (13 V max). If the Vcc voltage exceeds 22.5 V, an internal Zener diode (rated at 20 mA) is activated in order to clamp the voltage. Remember that during normal operation, the internal

Zener does not have to clamp the voltage because the power consumption of the device increases considerably, as does its junction temperature. The suggested operating condition for safe operation of the device is below the minimum clamping voltage of the pin.

4 Design example using the L6564-TM PFC Excel spreadsheet

An Excel spreadsheet is provided to allow quick and easy design of a boost PFC pre-regulator using the STM L6564 controller, operating in transition mode. *Figure 14* shows the first sheet already filled with the input design data used in *Chapter 3*.

Figure 14. Excel spreadsheet design specification input table

Parameter	Name	Value	Unit [ ]
Mains Voltage Range	VacMin	90	VACrms
Mains Voltage Range	VacMax	265	VACrms
Min.Mains Frequency	fl	47	Hz
Regulated Output Voltage	Vout	400	Vdc
Rated Output Power	Pout	100	W
Max. Output Low Frequency Ripple	ΔVout	20	Vpk-pk
Holdup Capability	Thold	10	ms
Min. Output Voltage after Line drop	VoutMin	300	Vdc
Min. Switching Frequency:	fmin	40	kHz
Expected Efficiency	η	94	%
Expected Power Factor	PF	0.99	---
Maximum Ambient Temperature	Tambx	50	C

AM05336v1

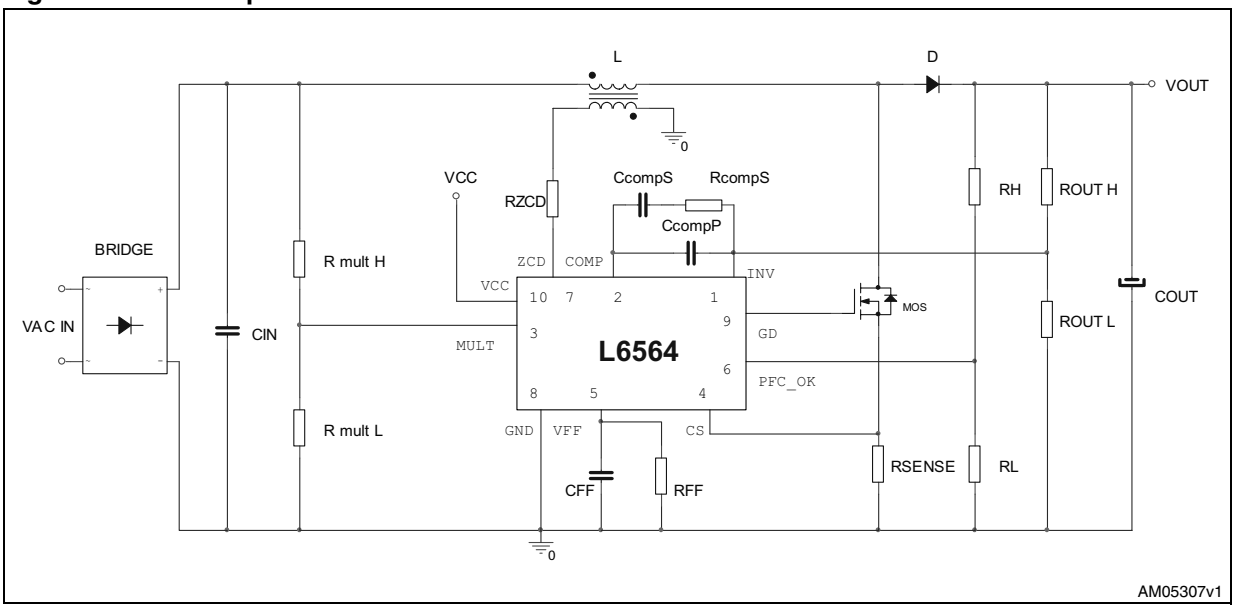
Figure 15. Other design data

Parameter	Name	Value	Unit [ ]
Maximum Magnetic Flux Density	Bx	0.25	T
Ripple Voltage Coefficient	r	0.15	---

AM05337v1

The tool can generate a complete parts list of the PFC schematic represented in *Figure 15*, including the power dissipation calculation of the main components.

Figure 16. Excel spreadsheet TM PFC schematic



The bill of material shown in *Figure 17* is automatically compiled by the Excel spreadsheet. It summarizes all the selected components as well as some salient data.

Figure 17. Excel spreadsheet BOM - 100 W TM PFC based on L6564

100W TM PFC BASED ON L6564
BILL OF MATERIAL

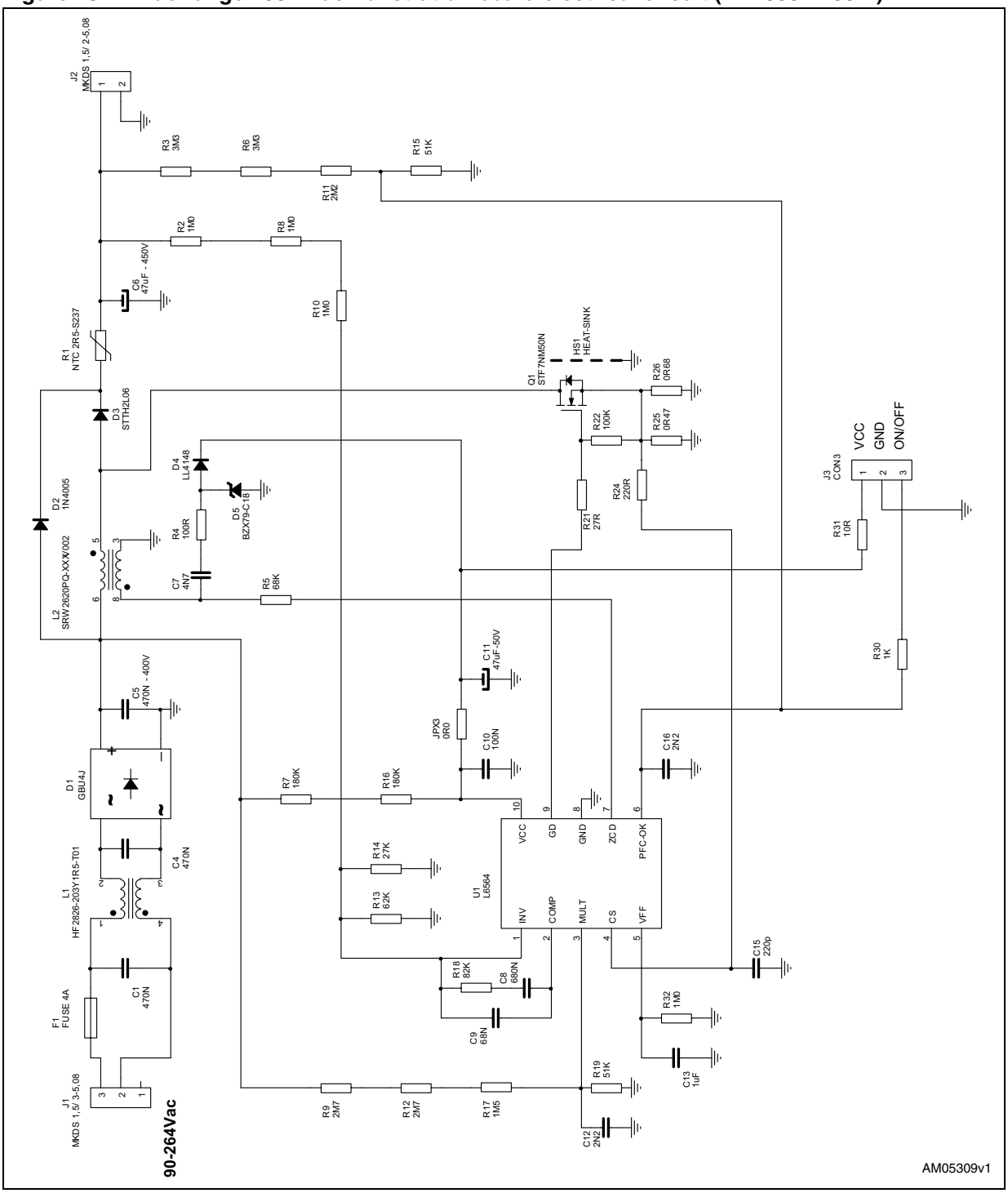
		Selected Value	Unit [ ]
BRIDGE RECTIFIER	*GBU4J*		
MOSFET P/N	*STF7NM50N*		
DIODE P/N	*STTH2L06*		
Inductor	*L*	*0.52*	*mH*
Max peak Inductor current	*Ilpkx*	*4.30*	*A*
Sense resistor	*Rsx*	*0.27*	Ω
Power dissipation	*Ps*	*0.37*	*W*
INPUT Capacitor	*Cin*	*0.47*	*¬F*
OUTPUT Capacitor	*Cout*	*47*	*¬F*
MULT Divider	*Rmult L*	*51*	*k*Ω
	Rmult H	*6900*	*k*Ω
ZCD Resistor	*Rzcd*	*68*	*k*Ω
Feedback Divider	*RoutH*	*3000*	*k*Ω
	RoutL	*18.8*	*k*Ω
Output divider for PFC_OK	*RH*	*51*	*k*Ω
	RL	*8800*	*k*Ω
Comp Network	*CcompP*	*68*	*nF*
	CcompS	*680*	*nF*
	RcompS	*82*	*k*Ω
Voltage Feedforward	*CFF*	*1000*	*nF*
	RFF	*1000*	*k*Ω
IC Controller	*L6564*		

AM05308v1

5 EVL6564-100W demonstration board

Figure 18 shows the schematic of a 100 W, wide-range TM PFC based on the L6564 device. It has been dimensioned using the Excel tool presented in *Chapter 4*.

Figure 18. Wide-range 100 W demonstration board electrical circuit (EVL6564-100W)



6 References

1. L6564 datasheet
2. “A systematic approach to frequency compensation of the voltage loop in boost PFC pre regulators”, abstract
3. AN1089
4. AN3022

7 Revision history

Table 1. Document revision history

Date	Revision	Changes
10-Feb-2010	1	Initial release.
07-May-2010	2	Modified: *Figure 10* and *15*
22-Oct-2010	3	Modified: *Section 3.4* and *Equation 40*
09-Feb-2011	4	Updated: *Figure 8*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com