AN-558

Introduction to Power MOSFETS and their Applications

Introduction

The Power MOSFETs that are available today perform the same function as Bipolar transistors except the former are voltage controlled in contrast to the current controlled Bipolar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown.

MOSFET Operation

An Understanding of the operation of MOSFETs can best be gleaned by the first considering the lateral N-channel MOSFET shown in Figure 1.

With no electrical bias applied to the gate G, no current can flow in either direction underneath the gate because there will always be a blocking PN junction. When the gate is forward biased with respect to the source S together with an applied drain-source voltage, as shown in Figure 2, the free hole carriers in the p-epitaxial layer are repelled away from the gate area creating a channel, which allows electrons to flow from the source to the drain. Note that since the holes have been repelled from the gate channel, the electrons are the “majority carriers” by default. This mode of operation is called “enhancement” but is easier to think of enhancement mode of operation as the device being “normally off”, i.e., the switch blocks the current until it receives a signal to turn on. The opposite is depletion mode, which is normally “on” device.

The advantages of the lateral MOSFET are:

1. Low gate signal power requirement. No gate current can flow into the gate after the small gate oxide capacitance has been charged.
2. Fast switching speeds because electrons can start to flow from drain to source as soon as the channel opens. The channel depth is proportional to the gate voltage and pinches closed as soon as the gate voltage is removed, so there is no storage time effect as occurs in transistors.

The major disadvantages are:

1. High resistance channels. In normal operation, the source is electrically connected to the substrate. With no gate bias, the depletion region extends out from the N+ drain in a pseudo hemispherical shape. The channel length L cannot be made shorter than the minimum depletion width required to support the rated voltage of the device.
2. Channel resistance may be decreased by creating wider channels but this is costly since it uses up valuable silicon real estate. It also slows down the switching speed of the device by increasing its gate capacitance.

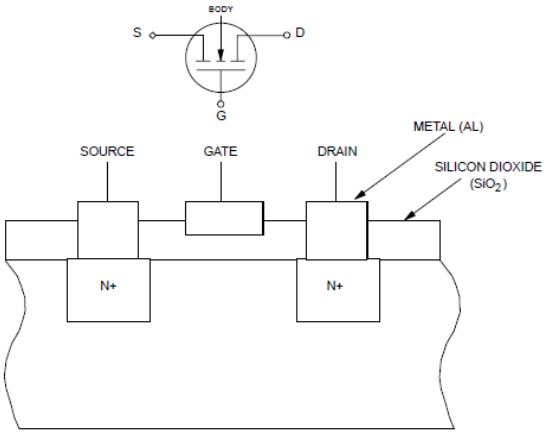

Figure 1. Lateral N-Channel MOSFET Cross-Section

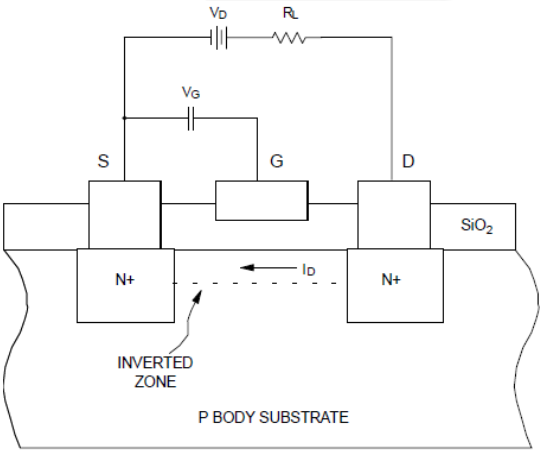

Figure 2. Lateral MOSFET Transistor Biased for Forward Current Conduction

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Enter Vertical MOSFETs!

The Power MOSFET structure (also known as DMOS) is shown Figure 3.

The current path is created by inverting the p-layer underneath the gate by the identical method in the lateral MOSFETs. Source current flows underneath this gate area and then vertically through the drain, spreading out as it flows down. A typical MOSFET consists of many thousands of N+ sources conducting in parallel. This vertical geometry makes possible lower on-state resistances ($R_{DS(ON)}$) for the same blocking voltage and faster switching than the lateral MOSFETs.

There are many vertical construction designs possible, e.g., V-groove and U-groove, and many source geometries, e.g. squares, triangles, hexagons, etc. The many considerations that determine the source geometry are $R_{DS(ON)}$, input capacitance, switching times and transconductance.

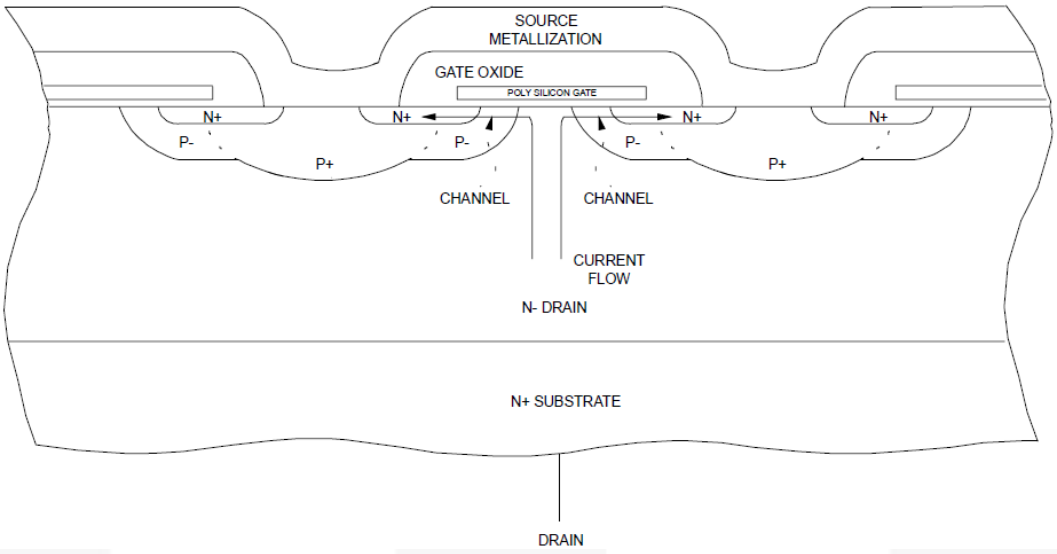

Figure 3. Vertical DMOS Cross-Sectional

Parasitic Diode

Early versions of MOSFETs were susceptible to voltage breakdown due to voltage transients and also had a tendency to turn on under high rates of rise of drain-to-source voltage (dV/dt). Both resulted in catastrophic failures. The dV/dt turn-on was due to the inherent parasitic NPN transistor incorporated within the MOSFET, shown schematically in Figure 4. Current flow needed to charge up junction capacitance C_{DG} acts like base current to turn on the parasitic NPN.

The parasitic NPN action is suppressed by shorting the N+ source to the P+ body using the source metallization. This now creates an inherent PN diode anti-parallel to the MOSFET transistor Figure 5. Because of its extensive junction area, the current ratings and thermal resistance of this diode exhibit a very long reverse recovery time and large reverse recovery current due to the long minority carrier lifetimes in the N-drain layer, which precludes the use of these diodes except for very low frequency applications. e.g., motor control circuit shown in Figure 6. However in high frequency applications, the parasitic diode must be paralleled externally by an ultra-fast rectifier to ensure that the parasitic diode does not turn on. Allowing it to turn will substantially increase the device power dissipation due to the reverse recovery losses within the diode and also leads to higher voltage transients due to the larger reverse recovery current.

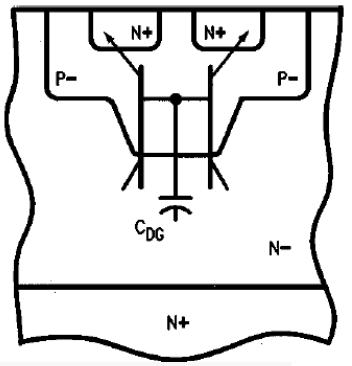

Figure 4. DMOS Construction Showing Location of the Parasitic NPN Transistor

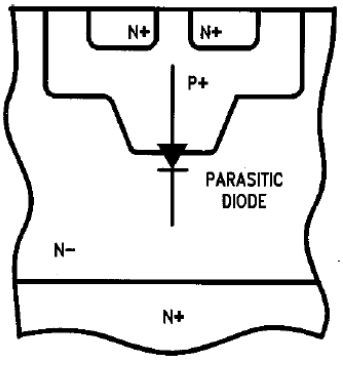

Figure 5. Parasitic Diode

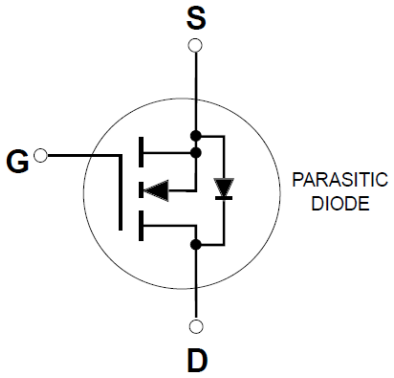

Figure 6. Circuit Symbol

Controlling the MOSFET

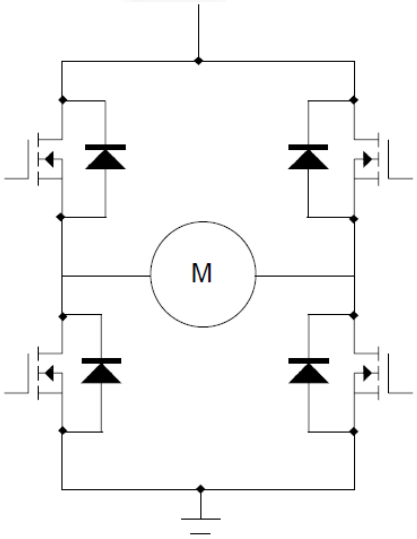

Figure 7. Full-Wave Motor Control Circuit

A major advantage of the Power MOSFET is its very fast switching speeds. The drain current is strictly proportional to gate voltage so that the theoretically perfect device could switch in 50 ps – 200 ps, the time it takes the carriers to flow from source to drain. Since the MOSFET is a majority carrier device, a second reason why it can outperform the junction transistor is that its turn-off is not delayed by minority carrier storage time in the base. A MOSFET begins to turn off as soon as its gate voltage drops down to its threshold voltage.

Switching Behavior

Figure 8 illustrates a simplified model for the parasitic capacitances of a Power MOSFET and switching voltage waveforms with a resistive load. There are several different phenomena occurring during turn-on.

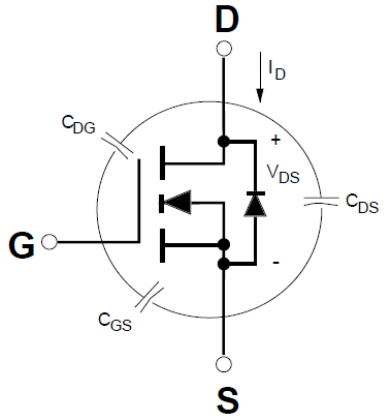

Figure 8. MOSFET Capacitance Model for Power MOSFET

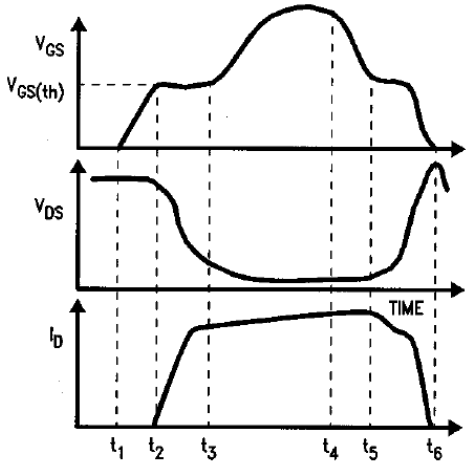

Figure 9. Switching Waveforms for Resistive Load

Time Interval t1<t<t2:

The initial turn-on delay time $t_{d(ON)}$ is due to the length of time it takes V_{GS} to rise exponentially to the threshold voltage $V_{GS(TH)}$. From Figure 8 and Figure 9 the time constant can be seen to be R_S x C_{GS}.

Typical turn-on delay approximation is:

$$t_{D(ON)} = -R_S \times C_S \times 1n\left(1 - \frac{V_{GS(TH)}}{V_{PK}}\right) \quad (1)$$

Note that since the signal source impedance appears in the td equation, it is very important to pay attention to the test conditions used in measuring switching times.

Physically one can only measure input capacitance C_{iss}, which consists of C_{GS} in parallel with C_{DG}. Even though C_{GS}>>C_{DG}, the later capacitance undergoes a much larger voltage excursion so its effect on switching time cannot be neglected.

Plots of C_{iss}, C_{oss}, and C_{rss} for the Fairchild Semiconductor Supersot™ NDS351N are shown in Figure 10 below. The charging and discharging of CDG is analogous to the "Miller" effect that was first discovered with electron tubes and dominates the next switching interval.

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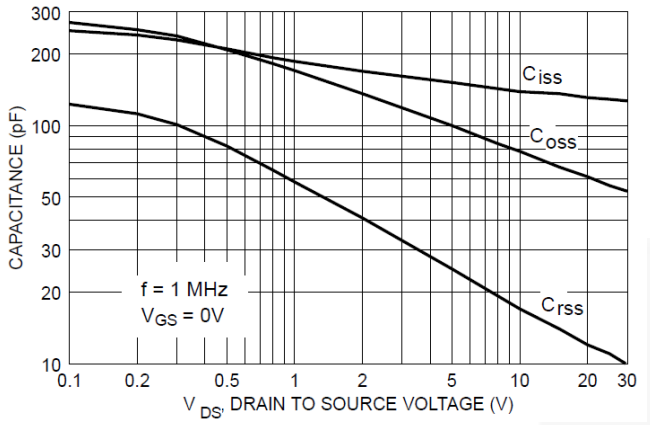

Figure 10. Typical Capacitance of NDS351N

Time Interval t2<t<t3:

Since V_{GS} has now achieved the threshold value, the MOSFET begins to draw increasing load current and V_{DS} decreases. C_{DG} must not only discharge but its capacitance value also increases since it is inversely proportional to V_{DS}, namely:

$$t_{DG} = \frac{C_{DG}(O)}{V_{DG}^{n}} \qquad (2)$$

Unless the gate driver can quickly supply the current required to discharged C_{DG}, voltage fall will be slowed with increases in turn-on time.

Time Interval t3<t<t4:

The MOSFET is now on so the gate voltage can rise to the overdrive level.

Turn-off Interval t4<t<t6:

Turn-off occurs in reverse order. V_{GS} must drop back close to the threshold value before $R_{DS(ON)}$ will start to increase. As V_{DS} starts to rise, the Miller effect due to C_{DG} re-occurs and impedes the rise of V_{DS} as C_{DG} recharges to V_{CC}.

Specific gate drive circuits for different applications are discussed and illustrated later in this paper.

MOSFET Characterization

The output characteristics (I_D vs. V_{DS}) of the Fairchild Semiconductor Supersot™ NDS351N are illustrated in Figure 11 and Figure 12. The two distinct regions of operation in Figure 11 have been labeled "linear" and "saturated". To understand the difference, recall that the actual current path in a MOSFET is horizontal through the channel created under the gate oxide and then vertical through the drain. In the linear region of operation, the voltage across the MOSFET channel is not sufficient for the carriers to reach their maximum current density. The static $R_{DS(ON)}$, defined simply as V_{DS}/I_{DS}, is a constant.

As V_{DS} is increased, the carriers reach their maximum drift velocity and the current amplitude cannot increase. Since the device is behaving like a current generator, it is said to have high output impedance. This is the so-called "saturation" regions. One should also note that in comparing MOSFET operation to Bipolar transistor, the linear and saturated regions are just the opposite to the MOSFET. The equal spacing between the output I_D curves for constant step in V_{GS} indicates that the transfer characteristics in Figure 12 will be linear in the saturated region.

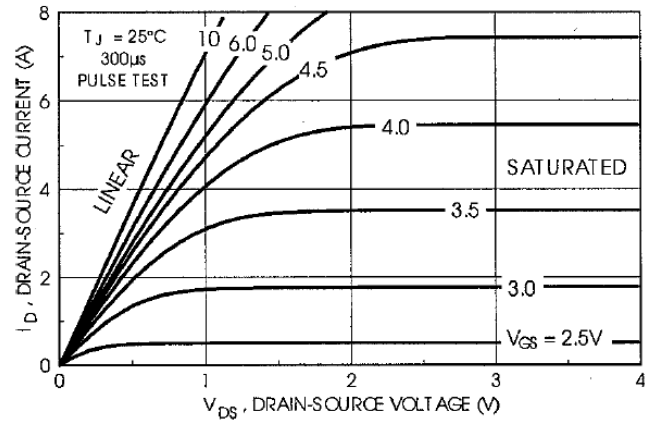

Figure 11. NDS351N Output Characteristics

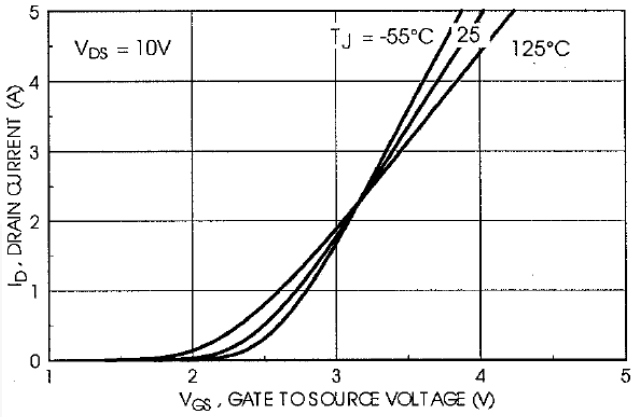

Figure 12. NDS351N Transfer Characteristics

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Importance of Threshold Voltage

Threshold voltage $V_{GS(th)}$ is the minimum gate voltage that initiates drain current flow. $V_{GS(th)}$ can be easily measured on a Tektronix 576 curve tracer by connecting the gate to the drain and recording the required drain voltage for a specified drain current, typically 250 µA. $V_{GS(th)}$ in Figure 12 is 1.6 V. While a high value of $V_{GS(th)}$, can apparently lengthen turn-on delay time, a low value for Power MOSFET is undesirable for the following reasons:

1. $V_{GS(th)}$ decreases with increased temperature.
2. The high gate impedance of a MOSFET makes it susceptible to spurious turn-on due to gate noise.
3. One of the more common modes of failure is gate-oxide voltage punch-through. Low $V_{GS(th)}$ requires thinner oxides, which lowers the gate oxide voltage rating.

Power MOSFET Thermal Model

Like all other power semiconductor devices, MOSFETs operate at elevated junction temperature. It is important to observe their thermal limitations in order to achieve acceptable performance and reliability. Specification sheets contain information on maximum junction temperature ($T_{J(max)}$), safe operating areas, current ratings and electrical characteristics as a function of T_J where appropriate.

However, since it is still not possible to cover all contingencies, it is still important that the designer perform some junction calculations to ensure that the device operates within specifications.

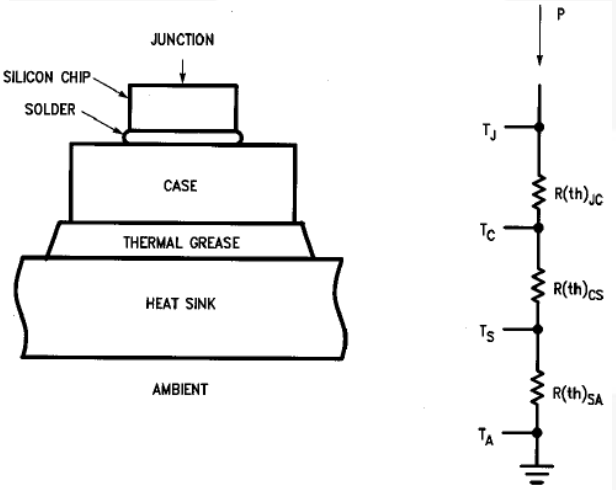

Figure 13. MOSFET Steady-State Thermal Resistance Model

Figure 13 shows an elementary, steady-state, thermal model for any power semiconductor and the electrical analogue. The heat generated at the junction flows through the silicon pellet to the case or tab and then to the heat sink. The junction temperature rise above the surrounding environment is directly proportional to this heat flow and the junction-to-ambient thermal resistance.

The following equation defined the steady-state thermal resistance $R_{\theta JA}$ between device junction to ambient:

$$R_{\theta JA} = \frac{T_J - T_A}{P} \quad (3)$$

where:

T_J = average temperature at the device junction (°C)

T_A = average temperature at ambient (°C)

P = average heat flow in watts (W).

Note that for thermal resistance to be meaningful, two temperature reference points must be specified. Units for $R_{\Theta JA}$ are °C/W.

The thermal model shows symbolically the locations for the reference points of junction temperature, case temperature, sink temperature and ambient temperature. These temperature reference define the following thermal resistances:

- $R_{\theta JC}$: Junction-to-Case thermal resistance.
- $R_{\theta CS}$: Case-to-Sink thermal resistance.
- $R_{\theta SA}$: Sink-to-Ambient thermal resistance.

Since the thermal resistances are in series:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (4)$$

The design and manufacture of the device determines $R_{\theta JC}$ so that while $R_{\theta JC}$ will vary somewhat from device to device, it is the SOLE RESPONSIBILITY of the manufacturer to guarantee a maximum value for $R_{\theta JC}$. Both the user and manufacturer must cooperate in keeping $R_{\theta CS}$ to an acceptable maximum. Finally, the user has sole responsibility for the external heat sinking.

By inspection of Figure 13 one can write an expression for T_J:

$$T_J = T_A + P \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \quad (5)$$

While this appears to be a very simple formula, the major problem using it is due to the fact that the power dissipated by the MOSFET depends upon T_J. Consequently one must use either an iterative or graphical solution to find the maximum $R_{\theta SA}$ to ensure stability. But an explanation of transient thermal resistance is in order to handle the case of pulsed applications.

Use of steady-state thermal resistance is not satisfactory for finding peak junction temperatures for pulsed applications. Plugging in the peak power value results in over estimating the actual junction temperature while using the average power value underestimates the peak junction temperature at the end of the power pulse. The reason for the discrepancy lies in the thermal capacity of the semiconductor and its housing, i.e., its ability to store heat and to cool down before the next pulse.

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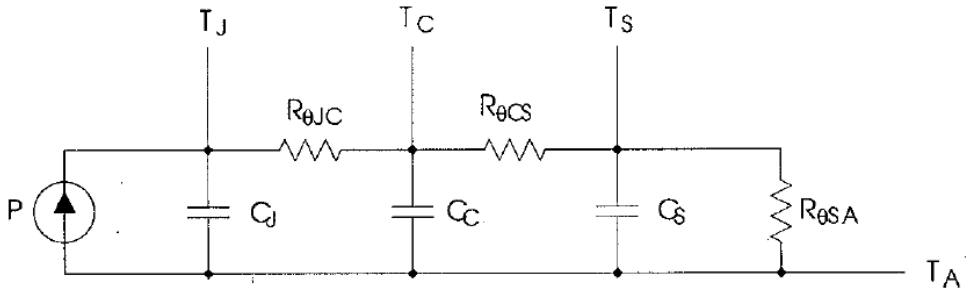

Figure 14. Transient Thermal Resistance Model

The modified thermal model for the MOSFET is shown in Figure 14. The normally distributed thermal capacitances have been lumped into single capacitors labeled C_J, C_C, and C_S. This simplification assumes current is evenly distributed across the silicon chip and that the only significant power losses occur in the junction. When a step pulse of heating power, P, is introduced at the junction, Figure 15 shows that T_J will rise at an exponential rate to some steady state value dependent upon the response of the thermal network. When the power input is terminated at time t2, T_J will decrease along the curve indicated by Tcool in Figure 15 back to its initial value. Transient thermal resistance at time t is thus defined as:

$$Z_{\theta JC} = \frac{\Delta T_{JC}(t)}{P} \quad (6)$$

The transient thermal resistance curve approaches the steady-state value at long times and the slope of the curve for short times is inversely proportional to C_J. In order to use this curve with confidence, it must represent the highest values $Z_{\Theta JC}$ for each time interval that can be expected from the manufacturing distribution of the products.

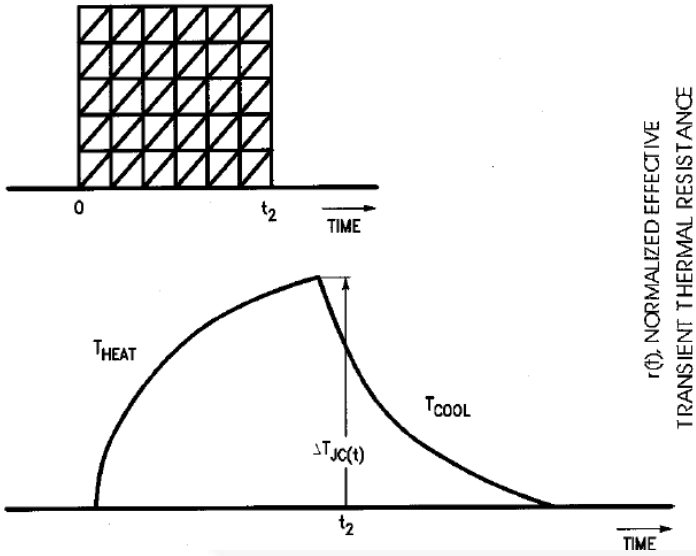

Figure 15. Junction Temperature Response to a Step Pulse of Heating Power

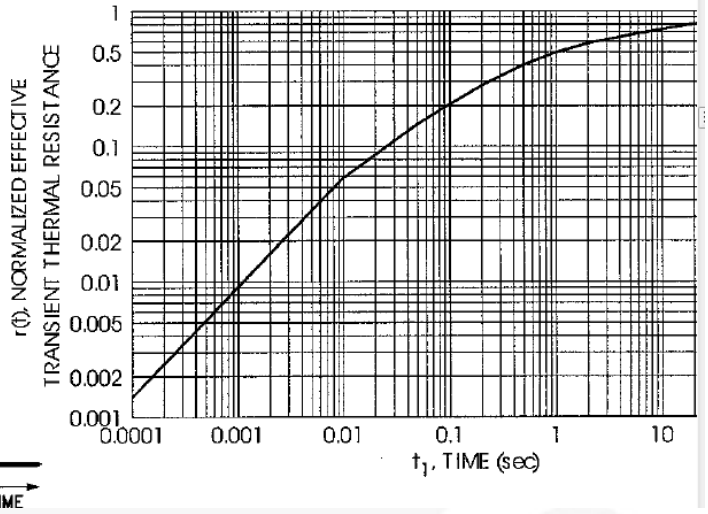

Figure 16. Transient Thermal Resistance Curve for NDS351N

While predicting T_J in response to a series of power pulses becomes very complex, superposition of power pulses offers a rigorous numerical method of using the transient thermal resistance curve to secure a solution. Superposition tests the response of a network to any input function by replacing the input with an equivalent series of superimposed positive and negative step functions. Each step function must start from zero and continue to the time for which T_J is to be computed. For example, Figure 17 through Figure 20 illustrates a typical train of heating pulses.

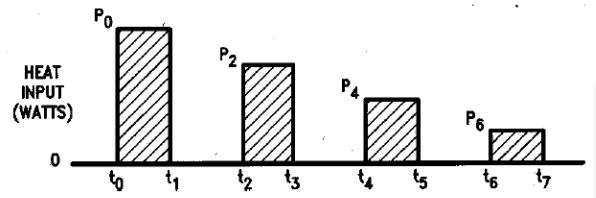

Figure 17. Heat Input

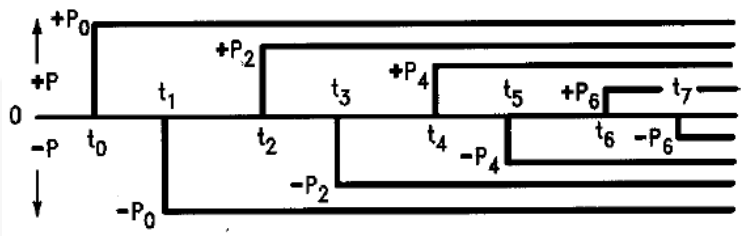

Figure 18. Equivalent Heat Input by Super-position of Power Pulses

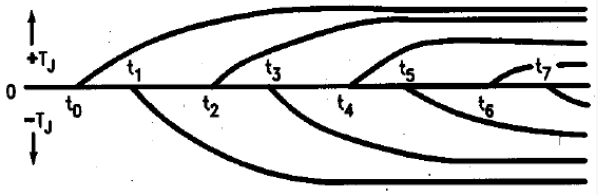

Figure 19. Junction Temperature Response to Individual Power Pulse

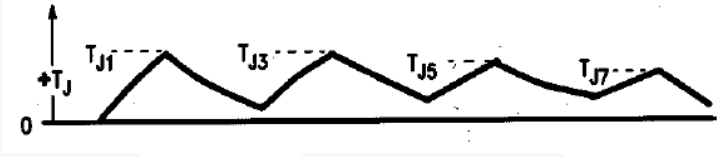

Figure 20. Use of Super-position to Determine Peak T_J

T_J at time is given by:

$$T_J(t) = T_J(O) + \Sigma\, P_i \times \left[Z_{\theta JC}(t_n - t_i) - Z_{\theta JC}\,(t_n + t_i + 1)\right] \quad (7)$$

The typical use condition is to compute the peak junction temperature at thermal equilibrium for a train of equal amplitude power pulses as shown in Figure 21 and Figure 22.

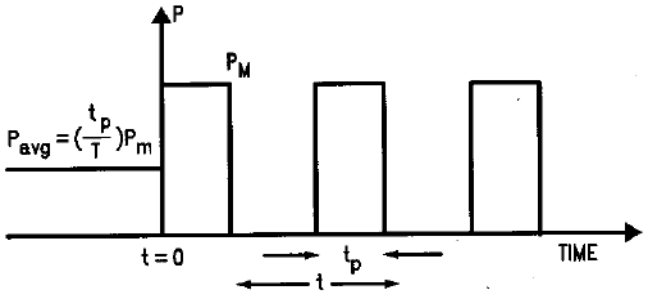

Figure 21. Train of Power Pulses

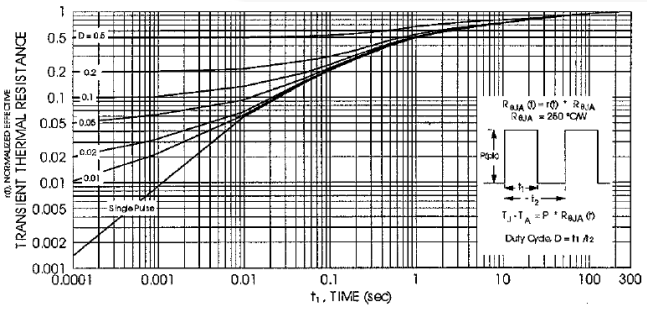

Figure 22. Normalized r(t) for NDS351N

To further simplify this calculation, the bracketed expression in equation (7) has been plotted for all Fairchild Semiconductor Power MOSFETs, as exemplified by the plot of $Z_{\Theta JC}$ in Figure 22. From this curve, one can readily calculate T_J if one knows PM. $Z_{\theta JC}$ and T_C using the expression:

$$T_J = T_C + P_M \times Z_{\theta JC} \quad (8)$$

Example: Compute the maximum junction temperature for a train of 1 W, 10 ms wide heating pulses repeated every 100 ms. Assume a case temperature of 55°C.

Duty factor=0.1

From Figure 22: $Z_{\theta JC}$=0.14*250°C/W=35°C/W

Substituting into Equation (7): $T_{J(max)}$=55+1*35=90°C

Safe Operating Area

The Power MOSFET is not subjected to forward or reverse bias second breakdown, which can easily occur in transistors. Second breakdown is a potentially catastrophic condition in transistors caused by thermal hot spots in the silicon as the transistor turns on or off. However in the MOSFET, the carriers travel through the device much as if it were a bulk semiconductor, which exhibits positive temperature coefficient**.** If current attempts to self-constrict to a localized area, the increasing temperature of the spot will raise the spot resistance due to positive temperature coefficient of the bulk silicon. The ensuing higher voltage drop will tend to redistribute the current away from the hot spot. Figure 23 shows the safe operating area of the Fairchild Semiconductor Supersot™ NDS351N device.

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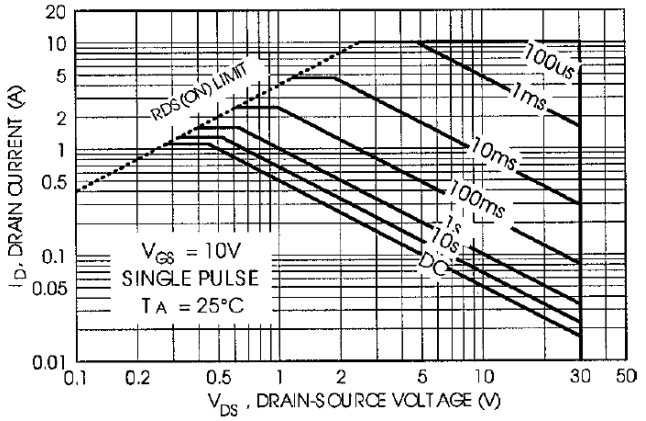

Figure 23. Safe Operating Area of NDS351N

Note that the safe area boundaries are only thermally limited and exhibit no derating for second breakdown. This shows that while the MOSFET transistor is very rugged, it may still be destroyed thermally by forcing it to dissipate too much power.

On-Resistance $R_{DS(ON)}$

The on-resistance of a Power MOSFET is a very important parameter because it determines how much current the device can carry for low to medium frequency (less than 200 kHz) applications. After being turned on, the on-state is defined simply as its on-state voltage divided by on-state current. When conducting current as a switch, the conduction losses P are:

$$P_C = I^2_{D(RMS)} \times R_{DS(ON)} \quad (9)$$

To minimize $R_{DS(ON)}$, the applied gate signal should be large enough to maintain operation in the linear or ohmic region as shown in Figure 11. Fairchild Semiconductor SUPERSOT^{TM}-3 NDS351N will conduct its rated current for V_{GS}=4.5 V, which is also the value used to generate the curves of $R_{DS(ON)}$ vs. I_D and T_J that are shown in Figure 24 for the Fairchild Semiconductor Supersot NDS351N. Since $R_{DS(ON)}$ is a function of T_J, Figure 24 plots this parameter at varies junction temperatures. Note that as the drain current rises, $R_{DS(on)}$ increases once I_D exceeds the rated current value. Because the MOSFET is a majority carrier device, the component of $R_{DS(ON)}$ due to the bulk resistance of the N- silicon in the drain region increases with temperature as well. While this must be taken into account to avoid thermal runaway, it does facilitate parallel operation of MOSFETs. Any imbalance between MOSFETs does not result in current hogging because the device with the most current heat up and ensuing higher on-voltage will divert some current to the other devices in parallel.

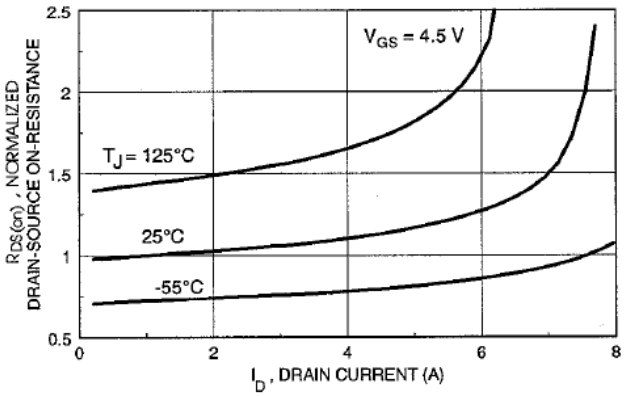

Figure 24. $R_{DS(ON)}$ of NDS351N

Transconductance

Since MOSFETs are voltage controlled, it has become necessary to resurrect the term transconductance g_{FS}, commonly used in the past with electron tubes. Referring to Figure 11, g_{FS} equals to the change in drain current divided by the change in gate voltage for a constant drain voltage. Mathematically:

$$g_{fs}(Siemens) = \frac{dV_D(A)}{dV_{GS}(V)} \quad (10)$$

Transconductance varies with operating conditions, starting at 0 for $V_{GS}<V_{GS(th)}$ and peaking at a finite value when the device is fully saturated. It is very small in the ohmic region because the device cannot conduct any more current. Transconductance is useful in designing linear amplifiers and does not have any significance in switching power supplies.

Gate Drive Circuits for Power MOSFETs

The drive circuit for a Power MOSFET will affect its switching behavior and its power dissipation. Consequently the type of drive circuitry depends upon the application. If on-state power losses due to $R_{DS(ON)}$, will predominate, there is little point in designing a costly drive circuit. This power dissipation is relatively independent of gate drive as long as the gate-source voltage exceeds the threshold voltage by several volts and an elaborate drive circuit to decrease switching times will only create additional EMI and voltage ringing. In contrast, the drive circuit for a device switching at 200 KHz or more will affect the power dissipation since switching losses are a significant part of the total power dissipation.

Compare to a junction transistor, the switching losses in a MOSFET can be made much smaller but these losses must still be taken into consideration. Examples of several typical loads along with the idealized switching waveforms and expressions for power dissipation are given in Figure 25 to Figure 27

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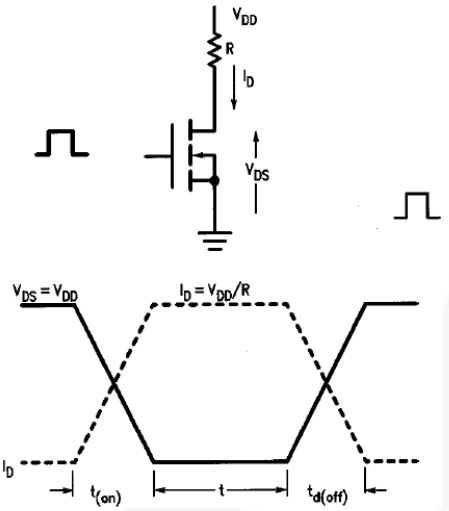

Figure 25. Resistive Load Switching Waveforms

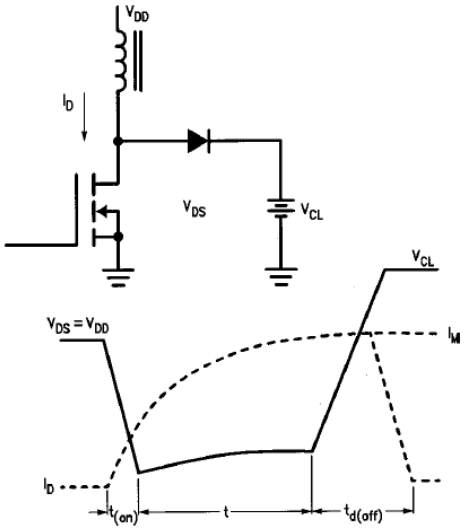

Figure 26. Clamped Inductive Load Switching Waveforms

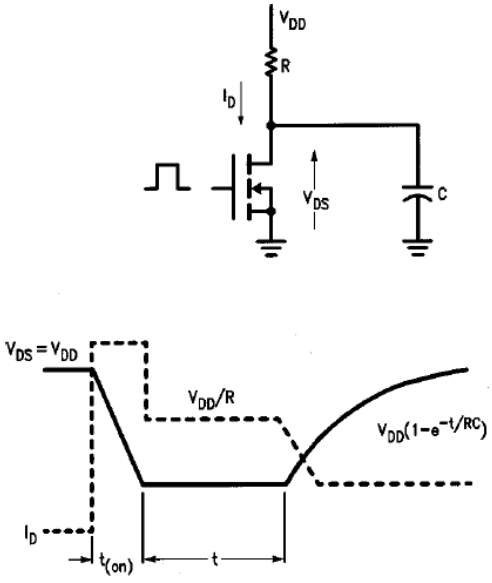

Figure 27. Capacitive Load Switching Waveforms

Their power losses can be calculated from the general expression:

$$P_D = \left(\frac{1}{t}\int I_D(t) \times V_{DS}(t)dt\right) \times f_S \quad (11)$$

where f_S =Switching frequency.

For the idealized waveforms shown in the figures, the integration can be approximated by the calculating areas of triangles:

Resistive Loads:

$$P_D = \frac{V_{DD}^2}{R}\left[\frac{t_{(ON)} + t_{OFF}}{6} - R_{DS(ON)} \times \mathrm{T}\right] \times f_S \quad (12)$$

Inductive Load:

$$P_D = \frac{V_{CL} \times f_m \times t_{OFF} \times f_S}{2} + P_C \quad (13)$$

where PC = conduction loss during period T.

Capacitive Load:

$$P_D = \left(\frac{C \times V_{DD}^2}{2} + \frac{V_{DD}^2 \times R_{DS(ON)}}{R^2} \times T\right) \times f_S \quad (14)$$

Gate losses and blocking losses can usually be neglected. Using these equations, circuit designer is able to estimate the required heat sink. A final heat run in a controlled temperature environment is necessary to ensure thermal stability.

Since a MOSFET is essentially voltage controlled, the only gate current required is that necessary to charge the input capacitance Ciss. In contrast to a 10 A transistor, which may require a base current of 2 A to ensure saturation, a Power MOSFET can be driven directly by CMOS or open-collector TTL logic circuit similar to that in Figure 28.

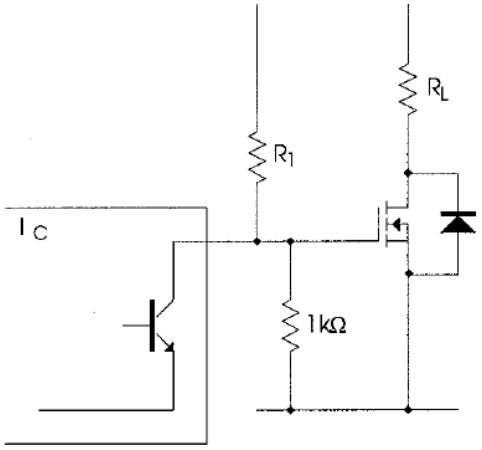

Figure 28. Open Collector TTL Drive Circuit

Turn-on speed depends upon the selection of resistor R1, whose minimum value will be determined by the current sinking rating of the IC. It is essential that an open collector TTL buffer be used since the voltage applied to the gate must exceed the MOSFET threshold voltage. CMOS devices can be used to drive the power device directly since they are capable of operating 15 V supplies.

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Interface ICs, originally intended for other applications, can be used to drive the Power MOSFETs, as shown below in Figure 29.

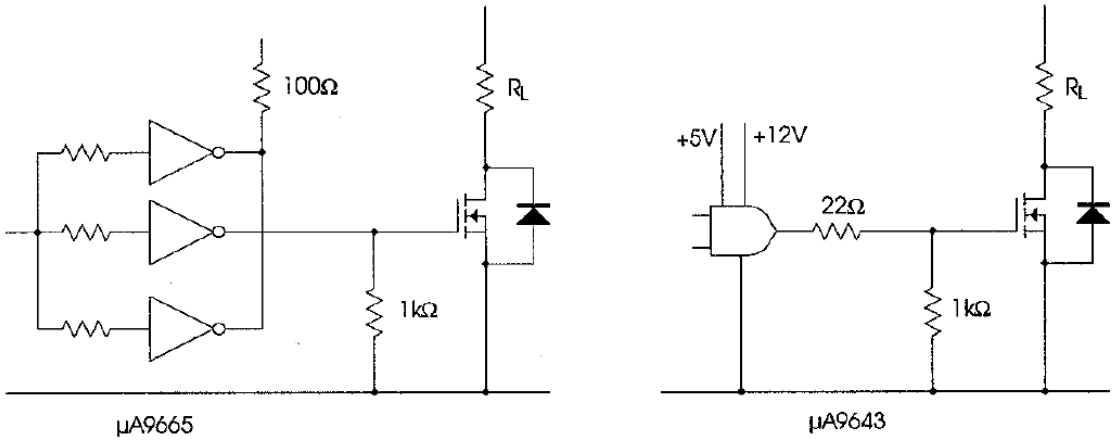

Figure 29. Interface ICs Used to Drive Power MOSFETs

Most frequently, switching power supply applications employ a pulse width modulator IC with an NPN transistor output stage. This output transistor is ON when the MOSFET should be ON, hence the type of drive used with open-collector TTL devices cannot be used. Figure 30 and Figure 31 give examples of typical drive circuits used with PWM ICs.

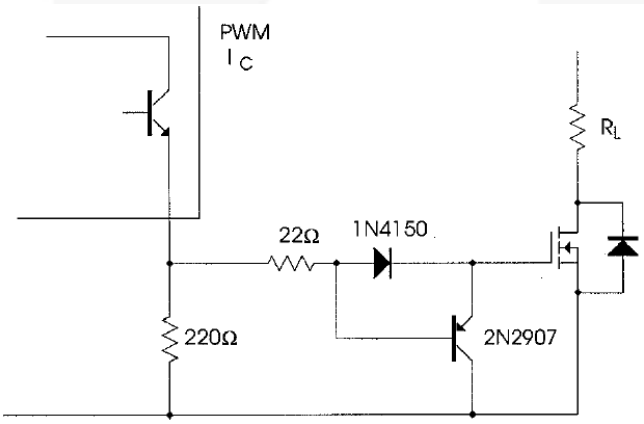

Figure 30. Circuit for PWM IC Driving MOSFET the PNP Transistor Speeds Up Turn-Off

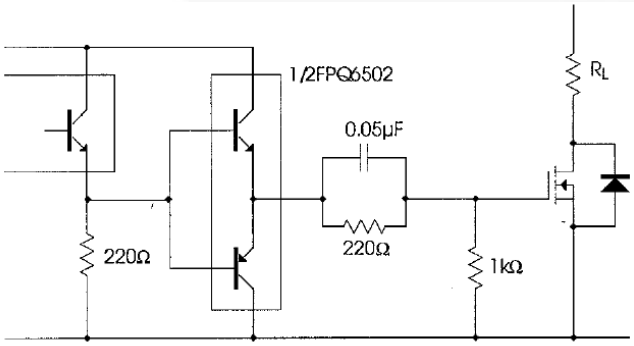

Figure 31. Emitter Follower with Speed-Up Capacitor

Isolation: Off-line switching power supplies use power MOSFETs in a half bridge configuration because inexpensive, high voltage devices with low $R_{DS(ON)}$ are not available.

Since one of the power devices is connected to the positive rail, its drive circuitry is also floating at a high potential. The most versatile method of coupling the drive circuitry is to use a pulse transformer. Pulse transformers are also normally used to isolate the logic circuitry from the MOSFETs operating at high voltage to protect it from a MOSFET failure.

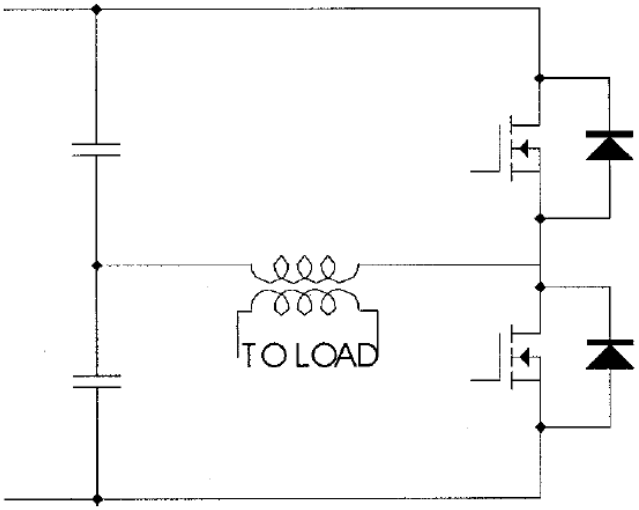

Figure 32. Half-Bridge Configuration

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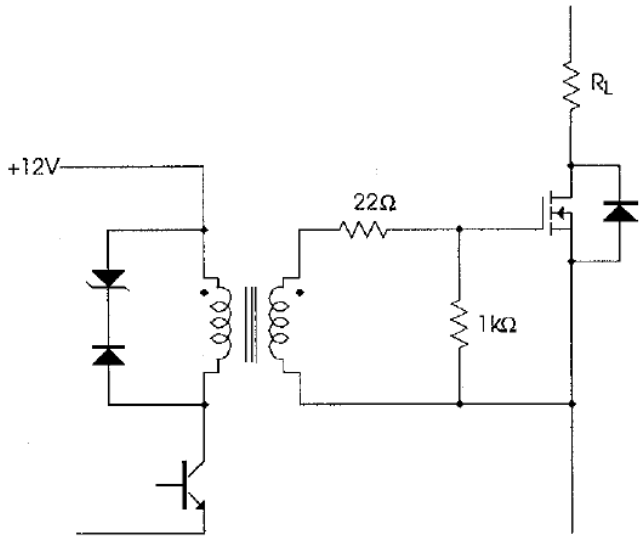

Figure 33. Simple Pulse Transformer Drive Circuit, the Transistor may be a Part of a PWM IC if Applicable

The Zener diodes shown in Figure 33 is included to reset the pulse transformer quickly. The duty cycle can approach 50% with a 12 V Zener diode. For better performance at turn-off, a PNP transistor can be added as shown in Figure 34.

Figure 35 illustrates an alternate method to reverse bias the MOSFET during turn-off by inserting a capacitor in series with the pulse transformer. The capacitor also ensures that the pulse transformer will not saturate due to DC bias.

Opto-isolators may also be used to drive power MOSFETs but their long switching times make them suitable only for low frequency applications.

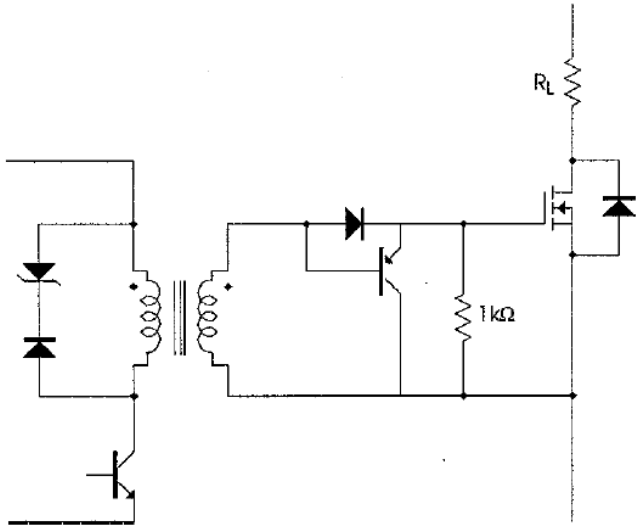

Figure 34. Improved Performance at Turn-Off with a Transistor

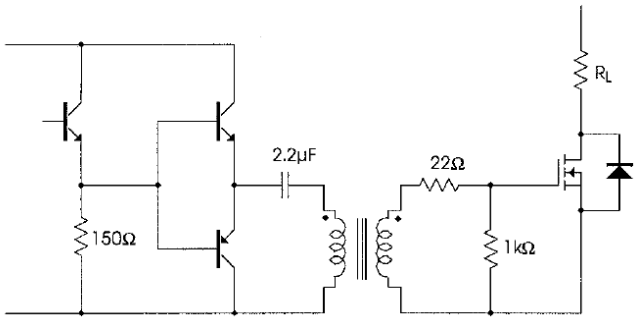

Figure 35. Emitter Follower Driver with Speed-Up Capacitor

Selecting a Drive Circuit

Any of the circuits shown are capable of turning a Power MOSFET on and off. The type of circuit depends upon the application. The current sinking and sourcing capabilities of the drive circuit will determine the switching time and switching losses of the power device. As a rule, the higher the gate current at turn-on and turn-off, the lower the switching losses will be. However, fast drive circuits may produce ringing in the gate circuit and drain circuits. At turn-on, ringing in the gate circuit may produce a voltage transient in excess of the maximum V_{GS} rating, which will puncture the gate oxide and destroy it. To prevent this occurrence, a Zener diode of appropriate value may be added to the circuit as shown in Figure 36. Note that the Zener should be mounted as close as possible to the device.

At turn-off, the gate voltage may ring back up to the threshold voltage and turn on the device for a short period. There is also the possibility that the drain-source voltage will exceed its maximum rated voltage due to ringing in the drain circuit. A protective RC snubber circuit or Zener diode may be added to limit drain voltage to a safe level.

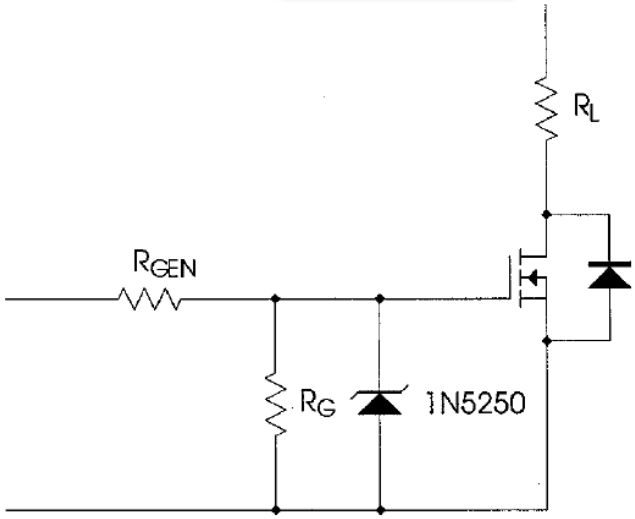

Figure 36. Zener Diode to Prevent Excessive Gate-Source Voltages

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