AN-1577
SG1577A Layout Guidelines

Abstract

This layout is important in high-frequency switching converter design. If designed improperly, PCB can radiate excessive noise and contribute to converter instability.

Place the Pulse-Width Modulated (PWM) power stage components first. Mount all the power components and connections in the top layer with wide copper areas. The switchers of buck, inductor, and output capacitor should be as close to each other as possible to reduce the radiation of EMI due to the high-frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered. Place the input capacitor near the drain of high-side MOSFET. In multi-layer PCB, use one layer as power ground and have a separate control signal ground as the reference for all signals. To avoid the signal ground being affected by noise and have best load regulation, it should be connected to the ground terminal of output.

Checklists for Double-Layer PCB

Follow the below guidelines for best performance:

- A double-layer printed circuit board is recommended.
- Use the bottom layer of the PCB as a ground plane and make all critical component ground connections through vias to this layer.
- Keep the traces running from the CLNx terminal to the output inductor be short.
- Use copper-filled polygons on the top (and bottom, if two-layer PCB) circuit layers for the CLNx node.
- The small-signal wiring traces from the DLx and DHx pins to the MOSFET gates should be kept short and wide enough to easily handle the several amps of drive current.
- The critical, small-signal components include any bypass capacitors (SMD-type of capacitors applied at VCC and SSx/ENB pins), feedback components (resistor divider), and compensation components (between INx and COMPx pins). Position those components close to their pins with a local, clear GND connection or directly to the ground plane. **Keep those small-signal components and their wiring-traces far away the noisy generator of CLNx node.**
- Place the bootstrap capacitor near the BSTx and CLNx pins.
- Place the ceramic capacitor (SMD or DIP type) near the VCC pin and GND pin to gain the noise immunity.
- The resistor on the RT pin should be near this pin and the GND return should be short and kept away from the noisy MOSFET GND (which is short together with IC's PGND pin to GND plane on back side of PCB).
- Place the compensation components close to the INx and COMPx pins.
- The feedback resistors for both regulators should be located as close as possible to the relevant INx pin with vias tied straight to the ground plane as required.
- Minimize the length of the connections between the input capacitors, CIN, and the power switchers (MOSFETs) by placing them nearby.
- Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain terminal as possible and make the GND returns (from the source terminal of lower MOSFET to V_{IN} capacitor GND) short.
- Position the output inductor and output capacitors between the upper MOSFET and lower MOSFET and the load.
- AGND should be on the clearer plane and kept away from the noisy MOSFET GND.
- PGND should be short, together with MOSFET GND, then through vias to GND plane on the bottom of PCB.

The best high-current power loop as shown in Figure 1.

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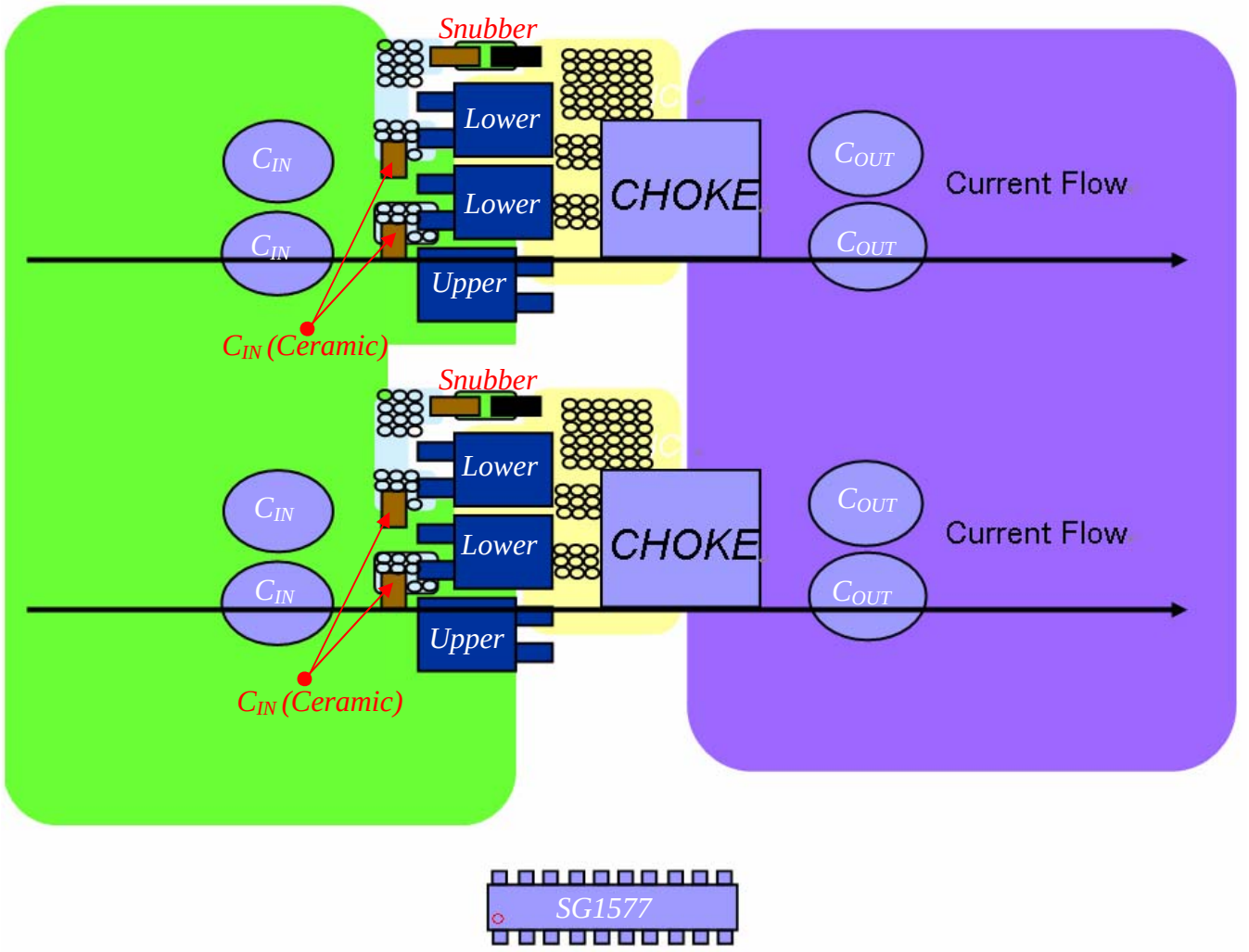


Figure 1. Power Loop

Practical Cases

SG1577A is used for ATX power supply field, so SG1577A hosts the single-layer board or a daughter board plugged into the main board. The below sections provide good possible layouts for two cases.

Case 1: Single-Layer

Power Loop

CLNx trace between high-side and low-side MOSFET should be copper-filled polygons. Do not use a jumper (which results in a parasitic inductance and induce a negative spike on this node).

The specification for CLN to GND is:

CLN to GND for 100ns Transient:

-4V Min. 18V Max

The high-current loop should be small to prevent EMI issues.

The input capacitors (ceramic and E/C) and output capacitors should be near the relative rail.

For a jumper used in the low-side MOSFET GND to V_{IN} GND, consider the rating current. Two/three pieces of paralleled jumpers not only improved the rating current, but also reduced the parasitic inductance. Due to this jumper, the IC PGND should not be connected here!

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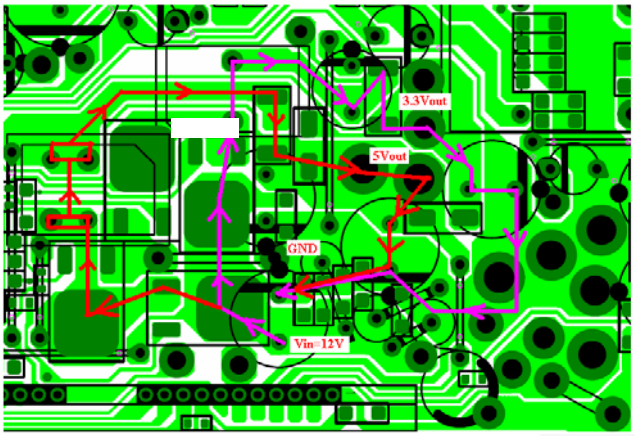


Figure 2. Power Loop

PGND & GND

Use wiring-trace to connect PGND & GND. Do not use a jumper. If necessary, use 0Ω 0805/1206 resistors to be the jumpers.

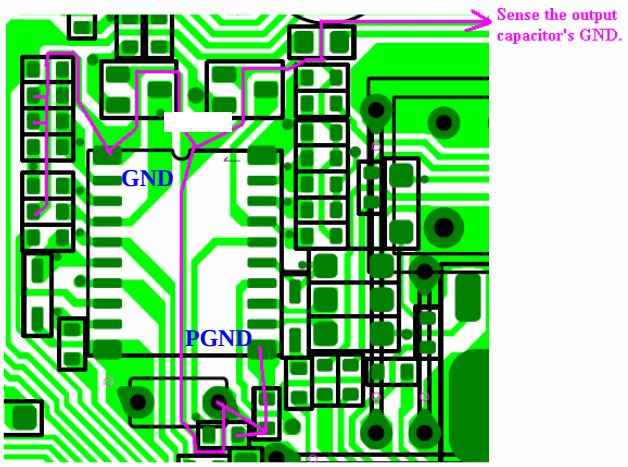


Figure 3. PGND & AGND Wiring-trace

Gate Connection

- "Short and wide" is hard to achieve in a one-layer board, do the best possible.
- Don't use the jumper to be the connector; 0Ω 0805/1206 resistors are recommended.
- Avoid passing through the CLNx node to avoid the noisy interference.
- Figure 4 also shows the position of SG1577A and power-MOSFETs relatively. Do not place SG1577A in the center of the power-MOSFETs even though this simplifies the trace wiring.

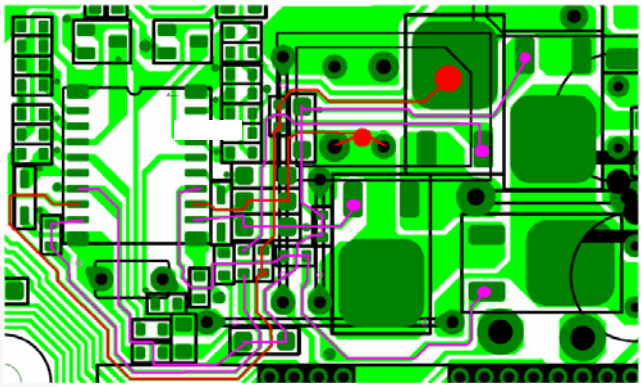


Figure 4. DHx & DLx Connection

Small Signals

The components related to this pin should be nearby. The critical pins are IN, COMP, BST, RT, SS/ENB, and VCC. If some of those components refer to ground, they should be tied to the GND pin (In this case, GND is the same as PGND). For any connection that can't use a jumper, 0Ω 0805/1206 resistors are recommended.

The DIP-type of VCC capacitor can be closer to the VCC and GND pins for the best noise immunity.

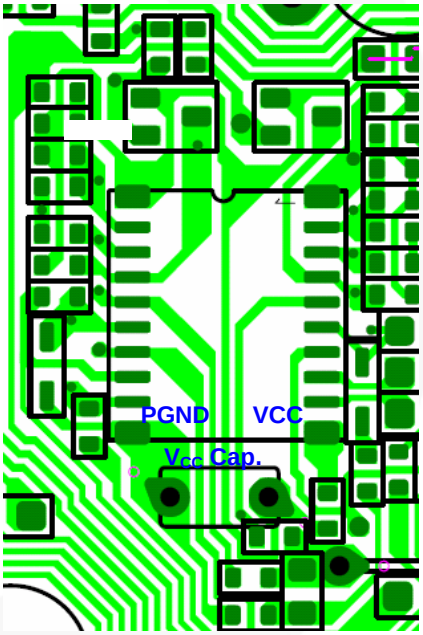


Figure 5. Small-Signal Components Placement

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Case 2: Double-Layer of Daughter Board

Power Loop

Plan the flow of the power loop as smoothly as possible.

The ceramic capacitors of VCC should be near the drain of upper MOSFET and the source of lower MOSFET. Use the copper planes in this loop as needed.

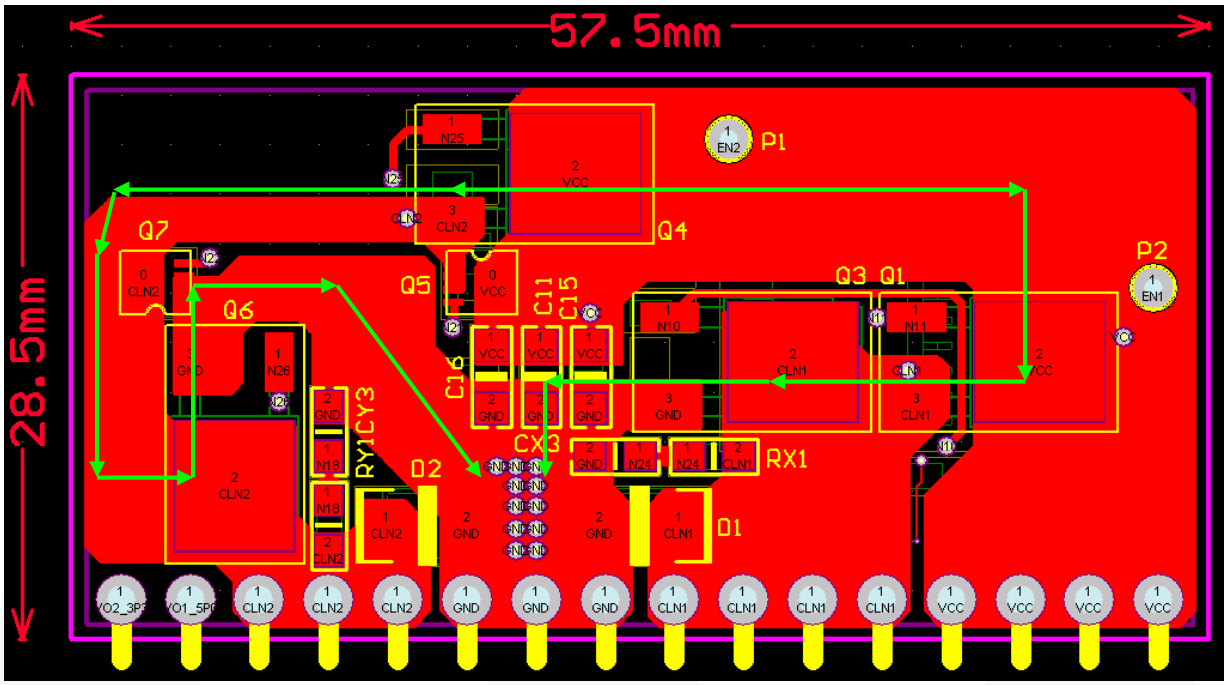


Figure 6. Daughter Board (Top Layer)

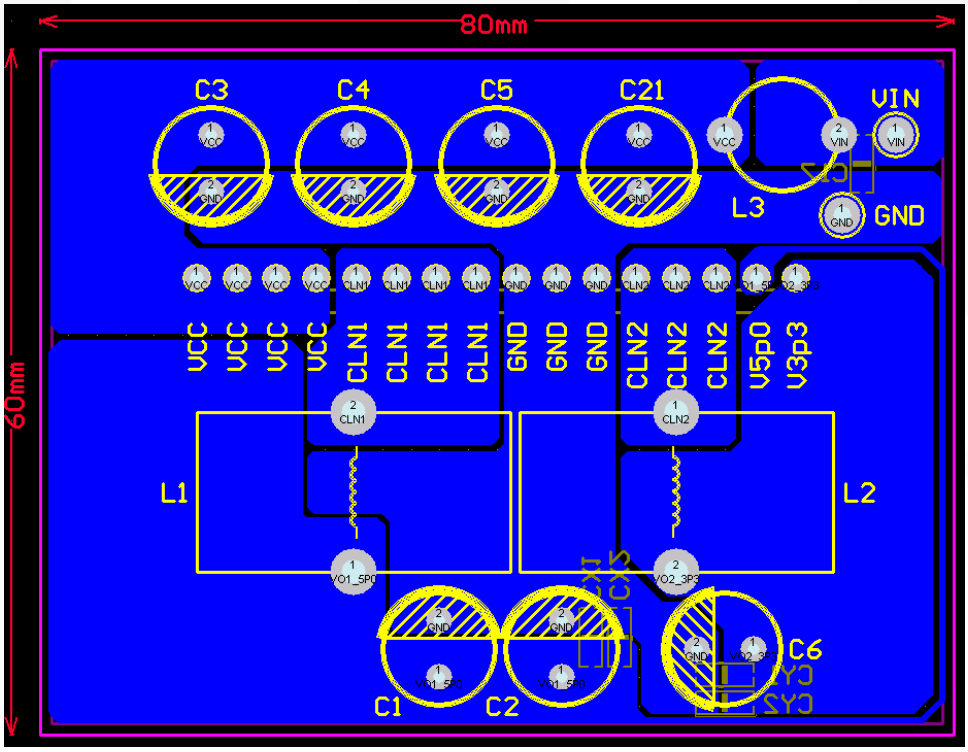


Figure 7. Main Board Power Loop

PGND & GND

Use wiring trace to connect all of GND nets together, then tie PGND and GND on the GND plane.

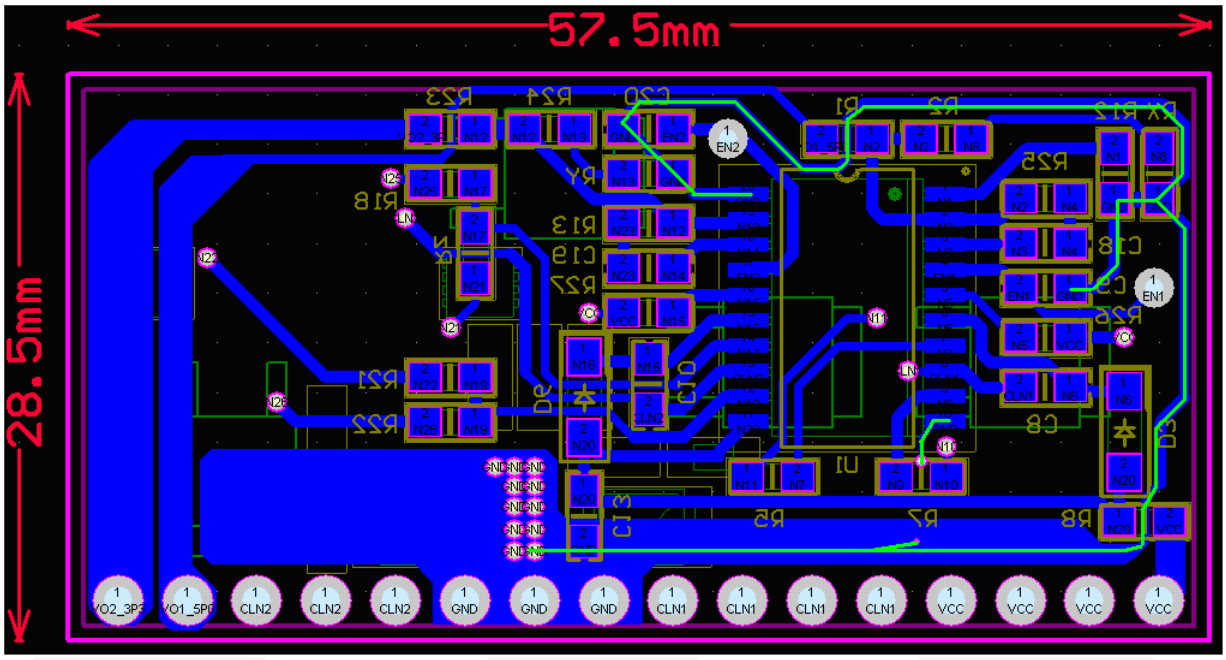


Figure 8. PGND & GND Wiring-Trace (Bottom Layer)

Gate Connection

- Keep traces as short and wide as possible.
- Keep tracing on the bottom layer. Don't put tracing on the top layer near the noisy node.
- Don't use more than one via on DHx/DLx/CLNx traces to avoid the parasitic effect of the PCB.

Small Signals

The components related to this pin should be located near by. The critical pins are IN, COMP, BST, RT, SS/ENB, and VCC, as shown in Figure 9.

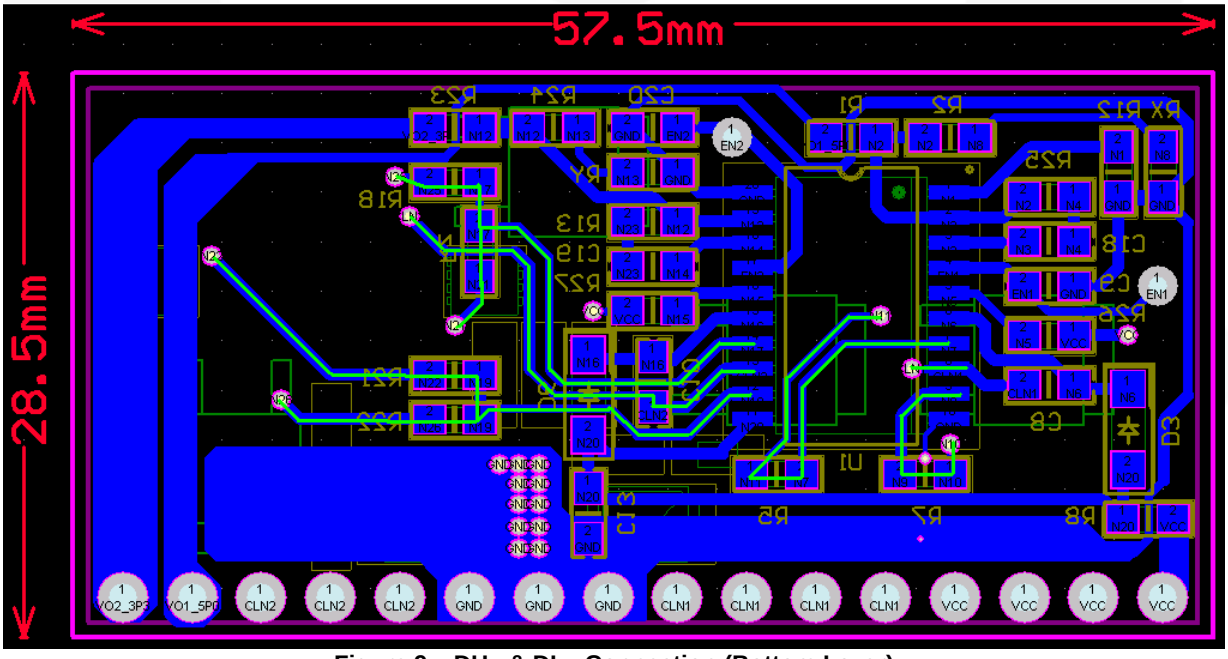


Figure 9. DHx & DLx Connection (Bottom Layer)

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Related Datasheets

SG1577A- Dual Synchronous DC/DC Controller

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