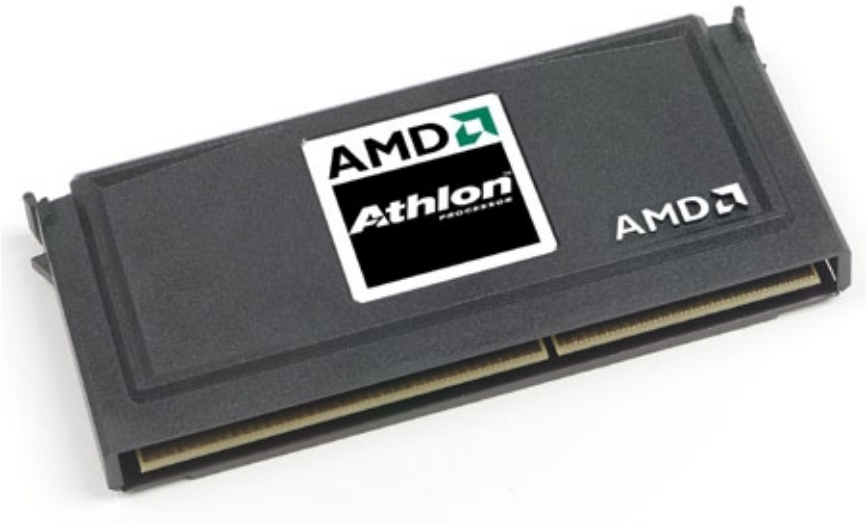
AMD

AMD-751™

System Controller

Revision Guide



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AMD-751™ System Controller Revision Guide

The purpose of the *AMD-751™ System Controller Revision Guide* is to communicate updated product information on the AMD-751™ system controller to designers of computer systems and software developers. This guide consists of three major sections:

- **Product Marking Identification:** This section, which starts on page 2, provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section, which starts on page 3, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. A product errata may cause the behavior of the AMD-751 system controller to deviate from the published specifications.
- **Revision Determination:** This section, which starts on page 11, describes the registers that identify the current revision of the part.
- **Technical and Documentation Support:** This section, which starts on page 12, provides a listing of available technical support resources.

Revision Guide Policy

Occasionally AMD identifies deviations from or changes to the specification of the AMD-751 system controller. These changes are documented in the *AMD-751 System Controller Revision Guide* as errata. Descriptions are written to assist system and software designers in using the AMD-751 and corrections to AMD's documentation on the AMD-751 system controller are included. This release documents currently characterized product errata.

1 Product Marking Identification

1.1 Production Marking

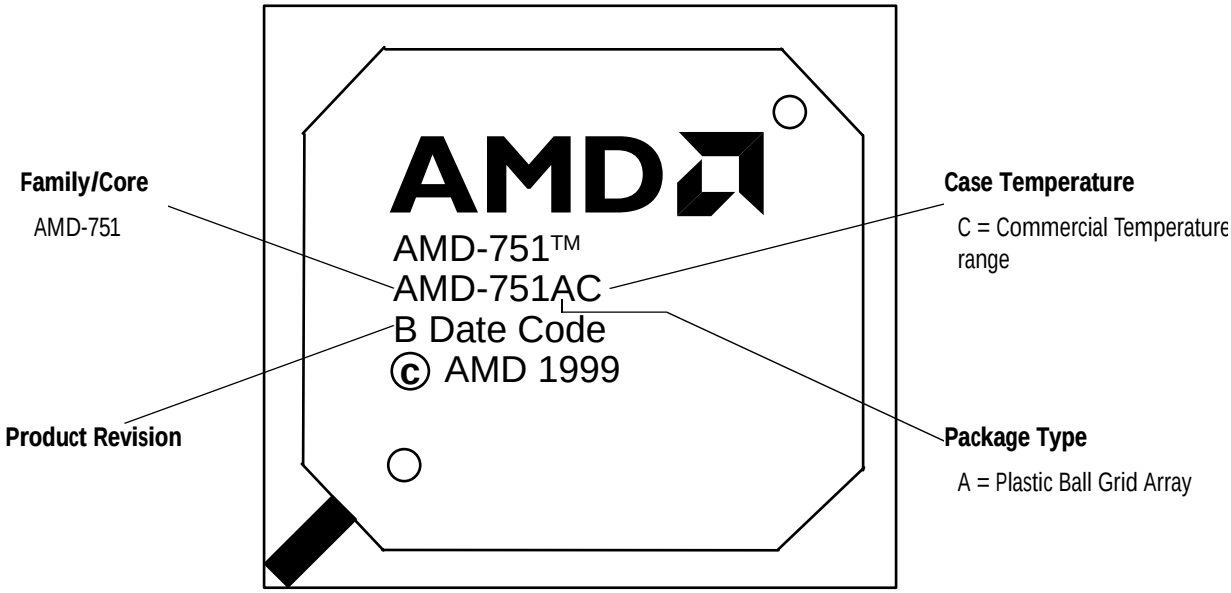


Table 1. Valid Combinations for Ordering Parts

OPN	Package Type	Operating Voltage	Case Temperature
AMD-751AC	492-pin PBGA ATX	3.135 V–3.6 V	85°C

Note:
Valid combinations are configurations that are or will be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

2 Product Errata

This section documents AMD-751 system controller product errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the processor to each erratum. An "X" indicates that the erratum applies to the revision. The absence of an "X" indicates that the erratum does not apply to the revision.

Note: *There can be missing errata numbers. Errata that have been resolved from early revisions of the controller have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 2. Cross-Reference of Product Revision to Errata

Erratum Number and Description	Revision Number			
			C3	C5
PCI				
1 Invalid Read Performed After a Slave PCI Target Abort			X	X
2 Arbitration Latency Due to No Bus Preemption			X	
3 PCI ARB_DIS Bit Set When DMA is Active			X	X
AGP				
8 GART Requestors Do Not Work With TLB Caches Off			X	X
18 Burst Writes to Non-Existent AGP Memory Hang System			X	X
20 AGP AD_STB[1:0] Strobe Glitch with Nvidia NV10-Based (GeForce) Cards			X	X
SDRAM				
19 Setting the Queue Bypass-Mode Bit Causes Memory Failure				X
21 Potential Memory Failure When Using Certain Double-Sided SDRAM Memory DIMMs			X	X
AMD Athlon™ System Bus				
12 Incomplete AMD Athlon System Bus Disconnect Causes AMD-751 To Hang			X	X
Functional				
14 BAR0[3] Initial Setting Causes OS/2 Warp Install Error			X	X
15 Ref_5V Cannot Be At A Lower Voltage Than Vcc (3.3V)			X	

1 Invalid Read Performed After a Slave PCI Target Abort

Products Affected. C3 and C5

Description. When the AMD-751 system controller initiates an unaligned doubleword PCI I/O read transaction and this I/O read receives a target abort from the PCI slave, the next PCI I/O read returns incorrect data. Aligned transactions are unaffected.

Potential Effect on System. A target abort on the PCI bus is an extremely rare event and the occurrence of the abort is considered a catastrophic error condition. This condition was artificially created for PCI testing and has not been observed in normal system validation testing.

Suggested Workaround. None

Resolution Status. Fixed in a future revision of the AMD-751 system controller.

2 Arbitration Latency Due to No Bus Preemption

Products Affected. C3

Description. The AMD-751 PCI arbiter can impose long latencies on external PCI bus masters when any master that currently owns the bus is attempting long transfers due to not correctly supporting bus preemption. When a PCI master's bus grant is active and another master requests the bus, the arbiter should immediately deassert the grant to the first master, thus preempting the first master. The first master is permitted to continue bus transactions for the duration of its master latency timer. Due to the anomaly in the arbiter, the original master does not get preempted if it owns the bus and it continues to keep its request pin asserted. Therefore, it could use the bus indefinitely. However, this problem has not been seen with any real system hardware and software.

Potential Effect on System. Some peripherals may experience timeouts. A lack of fairness on the bus.

Suggested Workaround. None

Resolution Status. Fixed in Rev C5.

3 PCI ARB_DIS Bit Set When DMA is Active

Products Affected. C3 and C5

Description. If DMA is active when ARB_DIS is set, the system can hang.

Potential Effect on System. System hang could occur.

Suggested Workaround. Prior to setting ARB_DIS, software suspends all DMA activity.

Resolution Status. Fixed in a future revision of the AMD-751 system controller.

8 GART Requestors Do Not Work With TLB Caches Off

Products Affected. C3 and C5

Description. Only partial support exists for the mode where GART TLB caches are disabled. GART caches disabled was intended primarily for performance evaluation, and is not supported.

Potential Effect on System. None

Suggested Workaround. The BIOS should set BAR1: Offset 02h bit 2.

Resolution Status. None required, proper operation

12 Incomplete AMD Athlon System Bus Disconnect Causes AMD-751 To Hang

Products Affected. C3, C5

Description. An incomplete AMD Athlon™ system bus disconnect sequence (from the AMD Athlon processor) can hang the AMD-751 system controller. The AMD Athlon may not complete a disconnect sequence when using STPCLK-throttling power management.

Potential Effect on System. This problem can occur with ACPI thermal zone support (thermal-throttling power management) or processor C2/C3 support enabled.

Suggested Workaround. STPCLK throttling (thermal zone) and processor C2/C3 are not supported at this time. STPCLK throttling is not required for support of the ACPI S1 state.

Resolution Status. Fixed in C3.

14 BAR0[3] Initial Setting Causes OS/2 Warp Install Error

Products Affected. All revisions

Description. BAR0[3] (Base Address Register 0 = Function 0, Device 0, Offset 10h) is initialized to 1, which indicates that the AGP aperture is prefetchable. With all base address bits (bits 4–30) reset and with bit 3 set to 1, OS/2 Warp 4.0 installation hangs. With AGP disabled, these bit settings are correct for the AMD-751.

Potential Effect on System. OS/2 Warp 4.0 hangs during installation.

Suggested Workaround. Enable AGP BIOS settings during the OS/2 Warp 4.0 installation. When the BIOS sets the Base Address bits of BAR1 for AGP mode, OS/2 Warp 4.0 loads correctly.

Resolution Status. No change to the AMD-751 is required.

15 Ref_5V Cannot Be At A Lower Voltage Than Vcc (3.3V)

Products Affected. C3

Description. Voltage on the Vcc (3.3-V supply) pins cannot exceed the voltage on the 5-V reference pin (Ref_5V).

Potential Effect on System. The AMD-751 can go into a latch-up state, and permanent damage to the part may result.

Suggested Workaround. Specify the system power supply whose outputs ramp up and ramp down, such that the 3.3V outputs never supply voltage higher than the 5-V outputs. For more information, see the *AMD Athlon™ Processor Voltage Regulation Application Note*, order# 22651.

In addition, providing a forward-biased diode on the motherboard from the 3.3-V supply to the 5-V supply limits any 3.3-V excursions to the diode voltage drop. The power supply connector should never be inserted or removed while power is applied to the motherboard.

Resolution Status. Fixed in Rev C5.

18 Burst Writes to Non-Existent AGP Memory Hang System

Products Affected. C3 and C5

Description. Running in DOS under Windows, MechWarrior2 creates burst writes to non-existent AGP memory that intentionally cause master abort cycles from the S3 Savage4 graphics card to the system controller. The AMD-751 system controller does not handle master abort cycles in the quantity generated by the S3 Savage4 graphics card. This behavior to the system controller is caused by the software/driver when write combining is enabled and is not considered appropriate nor indicative of any common software technique. Write combining is enabled when the AMD AGP miniport driver is installed.

Potential Effect on System. System hangs.

Suggested Workarounds.

I. Run the game differently:

1. Install and run the game directly under DOS, creating a BOOT floppy when asked.
2. Obtain the Windows version of the program on CD.
3. Upgrade to the newer MechWarrior3 product.

II. Change the BIOS

1. APC write chaining, device 0, function 0, register 84h, bit 17 must be left at 0.

Resolution Status. No planned fix.

19 Setting the Queue Bypass-Mode Bit Causes Memory Failure

Products Affected. C5

Description. A memory failure may occur if queue bypass mode is enabled.

Potential Effect on System. Memory failure, which causes a system error.

Suggested Workaround. Do not set the queue bypass-mode bit.

Resolution Status. Fixed in a future revision of the AMD-751.

20 AGP AD_STB[1:0] Strobe Glitch with Nvidia NV10-Based (GeForce) Cards

Products Affected. All revisions (C3 and C5)

Description. The AMD-751 system controller's AD_STB[1:0] signals may experience noise due to strong drive strengths. This noise may result in signal glitches, causing incorrect information to be strobed into the AGP adapter.

Potential Effect on System. System hangs.

Suggested Workaround. The issue can be alleviated by forcing the AGP subsystem into AGP 1X Mode. A driver update is available from Nvidia that performs this task by changing the system registry. Performance will decrease when enabling the lower speed AGP mode. To obtain this driver, go to the www.nvidia.com website, and follow the driver update links from the home page.

Please contact your AMD Specialist for details.

Resolution Status. Fixed in a future revision of the AMD-751 system controller.

21 Potential Memory Failure When Using Certain Double-Sided SDRAM Memory DIMMs

Products Affected. C3 and C5

Description. Under certain SDRAM double-sided DIMM loading conditions, systems based on the the AMD-751 system controller can experience reduced timing margins, resulting in memory failures during memory cycles.

This condition only occurs when using specific double-sided DIMMs with combinations of the following characteristics:

1. Printed Wiring Board (PWB) designed around the Intel LC_12_112 Gerber.
2. Memory ICs with lower V_{IL} input thresholds.

Potential Effect on System. Unstable system.

Suggested Workarounds.

1. Vendors should use memory DIMMs only from an approved vendor list (AVL). DIMMs from this list have been extensively tested on AMD-751 based platforms and qualified for usage. Please consult your OEM or AMD specialist for details.
2. Vendors developing new AMD-751 based motherboards should implement pulldown resistors on the MAA[14:0] and MAB[14:0] address buses. Use of this termination method will improve the timing margins. Please consult your OEM or AMD specialist for specific values.

Resolution Status. All future motherboards should be implemented with the suggested termination method.

3 Revision Determination

Table 3 summarizes the AMD-751 system controller configuration register offsets, devices, default values after reset, and access types. Access types are indicated as follows:

RW - Read/Write
RO - Read Only

Table 3. Function 0, Device 0 Configuration Registers

Offset	Cache Control	Reset	Access
01h–00h	Vendor ID (AMD)	1022h	RO
03h–02h	Device ID Single Processor Device	7006h	RO
08h	Revision ID	nn *	RO
63h–60h	BIU Status and Control	0000_0Cxxh	RW
86h	PCI and APCI Chaining	00h	RW

Note:
* *nn changes for each device revision. For example, 00h = Revision A0; 01h = Revision A1; 10h = Revision B0; 21h = Revision C1; 25h = Revision C5 etc.*

Vendor ID — Device 0 Offset 01h–00h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Vendor ID															
Reset	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0

This read-only value is defined as 1022h.

Device ID — Device 0 Offset 03h–02h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Device ID															
Reset	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0

This read-only value of 7006h represents the AMD-751 system controller single processor device.

Revision ID — Device 0 Offset 08h

	Bit 7	6	5	4	3	2	1	Bit 0
	AMD-751 System Controller Chip Revision and Stepping Code							
Reset	–	–	–	–	–	–	–	–

Bits 7–0

AMD-751™ System Controller Revision Code (RO) - The most-significant nibble indicates the die revision and the least-significant nibble represents the stepping. (For example, 00h = Revision A0; 01h = Revision A1; 10h = Revision B0; 21h = Revision C1; 25h = Revision C5; etc.)

4 Technical and Documentation Support

4.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD-751 system controller:

- AMD-751™ System Controller Data Sheet (order# 21910)
- AMD-756™ Peripheral Bus Controller Data Sheet (order# 22548)
- AMD Athlon™ System Bus Specification (order# 21902)
- AMD Athlon™ Processor BIOS, Software, and Debug Tools Developers Guide (order# 21656)
- AMD Athlon™ Processor Data Sheet (order# 21016)

For the latest updates, refer to www.amd.com and download the appropriate files. For documents under NDA, please contact your local sales representative for updates.