

AMC1300 Precision, ± 250 -mV Input, Reinforced Isolated Amplifier

1 Features

- ± 250 -mV input voltage range optimized for current measurement using shunt resistors
- Low offset error and drift:
 - AMC1300B: ± 0.2 mV (max), ± 3 $\mu\text{V}/^\circ\text{C}$ (max)
 - AMC1300: ± 2 mV (max), ± 4 $\mu\text{V}/^\circ\text{C}$ (max)
- Fixed gain: 8.2
- Very low gain error and drift:
 - AMC1300B: $\pm 0.3\%$ (max), ± 50 ppm/ $^\circ\text{C}$ (max)
 - AMC1300: $\pm 1\%$ (max), ± 50 ppm/ $^\circ\text{C}$ (typ)
- Low nonlinearity and drift: 0.03%, 1 ppm/ $^\circ\text{C}$ (typ)
- 3.3-V operation on high-side (AMC1300B)
- System-level diagnostic features
- Safety-related certifications:
 - 7071- V_{PK} reinforced isolation per DIN VDE V 0884-11: 2017-01
 - 5000- V_{RMS} isolation for 1 minute per UL1577
- High CMTI on AMC1300B: 140 kV/ μs (typ)

2 Applications

- Shunt-resistor-based current sensing in:
 - [Motor drives](#)
 - [Frequency inverters](#)
 - [Uninterruptible power supplies](#)

3 Description

The AMC1300 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The input of the AMC1300 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The excellent performance of the device supports accurate current control resulting in system-level power savings and, especially in . The integrated common-mode overvoltage and missing high-side supply voltage detection features of the AMC1300 simplify system-level design and diagnostics.

The AMC1300 is offered with two performance grade options: the AMC1300B is specified over the extended industrial temperature range of -55°C to $+125^\circ\text{C}$, and the AMC1300 for operation at -40°C to $+125^\circ\text{C}$.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1300	SOIC (8)	5.85 mm $\times$ 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

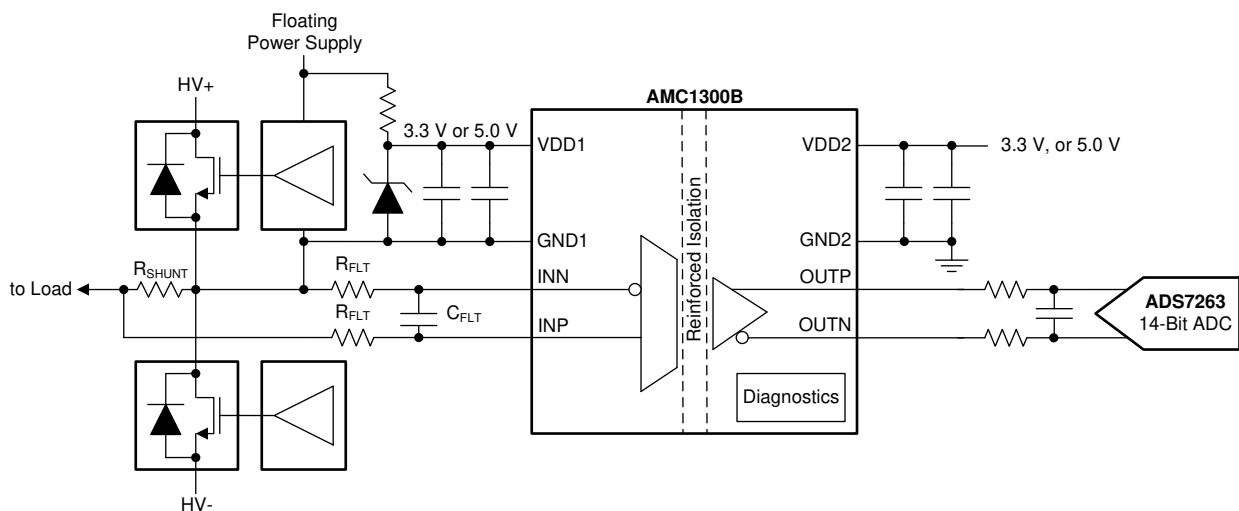


Table of Contents

1 Features	1	8.1 Overview	20
2 Applications	1	8.2 Functional Block Diagram	20
3 Description	1	8.3 Feature Description	20
4 Revision History	2	8.4 Device Functional Modes	22
5 Device Comparison Table	3	9 Application and Implementation	23
6 Pin Configuration and Functions	4	9.1 Application Information	23
7 Specifications	5	9.2 Typical Application	23
7.1 Absolute Maximum Ratings	5	9.3 What to Do and What Not to Do	25
7.2 ESD Ratings	5	10 Power Supply Recommendations	26
7.3 Recommended Operating Conditions	5	11 Layout	27
7.4 Thermal Information	6	11.1 Layout Guidelines	27
7.5 Power Ratings	6	11.2 Layout Example	27
7.6 Insulation Specifications	7	12 Device and Documentation Support	28
7.7 Safety-Related Certifications	8	12.1 Documentation Support	28
7.8 Safety Limiting Values	8	12.2 Receiving Notification of Documentation Updates	28
7.9 Electrical Characteristics	9	12.3 Community Resources	28
7.10 Switching Characteristics	11	12.4 Trademarks	28
7.11 Insulation Characteristics Curves	12	12.5 Electrostatic Discharge Caution	29
7.12 Typical Characteristics	13	12.6 Glossary	29
8 Detailed Description	20	13 Mechanical, Packaging, and Orderable Information	29

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

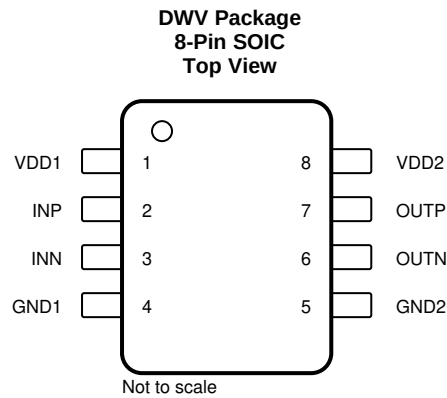
Changes from Revision A (June 2018) to Revision B	Page
• Changed <i>DIN V VDE V</i> to <i>DIN VDE V</i> in <i>Safety-related certifications</i> Features bullet	1
• Changed CLR and CPG parameter values from 9 mm to 8.5 mm in <i>Insulation Specifications</i> table	7
• Changed <i>Insulation Specifications</i> table per ISO standard	7
• Changed <i>Safety-Related Certification</i> table per ISO standard	8
• Changed P_S equation details in <i>Safety Limiting Values</i> table	8
• Added <i>Input Offset Voltage vs Temperature</i> figure	13
• Added <i>Common-Mode Rejection Ratio vs Input Frequency</i> figure	14
• Added <i>Gain Error vs Temperature</i> figure	15
• Added <i>Gain Error Drift Histogram</i> figure	15
• Changed <i>Do's and Don'ts</i> section title to <i>What to Do and What Not to Do</i>	25

Changes from Original (May 2018) to Revision A	Page
• Changed <i>Reinforced Isolation Capacitor Lifetime Projection</i> figure	12

5 Device Comparison Table

PARAMETER		AMC1300B	AMC1300
High-side supply voltage, VDD1		3.0 V to 5.5 V	4.5 V to 5.5 V
Specified ambient temperature, T _A		–55°C to +125°C	–40°C to +125°C
Input offset voltage, V _{OS}	4.5 V ≤ VDD1 ≤ 5.5 V	±0.2 mV	±2 mV
	3.0 V ≤ VDD1 ≤ 4.5 V		Not applicable
Input offset drift, TCV _{OS}		±3 μV/°C (max)	±4 μV/°C (max)
Gain error, E _G		±0.3%	±1%
Gain error drift, TCE _G		±15 ppm/°C (typ), ±50 ppm/°C (max)	±50 ppm/°C (typ)
Common-mode transient immunity, CMTI		75 kV/μs (min), 140 kV/μs (typ)	15 kV/μs (min), 30 kV/μs (typ)
Output bandwidth, BW		250 kHz (min), 310 kHz (typ)	170 kHz (min), 230 kHz (typ)
INP, INN to OUTP, OUTN signal delay (50% – 90%)		3 μs (max)	3.4 μs (max)

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	—	High-side power supply, 3.0 V to 5.5 V for the AMC1300B (4.5 V to 5.5 V for the AMC1300), relative to GND1. See the Power Supply Recommendations section for power-supply decoupling recommendations.
2	INP	I	Noninverting analog input
3	INN	I	Inverting analog input
4	GND1	—	High-side analog ground
5	GND2	—	Low-side analog ground
6	OUTN	O	Inverting analog output
7	OUTP	O	Noninverting analog output
8	VDD2	—	Low-side power supply, 3.0 V to 5.5 V. See the Power Supply Recommendations section for power-supply decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	–0.3	6.5	V
	VDD2 to GND2	–0.3	6.5	
Input voltage	INP, INN	GND1 – 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T _J		150	°C
	Storage, T _{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1, AMC1300	4.5	5	5.5	V
		VDD1 to GND1, AMC1300B	3.0	5	5.5	
	Low-side power supply	VDD2 to GND2	3.0	3.3	5.5	V
ANALOG INPUTS						
V _{Clipping}	Differential input voltage before clipping output	V _{IN} = V _{INP} – V _{INN}	±320			mV
V _{FSR}	Specified linear differential input full-scale	V _{IN} = V _{INP} – V _{INN}	–250		250	mV
	Absolute common-mode input voltage ⁽¹⁾	(V _{INP} + V _{INN}) / 2 to GND1	–2		VDD1	V
V _{CM}	Operating common-mode input voltage	(V _{INP} + V _{INN}) / 2 to GND1	–0.16		VDD1 – 2.1	V
TEMPERATURE RANGE						
T _A	Specified ambient temperature	AMC1300	–40		125	°C
		AMC1300B	–55		125	

- (1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the [Absolute Maximum Ratings](#) table.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AMC1300x	UNIT
		DWV (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	98.45	mW
		VDD1 = VDD2 = 3.6 V, AMC1300B only	56.52	
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = 5.5 V	53.90	mW
		VDD1 = 3.6 V, AMC1300B only	30.60	
P_{D2}	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V	44.55	mW
		VDD2 = 3.6 V	25.92	

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage ⁽¹⁾	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2121	V _{PK}
V _{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); see Figure 4	1500	V _{RMS}
		At DC voltage	2121	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification test)	7071	V _{PK}
		V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test)	8485	
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50-μs waveform, V _{TEST} = 1.6 × V _{IOSM} = 12800 V _{PK} (qualification)	8000	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a, after input/output safety test subgroup 2 / 3, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.2 × V _{IORM} = 2545 V _{PK} , t _m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.6 × V _{IORM} = 3394 V _{PK} , t _m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.875 × V _{IORM} = 3977 V _{PK} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.5 V _{PP} at 1 MHz	~1	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V at T _A = 25°C	> 10 ¹²	Ω
		V _{IO} = 500 V at 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
	Climatic category		55/125/2 1	
UL1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 5000 V _{RMS} or 7000 V _{DC} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} = 6000 V _{RMS} , t = 1 s (100% production test)	5000	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 62368-1: 2016-05, EN 62368-1: 2014, and IEC 62368-1: 2014	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current	R _{θJA} = 85.4°C/W, T _J = 150°C, T _A = 25°C, VDD1 = VDD2 = 5.5 V, see Figure 2			266	mA
		R _{θJA} = 85.4°C/W, T _J = 150°C, T _A = 25°C, VDD1 = VDD2 = 3.6 V, AMC1300B only, see Figure 2			406	
P _S	Safety input, output, or total power ⁽¹⁾	R _{θJA} = 85.4°C/W, T _J = 150°C, T _A = 25°C, see Figure 3			1463	mW
T _S	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.

T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum junction temperature.

P_S = I_S × VDD1_{max} + I_S × VDD2_{max}, where VDD1_{max} is the maximum high-side supply voltage and VDD2_{max} is the maximum low-side supply voltage.

7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1300 apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 4.5\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $I_{NP} = -250\text{ mV}$ to $+250\text{ mV}$, and $I_{NN} = \text{GND1} = 0\text{ V}$; minimum and maximum specifications of the AMC1300B apply from $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $I_{NP} = -250\text{ mV}$ to $+250\text{ mV}$, and $I_{NN} = \text{GND1} = 0\text{ V}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V _{CMov}	Common-mode overvoltage detection level		VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level		95			mV
V _{OS}	Input offset voltage ⁽¹⁾	AMC1300, initial, at T _A = 25°C, V _{INP} = V _{INN} = GND1	–2	±0.01	2	mV
		AMC1300B, initial, at T _A = 25°C, V _{INP} = V _{INN} = GND1	–0.2	±0.01	0.2	
TCV _{OS}	Input offset drift ⁽¹⁾	AMC1300	–4	±1.3	4	µV/°C
		AMC1300B	–3	±1	3	
CMRR	Common-mode rejection ratio	f _{IN} = 0 Hz, V _{CM min} ≤ V _{CM} ≤ V _{CM max}	–100			dB
		f _{IN} = 10 kHz, V _{CM min} ≤ V _{CM} ≤ V _{CM max}	–98			
C _{IN}	Single-ended input capacitance	INN = GND1, f _{IN} = 275 kHz	2			pF
C _{IND}	Differential input capacitance	f _{IN} = 275 kHz	1			pF
R _{IN}	Single-ended input resistance	INN = GND1	19			kΩ
R _{IND}	Differential input resistance		22			kΩ
I _{IB}	Input bias current	INP = INN = GND1, I _{IB} = (I _{IBP} + I _{IBN}) / 2	–41	–30	–24	µA
TCI _{IB}	Input bias current drift		±1			nA/°C
I _{IO}	Input offset current		±5			nA

(1) The typical value includes one sigma statistical variation.

Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1300 apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 4.5\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $\text{INN} = \text{GND1} = 0\text{ V}$; minimum and maximum specifications of the AMC1300B apply from $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $\text{INN} = \text{GND1} = 0\text{ V}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
ANALOG OUTPUT							
	Nominal gain		8.2			V/V	
E _G	Gain error ⁽¹⁾	AMC1300, initial, at T _A = 25°C	−1%	0.4%	1%		
		AMC1300B, initial, at T _A = 25°C	−0.3%	±0.05%	0.3%		
TCE _G	Gain error drift ⁽¹⁾	AMC1300	±50			ppm/°C	
		AMC1300B	−50	±15	50		
	Nonlinearity ⁽¹⁾		−0.03%	±0.01%	0.03%		
	Nonlinearity drift		±1			ppm/°C	
THD	Total harmonic distortion	V _{IN} = 0.5 V, f _{IN} = 10 kHz, BW = 100 kHz	−85			dB	
	Output noise	V _{INP} = V _{INN} = GND1, BW = 100 kHz	230			μV _{RMS}	
SNR	Signal-to-noise ratio	V _{IN} = 0.5 V, f _{IN} = 1 kHz, BW = 10 kHz	80	85		dB	
		V _{IN} = 0.5 V, f _{IN} = 10 kHz, BW = 100 kHz	72				
PSRR	Power-supply rejection ratio ⁽²⁾	PSRR vs VDD1, at DC	−103			dB	
		PSRR vs VDD1, 100-mV and 10-kHz ripple	−96				
		PSRR vs VDD2, at DC	−106				
		PSRR vs VDD2, 100-mV and 10-kHz ripple	−86				
V _{CMout}	Common-mode output voltage		1.39	1.44	1.49	V	
V _{FAILSAFE}	Failsafe differential output voltage	V _{CM} ≥ V _{CMov} or VDD1 missing	−2.6			−2.5	V
BW	Output bandwidth	AMC1300	170	230		kHz	
		AMC1300B	250	310			
R _{OUT}	Output resistance	On OUTP or OUTN	< 0.2			Ω	
	Output short-circuit current		±13			mA	
CMTI	Common-mode transient immunity	GND1 − GND2 = 1 kV, AMC1300	15	30		kV/μs	
		GND1 − GND2 = 1 kV, AMC1300B	75	140			
POWER SUPPLY							
VDD1 _{UV}	VDD1 undervoltage detection threshold voltage	VDD1 falling	1.75	2.53	2.7	V	
IDD1	High-side supply current	AMC1300B only, 3.0 V ≤ VDD1 ≤ 3.6 V	6.3			8.5	mA
		4.5 V ≤ VDD1 ≤ 5.5 V	7.2			9.8	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V	5.3			7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V	5.9			8.1	

(2) This parameter is output referred.

7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time of OUTP, OUTN	See Figure 1		1.3		μs
t_f	Fall time of OUTP, OUTN	See Figure 1		1.3		μs
	INP, INN to OUTP, OUTN signal delay (50% – 10%)	AMC1300, unfiltered output, see Figure 1		1.5	2.2	μs
		INP, INN to OUTP, OUTN signal delay (50% – 50%)		1	1.5	
	INP, INN to OUTP, OUTN signal delay (50% – 90%)	AMC1300, unfiltered output, see Figure 1		2	2.7	μs
		AMC1300B, unfiltered output, see Figure 1		1.6	2.1	
	INP, INN to OUTP, OUTN signal delay (50% – 90%)	AMC1300, unfiltered output, see Figure 1		2.7	3.4	μs
		AMC1300B, unfiltered output, see Figure 1		2.5	3	
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 $\geq$ 3.0 V, to OUTP, OUTN valid, 0.1% settling		500		μs

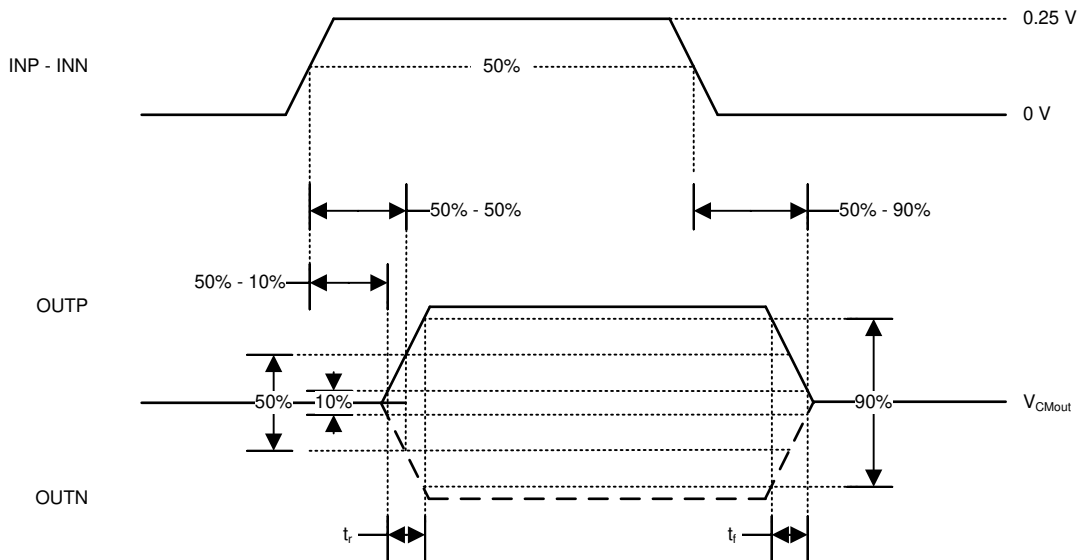


Figure 1. Rise, Fall, and Delay Time Waveforms

7.11 Insulation Characteristics Curves

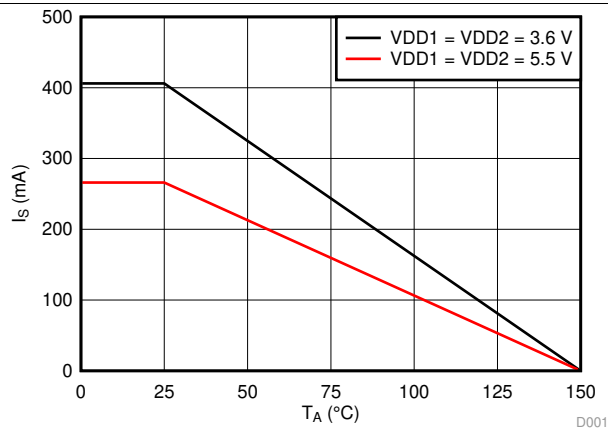


Figure 2. Thermal Derating Curve for Safety-Limiting Current per VDE

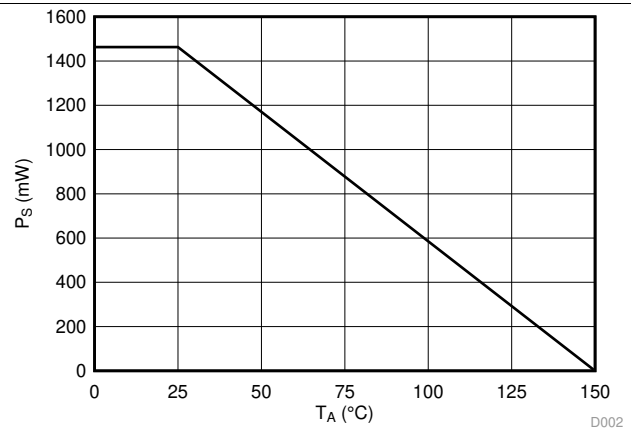
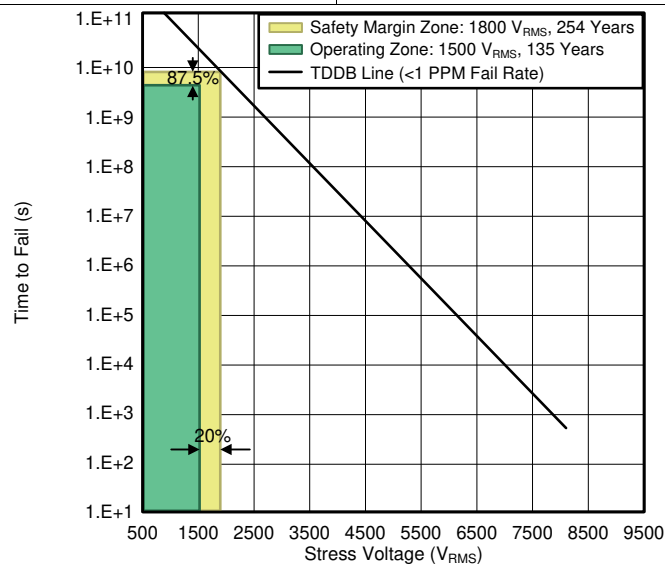


Figure 3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS} , operating lifetime = 135 year

Figure 4. Reinforced Isolation Capacitor Lifetime Projection

7.12 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

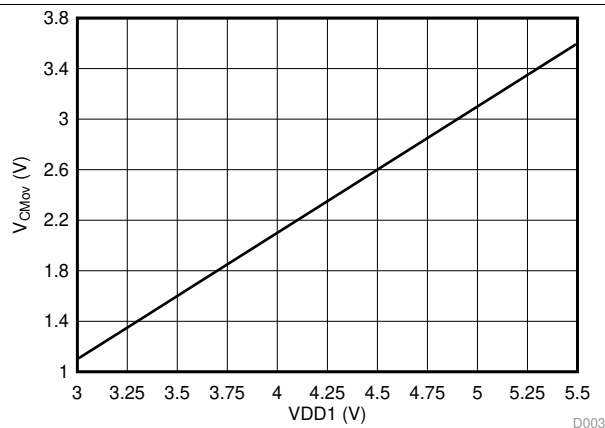


Figure 5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

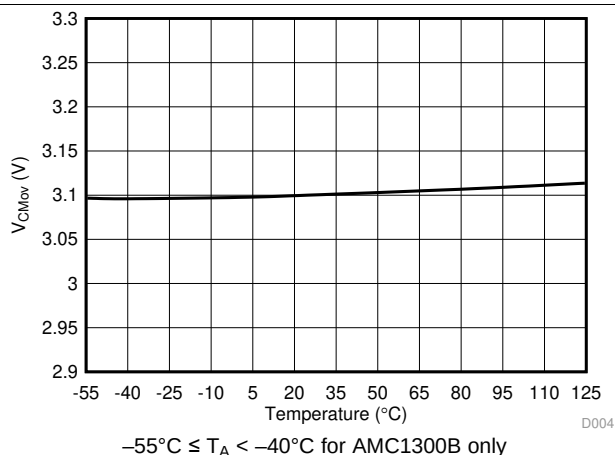


Figure 6. Common-Mode Overvoltage Detection Level vs Temperature

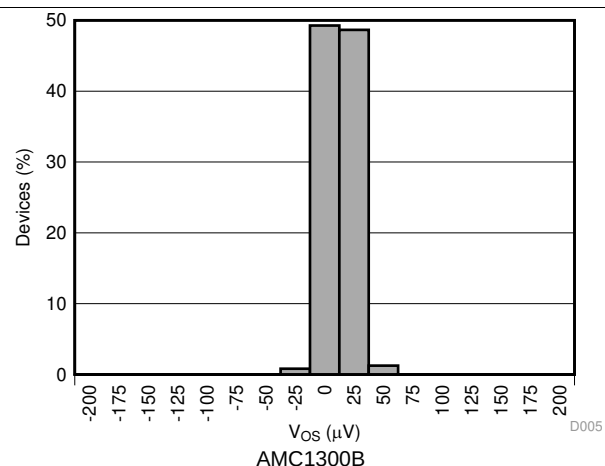


Figure 7. Input Offset Voltage Histogram

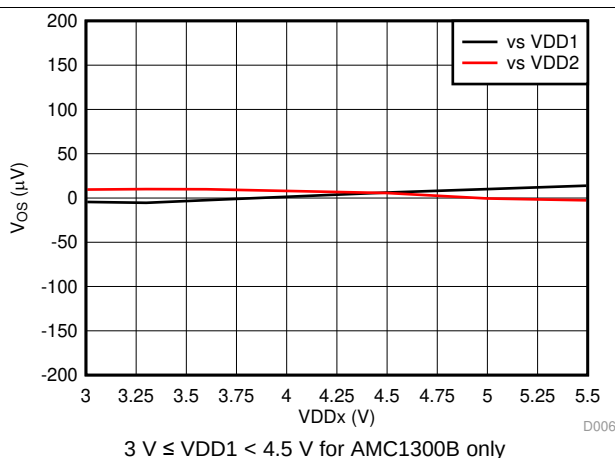


Figure 8. Input Offset Voltage vs Supply Voltage

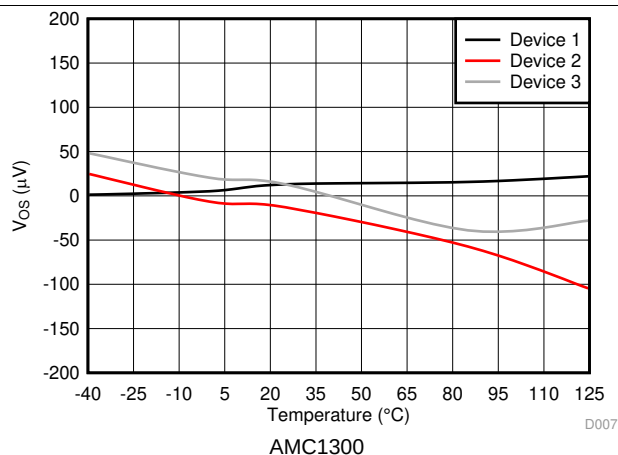


Figure 9. Input Offset Voltage vs Temperature

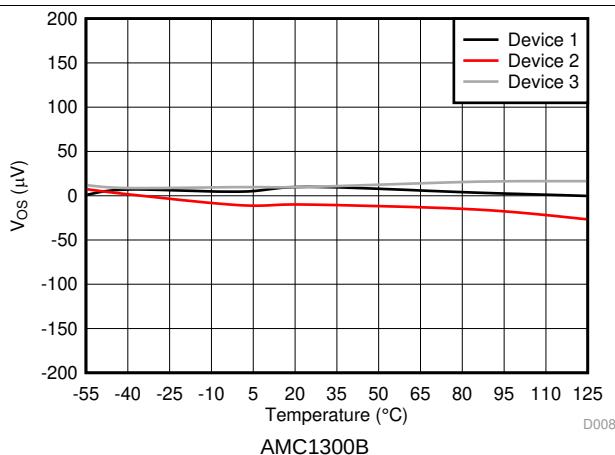


Figure 10. Input Offset Voltage vs Temperature

Typical Characteristics (continued)

at $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -250\text{ mV}$ to 250 mV , $V_{INN} = 0\text{ V}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

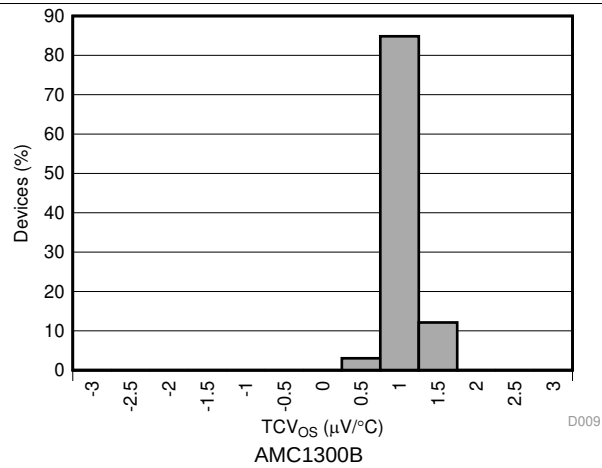


Figure 11. Input Offset Drift Histogram

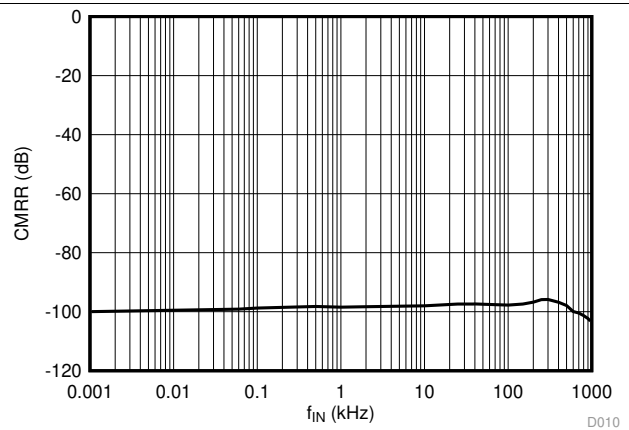


Figure 12. Common-Mode Rejection Ratio vs Input Frequency

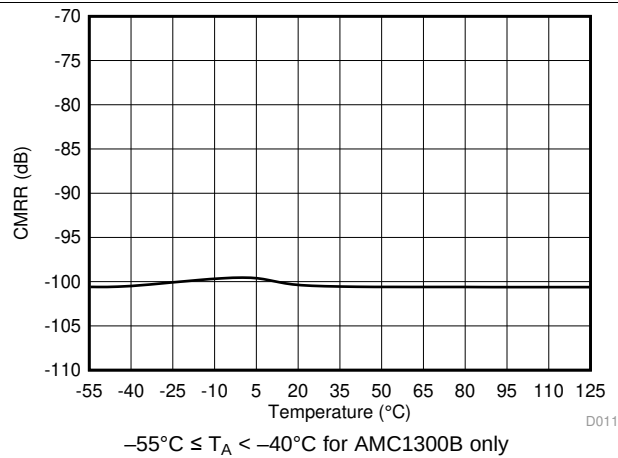


Figure 13. Common-Mode Rejection Ratio vs Temperature

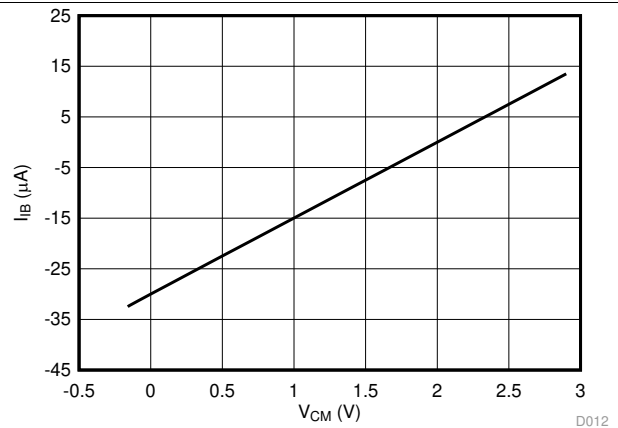


Figure 14. Input Bias Current vs Common-Mode Input Voltage

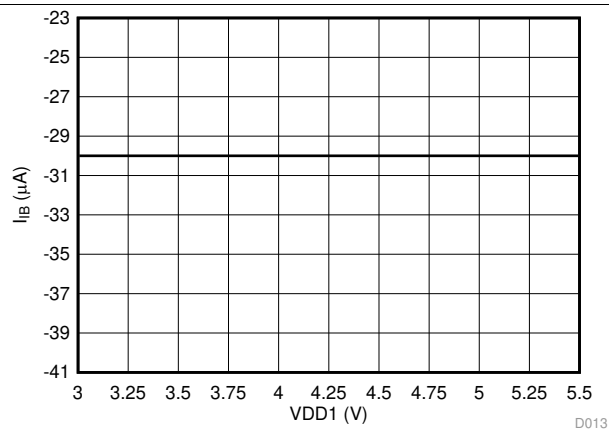


Figure 15. Input Bias Current vs High-Side Supply Voltage

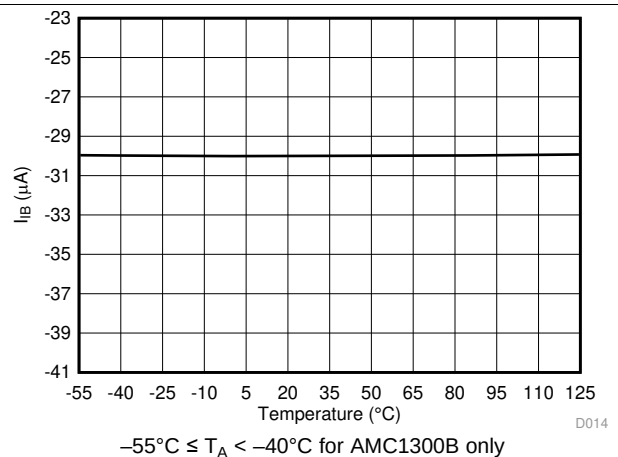


Figure 16. Input Bias Current vs Temperature

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

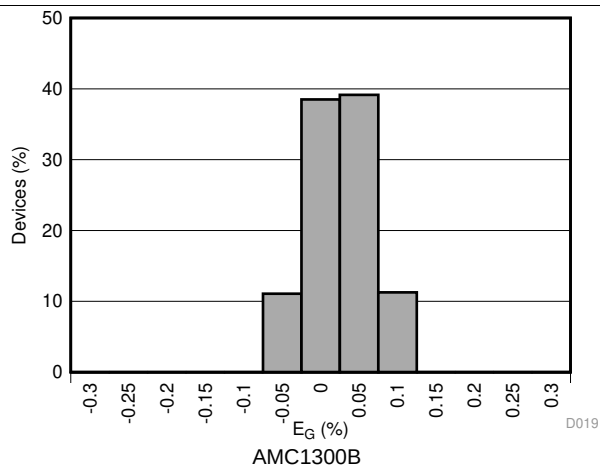


Figure 17. Gain Error Histogram

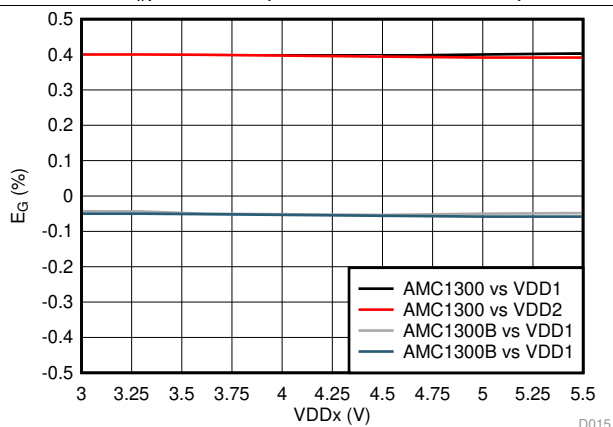


Figure 18. Gain Error vs Supply Voltage

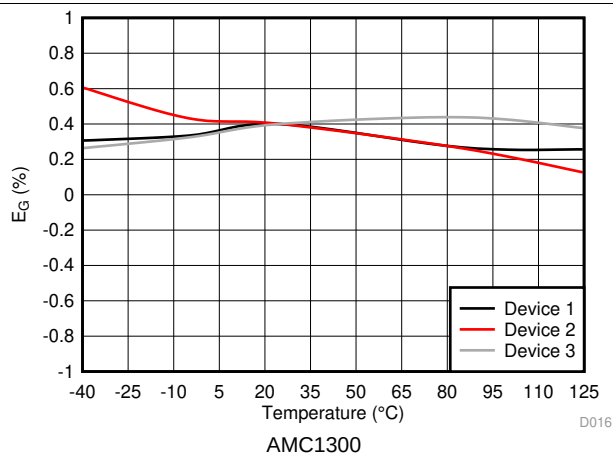


Figure 19. Gain Error vs Temperature

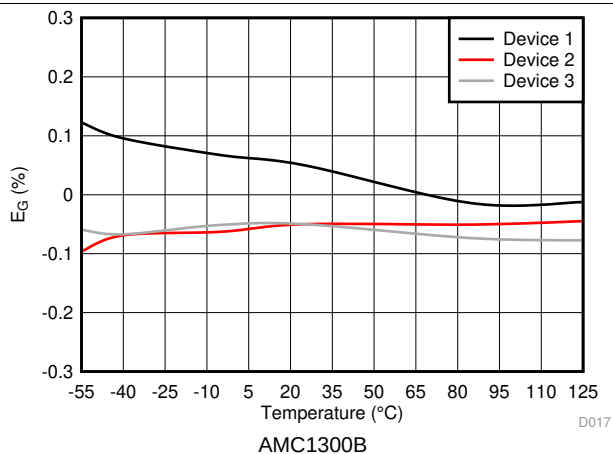


Figure 20. Gain Error vs Temperature

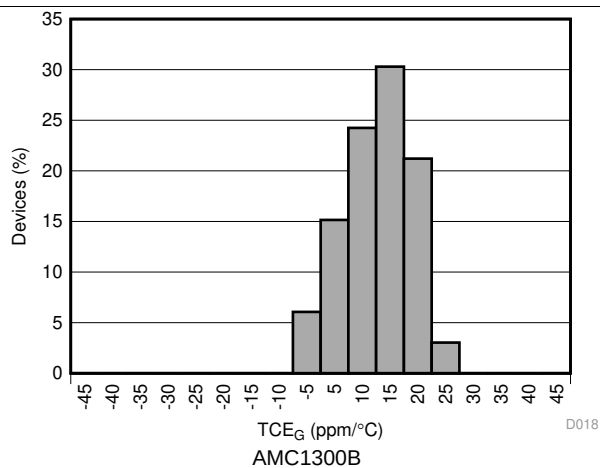


Figure 21. Gain Error Drift Histogram

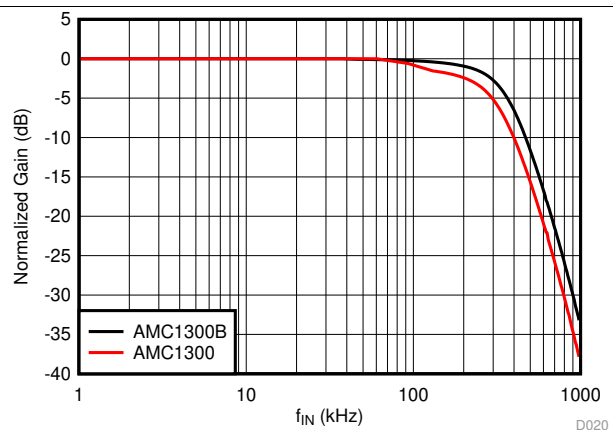


Figure 22. Normalized Gain vs Input Frequency

Typical Characteristics (continued)

at $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -250\text{ mV}$ to 250 mV , $V_{INN} = 0\text{ V}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

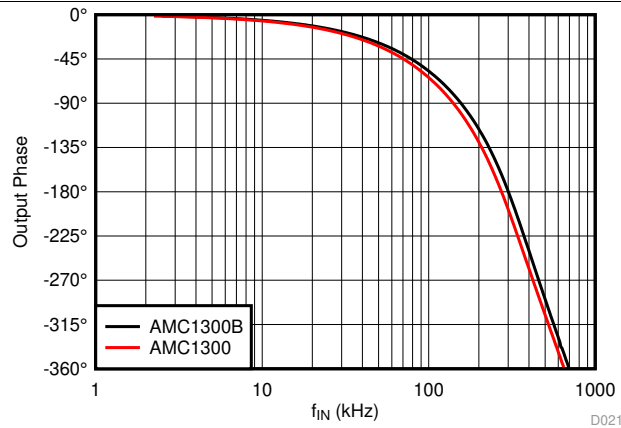


Figure 23. Output Phase vs Input Frequency

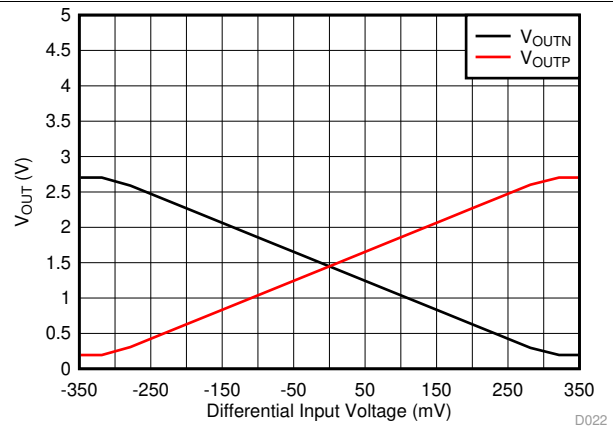


Figure 24. Output Voltage vs Input Voltage

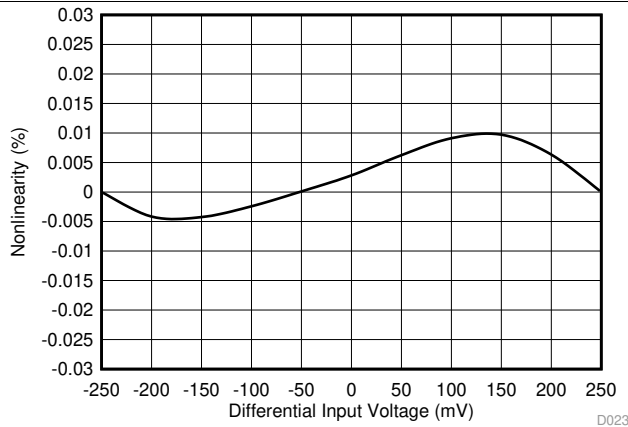


Figure 25. Nonlinearity vs Input Voltage

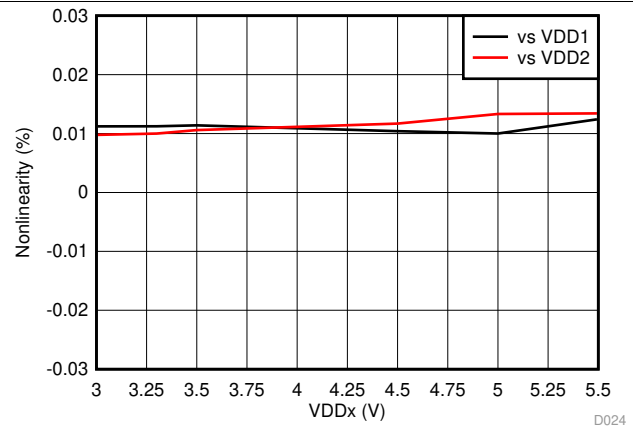
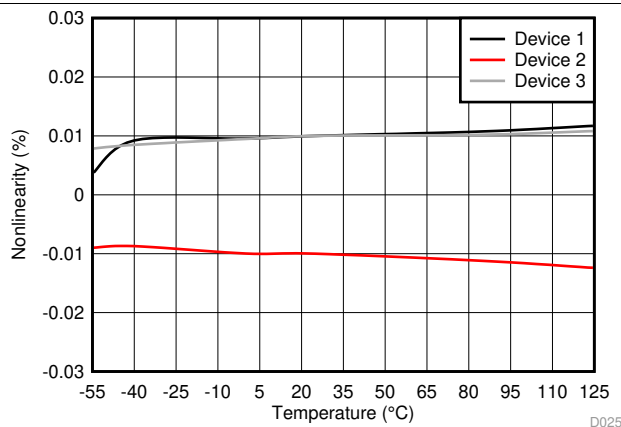
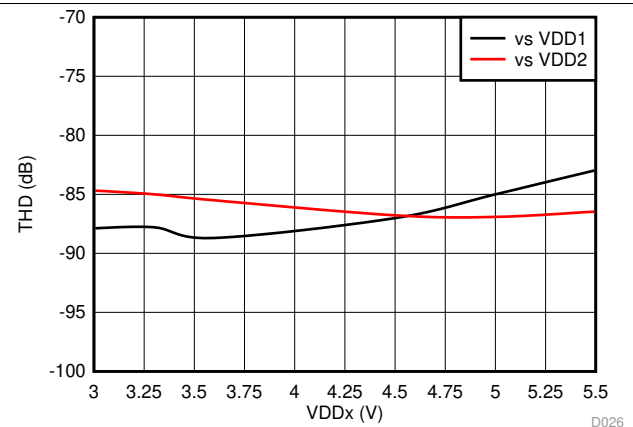


Figure 26. Nonlinearity vs Supply Voltage



$-55^{\circ}\text{C} \leq T_A < -40^{\circ}\text{C}$ for AMC1300B only

Figure 27. Nonlinearity vs Temperature



$3\text{ V} \leq V_{DD1} < 4.5\text{ V}$ for AMC1300B only

Figure 28. Total Harmonic Distortion vs Supply Voltage

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

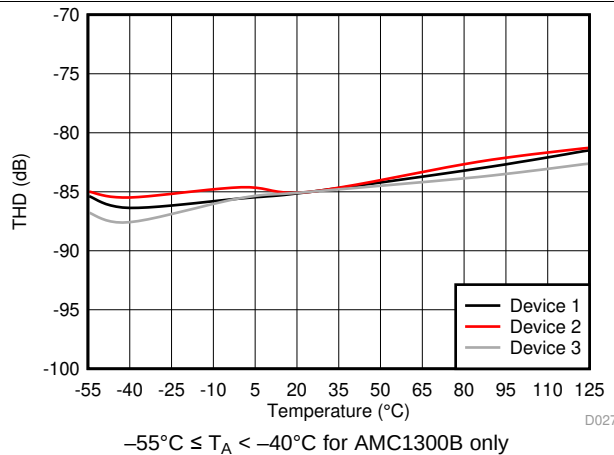


Figure 29. Total Harmonic Distortion vs Temperature

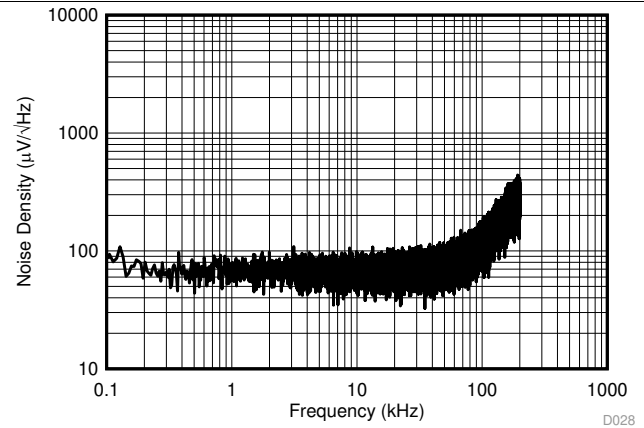


Figure 30. Input-Referred Noise Density vs Frequency

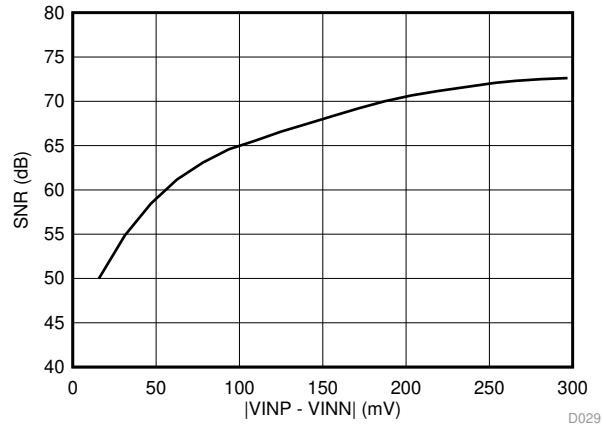


Figure 31. Signal-to-Noise Ratio vs Input Voltage

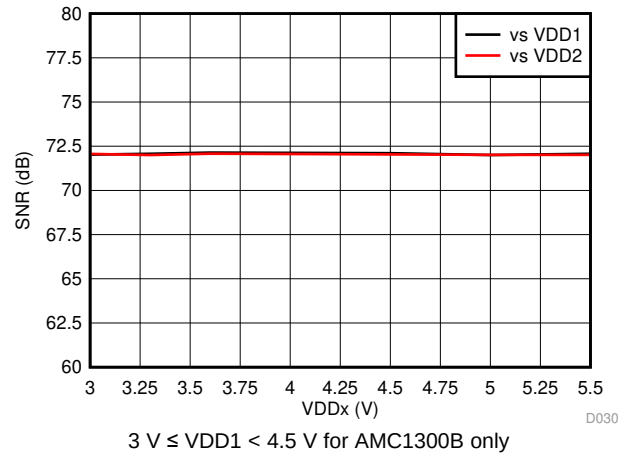


Figure 32. Signal-to-Noise Ratio vs Supply Voltage

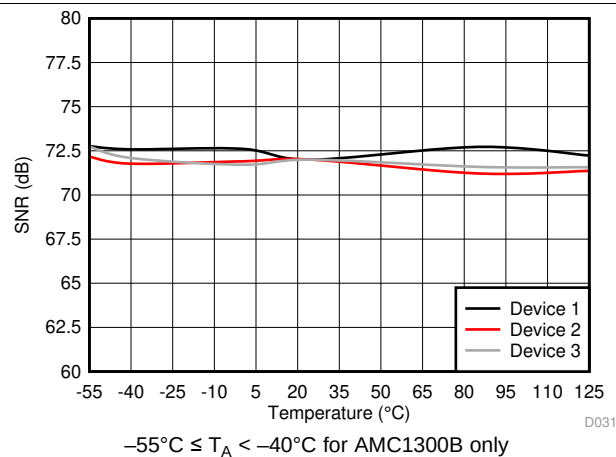


Figure 33. Signal-to-Noise Ratio vs Temperature

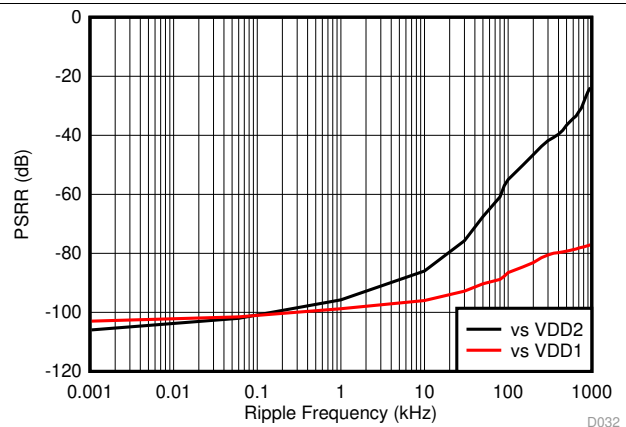


Figure 34. Power-Supply Rejection Ratio vs Ripple Frequency

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

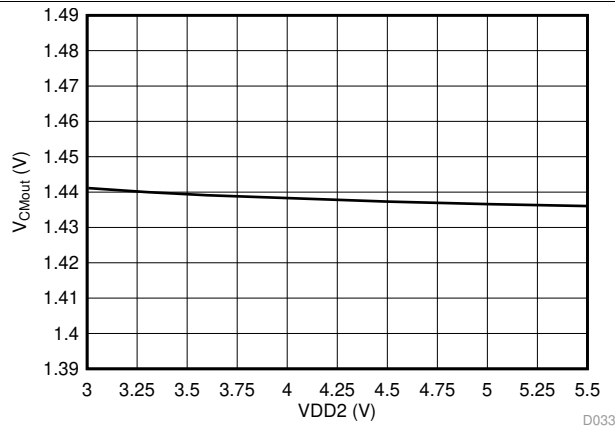


Figure 35. Output Common-Mode Voltage vs Low-Side Supply Voltage

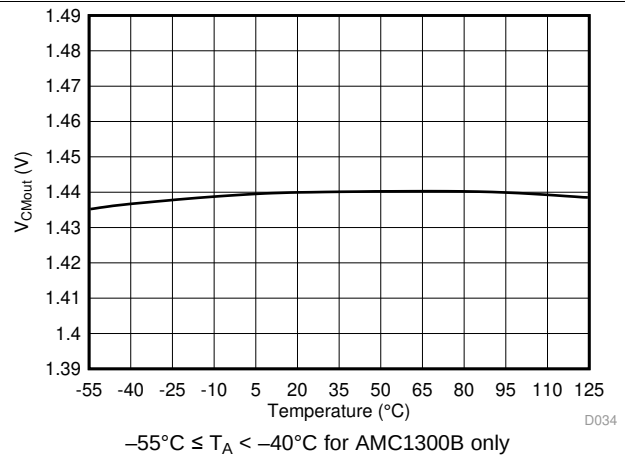


Figure 36. Output Common-Mode Voltage vs Temperature

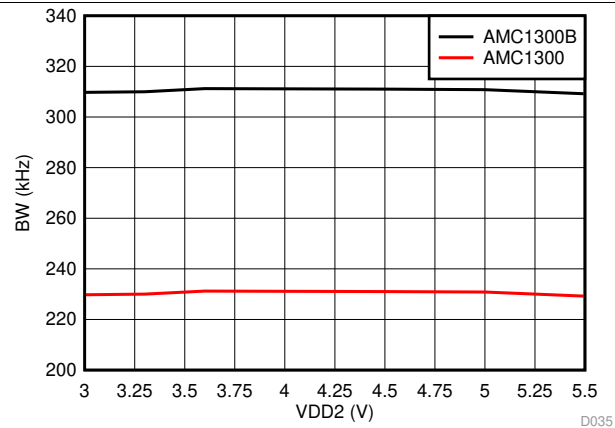


Figure 37. Output Bandwidth vs Low-Side Supply Voltage

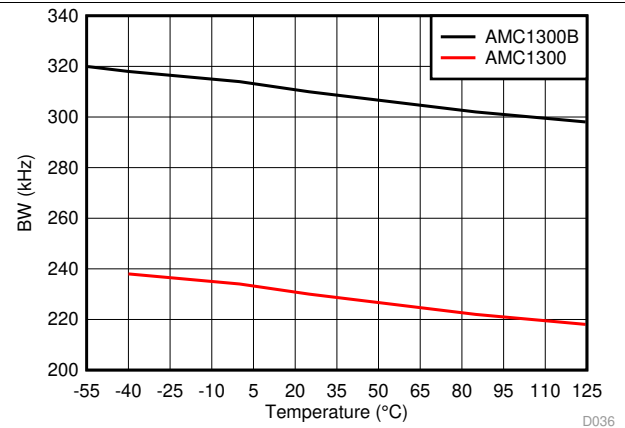


Figure 38. Output Bandwidth vs Temperature

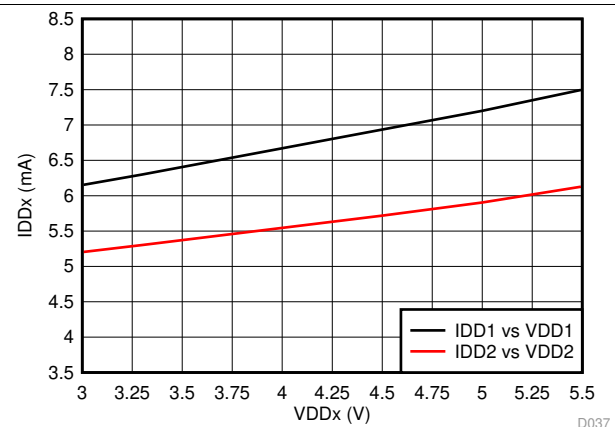


Figure 39. Supply Current vs Supply Voltage

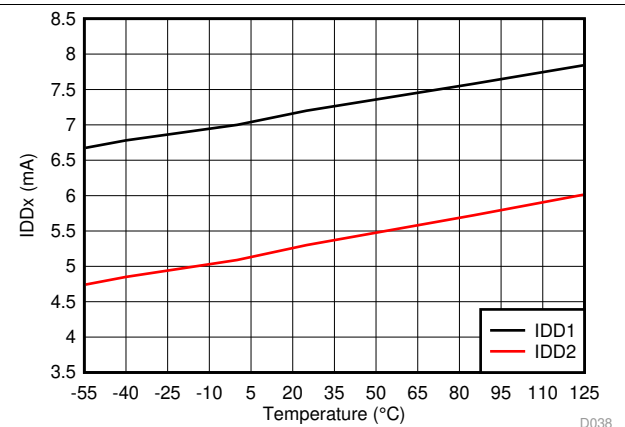


Figure 40. Supply Current vs Temperature

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

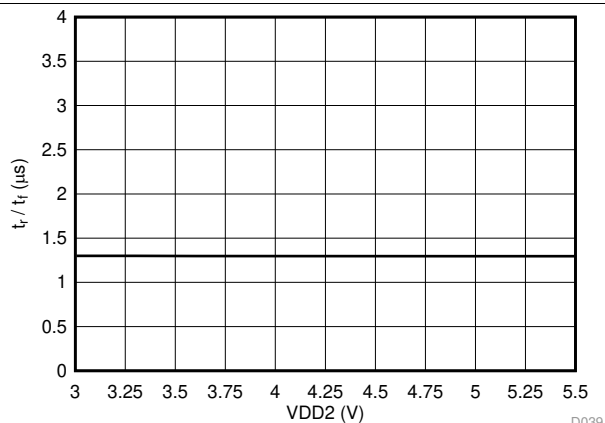


Figure 41. Output Rise and Fall Time vs Low-Side Supply

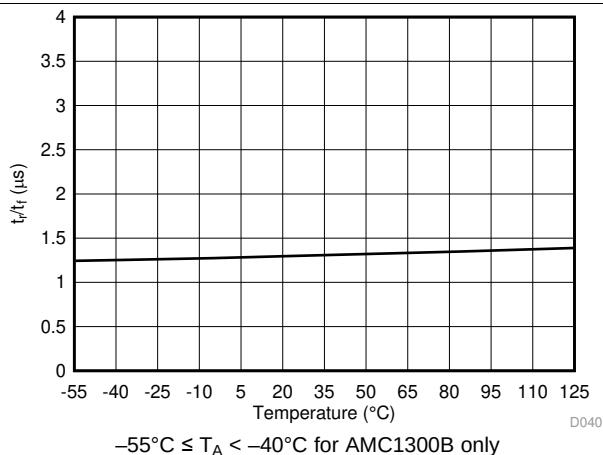


Figure 42. Output Rise and Fall Time vs Temperature

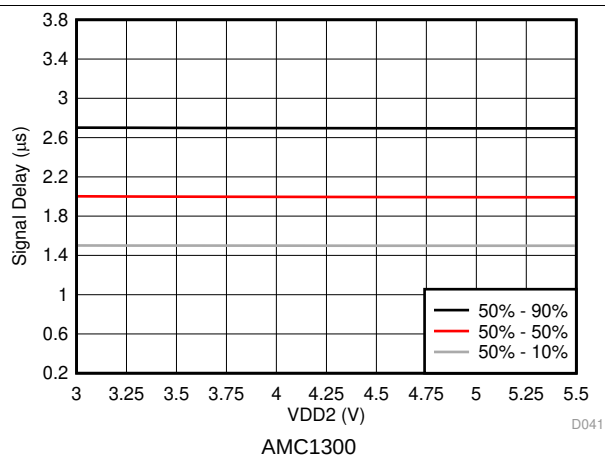


Figure 43. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

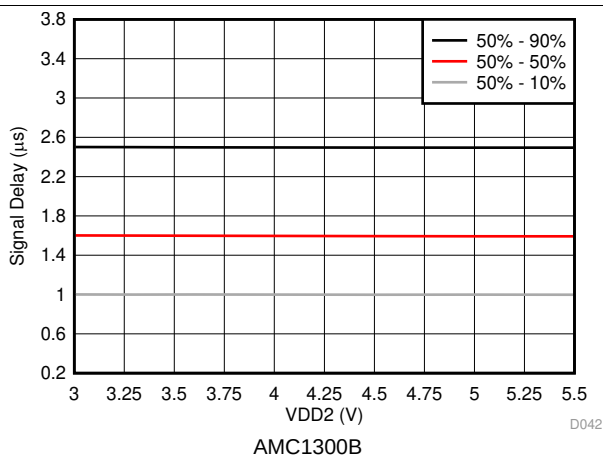


Figure 44. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

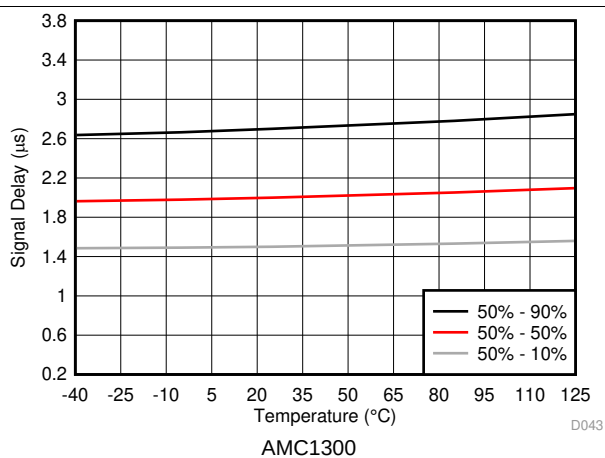


Figure 45. V_{IN} to V_{OUT} Signal Delay vs Temperature

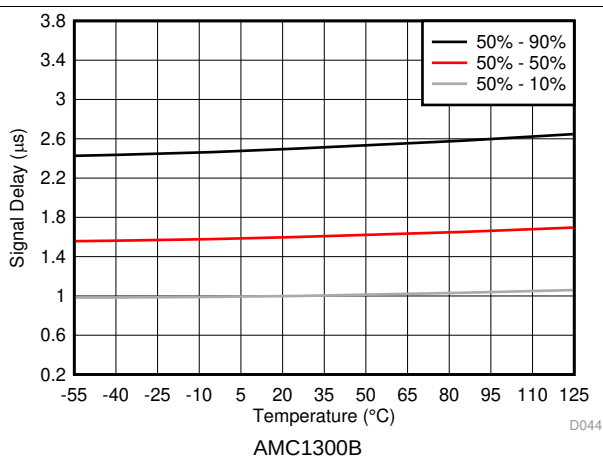


Figure 46. V_{IN} to V_{OUT} Signal Delay vs Temperature

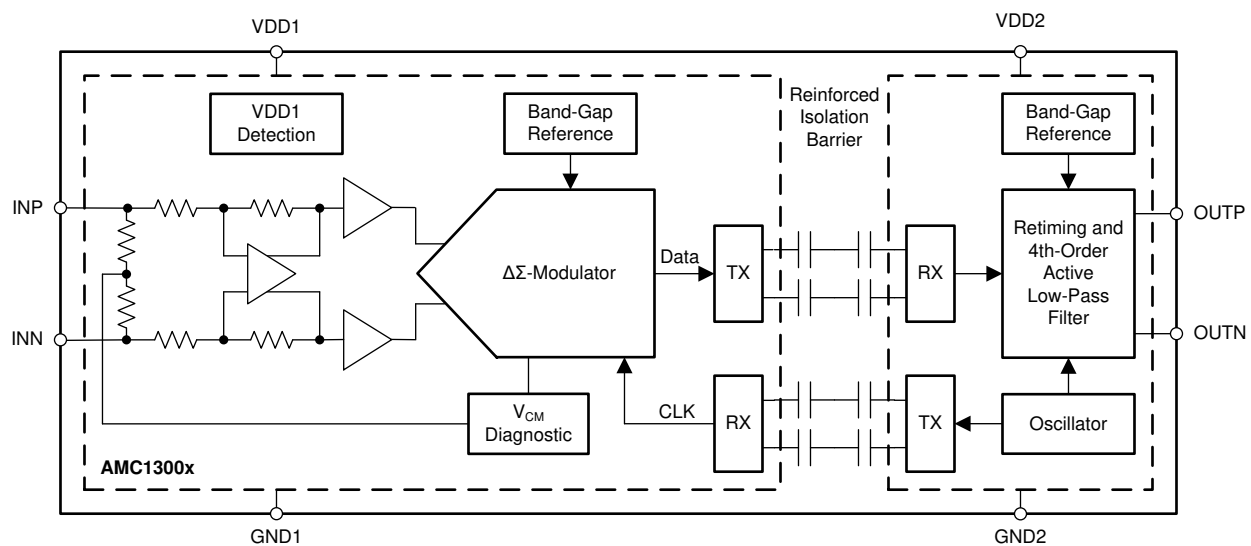
8 Detailed Description

8.1 Overview

The AMC1300 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called TX in the [Functional Block Diagram](#)) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed, as shown in the [Functional Block Diagram](#), by a fourth-order analog filter on the low-side and presented as a differential output of the device.

The SiO₂-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in [ISO72x Digital Isolator Magnetic-Field Immunity](#). The digital modulation used in the AMC1300 and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The differential amplifier input stage of the AMC1300 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 22 k Ω . The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

There are two restrictions on the analog input signals (V_{INP} and V_{INN}). First, if the input voltage exceeds the range $GND1 - 6\text{ V}$ to $VDD1 + 0.5\text{ V}$, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

Feature Description (continued)

8.3.2 Isolation Channel Signal Transmission

The AMC1300 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO₂-based isolation barrier. As shown in [Figure 47](#), the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the AMC1300 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The AMC1300 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

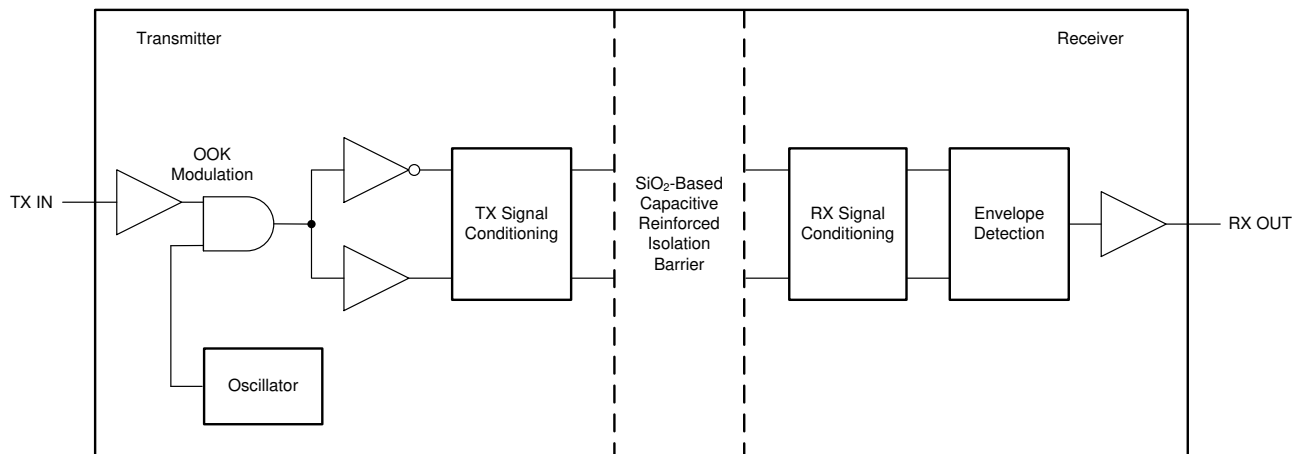


Figure 47. Block Diagram of an Isolation Channel

[Figure 48](#) shows the concept of the OOK scheme.

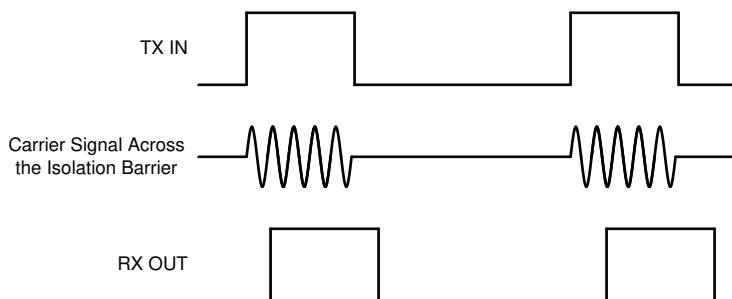


Figure 48. OOK-Based Modulation Scheme

Feature Description (continued)

8.3.3 Fail-Safe Output

The AMC1300 offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the AMC1300 is missing, or
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the minimum common-mode overvoltage detection level V_{CMOV} of $V_{DD1} - 2\text{ V}$.

Figure 49 and Figure 50 show the fail-safe output of the AMC1300 as a negative differential output voltage value that does not occur under normal device operation. Use the $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for the fail-safe detection on a system level.



Figure 49. Typical Negative Clipping Output of the AMC1300



Figure 50. Typical Fail-Safe Output of the AMC1300

8.4 Device Functional Modes

The AMC1300 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table in the [Specifications](#) section.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the AMC1300 a high-performance solution for industrial applications where shunt-based current sensing with high common-mode voltage levels is required.

9.2 Typical Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, and other industrial applications. The input structure of the AMC1300 is optimized for use with low-value shunt resistors in current sensing applications.

Figure 51 depicts a typical operation of the AMC1300 for current sensing in a frequency inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the AMC1300 ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive). The high-impedance input and wide input voltage range make the AMC1311 suitable for DC bus voltage sensing.

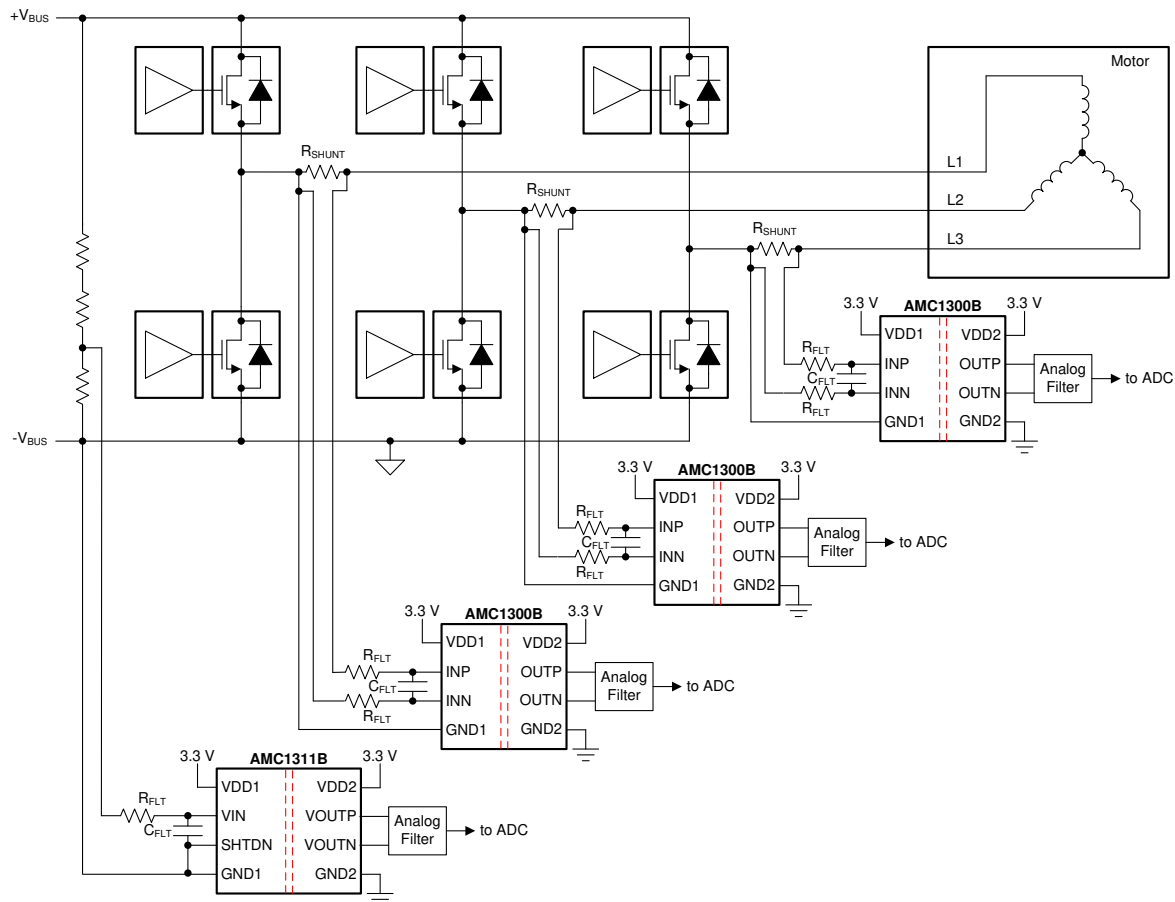


Figure 51. Using the AMC1300 for Current Sensing in Frequency Inverters

Typical Application (continued)

9.2.1 Design Requirements

Table 1 lists the parameters for this typical application.

Table 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	± 250 mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	3 μs (maximum)

9.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the AMC1300 is derived from the power supply of the upper gate driver. Further details are provided in the [Power Supply Recommendations](#) section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1300 (INN). If a four-pin shunt is used, the inputs of the AMC1300 device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT} :

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250 \text{ mV}$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$

For systems using single-ended input ADCs, Figure 52 shows an example of a TLV6001-based signal conversion and filter circuit as used on the AMC1311EVM. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

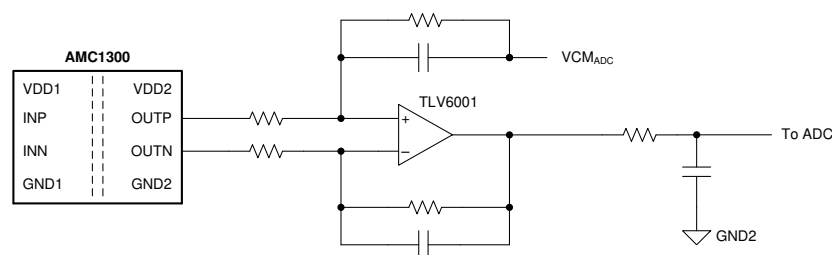


Figure 52. Connecting the AMC1300 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guides, available for download at www.ti.com.

9.2.3 Application Curves

In frequency inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. Figure 53 shows the typical full-scale step response of the AMC1300. Consider the delay of the required window comparator and the micro control unit (MCU) to calculate the overall response time of the system.



Figure 53. Step Response of the AMC1300

The high linearity and low temperature drift of offset and gain errors of the AMC1300, as shown in Figure 54, allow design of motor drives with low torque ripple.

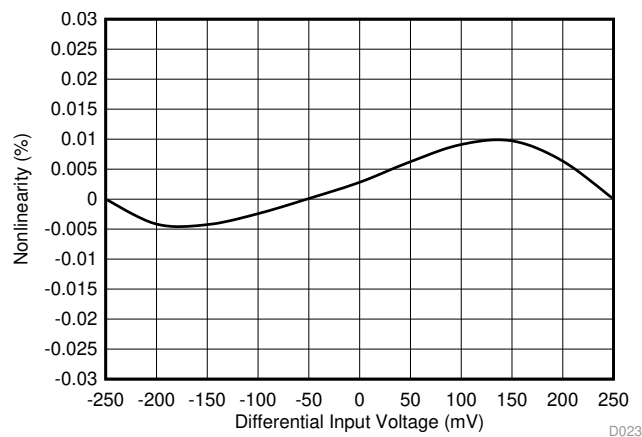


Figure 54. Typical Nonlinearity of the AMC1300

9.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1300 unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives these inputs to the output common-mode of the analog front-end of approximately 2 V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and the output functions as described in the [Fail-Safe Output](#) section, which may lead to an undesired reaction on the system level.

11 Layout

11.1 Layout Guidelines

Figure 56 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1300 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1300 and keep the layout of both connections symmetrical.

11.2 Layout Example

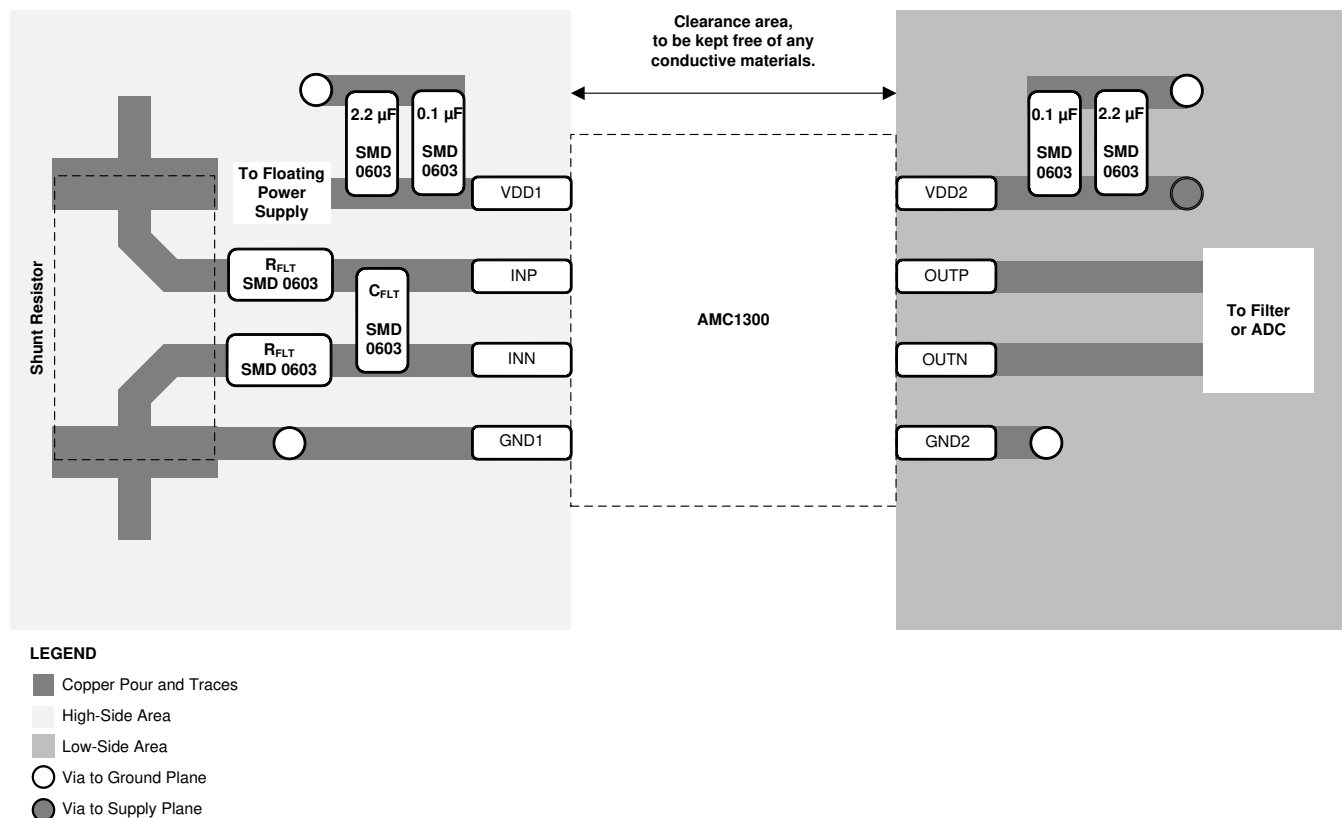


Figure 56. Recommended Layout of the AMC1300

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary](#) application report
- Texas Instruments, [ADSxxx3 Dual, 1-MSPS, 16-, 14-, and 12-Bit, 4×2 or 2×2 Channel, Simultaneous Sampling Analog-to-Digital Converter](#) data sheet
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application report
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity](#) application report
- Texas Instruments, [AMC1311x High-Impedance, 2-V Input, Reinforced Isolated Amplifier](#) data sheet
- Texas Instruments, [TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#) data sheet
- Texas Instruments, [AMC1311EVM](#) user guide
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) reference guide
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guide
- Texas Instruments, [LM117, LM317-N Wide Temperature Three-Pin Adjustable Regulator](#) data sheet
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies](#) data sheet
- Texas Instruments, [High-Bandwidth Phase Current and DC-Link Voltage Sensing Reference Design for Three-Phase Inverters](#)
- Texas Instruments, [Three-Phase Inverter Reference Design Using Gate Driver With Built-in Dead Time Insertion](#)
- Texas Instruments, [High Accuracy Analog Front End Using 16-Bit SAR ADC with ±10V Measurement Range](#) Reference Design
- Texas Instruments, [2kW, 48V to 400V, >93% Efficiency, Isolated Bidirectional DC-DC Converter Reference Design for UPS](#)
- Texas Instruments, [Reference Design for Reinforced Isolation 3-Phase Inverter with Current, Voltage and Temp Protection](#)
- Texas Instruments, [Shunt-Based High Current Measurement \(200-A\) Reference Design with Reinforced Isolation Amplifier](#)
- Texas Instruments, [High Accuracy ±0.5% Current and Isolated Voltage Measurement Ref Design Using 24-Bit Delta-Sigma ADC](#)
- Texas Instruments, [Shunt-Based 200A Peak Current Measurement Reference Design Using Isolation Amplifier](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1300BDWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B	Samples
AMC1300BDWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B	Samples
AMC1300DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1300	Samples
AMC1300DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1300	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

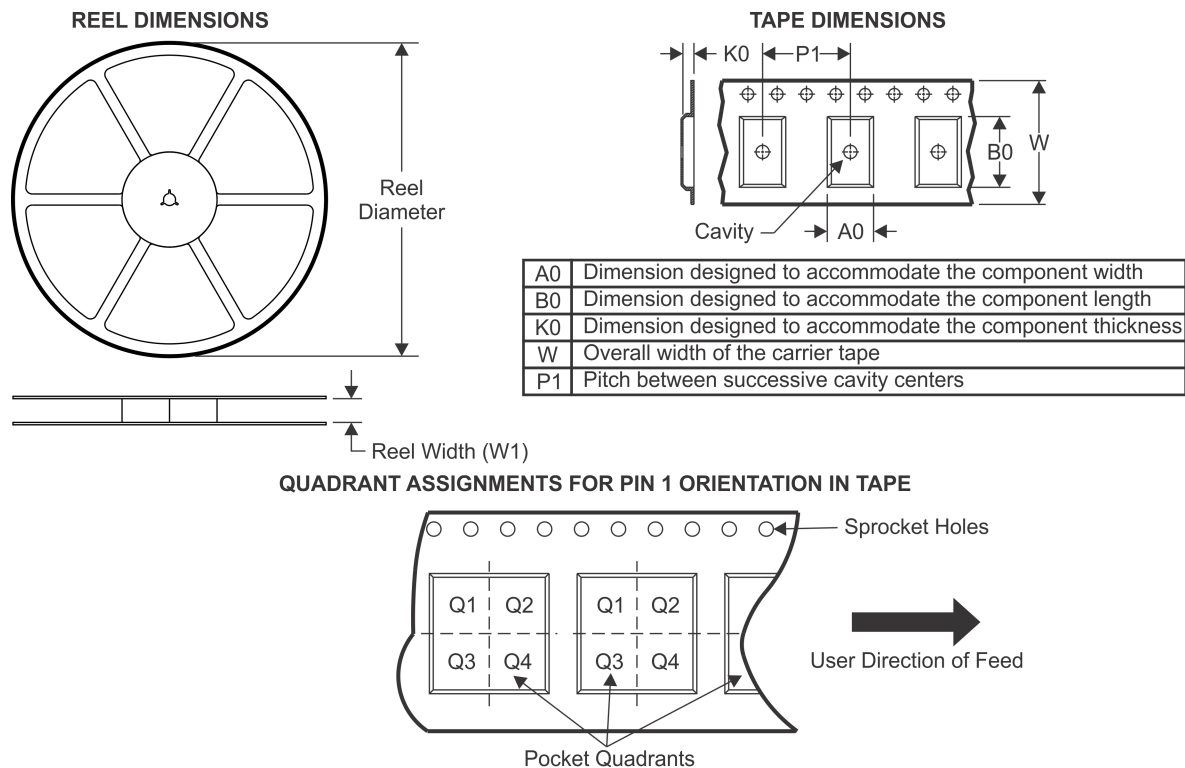
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

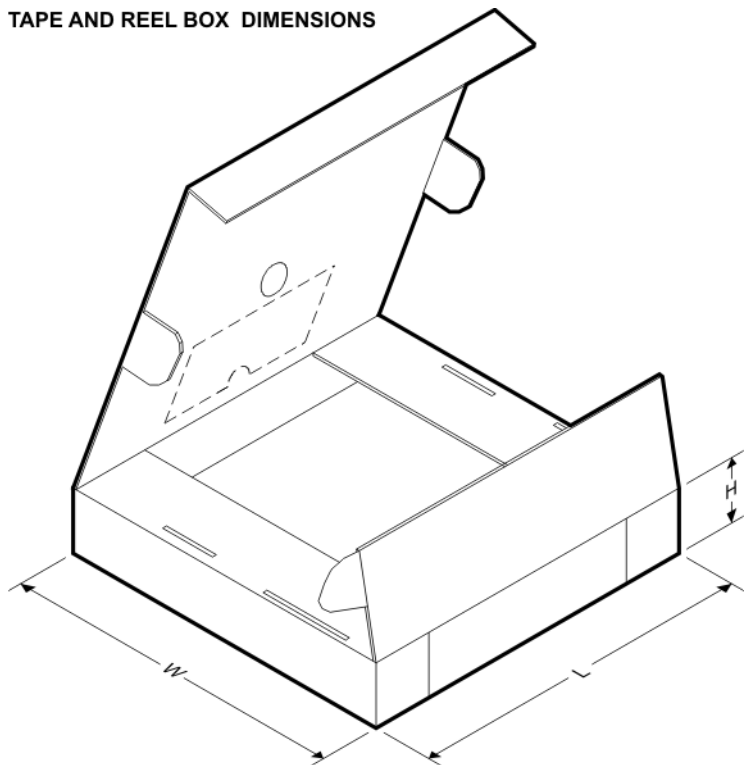
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1300BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1300DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

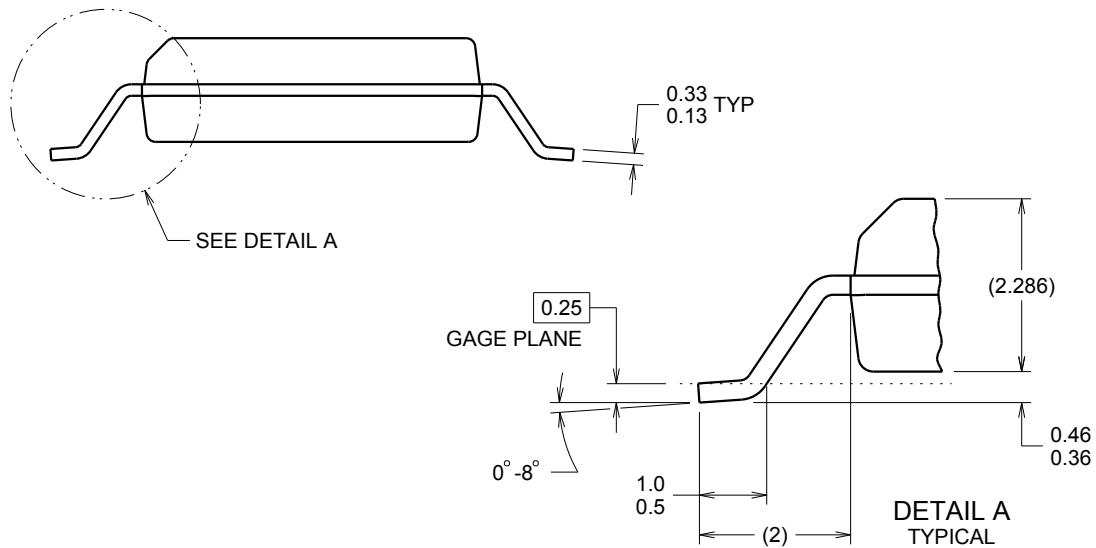


*All dimensions are nominal

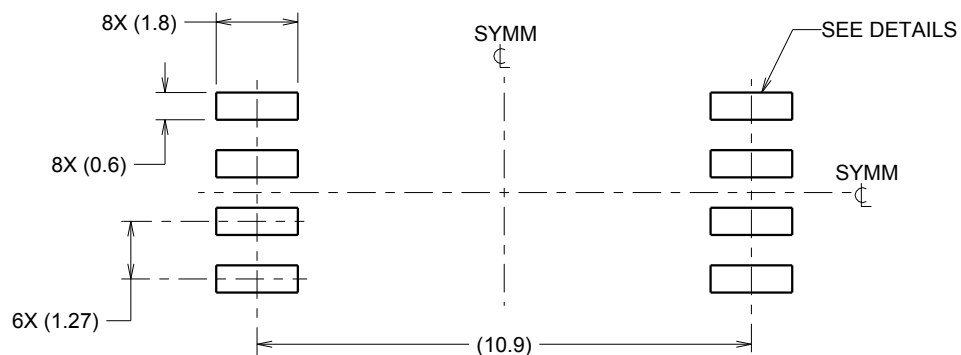
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1300BDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1300DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0

SOIC - 2.8 mm max height

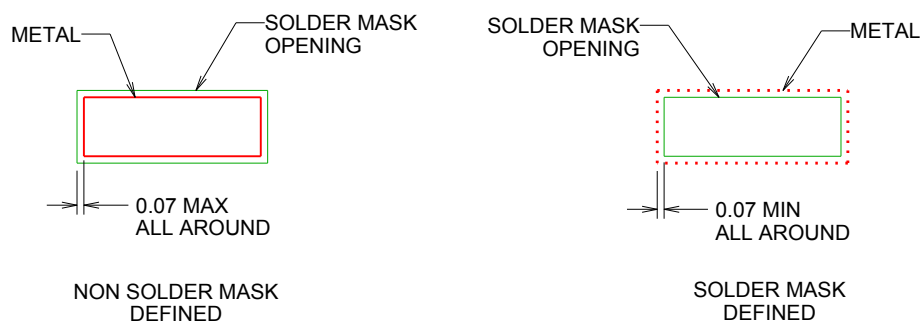
PIN 1 ID AREA
 11.5 ± 0.25 TYP
 5.95
 5.75
 NOTE 3
 4
 8
 6X 1.27
 2X 3.81
 5
 8X 0.51 / 0.31
 7.6
 7.4
 NOTE 4
 A
 B
 SEATING PLANE
 0.1 C
 2.8 MAX
 C
 A
 B



1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

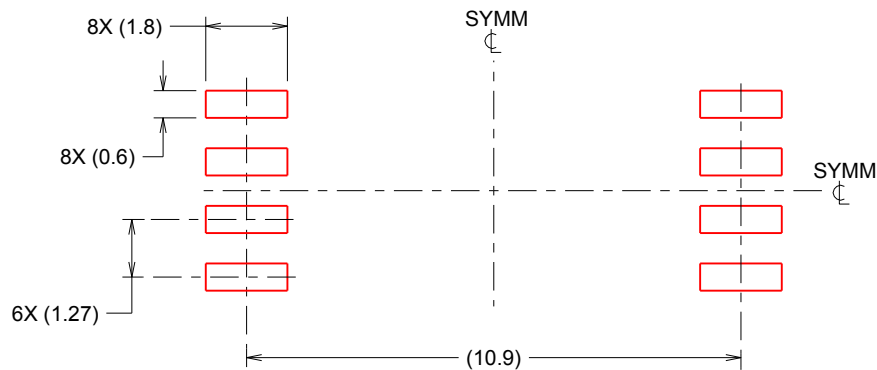


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated