PRELIMINARY

AMD

Am79C901A

HomePHY™
Single-Chip 1/10 Mbps Home Networking PHY

DISTINCTIVE CHARACTERISTICS

- **Fully integrated 1 Mbps HomePNA Physical Layer (PHY) as defined by Home Phoneline Networking Alliance (HomePNA) specification 1.1**
  - **— Optimized for home networking applications over existing telephone wire**
  - **— Media Independent Interface (MII)-compatible for connecting external Media Access Controller (MAC)**
  - **— In-band control features:**
    - **Adjustable power and speed levels**
    - **32 bits of reserved in-band messaging piggy-backed on Ethernet packet**
  - **— Register programmable features:**
    - **Power control**
    - **Speed control**
    - **Performance registers**
    - **Optional control of Squelch algorithm**
    - **Major frame timing parameters programmable: ISBI, AID ISBI, pulse width, inter-symbol time**
  - **— any1Home™ link detection:**
    - **Indicates to the MAC that a valid home networking node has been detected**
    - **Detects a network failure and allows the upper layer protocol to take corrective action**
- **Fully integrated 10 Mbps Ethernet transceiver**
  - **— Comprehensive Auto-Negotiation implementation**
  - **— IEEE 802.3u-compliant MII**
  - **— Full-duplex operation supported on the MII port with independent Transmit (TX) and Receive (RX) channels**
  - **— Optimized for 10BASE-T applications**
- **Compliant with HomePNA specification 1.1**
- **General Purpose Serial Interface (GPSI)/Serial Peripheral Interface (SPI)**
- **Extensive programmable internal/external loopback capabilities**
- **Extensive LED status support**
- **IEEE 1149.1-compliant JTAG Boundary Scan test access port interface**
- **Very low power consumption**
- **+3.3 V power supply along with 5 V tolerant I/Os enable broad system compatibility**
  - **— XTAL1 supports 3.3 V I/O only**
  - **— XTAL2 supports 1.0 V I/O only**
- **Available in 68-pin PLCC and 80-pin TQFP packages**
- **Industrial Temperature Support (-40ºC to +85ºC)**

GENERAL DESCRIPTION

The Am79C901A HomePHY is a single-chip device that contains both a physical layer (PHY) for 1 Mbps data networking over existing residential telephone wiring based on the specification published by HomePNA and a physical layer for supporting the IEEE 802.3 standard for 10BASE-T. The HomePHY is targeted at embedded applications and has both GPSI and MII-compatible interfaces.

The integrated HomePNA transceiver is a physical layer device that enables data networking at speeds up to 1 Mbps over existing residential phone wiring regardless of topology and without disrupting telephone (POTS) service.

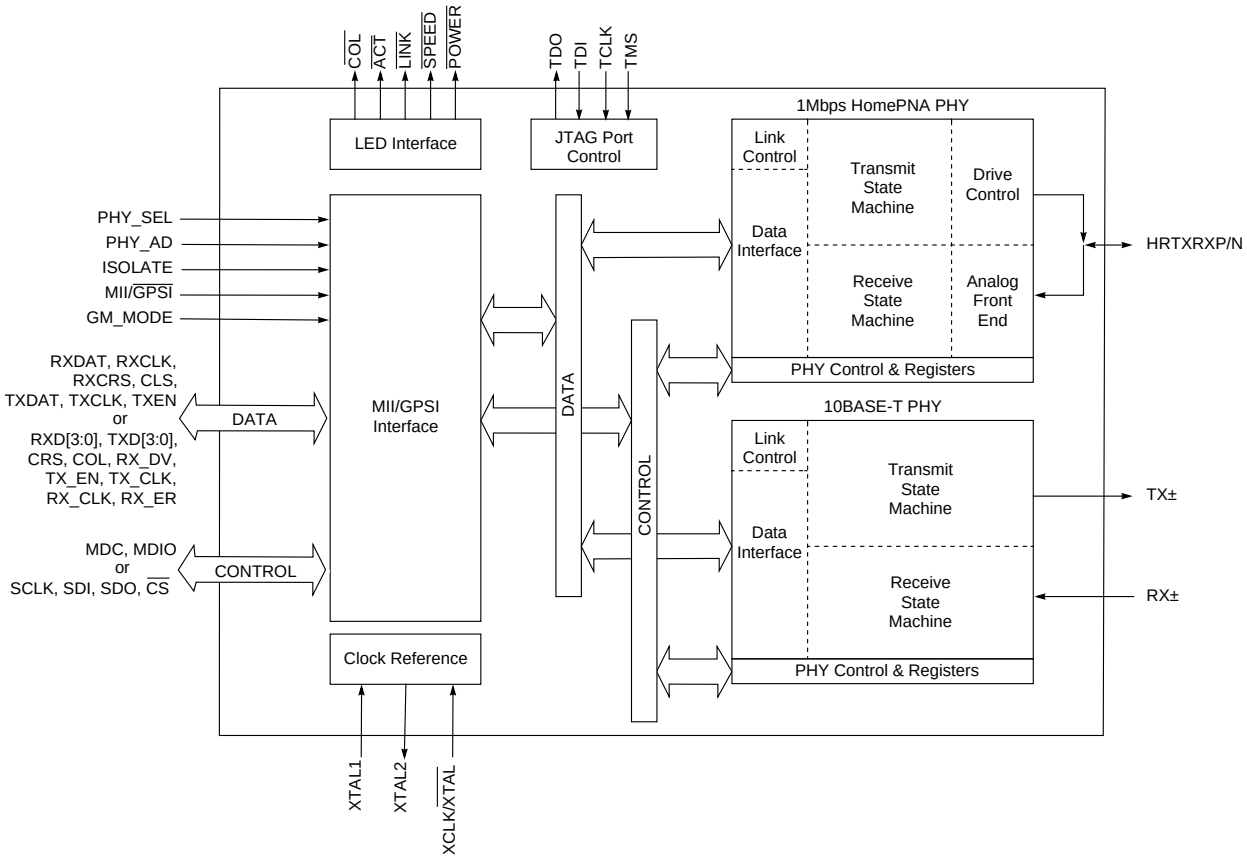
The integrated Ethernet transceiver is a physical layer device supporting the IEEE 802.3 standard for 10BASE-T. It provides all of the PHY layer functions required to support 10 Mbps data transfer speeds. A compliant IEEE 1149.1 JTAG test interface for board level testing is provided. The Am79C901A PHY also provides on-chip LED drivers for collision, link integrity, speed, activity, and power output.

The Am79C901A PHY is fabricated in an advanced low power 3.3 V CMOS process to provide low operating current for power sensitive applications.

The Am79C901A PHY is available in the commercial temperature range (0ºC to +70ºC) in 68-pin PLCC and 80-pin TQFP packages. The Am79C901A also supports the industrial temperature range (-40ºC to +85ºC) in the 80-pin TQFP package. The industrial temperature range is well suited to environments with enclosures with restricted air flow or outdoor equipment.

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BLOCK DIAGRAM



22304B-1

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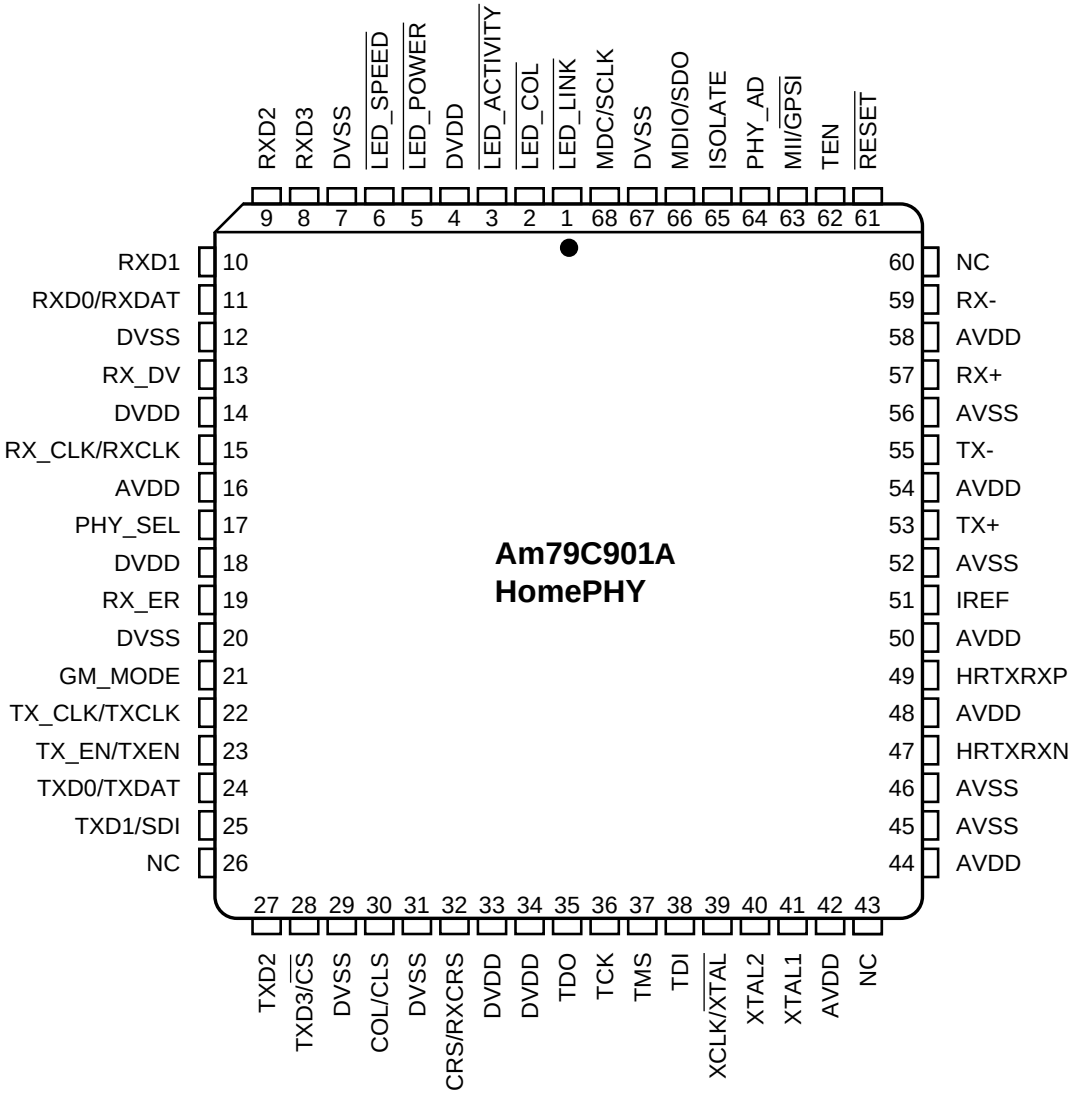
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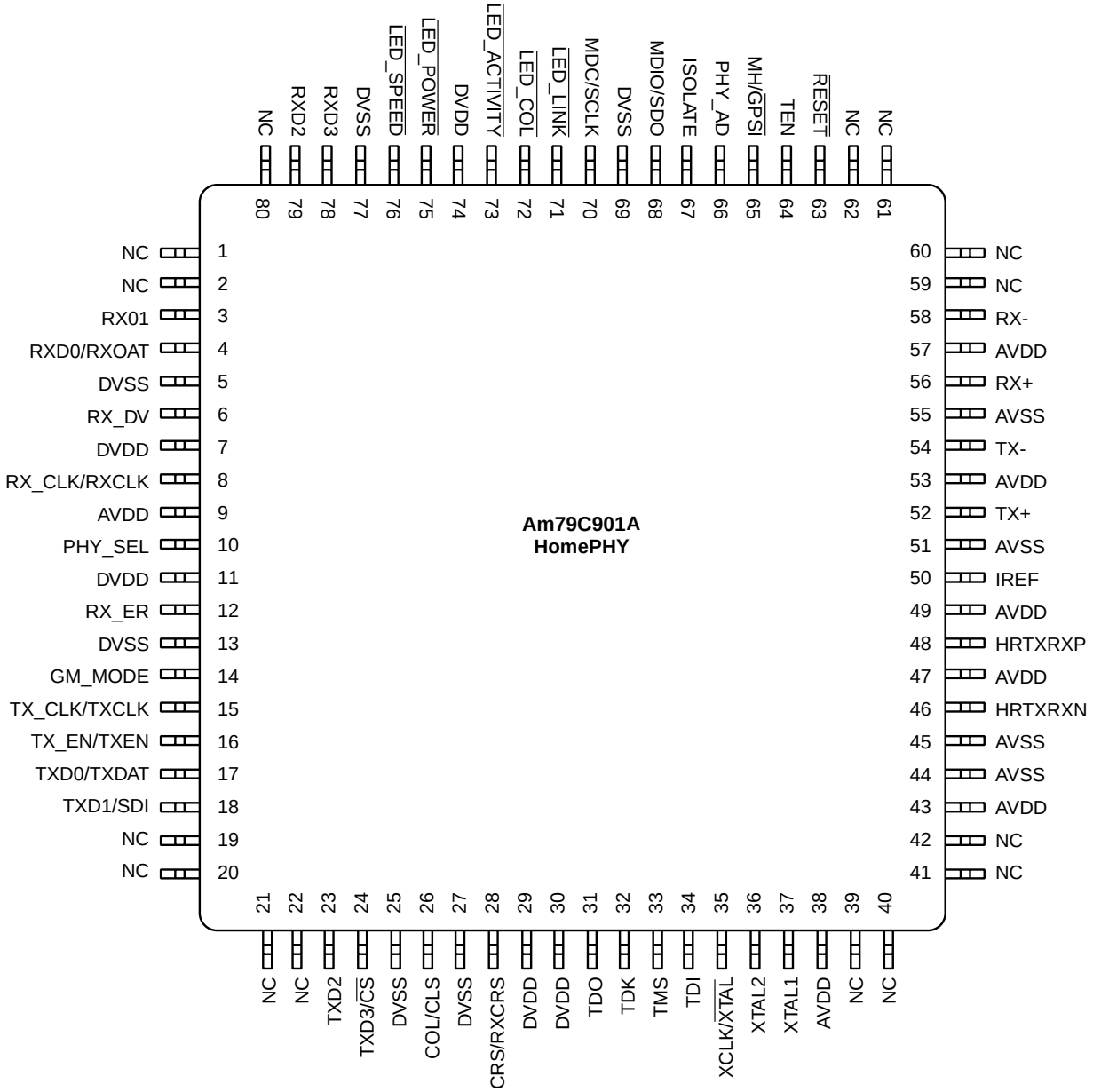
CONNECTION DIAGRAM (PL 068)



***Note**: NC pins are reserved and should be left unconnected.*

22304B-2

CONNECTION DIAGRAM (PQT 80)



***Note**: NC pins are reserved and should be left unconnected.*

22304B-

PIN DESIGNATIONS (PL 068)

Listed By Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	LED_LINK	18	DVDD	35	TDO	52	AVSS
2	LED_COL	19	RX_ER	36	TCK	53	TX+
3	LED_ACTIVITY	20	DVSS	37	TMS	54	AVDD
4	DVDD	21	GM_MODE	38	TDI	55	TX-
5	LED_POWER	22	TX_CLK/TXCLK	39	XCLK/XTAL	56	AVSS
6	LED_SPEED	23	TX_EN/TXEN	40	XTAL2	57	RX+
7	DVSS	24	TXD0/TXDAT	41	XTAL1	58	AVDD
8	RXD3	25	TXD1/SDI	42	AVDD	59	RX-
9	RXD2	26	NC	43	NC	60	NC
10	RXD1	27	TXD2	44	AVDD	61	RESET
11	RXD0/RXDAT	28	TXD3/CS	45	AVSS	62	TEN
12	DVSS	29	DVSS	46	AVSS	63	MII/GPSI
13	RX_DV	30	COL/CLS	47	HRTXRXN	64	PHY_AD
14	DVDD	31	DVSS	48	AVDD	65	ISOLATE
15	RX_CLK/RXCLK	32	CRS/RXCRS	49	HRTXRXP	66	MDIO/SDO
16	AVDD	33	DVDD	50	AVDD	67	DVSS
17	PHY_SEL	34	DVDD	51	IREF	68	MDC/SCLK

Note: *NC pins are reserved and should be left unconnected.*

PIN DESIGNATIONS (PQT 80)

Listed By Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	21	NC	41	NC	61	NC
2	NC	22	NC	42	NC	62	NC
3	RXD1	23	TXD2	43	AVDD	63	$\overline{\text{RESET}}$
4	RXD0/RXDAT	24	TXD3/$\overline{\text{CS}}$	44	AVSS	64	TEN
5	DVSS	25	DVSS	45	AVSS	65	MII/$\overline{\text{GPSI}}$
6	RX_DV	26	COL/CLS	46	HRTXRXN	66	PHY_AD
7	DVDD	27	DVSS	47	AVDD	67	ISOLATE
8	RX_CLK/RXCLK	28	CRS/RXCRS	48	HRTXRXP	68	MDIO/SDO
9	AVDD	29	DVDD	49	AVDD	69	DVSS
10	PHY_SEL	30	DVDD	50	IREF	70	MDC/SCLK
11	DVDD	31	TDO	51	AVSS	71	$\overline{\text{LED_LINK}}$
12	RX_ER	32	TCK	52	TX+	72	$\overline{\text{LED_COL}}$
13	DVSS	33	TMS	53	AVDD	73	$\overline{\text{LED_ACTIVITY}}$
14	GM_MODE	34	TDI	54	TX-	74	DVDD
15	TX_CLK/TXCLK	35	XCLK/$\overline{\text{XTAL}}$	55	AVSS	75	$\overline{\text{LED_POWER}}$
16	TX_EN/TXEN	36	XTAL2	56	RX+	76	$\overline{\text{LED_SPEED}}$
17	TXD0/TXDAT	37	XTAL1	57	AVDD	77	DVSS
18	TXD1/SDI	38	AVDD	58	RX-	78	RXD3
19	NC	39	NC	59	NC	79	RXD2
20	NC	40	NC	60	NC	80	NC

Note: *NC pins are reserved and should be left unconnected.*

PIN DESIGNATIONS (PL 068)

Listed By Group

Pin Name	Pin Function	Type	Driver Type	Number of Pins
Configuration				
MII/$\overline{\text{GPSI}}$	Selects MII or GPSI mode	I	–	1
GM_MODE	Selects MDC/MDIO and GPSI data	I	–	1
ISOLATE	Isolates device if register isolate bit is set = 1	I	–	1
PHY_SEL	Defines default PHY	I	–	1
PHY_AD	Defines bit 2 of the PHY address	I	–	1
Board Interface				
RESET	RESET	I	–	1
XCLK/$\overline{\text{XTAL}}$	Oscillator/Crystal Select	I	–	1
XTAL1	Crystal Input (20 MHz XTAL/60 MHz CLK)	I	–	1
XTAL2	Crystal Output (20 MHz XTAL)	O	XTAL	1
IREF	Tied to GND via a 12.1 kΩ 1% resistor	I	–	1
$\overline{\text{LED_COL}}$	Collision Indication	O	LED	1
$\overline{\text{LED_ACTIVITY}}$	Activity Indication	O	LED	1
$\overline{\text{LED_LINK}}$	Link Valid Indication	O	LED	1
$\overline{\text{LED_SPEED}}$	High Speed Indication	O	LED	1
$\overline{\text{LED_POWER}}$	High Power Indication	O	LED	1
1 Mbps HomePNA PHY Network Ports				
HRTXRXP/N	Receive/Transmit Data	I/O	–	2
10BASE-T PHY Network Ports				
TX±	Serial Transmit Data	O	–	2
RX±	Serial Receive Data	I	–	2
MII Interface				
TX_CLK	MII Transmit Clock	O	OMII	1
TXD[3:0]	MII Transmit Data	I	–	4
TX_EN	MII Transmit Enable	I	–	1
RX_CLK	MII Receive Clock	O	OMII	1
RXD[3:0]	MII Receive Data	O	OMII	4
RX_ER	MII Receive Error	O	OMII	1
RX_DV	MII Receive Data Valid	O	OMII	1
MDC	MII Management Data Clock	I	–	1
MDIO	MII Management Data Input/Output	I/O	TSMII	1
CRS	Carrier Sense	O	OMII	1
COL	Collision	O	OMII	1

Pin Name	Pin Function	Type	Driver Type	Number of Pins
GPSI Interface				
TXCLK	GPSI Transmit Clock	O	OMII	1
TXDAT	GPSI Transmit Data	I	–	1
TXEN	GPSI Transmit Enable	I	–	1
RXCLK	GPSI Receive Clock	O	OMII	1
RXDAT	GPSI Receive Data	O	OMII	1
RXCRS	Carrier Sense	O	OMII	1
CLS	Collision	O	OMII	1
SPI Interface				
SCLK	SPI Clock	I	–	1
SDI	SPI Data In	I	–	1
SDO	SPI Data Out	O	TSMII	1
$\overline{CS}$	Chip Select	I	–	1
IEEE 1149.1 (JTAG) Test Access Port Interface				
TCK	Test Clock	I	–	1
TMS	Test Mode Select	I	–	1
TDI	Test Data In	I	–	1
TDO	Test Data Out	O	TS	1
Power Supply				
DVDD	Digital Power	P	–	6
AVDD	Analog Power	P	–	6
DVSS	Digital Ground	G	–	7
AVSS	Analog Ground	G	–	3
Test Interface				
TEN	Test Enable	I	–	1

PIN DESIGNATIONS (PQT 80)

Listed By Group

Pin Name	Pin Function	Type	Driver Type	Number of Pins
Configuration				
MII/$\overline{\text{GPSI}}$	Selects MII or GPSI mode	I	–	1
GM_MODE	Selects MDC/MDIO and GPSI data	I	–	1
ISOLATE	Isolates device if register isolate bit is set = 1	I	–	1
PHY_SEL	Defines default PHY	I	–	1
PHY_AD	Defines bit 2 of the PHY address	I	–	1
Board Interface				
RESET	RESET	I	–	1
XCLK/$\overline{\text{XTAL}}$	Oscillator/Crystal Select	I	–	1
XTAL1	Crystal Input (20 MHz XTAL/60 MHz CLK)	I	–	1
XTAL2	Crystal Output (20 MHz XTAL)	O	XTAL	1
IREF	Tied to GND via a 12.1 kΩ 1% resistor	I	–	1
$\overline{\text{LED_COL}}$	Collision Indication	O	LED	1
$\overline{\text{LED_ACTIVITY}}$	Activity Indication	O	LED	1
$\overline{\text{LED_LINK}}$	Link Valid Indication	O	LED	1
$\overline{\text{LED_SPEED}}$	High Speed Indication	O	LED	1
$\overline{\text{LED_POWER}}$	High Power Indication	O	LED	1
1 Mbps HomePNA PHY Network Ports				
HRTXRXP/N	Receive/Transmit Data	I/O	–	2
10BASE-T PHY Network Ports				
TX±	Serial Transmit Data	O	–	2
RX±	Serial Receive Data	I	–	2
MII Interface				
TX_CLK	MII Transmit Clock	O	OMII	1
TXD[3:0]	MII Transmit Data	I	–	4
TX_EN	MII Transmit Enable	I	–	1
RX_CLK	MII Receive Clock	O	OMII	1
RXD[3:0]	MII Receive Data	O	OMII	4
RX_ER	MII Receive Error	O	OMII	1
RX_DV	MII Receive Data Valid	O	OMII	1
MDC	MII Management Data Clock	I	–	1
MDIO	MII Management Data Input/Output	I/O	TSMII	1
CRS	Carrier Sense	O	OMII	1
COL	Collision	O	OMII	1

Pin Name	Pin Function	Type	Driver Type	Number of Pins
GPSI Interface				
TXCLK	GPSI Transmit Clock	O	OMII	1
TXDAT	GPSI Transmit Data	I	–	1
TXEN	GPSI Transmit Enable	I	–	1
RXCLK	GPSI Receive Clock	O	OMII	1
RXDAT	GPSI Receive Data	O	OMII	1
RXCRS	Carrier Sense	O	OMII	1
CLS	Collision	O	OMII	1
SPI Interface				
SCLK	SPI Clock	I	–	1
SDI	SPI Data In	I	–	1
SDO	SPI Data Out	O	TSMII	1
$\overline{CS}$	Chip Select	I	–	1
IEEE 1149.1 (JTAG) Test Access Port Interface				
TCK	Test Clock	I	–	1
TMS	Test Mode Select	I	–	1
TDI	Test Data In	I	–	1
TDO	Test Data Out	O	TS	1
Power Supply				
DVDD	Digital Power	P	–	6
AVDD	Analog Power	P	–	6
DVSS	Digital Ground	G	–	7
AVSS	Analog Ground	G	–	3
Test Interface				
TEN	Test Enable	I	–	1

PIN DESIGNATIONS

Listed By Driver Type

The following table describes the various types of output drivers used in the Am79C901A PHY. All I_{OL} and I_{OH} values shown in the table apply to 3.3 V signaling.

A sustained tri-state signal is an active-low signal that is driven high for one clock period before it is left floating.

TX± is a differential output driver. Its characteristics and those of the XTAL2 output are described in the *DC Characteristics* section.

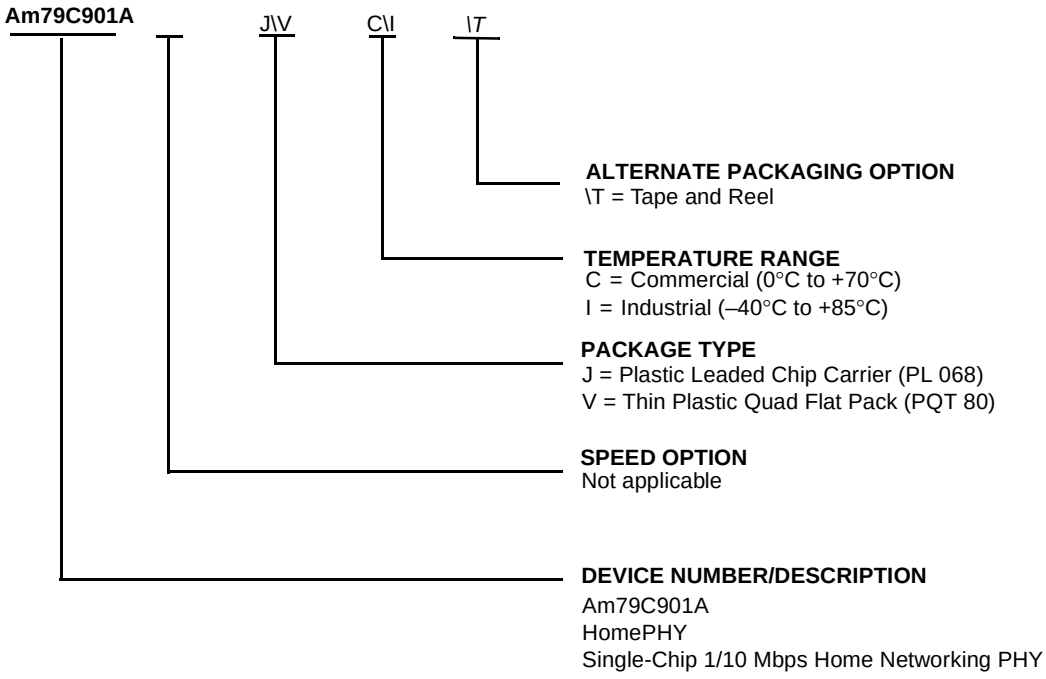
Driver Name	Type	I_{OL} (mA)	I_{OH} (mA)	Load (pF)
LED	LED	12	0.4	50
TS	Tri-State	6	2	50
OMII	Tri-State	4	4	50
TSMII	Tri-State	4	4	150

Note: *For reference only. See DC specification for actual limits.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am79C901A	JC, JC\T VC, VI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTIONS

Configuration Pins

MII/$\overline{\text{GPSI}}$

MII/$\overline{\text{GPSI}}$ Input

MII/$\overline{\text{GPSI}}$ selects between the MII and the GPSI interface. This pin must be connected to either V_{DD} or V_{SS}. Changing the state of this pin is prohibited.

GM_MODE

GM_MODE Input

This input pin selects between the MDC/MDIO command and control interface and the SPI interface normally available in the GPSI mode. This pin must be connected to either V_{DD} or V_{SS}. Changing the state of this pin is prohibited.

GM_MODE	MII/$\overline{\text{GPSI}}$	Data Interface	Command and Control Interface
0	1	MII	MDC/MDIO
0	0	GPSI	SPI
1	X	GPSI	MDC/MDIO

Note: *GM_MODE = 1 overrides the value on the MII/$\overline{\text{GPSI}}$ configuration pin.*

PHY_AD

PHY Address Input

Sets bit 2 of the PHY Address field. The PHYs have default MII address of 0x00 (0000b) for the 1 Mbps HomePNA PHY and 0x01 (0001b) for the 10BASE-T PHY. If this bit is set, the address for the HomePNA PHY is 0x02 (00010b) and 0x03 (00011b) for the 10BASE-T PHY.

ISOLATE

Isolate Input

In an environment that utilizes the MII or the SPI command and control interface (managed mode), this pin must be held HIGH. In an environment that does not use the MII or the SPI command and control interface (external control mode), this pin enables the data interface when set to a LOW, and forces the interface into a high impedance state when held HIGH. This pin functions in conjunction with the PHY_SEL pin and HPR0, bit 10, and TBR0, bit 10.

PHY_SEL

PHY Select Input

In an environment that utilizes the MII or the SPI command and control interface (managed mode), this pin must be held LOW. In an environment that does not use the MII or the SPI command and control interface (external control mode), this pin selects which PHY data and status signals will be driven onto the interface. When set to a LOW, the HomePNA PHY data and status signals will be driven onto the interface. When set to a HIGH, the 10BASE-T PHY data and status signals will be driven onto the interface. This pin functions in conjunction with the ISOLATE pin.

LOW = 1 Mbps HomePNA PHY

HIGH = 10BASE-T PHY

HPR0 Bit 10	TBR0 Bit 10	PHY_SEL	ISOLATE	Interface Source
Managed Mode				
1	1	0	1	Hi Z
0	1	0	1	1 Mbps HomePNA
1	0	0	1	10BASE-T
0	0	0	1	Non Valid
External Control Mode				
1	1	1	0	10BASE-T
1	1	0	0	1 Mbps HomePNA
1	1	Don't Care	1	Hi Z

Board Interface

$\overline{\text{LED_COL}}$

LED_COL Output

This output is designed to directly drive an LED. COL low indicates that a collision has been detected on the currently active PHY. An internal pulse stretching circuit will ensure that the minimum output pulse is approximately 100 ms.

$\overline{\text{LED_ACTIVITY}}$

LED_ACTIVITY Output

This output is designed to directly drive an LED. ACTIVITY low indicates that there is receive or transmit activity on the network of the currently active PHY. An internal pulse stretching circuit will ensure that the minimum output pulse is approximately 100 ms.

$\overline{\text{LED_LINK}}$

LED_LINK Output

This output is designed to directly drive an LED. LINK low indicates that a valid link has been detected on the currently active PHY.

LED_SPEED

LED_SPEED **Output**

This output is designed to directly drive an LED. SPEED low indicates that the HomePNA PHY is currently in the high-speed mode. When operating in the 10BASE-T mode this output will be held high.

LED_POWER

LED_POWER **Output**

This output is designed to directly drive an LED. POWER low indicates that the HomePNA PHY is currently in high-power mode. When operating in the 10BASE-T mode this output will be held high.

RESET

RESET **Input**

The RESET is an active-low, asynchronous RESET signal. This signal must be held low for a minimum of 5 µs and requires 60 µs for recovery after the rising edge of RESET.

GPSI Interface

RXDAT

Receive Data **Output**

RXDAT is the serial data received from the selected port. Data on RXDAT is driven on the falling edge of RXCLK.

RXCLK

Receive Data Clock **Output**

RXCLK provides the timing reference for transfer of the receive data. RXCLK is driven by the device and operates at a maximum frequency of 10 MHz.

RXCRS

Receive Carrier Sense **Output**

The RXCRS pin is active during receive or transmit activity for the HomePNA PHY or during receive (based on TBR17, bit 2) for the 10BASE-T PHY.

CLS

Collision **Output**

This signal is asserted whenever a collision is detected on the transmit and receive path of the selected port. This signal will also be asserted for ~1 µs within 40 µs after the negation of the TXEN signal in support of the SQE test. The SQE functionality may be controlled via TBR17, bit 11, and HPR16, bit 12.

TXDAT

Transmit Data **Input**

TXDAT is the serial data driven from the MAC. Data on TXDAT is latched on the falling edge of TXCLK.

TXCLK

Transmit Data Clock **Output**

TXCLK provides the timing reference for transfer of the transmitted data. TXCLK is driven by the device and operates at a maximum frequency of 10 MHz.

TXEN

Transmit Enable **Input**

TXEN indicates when the MAC device is presenting valid transmit data on the TXDAT pin. TXEN must be asserted with the first bit of preamble and remain asserted throughout the duration of the packet until it is deasserted prior to the first TXCLK following the final bit of the frame. TXEN transitions are synchronous to TXCLK.

SPI Interface (Slave Mode Only)

SCLK

SPI Clock **Input**

SCLK is driven from the controlling device as a timing reference for transfer of information on the SDI and SDO signals. The maximum clock frequency is 2.5 MHz.

CS

SPI Chip Select **Input**

This pin is used to enable the Am79C901A for slave mode transfers. When this pin is inactive (HIGH), the device ignores SCLK and SDI inputs and holds SDO in high-impedance.

SDI

SPI Serial Data In **Input**

This data line provides input data from the master device to the Am79C901A. The data presented on this pin is latched on the rising edge of SCLK.

SDO

SPI Serial Data Out **Output**

This data line provides output data from the Am79C901A to the master device. To provide for a robust interface, this data is driven on the rising edge of SCLK.

MII Interface

RX_CLK

Receive Clock **Output**

RX_CLK is a clock input that provides the timing reference for the transfer of the RX_DV, RXD[3:0], and RX_ER signals from the Am79C901A device. RX_CLK will provide a nibble rate clock. It operates at a maximum frequency of 2.5 MHz.

RXD[3:0]

Receive Data **Output**

RXD[3:0] is the nibble-wide receive data bus. Data on RXD[3:0] is driven on the falling edge of RX_CLK. RXD[3:0] should be ignored while RX_DV is deasserted.

RX_DV

Receive Data Valid **Output**

RX_DV is an output used to indicate that valid received data is being presented on the RXD[3:0] pins and RX_CLK is synchronous to the receive data. RX_DV will be asserted prior to the RX_CLK rising edge, when the first nibble of the Start of Frame Delimiter (SFD) is driven on RXD[3:0], and will remain asserted until after the rising edge of RX_CLK, when the last nibble of the CRC is driven on RXD[3:0]. RX_DV will be deasserted prior to the RX_CLK rising edge which follows this final nibble. RX_DV transitions are driven on the falling edge of RX_CLK.

CRS

Carrier Sense **Output**

The CRS pin is active during receive or transmit activity for the HomePNA PHY or during receive (based on TBR17, bit 2) for the 10BASE-T PHY.

COL

Collision **Output**

This signal is asserted whenever a collision is detected on the transmit and receive path of the selected port. This signal will also be asserted for ~1 µs within 40 µs after the negation of the TXEN signal in support of the SQE test. The SQE functionality may be controlled via TBR17, bit 11, and HPR16, bit 12.

RX_ER

Receive Error **Output**

RX_ER is an output for the 10BASE-T PHY that indicates that the transceiver device has detected a coding error in the receive data frame currently being transferred on the RXD[3:0] pins. RX_ER is ignored while RX_DV is deasserted. Special code groups generated on RXD while RX_DV is deasserted are ignored (e.g., bad SSD in TX and idle in T4). RX_ER transitions are synchronous to RX_CLK.

TX_CLK

Transmit Clock **Output**

TX_CLK is a clock output that provides the timing reference for the transfer of the TXD[3:0] and TX_ER signals from the Am79C901A device. TX_CLK provides a nibble rate clock.

TXD[3:0]

Transmit Data **Input**

TXD[3:0] is the nibble-wide data bus. Valid data is generated on TXD[3:0] on every rising edge of TX_CLK while TX_EN is asserted. While TX_EN is deasserted, TXD[3:0] values are ignored. TXD[3:0] transitions are latched on the falling edge of TX_CLK.

TX_EN

Transmit Enable **Input**

TX_EN indicates that the MAC device is presenting valid transmit data on the TXD[3:0] bus. TX_EN must be asserted with the first nibble of preamble and remains asserted throughout the duration of the packet until it is deasserted prior to the first TX_CLK following the final nibble of the frame. TX_EN transitions are latched on the falling edge of TX_CLK.

MDC

Management Data Clock **Input**

MDC is the non-continuous clock input that provides a timing reference for bits on the MDIO pin. During MII management port operations, MDC runs at a nominal frequency of 2.5 MHz.

MDIO

Management Data Input/Output **Input/Output**

MDIO is a bidirectional MII management port data pin. MDIO is an input during the header portion of the management frame transfers and during the data portion of write operations. MDIO is an output during the data portion of read operations.

The MDIO pin should be externally pulled up to V_{DD} with a 1.5 kΩ ±5% resistor.

IEEE 1149.1 (JTAG) Test Access Port Interface

TCK

Test Clock **Input**

TCK is the clock input for the boundary scan test mode operation. It can operate at a frequency of up to 10 MHz. TCK has an internal pull-up resistor.

TDI

Test Data In **Input**

TDI is the test data input path to the Am79C901A PHY. The pin has an internal pull-up resistor.

TDO

Test Data Out **Output**

TDO is the test data output path from the Am79C901A PHY. The pin is tri-stated when the JTAG port is inactive.

TMS

Test Mode Select **Input**

A serial input bit stream on the TMS pin is used to define the specific boundary scan test to be executed. The pin has an internal pull-up resistor.

Ethernet Network Interfaces

TX±

Serial Transmit Data **Output**

These pins carry the transmit output data and are connected to the transmit side of the magnetics module.

RX±

Serial Receive Data **Input**

These pins accept the receive input data from the magnetics module.

IREF

Internal Current Reference **Input**

This pin serves as a current reference for the integrated 1/10 PHY. It must be connected to GND through a 12.1 kΩ resistor (1%).

HomePNA PHY Network Interface

HRTXRXP/HRTXRXN

Serial Receive Data **Input/Output**

These pins accept the receive input data from the magnetics module and carry the transmit output data. A 102-Ω resistor should be placed between these pins.

Clock Interface

XCLK/$\overline{\text{XTAL}}$

External Clock/Crystal Select **Input**

When HIGH, an external 60-MHz clock source is selected bypassing the crystal circuit and clock trippler. When LOW, a 20-MHz crystal is used instead. Table 1 illustrates how this pin works.

Table 1. Clock Source Selection

Input Pin	Output Pin	XCLK/$\overline{\text{XTAL}}$	Clock Source
XTAL1	XTAL2	0	20-MHz Crystal
XTAL1	NC	1	60-MHz Oscillator/ External CLK Source

XTAL1

Crystal Oscillator In **Input**

The internal clock generator utilizes either a 20-MHz crystal that is attached to pins XTAL1 and XTAL2 or a 60-MHz clock source connected to XTAL1. This pin is not 5 V tolerant, and the 60 MHz clock source should be from a 3.3 V source.

XTAL2

Crystal Oscillator Out **Output**

The internal clock generator utilizes a 20-MHz crystal that is attached to pins XTAL1 and XTAL2. In XCLK mode, this pin should be left unconnected.

Power Supply

DVDD

Digital Power (5 Pins) **+3.3 V Power**

These pins are the power supply pins that are used to provide power to the digital portions of the design. All DVDD pins must be connected to a +3.3 V supply.

AVDD

Analog Power (7 Pins) **+3.3 V Power**

These pins are the power supply pins that are used to provide power to the analog portions of the design. All AVDD pins must be connected to a +3.3 V supply.

DVSS

Digital Ground (6 Pins) **Ground**

These pins are the ground connections for the digital portions of the design.

AVSS

Analog Ground (4 Pins) **Ground**

These pins are the ground connections for the analog portion of the design.

Scan Test Interface

TEN

Test Enable **Input**

The test enable pin is for factory use only. It must be connected to V_{SS} for normal operation.

BASIC FUNCTIONS

Network Interfaces

The Am79C901A PHY contains an integrated 1 Mbps home networking PHY and a 10BASE-T PHY. This device is compliant with the HomePNA specification 1.0 and IEEE 802.3 specification.

The integrated HomePNA transceiver is a physical layer device that enables data networking at speeds up to 1 Mbps over existing residential phone wiring regardless of topology and without disrupting telephone (POTS) service.

The integrated Ethernet transceiver is a physical layer device supporting the IEEE 802.3 standard for 10BASE-T. It provides all of the PHY layer functions required to support 10 Mbps data transfer speeds. The 10BASE-T PHY supports both half-duplex and full-duplex operation.

PHY Data Interfaces

The Am79C901A PHY has both GPSI and MII-compatible data interfaces. In addition, a special mode, GM_MODE, allows access to the MDC/MDIO command and control interface while in the GPSI mode. For more information, see the *Pin Descriptions* and the *Detailed Functions* sections.

Reset

There are two different types of RESET operations that may be performed on the Am79C901A device, H_RESET or S_RESET. The following is a description of each type of RESET operation.

H_RESET

Hardware Reset (H_RESET) is a reset operation that has been initiated by the proper assertion of the $\overline{\text{RESET}}$ pin of the Am79C901A device. When the minimum pulse width timing as specified in the $\overline{\text{RESET}}$ pin description has been satisfied, an internal reset operation will be performed.

H_RESET will program all of the registers to their default value.

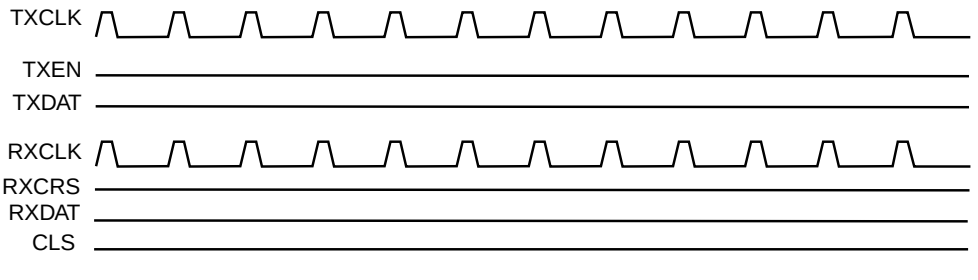
S_RESET

In a software reset (S_RESET), programming bit 15 of HPR0 to 1 will reset all the registers in the 1 Mbps HomePNA PHY (HPRs), and programming bit 15 of TBR0 to 1 will reset TBR4, TBR7, TBR17, and TBR24 in the 10BASE-T PHY. These bits are self-clearing.

DETAILED FUNCTIONS

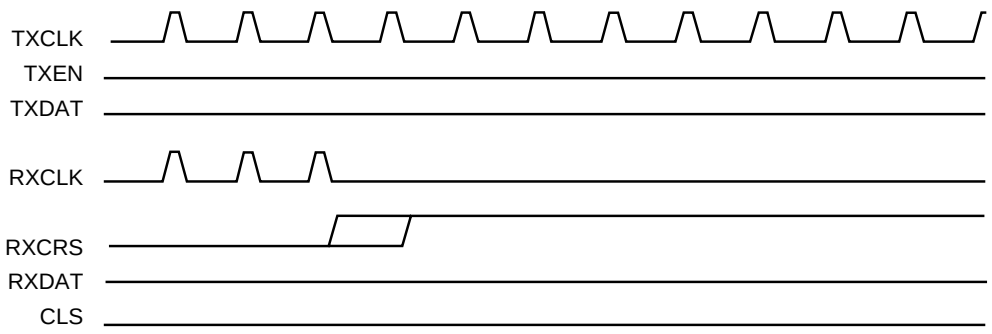
GPSI Interface

The seven signals that comprise the GPSI are TXCLK, TXEN, TXDAT, RXCLK, RXCRS, RXDAT, and CLS. Of these, only TXEN and TXDAT are inputs to the PHY; the other five are outputs from the PHY. These signals behave differently depending on which operation is currently happening in the PHY. The operations of the PHY are as follows: Idle (no activity in either direction), RXPKT (receiving data), and TXPKT (transmitting data). The subsequent subsections analyze each GPSI-related state of the PHY in detail.



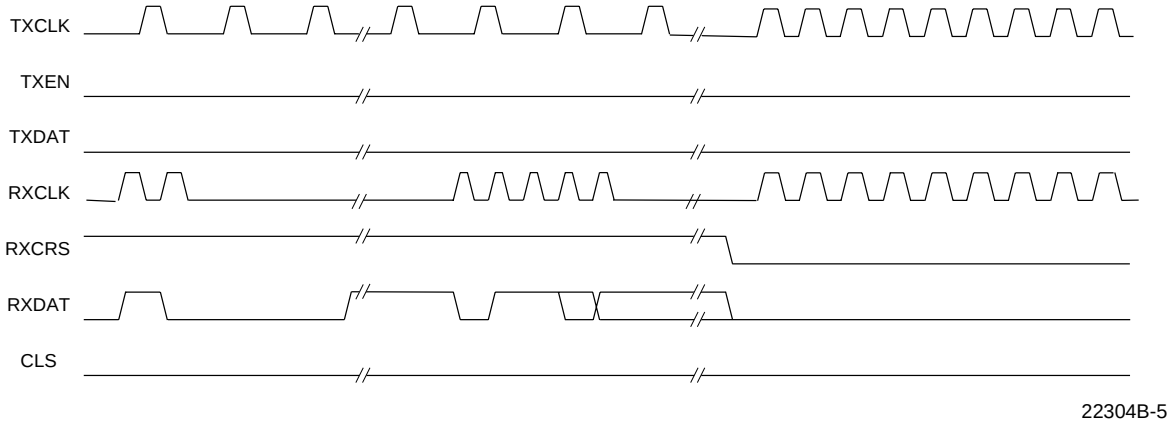
***Note**: RXCLK and TXCLK are synchronized to the same phase. All other signals are inactive. The two clock signals toggle for an overall period of 583.3ns (about 1.7 MHz).*

Figure 1. Idle State



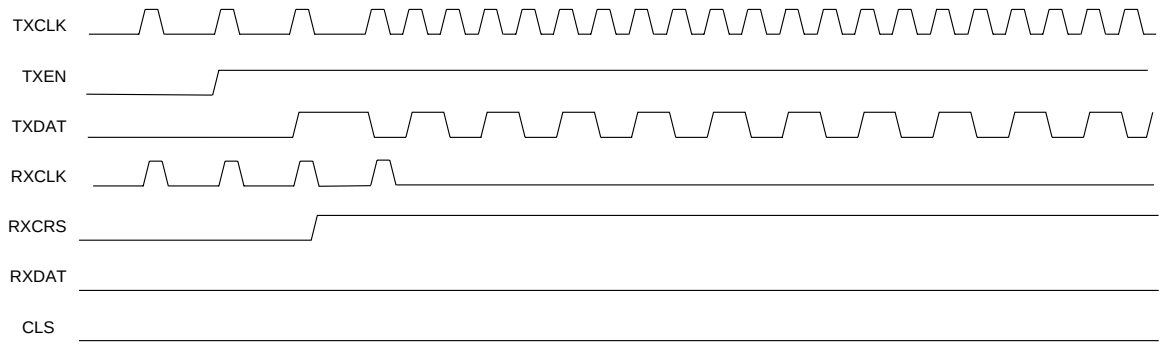
Note: RXCLK becomes disabled as soon as RXCRS is asserted.

Figure 2. RXPKT - RXCRS Asserted



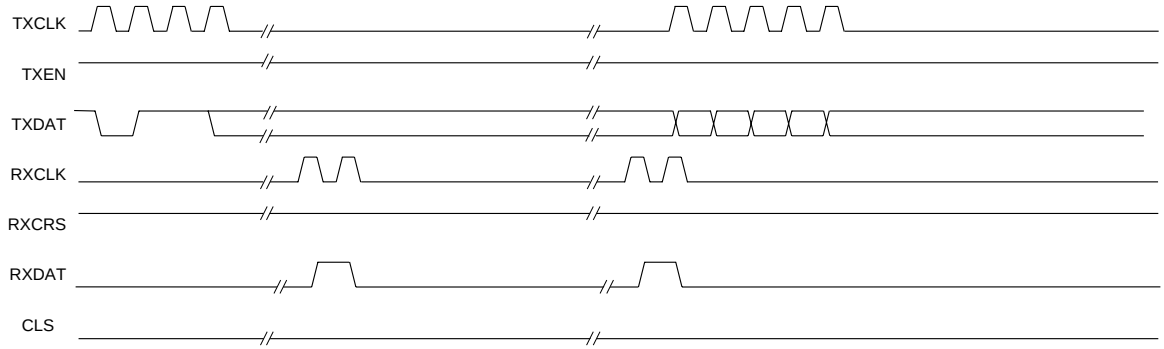
Note: RXCLK and TXCLK are unrelated to each other during this time. When a symbol has been received and decoded, RXCLK toggles in order to shift out the three to six bits encoded in the symbol. The middle portion of this diagram shows the end of the preamble, followed by an SFD and the beginning of the data. RXCRS will fall after the last received symbol. Once RXCRS falls, RXCLK and TXCLK are toggled continuously for 96 cycles, after which the PHY returns to the Idle state.

Figure 3. RXPKT - RXCRS Cleared



Note: *Once TXEN is asserted, the PHY stops RXCLK, asserts RXCRS, and toggles TXCLK.* 22304B-6

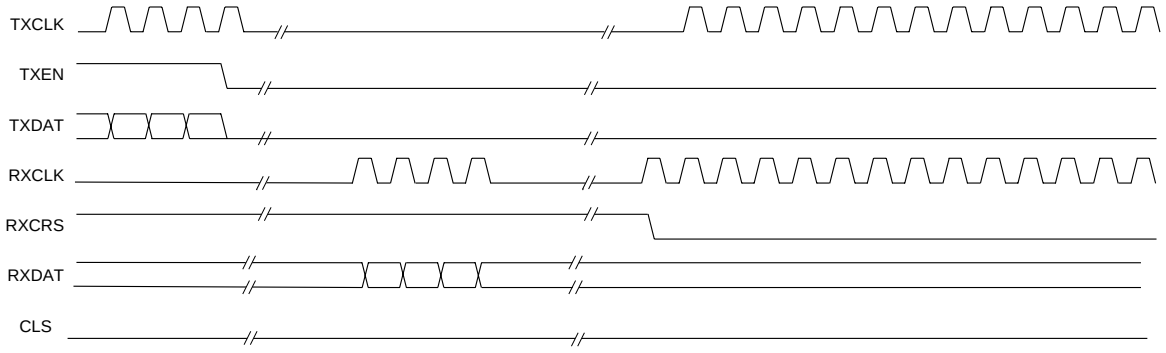
Figure 4. TXPKT - TXEN Asserted



22304B-7

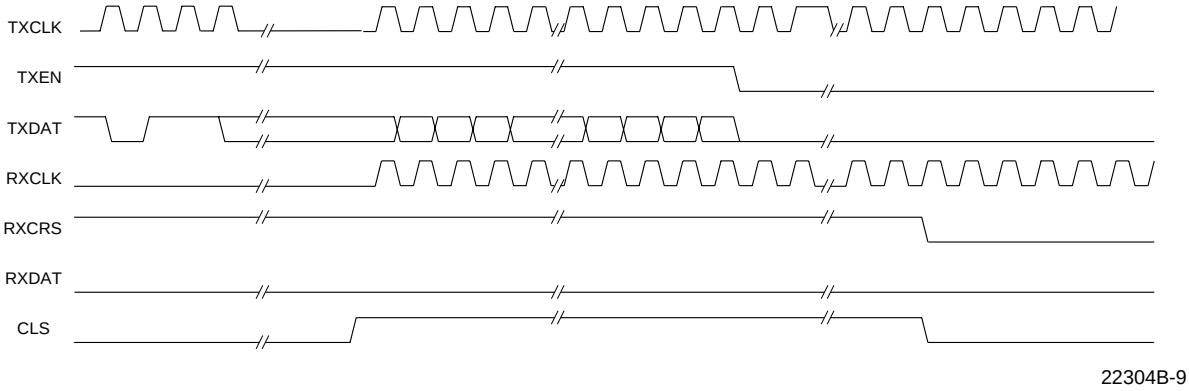
Note*: TXCLK continues to toggle until the SFD is observed, as shown in the first section of the above diagram. At this point, TXCLK is disabled (low) until the AID header has been transmitted on the wire (or until a CLS has been detected). At this time RXCLK starts toggling, thereby, shifting 32 bits of preamble and SFD back to the MAC. Sometime later, the TXCLK restarts as symbols get sent onto the wire in an analogous manner as RXCLK during packet reception.*

Figure 5. TXPKT - RXCLK Active



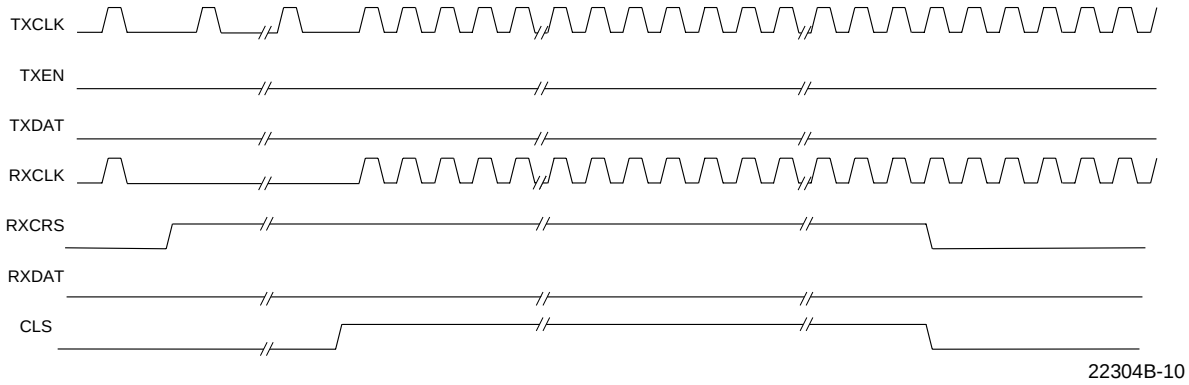
***Note**: Once TXEN is cleared, the last symbol gets encoded and transmitted, the looped-back data is presented back to the MAC, and RXCRS falls. Once RXCRS falls, TXCLK and RXCLK toggle for 96 clocks, after which the system returns to the Idle state.*

Figure 6. TXPKT - TXEN Cleared



Note: CLS will be asserted some time after the preamble and SFD have been clocked in. TXCLK and RXCLK are then clocked until RXCRS drops. TXEN drops about 32 clocks after CLS was asserted. RXCRS and CLS are dropped together after more than 500 clocks (about 120 µs). TXCLK and RXCLK keep toggling for approximately another 100 clock cycles, when the system returns to the Idle state.

Figure 7. TXPKT - CLS Asserted



Note: CLS may be asserted up to 120 µs after RXCRS has been asserted. Once CLS has been asserted, TXCLK and RXCLK run until 96 cycles after CLS and RXCRS are cleared. It can take a maximum of approximately 60 µs for RXCRS to clear.

Figure 8. RXPKT - CLS Asserted

Table 2. GPSI Timing

Condition	CLK Period	CLK Frequency
Idle (excluding IPG time)	583.3 ns	1.7 MHz
Preamble (first 64 bits of TX MAC frame)	233.3 ns	4.3 MHz
Data (throughout the data phase)	100 ns - 10 µs	1.0 MHz avg.
IPG (96 bit times following CRS ↓)	233.3 ns	4.3 MHz

Note: *During the AID interval, TXCLK and RXCLK stop for up to 140 µs.*

Serial Peripheral Interface (SPI-Slave) Mode

When MII/$\overline{\text{GPSI}}$ is set to 0, the device is in "SPI" mode. The device acts as an SPI slave peripheral in this mode of operation. Commands are issued to the device by asserting the $\overline{\text{CS}}$ signal (active low), shifting in an 4-bit opcode, followed by an 10-bit register address and 2 bits of end delimiter. If the operation is a write, the data bits are written into the desired register. If the operation is a read, then these data bits are ignored. The SDO pin will shift out 16 data bits representing the contents of the register referenced by the address field for read operations. All commands must be initiated with a high-to-low transition on the $\overline{\text{CS}}$ pin. Only one command can be sent in one $\overline{\text{CS}}$ cycle.

For assistance in debugging access to the SPI interface, an error code is driven onto the SDO. If there is less than 32 bits of SCLK during the time that $\overline{\text{CS}}$ is asserted, the error code field of SDO on the next command will indicate AAAA. When there is an incorrect opcode in the command on SDI AAAA will be immediately driven out on SDO until $\overline{\text{CS}}$ deasserts. If there are more than 32 clock cycles while $\overline{\text{CS}}$ is low, the first 32 are assumed to contain the data, and the additional clock bits and associated data are ignored. In this case, the SDO might generate AAAA under the additional clock bits. See Figure 9.

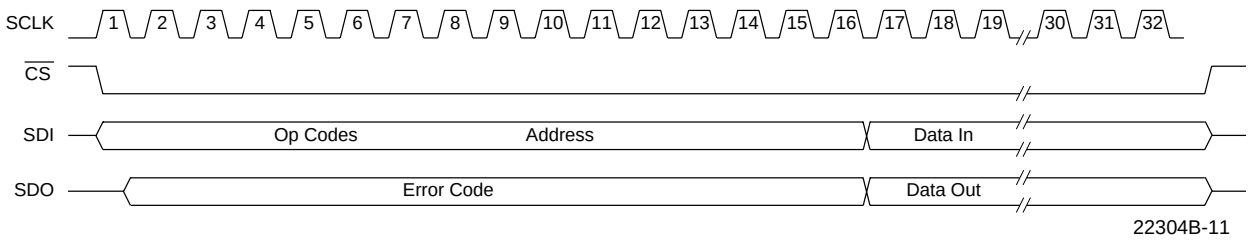


Figure 9. Operation of the SPI Interface

Table 3. SPI Op Codes

SDI						
	Op Codes		Address			Data In
	ST	OP	PHYADD	REGADD	ED	
READ	01	10	AAAAA	RRRRR	10	Don't Care
WRITE	01	01	AAAAA	RRRRR	10	D15……D0
SDO						
	Error Code					Data Out
READ	0000 = No Error/AAAA = Error Detected					D15...D0
WRITE	0000 = No Error/AAAA = Error Detected					Don't Care

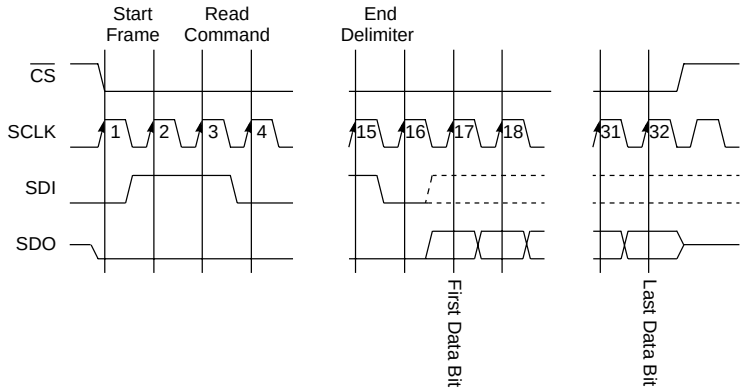


Figure 10. SPI Read Operation

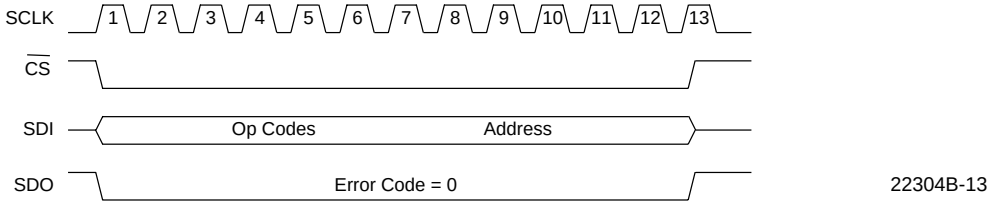


Figure 11. Aborted Operation of the SPI Interface

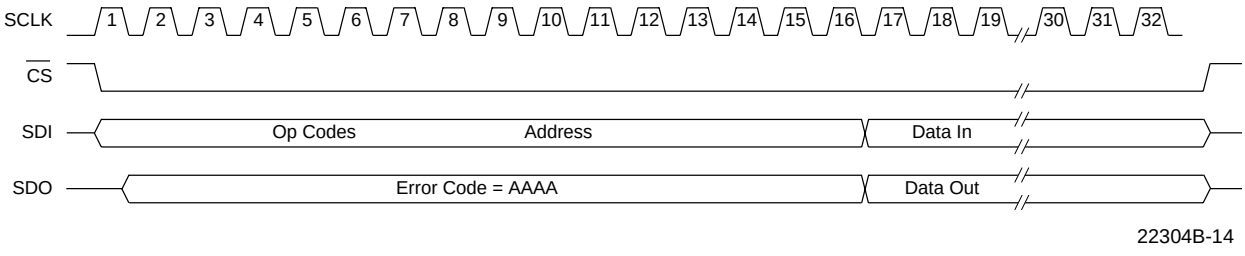


Figure 12. First Operation Following an Abort

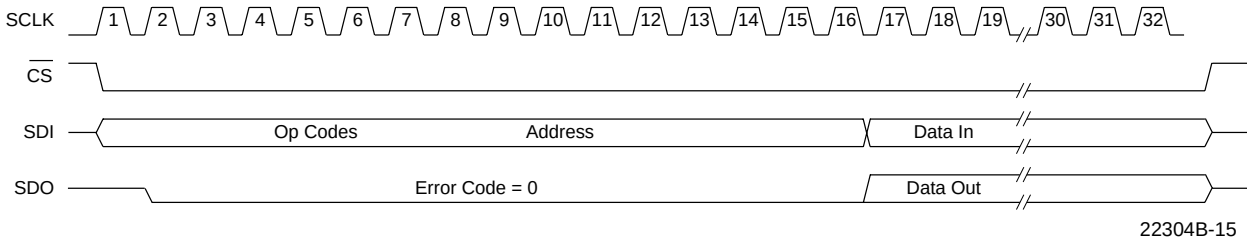


Figure 13. Normal Operation

MII-Compatible Interface for HomePNA PHY

The control and data signals that are utilized in the MII-compatible interface of the 1 Mbps HomePNA PHY function in an manner that is identical to that as defined in the 802.3u specification. The signals RX_CLK and TX_CLK function in a slightly different manner in that they operate at a reduced data rate and that these clock signals do not run at a constant rate due to the RLL25™ encoding scheme. See Table 4.

Table 4. MII-Compatible Timing

Condition	CLK Period	CLK Frequency
Idle (excluding IPG time)	2333.34 ns	428.6 kHz
Preamble (first 64 bits of TX MAC frame)	933.33 ns	1.07 MHz
Data (throughout the data phase)	400 ns - 40 µs	250 kHz avg.
IPG (96 bit times following CRS↓)	933.33 ns	1.07 MHz

Note: *During the AID interval, TX_CLK and RX_CLK stop for up to 140* µs.

Figure 14 and Figure 15 represent the signal relationships when the MII-compatible data interface is utilized.

The signals TX_CLK and RX_CLK will toggle at a rate of approximately 428 kHz during idle time. When the TX_EN signal is asserted to indicate the beginning of a transmission, the clock rate will enter the preamble phase. Once the SFD has been detected and the HomePNA PHY has begun the transmission of the HomePNA header, the clock enters the data phase.

When the TX_EN signal is deasserted to indicate the ending of a transmission, TX_CLK is halted until the RXDATA path detects the end of the packet. At this time, the clock rate is increased to the IPG data rate for 96 bit times and then returns to the Idle state.

MII-Compliant Interface for 10BASE-T PHY

The MII interface is fully IEEE 802.3u-compliant when the 10BASE-T PHY is selected. The management interface specified in Clause 22 of the IEEE 802.3u standard provides for a simple two wire, serial interface to connect a management entity and a managed PHY for the purpose of controlling the PHY and gathering status information. The two lines are Management Data Input/Output (MDIO) and Management Data Clock (MDC). A station management entity, which is attached to multiple PHY entities, must have prior knowledge of the appropriate PHY address for each PHY entity.

The management interface physically transports management information across the MII. The information is encapsulated in a frame format as specified in Clause 22 of the IEEE 802.3u standard and is shown in Table 5.

Table 5. MII Control Frame Format

	PRE	ST	OP	PHYADD	REGADD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	D15……D0	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	D15……D0	Z

The operation field (OP) follows the start field (ST). The OP indicates whether the operation is a read or a write operation. The PHY address (PHYADD) and the register address (REGADD) that were programmed follow this. A bus turnaround field (TA) follows the REGADD field. During the read operation, the bus TA field is used to determine if the PHY is responding properly to the read request. The final field is the idle field, and it is required to allow the drivers to turn off.

The PHYADD field, which is five bits wide, allows 32 unique PHY addresses. The managed PHY layer device that is connected to a station management entity via the MII interface has to respond to transactions addressed to the PHY's address. A station management entity attached to multiple PHYs is required to have prior knowledge of the appropriate PHY address.

For more information, see the IEEE 802.3 specification and the MII pin descriptions.

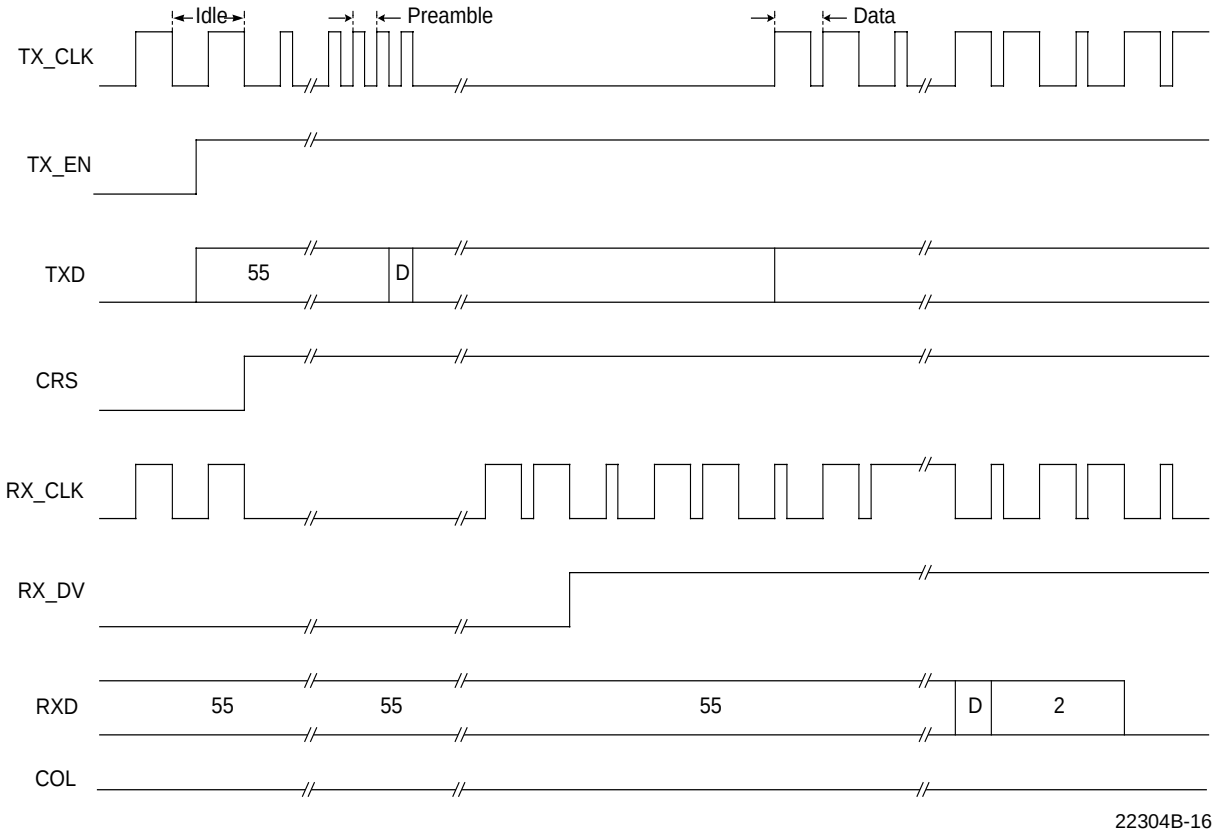


Figure 14. MII Start of Transmission

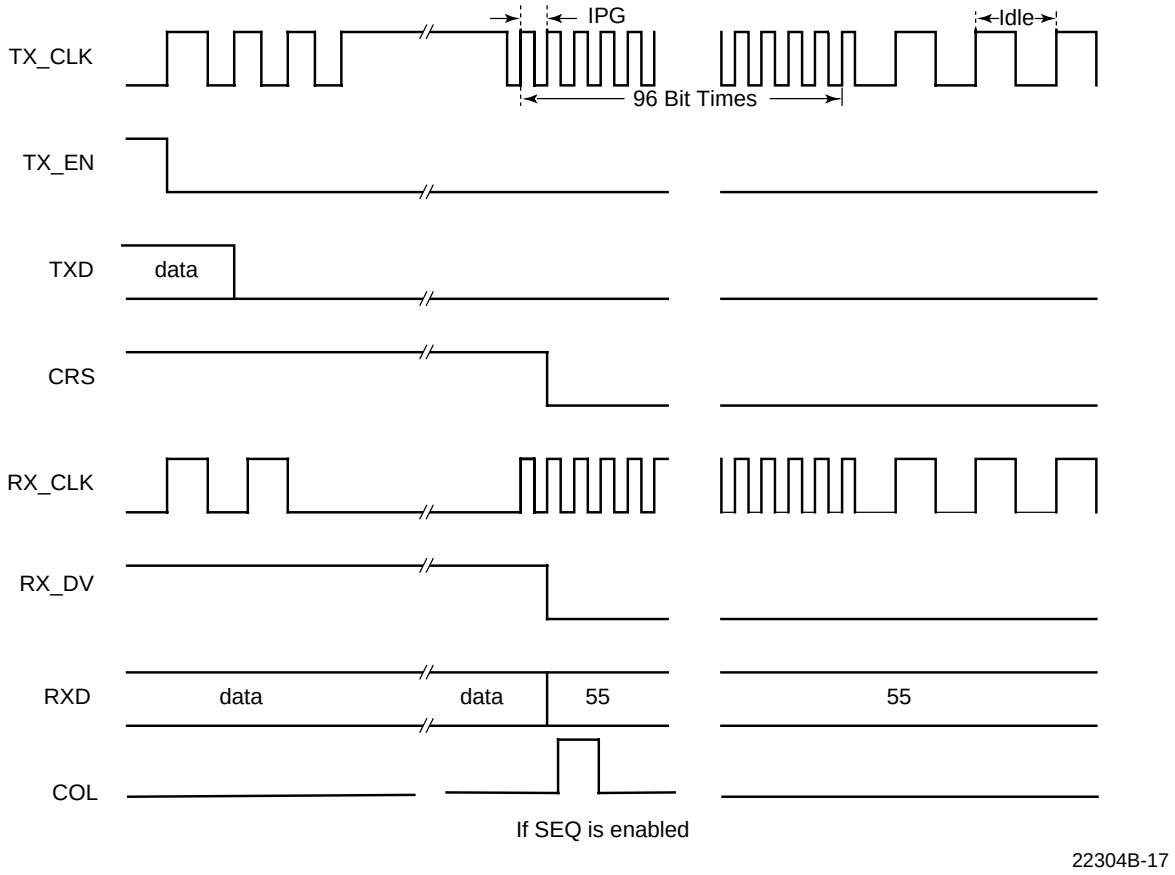


Figure 15. MII End of Transmission

1 Mbps HomePNA PHY

The integrated HomePNA transceiver is a physical layer device supporting HomePNA specification 1.0 for home phoneline networking. It provides all of the PHY layer functions required to support 1 Mbps data transfer speeds over existing residential phone wiring.

All data bits are encoded into the relative time position of a pulse with respect to the previous one. The waveform on the wire consists of a 7.5 MHz carrier sinusoid enclosed within an exponential (bell shaped) envelope. The waveform is produced by generating four 7.5 MHz square wave cycles and passing them through an external bandpass filter.

The HomePNA PHY frame consists of a HomePNA header that replaces the normal Ethernet 64-bit preamble and delimiter. The frame header is prepended to a standard Ethernet packet starting with the destination address and ending with the CRC.

Only the PHY layer and its parameters are modified from that of the standard Ethernet implementation. The HomePNA PHY layer is designed to operate with a standard Ethernet MAC layer controller implementing all the CSMA/CD protocol features.

The frame begins with a characteristic SYNC interval that delineates the beginning of a HomePNA frame followed by an Access ID (AID) which encodes 8 bits of AID and 4 bits of control word. The AID is used to detect collisions and is dynamically assigned, while the control word carries speed and power information.

The AID is followed by a silence interval, then 32 bits of data reserved for PHY layer communication. These bits are accessible via internal registers and are for future use.

Data encoding consists of two symbol types: an AID symbol and a data symbol. The AID symbol is always transmitted at the same speed and encodes 2 bits that determine the pulse position (one of four) relative to the previous pulse. These bits are transmitted LSB first. The access symbol interval is fixed.

The data symbol interval is variable. The arriving bit stream is blocked into from 3-bit to 6-bit blocks according to a proprietary (RLL25) algorithm. The bits in each block are then used to encode a data symbol. Each symbol consists of a Data Inter Symbol Blanking Interval (DISBI) and then a pulse at one of 25 possible positions. The bits in the data block determine the pulse position. Immediately after the pulse a new symbol interval begins. During the DISBI the receiver ignores all incoming pulses to allow network reflections to die out.

Any station may be programmed to assume the role of a PHY master and remotely command, via the control word, the rest of the units on the network to change their transmit speed or power level.

Many of the framing parameters are programmable in the HomePNA PHY and will allow modifications to transmission speed center frequency as well as noise and reflection rejection algorithms.

Two default speeds are provided, low at 0.7 Mbps and high at 1 Mbps.

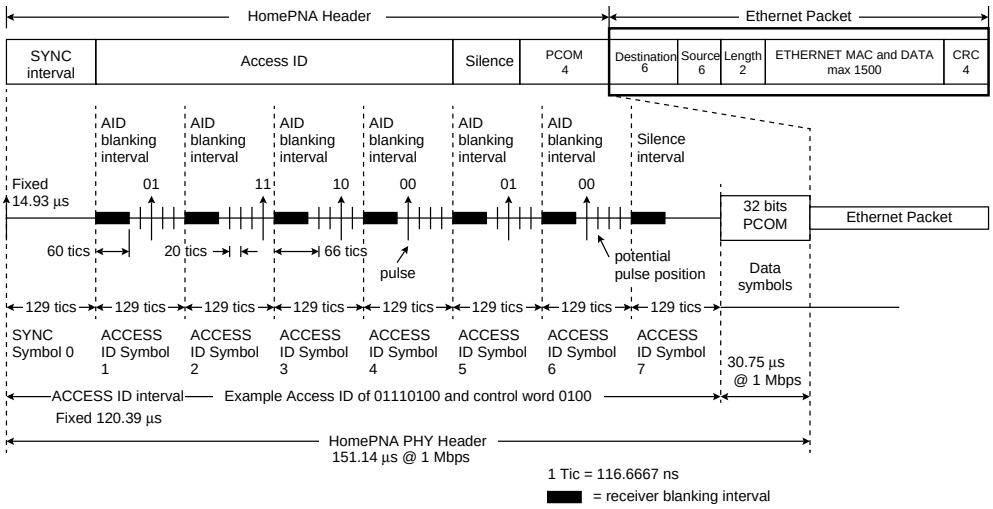
HomePNA PHY Medium Interface

Framing

The HomePNA frame on the phone wire network consists of a header generated in the PHY prepended to an IEEE 802.3 Ethernet data packet received from the MAC layer. See Figure 16.

When transmitting on the phone wire pair, the HomePNA PHY first receives an Ethernet MAC frame from the MAC. The 8 octets of preamble and delimiter are stripped off and replaced with the HomePNA PHY header described below, then transmitted on the home network with the LSB of each symbol being transmitted first.

During a receive operation, the reverse process is executed. When a HomePNA PHY frame is received by the PHY, the header is stripped off and replaced with the 4 octets of preamble and delimiter of the IEEE 802.3 Ethernet MAC frame specification and then passed on to the MAC layer.



***Note**: Using default configurations.*

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Figure 16. HomePNA PHY Framing

HomePNA PHY Symbol Waveform

All HomePNA PHY symbols are composed at the transmitter of a silence interval and a pulse formed of an integer number of cycles (TX_PULSE_CYCLES_P/N in HPR29) of a square wave of frequency (CENTER_FREQUENCY TX_PULSE_WIDTH in HPR29) that has been filtered with an external bandpass filter. Data is encoded in the time interval from the preceding pulse.

Table 6. HomePNA PHY Pulse Parameters

Parameter	Value	Tolerance	Unit
CENTER_FREQUENCY	7.5	500 PPM	MHz
CYCLES_PER_PULSE	4	–	Cycles

Time Interval Unit

HomePNA PHY time intervals are expressed in Time Interval Clock (TIC) units. One TIC is defined as 7/60E6 seconds or approximately 116.7 ns.

Access ID Intervals

A HomePNA frame begins with an Access ID (AID) interval which is composed of eight equally spaced subintervals termed AID symbols 0 through 7 as shown in Figure 17.

An AID symbol is 129 TICs long. Transmit timing is shown in Figure 17; receive timing in Figure 18. Timing starts at the beginning of each AID symbol at TIC = 0 and ends at TIC = 129.

These symbols are described in the following sections.

Symbol 0 (SYNC interval)

SYNC Transmit Timing: The SYNC interval (AID symbol 0) delineates the beginning of a HomePNA PHY frame and is composed of a SYNC_START pulse, followed by a SYNC_END pulse, after a fixed silence interval as shown in Figure 17. Timing for this (AID symbol 0) starts (TIC = 0) at the beginning of the SYNC_START pulse. The SYNC_END pulse starts at TIC = 126.

At TIC = 129, this AID symbol 0 ends and the next AID symbol begins, with the symbol timing reference reset to TIC = 0. No information bits are coded in the SYNC (AID symbol 0 interval).

SYNC Receive Timing: As soon as the SYNC_START pulse is detected the receiver disables (blanks) further detection until time TIC = 61, after which detection is re-enabled for the next received pulse. The receiver allows for jitter by establishing a window around each legal pulse position. This asymmetrical window is two TICS wide on one side of the position and one TIC wide on the other.

A SYNC_END pulse that arrives outside the window of the legal TIC = 126 is considered a noise event which is used in setting the adaptive squelch level, aborts the packet, and sets the receiver in search of a new SYNC_START pulse and SYNC interval. If it is a transmitting station, the COLLISION event is asserted as described in the *Collisions* section.

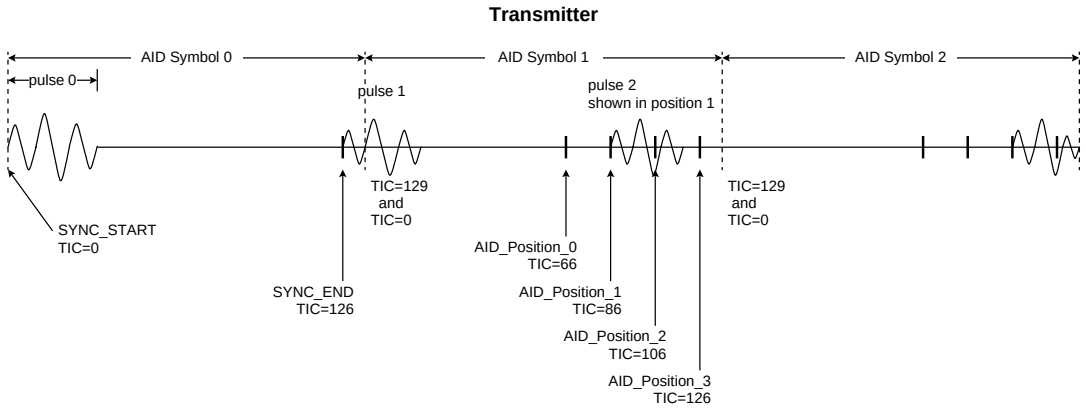


Figure 17. AID Symbol Transmit Timing

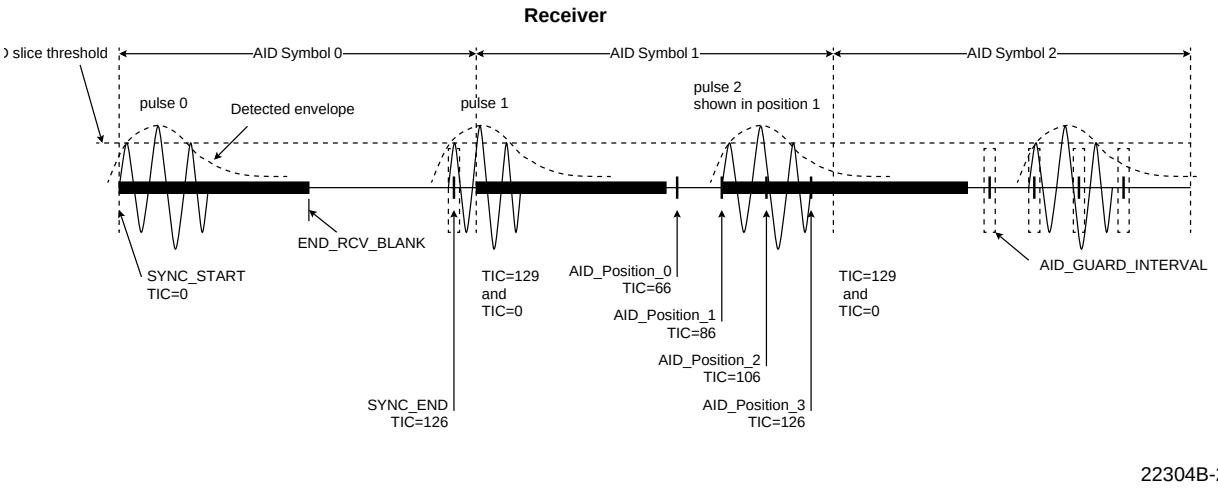


Figure 18. AID Symbol Receive Timing

The SYNC interval is followed by six AID symbols (symbols 1 through 6). Transmit timing is shown in Figure 17; receive timing in Figure 18. Data is encoded in the relative position of each pulse with respect to the previous one. A pulse may occur at one, and only one, of the four possible positions within an AID symbol yielding two bits of data coded per AID symbol.

The decoded bits from the AID symbols 1 to 4 produce eight bits of Access ID which is used to identify individual HomePNA stations and to detect collisions. The MSB is encoded in AID Symbol 1 and is the leftmost bit in Table 7.

Table 7. Access ID Symbol Pulse Positions and Encoding

Pulse Position	TICs from Beginning of AID Symbol	Bit Encoding
1	66	00
2	86	01
3	106	10
4	126	11

The next two AID symbols (5 and 6) encode four bits of control word information. The MSB is encoded in AID Symbol 5. Control word messages are described further in the *Mode Interface* section.

AID Transmit Timing: The transmitter encodes the Access ID in a pulse position in each 129 TIC interval. Each AID symbol interval must have only one pulse. Pulse transmission must start in only one of the four possible positions (measured from the beginning of the Access ID symbol) defined in Table 7.

AID Receive Timing: The receiver allows for jitter by establishing a window around each legal pulse position. This asymmetrical window is two TICS wide on one side of the position and one TIC wide on the other. A pulse that arrives outside of the legal AID positions is considered a COLLISION event.

Collisions

A Collision is detected only during Access ID and silent intervals (AID symbols 0 through 7). In general during a collision, a transmitting station will read back an AID value that does not match its own, recognize the event as a collision, and alert other stations with a JAM signal. Non-transmitting stations may also detect some collisions by interpreting received non-conforming AID pulses as collisions.

With two transmitters colliding, each transmitter normally blanks its receive input immediately after transmitting (and simultaneously receiving) a pulse. Therefore, only when a transmitting station receives pulses in a position earlier than the position it transmitted will it recognize it as a pulse transmitted by another station and signal a collision.

For this reason, guaranteed collision detection is possible only as long as the spacing between successive possible pulse positions in an AID symbol (20 TICs or 2.3 μs) is greater than the roundtrip delay between the colliding nodes. At approximately 1.5 ns propagation delay per foot, the maximum distance between two HomePNA units must not be greater than 500 feet for collision detection purposes (1.5 μs roundtrip delay plus margin).

The following criteria must be met to guarantee reliable collision detection:

At least one HomePNA station of a colliding group must always detect a collision when the delay between the beginning of its transmitted packet and the beginning of the received colliding packet is between -1.5 μs and +1.5 μs.

In general, any received pulse at a HomePNA station that does not conform to the pulse position requirements of AID symbols 0 through 7 shall indicate a collision on the wire. When a transmitting station senses a collision, it emits a JAM signal to alert all other stations to the collision. The following conditions signify a COLLISION event:

1. A HomePNA station receives an AID that does not match the one being sent.
2. A HomePNA station receives a pulse outside the AID_GUARD INTERVAL in AID intervals 0 to 7.
3. A HomePNA station receives a pulse inside the SILENT_INTERVAL (AID symbol 7).

As in all cases, pulses received during a blanking interval are ignored.

Passive stations (stations not actively transmitting during the collision) cannot reliably detect collisions. Therefore, once a collision is detected by a transmitting station, the station must inform the rest of the stations of the collision with a JAM pattern described below. Only a transmitting station emits a JAM signal.

Once a collision is detected, the COLLISION signal to the MAC interface is asserted and is not reset until the MAC deactivates the TXEN signal.

JAM Signal

A JAM pattern consists of 1 pulse every 32 TICs and continues until at least the end of the AID intervals. After the AID interval, the JAM pattern will continue until TXEN from the MAC is deactivated.

Access ID Values

The access ID values for stations are randomly picked by each individual station from the set of AID numbers described in the management section. During operation, each HomePNA station monitors HomePNA frames received on the wire. If it detects another HomePNA station using the same AID, it will select a new random AID.

Silence Interval (AID symbol 7)

The Access ID symbols are followed by a fixed silence interval of 129 TICs. The receive blanking interval is the same as that of the AID symbols (1 through 6).

Any pulses detected in the silence interval are considered a COLLISION event for transmitting stations and are handled as described in the *Collisions* section.

Data Symbols

Data symbols encode data for a much higher transmission rate, and they do not allow collision detection.

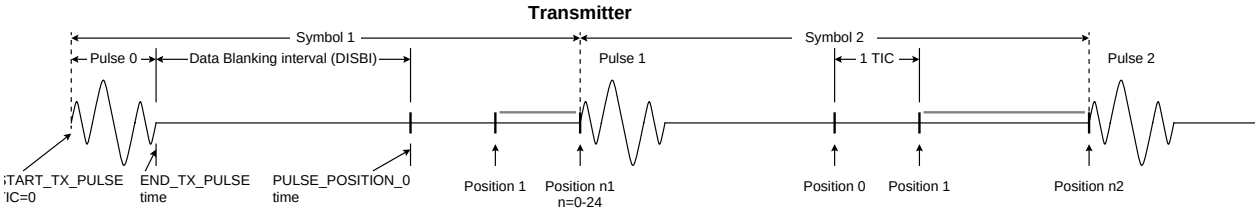
Data Transmit Timing

A data symbol interval begins with the start of transmission of a pulse as shown in Figure 19. Transmit Symbol timing (in TICs) is measured from this point (TIC = 0).

Depending on the data code, the next pulse may begin at any PULSE_POSITION_N where N = 0 to 24. Each position is separated from the previous one by one TIC. PULSE_POSITION_0 occurs at a value defined in Table 8 which determines the transmission speed. When a pulse begins transmission, the previous symbol interval ends and a new one begins immediately.

Table 8. Blanking Interval Speed Settings

Speed Setting	Nominal Data Rate	PULSE_POSITION_0 Value (in TICs)
LOW_SPEED	0.7 Mbps	44
HIGH_SPEED	1.0 Mbps	28



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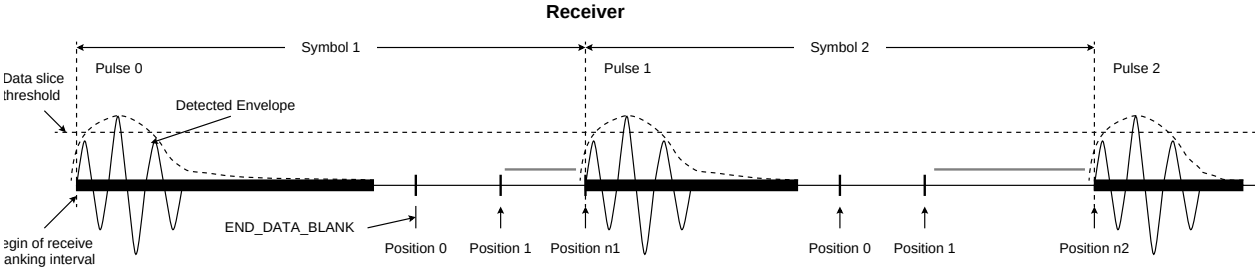
Figure 19. Transmit Data Symbol Timing

Data Receive Timing

The incoming waveform is formed from the transmitted pulse along with any distortions and reflections that occur in the wiring network. The receiver detects the point at which the envelope of the received waveform crosses a set threshold. See Figure 20.

Immediately after the threshold crossing, the receiver disables any further detection for a period ISBI-3 TICs (HPR28, ISBI_SLOW or ISBI_FAST) starting with the detection of the pulse peak.

The receiver is then re-enabled for pulse detection. Upon reception of the next pulse, the receiver measures the elapsed time from the previous pulse. This value is then placed in the nearest pulse position bin (one of 25) where pulse position 0 is at PULSE_POSITION_0 and each subsequent position is spaced one TIC from the previous one as defined in the *Data Transmit Timing* section. Data symbol intervals are therefore variable and depend on the encoded data.



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Figure 20. Receive Symbol Timing

Data Symbol RLL25 Encoding

The RLL25 code is the version of TM32 that was developed for the HomePNA PHY. It produces the highest bit rate for a given value of ISBI and TIC size. In a manner similar to run length limited disk coding, RLL25 encodes data bits in groups of varying sizes, specifically: 3, 4, 5, and 6 bits. Pulse positions are assigned to the encoded bit groups in a manner, which causes more data bits to be encoded in positions that are farther apart. This keeps both the average and minimum bit rates higher.

Data symbol RLL25 codes data by traversing a tree as illustrated in Figure 21. Assuming that successive data bits are encoded and labeled A, B, C, D,…, etc., the encoding process begins at the root node and proceeds as follows:

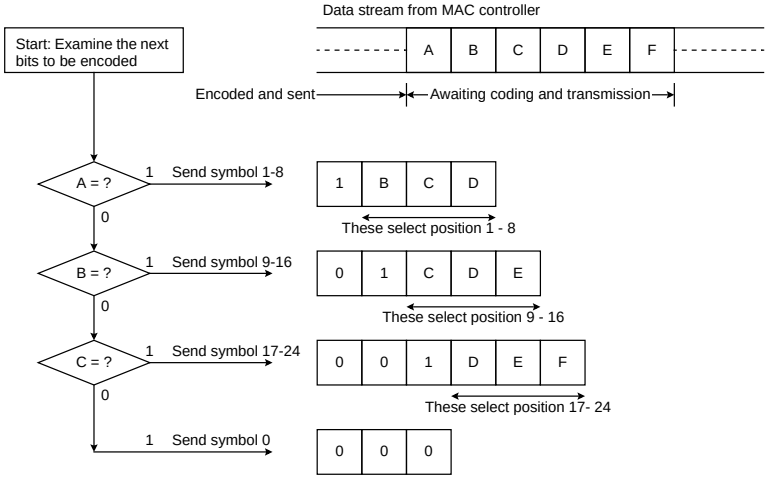
1. If the first bit (bit A) is a one, the next three bits (B, C, and D) select which one of the eight positions 1-8 is transmitted. The encoding process then continues at the root node.
2. If bit A is a zero and bit B is a one, the next three bits (C, D, and E) select which one of the eight positions 9-16 is transmitted. The encoding process then continues at the root node.
3. If bit A is a zero, bit B is a zero, and bit C is a one, the next three bits (D, E, and F) select which one of the eight positions 17-24 is transmitted. The encoding process then continues at the root node.
4. Finally, if bits A, B, and C are all zeros, position 0 is transmitted. The encoding process then continues at the root node.

As a result, Symbol 0 encodes the 3-bit data pattern 000, positions 1-8 encode the 4-bit data pattern 1BCD, positions 9-16 encode the 5-bit data pattern 01CDE, and positions 17-24 encode the 6-bit data pattern 001DEF. If the data encoded is random, 50% of the positions used will be for 4-bit patterns, 25% will be for 5-bit patterns, 12.5% will be for 6-bit patterns, and 12.5% will be for 3-bit patterns.

Mode Interface

The HomePNA PHY may be managed from either of two interfaces (the managed parameters vary depending on the interface):

1. Remote Control-Word management commands embedded in the HomePNA AID header on the wire network.
2. Management messages from a local management entity.



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Figure 21. RLL 25 Coding Tree

Header AID Remote Control Word Commands

Stations may be configured either as master stations or as slave stations. Only one master may exist on a given HomePNA segment or network over which the HomePNA PHY header is preserved.

The master station may send commands embedded in the HomePNA header control word to remotely set various parameters of the remote slave stations. Stations are identified via the AID as follows:

1. The master station is identified on the HomePNA wire network with an AID of FFh.
2. A slave is identified with an AID of 00h to EFh.
3. AID values of F0h to FEh are reserved for future use.

Once a command has been transmitted, the master station will revert to a slave AID, so that subsequent control words are not interpreted by the slave stations as new commands.

Master mode is entered by writing to the PHY control register (HPR16, bits 8 to 11) and is exited upon the completion of the command sequence.

A valid master remote command consists of three HomePNA frames with an AID of FFh. Since the HomePNA PHY header is prepended to packets received from the MAC, as well as any1Home packets, packets from the master station may be separated by intervals during which other (slave) stations may transmit their frames.

A remote master Control Word command will be recognized and executed by a HomePNA PHY when it receives three consecutive valid HomePNA frames with an AID of FFh.

Valid commands are as follows:

1. SET_POWER: Commands slave stations to set their transmit level to a prescribed level until another master command is received.
2. SET_SPEED: Commands slave stations to set their transmit speed to a prescribed value until another master command is received.

The control word bit encoding and possible values are described in Table 9.

Table 9. Master Station Control Word Functions

AID	Bit No.	Command Function
5	LSB	0 = version 0
5	MSB	0 = Set to low-power transmit mode. 1 = Set to high-power transmit mode.
6	LSB	0 = Set to low-speed transmit mode. 1 = Set to high-speed transmit mode.
6	MSB	Reserved

Slave stations transmit the following status messages in the HomePNA header control word of all outgoing frames:

1. VERSION_STATUS: The HomePNA PHY version of the slave station. The receiving station must revert to this version to interpret the packet.
2. POWER_STATUS: The transmit power level of the transmitting slave station for the current frame. All HomePNA units support both LOW_POWER and HIGH_POWER modes of operation.
3. SPEED_STATUS: The transmit speed of the slave station for the current frame. Receiving stations will adjust their receiver parameters to correctly interpret this frame.

The slave control word bit encoding is identical to the master control word format.

1 Mbps HomePNA PHY Loopback

The HomePNA PHY is capable of supporting internal loopback only.

Internal Loopback

In internal loopback, the transmitted data is returned to the receive data bus without transmitting data on the network. The MAC must be programmed to support full-duplex operation and is responsible for comparing the transmitted data to that received. Internal loopback is accomplished by setting the “enable loopback mode” in HPR0, bit 14, to 1.

any1Home Link Detection

While consuming minimal network resources, AMD’s innovative any1Home Link Detection Packet provides a means to indicate to the MAC, and thus the upper layers of the system protocol, that a valid network (as defined by HomePNA) has been detected. The Link Detection Packet is also capable of detecting a network failure and allows the upper layer protocol to take corrective action. Thus, the any1Home Packet provides link indication that the MAC requires for compliance to the Microsoft PC98, PC99, and HomePNA revision 1.1 requirements without utilizing resources from the upper layers of the system protocol

The any1Home link packet consists of valid AID and PCOM fields followed by four bytes of data. The receiving node's MAC will interpret this packet as a runt frame and will not forward the frame to upper layers, thus ensuring that no system resources are required.

The Am79C901A HomePHY will transmit the any1Home Link Packet as a result of not transmitting a normal Data packet within the last 400 ms time period. Similarly, the HomePHY will determine that it is not connected to a valid network (a link down state) after not receiving any Data or Link packets for a period greater than four seconds. The any1Home Link detection status is reported via the LED_LINK output pin and in the HomePNA PHY Status Register (HPR1, bit 2). See Table 18.

10BASE-T PHY

The 10BASE-T transceiver incorporates the physical layer function, including both clock recovery (ENDEC) and transceiver function. Data transmission over the 10BASE-T medium requires an integrated 10BASE-T MAU. The transceiver meets the electrical requirements for 10BASE-T as specified in IEEE 802.3i. The transmit signal is filtered on the transceiver to reduce harmonic content per IEEE 802.3i. Since filtering is performed in silicon, external filtering modules are not needed. The 10BASE-T PHY transceiver receives 10 Mbps data from the MAC across the MII at 2.5 million nibbles per second (parallel), or 10 million bits per second (serial) for 10BASE-T. It then Manchester encodes the data before transmission to the network.

The 10BASE-T block consists of the following sub-blocks:

— Transmit Process
— Receive Process
— Interface Status
— Collision Detect Function
— Jabber Function
— Reverse Polarity Detect

Refer to Figure 22 for the 10BASE-T block diagram.

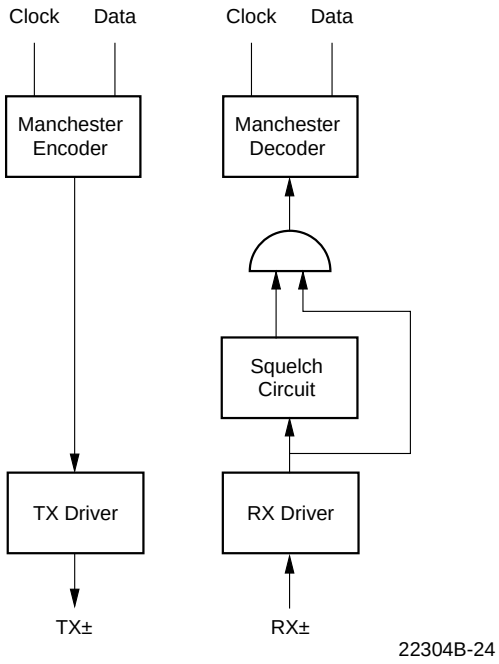


Figure 22. 10BASE-T Transmit and Receive Data Paths

Twisted Pair Transmit Function

Data transmission over the 10BASE-T medium requires use of the integrated 10BASE-T MAU and uses the differential driver circuitry on the TX± pins.

TX± is a differential twisted-pair driver. When properly terminated, TX± will meet the transmitter electrical requirements for 10BASE-T transmitters as specified in IEEE 802.3, Section 14.3.1.2. The load is a twisted pair cable that meets IEEE 802.3, Section 14.4.

Twisted Pair Receive Function

The RX± port is a differential twisted-pair receiver. When properly terminated, the RX± port will meet the electrical requirements for 10BASE-T receivers as specified in IEEE 802.3, Section 14.3.1.3. The receiver has internal filtering and does not require external filter modules or common mode chokes.

Signals appearing at the RX± differential input pair are routed to the internal decoder. The receiver function meets the propagation delays and jitter requirements specified by the 10BASE-T standard. The receiver squelch level drops to half its threshold value after unsquelch to allow reception of minimum amplitude signals and to mitigate carrier fade in the event of worst case signal attenuation and crosstalk noise conditions.

Twisted Pair Interface Status

The Am79C901A device will power up in the Link Fail state. The Auto-Negotiation algorithm will apply to allow it to enter the Link Pass state.

In the Link Pass state, receive activity which passes the pulse width/amplitude requirements of the RX± inputs will cause the PCS Control block to assert the Carrier Sense (CRS) signal at the MII interface. A collision would cause the PCS Control block to assert Carrier Sense (CRS) and Collision (COL) signals at the MII. In the Link Fail state, this block would cause the PCS Control block to deassert Carrier Sense (CRS) and Collision (COL).

In jabber detect mode, this block would cause the PCS Control block to assert the COL signal at the MII and allow the PCS Control block to assert or deassert the CRS pin to indicate the current state of the RX± pair. If there is no receive activity on RX±, this block would cause the PCS Control block to assert only the COL pin at the MII. If there is RX± activity, this block would cause the PCS Control block to assert both COL and CRS at the MII.

Collision Detect Function

Simultaneous activity (presence of valid data signals) from both the internal encoder transmit function and the twisted pair RX± pins constitutes a collision, thereby causing the PCS Control block to assert the COL pin at the MII.

Jabber Function

The Jabber function inhibits the 10BASE-T twisted pair transmit function of the Am79C901A device if the TX± circuits are active for an excessive period (20-150 ms). This prevents one port from disrupting the network due to a stuck-on or faulty transmitter condition. If the maximum transmit time is exceeded, the data path through the 10BASE-T transmitter circuitry is disabled (although Link Test pulses will continue to be sent). The PCS Control block also asserts the COL signal at the MII and sets the Jabber Detect bit in Register 1 of the active PHY. Once the internal transmit data stream from the MENDEC stops, an unjab time of 250-750 ms will elapse before this block causes the PCS Control block to deassert the COL indication and re-enable the transmit circuitry.

When jabber is detected, this block will cause the PCS Control block to assert the COL signal and allow the PCS Control block to assert or deassert the CRS signal to indicate the current state of the RX± pair. If there is no receive activity on RX±, this block causes the PCS Control block to assert only the COL signal at the MII. If there is RX± activity, this block will cause the PCS Control block to assert both COL and CRS on the MII.

Reverse Polarity Detect

The polarity for 10BASE-T signals is set by reception of Normal Link Pulses (NLP) or packets. Polarity is locked, however, by incoming packets only. The first NLP received when trying to bring the link up will be ignored, but it will set the polarity to the correct state. The reception of two consecutive packets will cause the polarity to be locked, based on the polarity of the End of Transmit Data (ETD). In order to change the polarity once it has been locked, the link must be brought down and back up again.

Auto-Negotiation

The object of the Auto-Negotiation function is to determine the abilities of the devices sharing a link. After exchanging abilities, the Am79C901A device and remote link partner device acknowledge each other and make a choice of which advertised abilities to support. The Auto-Negotiation function facilitates an ordered resolution between exchanged abilities. This exchange allows both devices at either end of the link to take maximum advantage of their respective shared abilities.

The Auto-Negotiation algorithm uses a burst of link pulses called Fast Link Pulses (FLPs). The burst of link pulses are spaced between 55 and 140 µs so as to be ignored by the standard 10BASE-T algorithm. The FLP burst conveys information about the abilities of the sending device. The receiver can accept and decode an FLP burst to learn the abilities of the sending device. The link pulses transmitted conform to the standard 10BASE-T template. The device can perform Auto-Negotiation with reverse polarity link pulses.

The Am79C901A device uses the Auto-Negotiation algorithm to select the type connection to be established according to the following priority: 10BASE-T full duplex, then 10BASE-T half-duplex. See Table 10.

The Auto-Negotiation algorithm is initiated by the following events: Auto-Negotiation enable bit is set, hardware reset, soft reset, transition to link fail state (when Auto-Negotiation enable bit is set), or Auto-Negotiation restart bit is set. The result of the Auto-Negotiation process can be read from the status register (Summary Status Register, TBR24).

By default, the link partner must be at least 10BASE-T half-duplex capable. The Am79C901A PHY can automatically negotiate with the network and yield the highest performance possible without software support.

Table 10. Auto-Negotiation Capabilities

Network Speed	Physical Network Type
20 Mbps	10BASE-T, Full Duplex
10 Mbps	10BASE-T, Half Duplex

Auto-Negotiation goes further by providing a message-based communication scheme called *Next Pages* before connecting to the Link Partner.

Soft Reset Function

The PHY Control Register (TBR0) incorporates the soft reset function (bit 15). It is a read/write register and is self-clearing. Writing a 1 to this bit causes a soft reset. When read, the register returns a 1 if the soft reset is still being performed; otherwise, it is cleared to zero. *Note that the register can be polled to verify that the soft reset has terminated*. Under normal operating conditions, soft reset will be finished in 150 clock cycles.

Soft reset only resets the 10BASE-T PHY unit registers to default values (some register bits retain their previous values). Soft reset does not reset the management interface.

10BASE-T Loopback

The 10BASE-T PHY is capable of supporting two different types of loopback, referred to as internal and external loopback.

Internal Loopback

In internal loopback, the transmitted data is returned to the receive data bus without transmitted data appearing on the network. The MAC must be programmed to support full-duplex operation and is responsible for comparing the transmitted data to that received. Internal loopback is accomplished by setting the “enable loopback mode” in TBR0, bit 14, to 1.

External Loopback

External loopback is accomplished by the use of an external shorting plug. In this environment, the 10BASE-T PHY is left in through mode (i.e., enable loopback mode in TBR0 = 0), the MAC in full duplex. The transmitted data will then be looped back at the shorting plug into the receive circuitry and driven onto the receive data bus for the MAC to process and verify.

LED Support

The controller can support up to five LEDs. LED outputs $\overline{\text{LED_COL}}$, $\overline{\text{LED_ACTIVITY}}$, $\overline{\text{LED_LINK}}$, $\overline{\text{LED_SPEED}}$, and $\overline{\text{LED_POWER}}$ allow for direct connection of an LED and its supporting pull-up device.

The outputs are stretched to allow the human eye to recognize even short events that last only several microseconds. The five LED outputs are configured as shown in Table 11.

Table 11. LED Default Configuration

LED Output	Indication	Driver Mode	Pulse Stretch
LED_COL	Collision	Open Drain - Active Low	Enabled
LED_ACTIVITY	Activity	Open Drain - Active Low	Enabled
LED_LINK	Link	Open Drain - Active Low	Not applicable
LED_SPEED	Speed	Open Drain - Active Low	Not applicable
LED_POWER	Power	Open Drain - Active Low	Not applicable

IEEE 1149.1 (JTAG) Test Access Port Interface

An IEEE 1149.1-compatible boundary scan Test Access Port is provided for board-level continuity test and diagnostics. All digital input, output, and input/output pins are tested. The following paragraphs summarize the IEEE 1149.1-compatible test functions implemented in the controller. Refer to the IEEE 1149.1 Boundary Scan Architecture document for details.

Boundary Scan Circuit

The boundary scan test circuit requires four pins (TCK, TMS, TDI, and TDO), defined as the Test Access Port (TAP). It includes a finite state machine (FSM), an instruction register, a data register array, and a power-on reset circuit. Internal pull-up resistors are provided for the TDI, TCK, and TMS pins.

TAP Finite State Machine

The TAP engine is a 16-state FSM driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power-on reset circuit is provided to ensure that the FSM is in the TEST_LOGIC_RESET state at power-up. Therefore, the $\overline{\text{TRST}}$ is not provided. The FSM is also reset when TMS and TDI are high for five TCK periods.

Supported Instructions

In addition to the minimum IEEE 1149.1 requirements (BYPASS, EXTEST, and SAMPLE instructions), two additional instructions (IDCODE and TRI_ST) are provided to further ease board-level testing. All unused instruction codes are reserved. See Table 12 for a summary of supported instructions.

Table 12. IEEE 1149.1 Supported Instruction Summary

Instruction Name	Instruction Code	Description	Mode	Selected Data Register
EXTEST	0000	External Test	Test	BSR
IDCODE	0001	ID Code Inspection	Normal	ID REG
SAMPLE	0010	Sample Boundary	Normal	BSR
TRI_ST	0011	Force Tri-State	Normal	Bypass
BYPASS	1111	Bypass Scan	Normal	Bypass
TRI_ST	0011	Force Tri-State	Normal	Bypass
BYPASS	1111	Bypass Scan	Normal	Bypass

Instruction Register and Decoding Logic

After the TAP FSM is reset, the IDCODE instruction is always invoked. The decoding logic gives signals to control the data flow in the data registers according to the current instruction.

Boundary Scan Register

Each Boundary Scan Register (BSR) cell has two stages. A flip-flop and a latch are used for the Serial Shift Stage and the Parallel Output Stage, respectively. There are four possible operation modes in the BSR cell shown in Table 13.

Table 13. BSR Mode Of Operation

1	Capture
2	Shift
3	Update
4	System Function

Other Data Registers

Other data registers are the following:

1. Bypass register (1 bit)
2. Device ID register (32 bits) (Table 14).

Table 14. Device ID Register

Bits 31-28	Version
Bits 27-12	Part Number (1001 0000 0001 0000)
Bits 11-1	Manufacturer ID. The 11-bit manufacturer ID code for AMD is 00000000001 in accordance with JEDEC publication 106-A.
Bit 0	Always a logic 1

Boundary Scan Cells

In Boundary Scan, most of the chip input and output latches are linked together to form a scan chain. The main purpose of this is board-level testing. See Table 15.

To force the output pins, use SAMPLE to load the BSR cells via the TDI pin and EXTEST to force the output. Program the output cells, and set the control cells to enable the output, or clear the control cells to float the output.

To sample the chip inputs and outputs, use a SAMPLE command and cell values are shifted out through the TDO pin. Check the values in the input cells. Both input and output pins have input-type cells.

Table 15. Boundary Scan Ring Order

BSR Cell No.	Cell Name	Cell Type[1]	Pin No.
53	XTAL_SEL_L	IN	39
52	CRS	IN	32
51	CRS	OUT	32
50	CRS_COL_OEN	CO	–
49	COL	IN	30
48	COL	OUT	30
47	TXD3_CSN	IN	28
46	TXD2	IN	27
45	TXD1_SDI	IN	25
44	TXD0_TXDAT	IN	24
43	TX_EN	IN	23
42	TX_CLK_OEN	CO	–
41	TX_CLK	IN	22
40	TX_CLK	OUT	22
39	GM_MODE	IN	21
38	RX_ER	IN	19
37	RX_ER	OUT	19
36	PHY_SEL	IN	17
35	RX_CLK	IN	15
34	RX_CLK	OUT	15
33	RX_DV_RXEN	IN	13
32	RX_DV_RXEN	OUT	13
31	RXD_OEN	CO	–
30	RXD0_RXDAT	IN	11
29	RXD0_RXDAT	OUT	11
28	RXD1	IN	10
27	RXD1	OUT	10
26	RXD2	IN	9
25	RXD2	OUT	9
24	RXD3	IN	8
23	RXD3	OUT	8
22	LED_SPEED	CO	6
21	LED_SPEED	IN	6
20	LED_SPEED	OUT	6
19	LED_POWER	CO	5

18	LED_POWER	IN	5
17	LED_POWER	OUT	5
BSR Cell No.	**Cell Name**	**Cell Type[1]**	**Pin No.**
16	LED_ACTIVITY	CO	3
15	LED_ACTIVITY	IN	3
14	LED_ACTIVITY	OUT	3
13	LED_COL	CO	2
12	LED_COL	IN	2
11	LED_COL	OUT	2
10	LED_LINK	CO	1
9	LED_LINK	IN	1
8	LED_LINK	OUT	1
7	MDC_SCLK	IN	68
6	MDIO	IN	66
5	MDIO	OUT	66
4	MDIO_OEN	CO	–
3	ISOLATE	IN	65
2	PHY_AD	IN	64
1	MODE_MII	IN	63
0	RESET_L	IN	61

Notes:

1. *IN = input cells, samples the device inputs and internal outputs; OUT = output cells, drives the device outputs and internal inputs; and CO = control cells, controls the output enable.*
2. *BSR Cell 0 is closest to TDO.*
3. *Boundary register is 54 bits long. Data path starts from TDI to cell 53, cell 0 to TDO.*

USER ACCESSIBLE REGISTERS

The Am79C901A PHY has two types of user registers: 1 Mbps HomePNA PHY management registers (HPRs) and 10BASE-T PHY management registers (TBRs).

1 Mbps HomePNA PHY Management Registers (HPRs)

The registers of the HomePNA PHY are accessible via the MII or the SPI interface. All reserved registers should not be written to, and reading them will return an undetermined value. Table 16 lists all the registers implemented in the HomePNA PHY.

Table 16. 1 Mbps HomePNA PHY Management Registers (HPRs)

Register Address	Symbol	Name	Basic/Extended	Default Value After H_RESET
0	HPR0	Control Register	B	0400h
1	HPR1	Status Register	B	0841h
2	HPR2	PHY_ID Register	E	0000h
3	HPR3	PHY_ID Register	E	6B91h
4	HPR4	Auto-Negotiation Register	E	0021h
5	HPR5	Auto-Negotiation Register	E	0000h
6	HPR6	Auto-Negotiation Register	E	0000h
7	HPR7	Auto-Negotiation Register	E	0000h
8-15	HPR8-HPR15	Reserved	E	–
16	HPR16	PHY Control Register	E	0005h
17	HPR17	Status/Control Register	E	000xh
18	HPR18	PHY TXCOMM Register	E	0000h
19	HPR19	PHY TXCOMM Register	E	0000h
20	HPR20	PHY RXCOMM Register	E	0000h
21	HPR21	PHY RXCOMM Register	E	0000h
22	HPR22	PHY AID Register	E	0000h
23	HPR23	PHY Noise Control Register	E	03FFh
24	HPR24	PHY Noise Control 2 Register	E	F4xxh
25	HPR25	PHY Noise Statistics Register	E	03FFh
26	HPR26	Event Status Register	E	0000h
27	HPR27	AID Control Register	E	1440h
28	HPR28	ISBI Control Register	E	2C1Ch
29	HPR29	TX Control Register	E	0444h
30	HPR30	Drive Level Control Register	E	x549h
31	HPR31	Analog Control Register	E	C000h

HPR0: HomePNA PHY Control Register (Register 0)

Table 17. HPR0: HomePNA PHY Control Register (Register 0)

Bits	Name	Description	Read/ Write	Default Value (hex)
15	RESET	1 = RESET When read, 1= reset in process 0 = Normal operation ** Self Clearing after ~70 µs	R/W	0
14	Enable Loopback Mode	1 = Loopback mode enable 0 = Loopback mode disable	R/W	0
13	Speed Selection	0 = 10 Mbps	R	0
12	Auto-Negotiation Enabled	1 = Enabled 0 = Disabled	R	0
11	Power Down	1 = Power down 0 = Normal operation (This bit is mirrored in PHY Control bit 4)	R	0
10	Isolate	1 = Electrically isolates PHY from the MII/GPSI 0 = Normal operation	R/W	1
9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation 0 = Normal operation ** Self Clearing	R	0
8	Duplex Mode	1 = Full-Duplex (for Loopback test only) 0 = Half-Duplex	R/W	0
7	Collision Test (Note 1)	1 = Enable COL test signal 0 = Disable COL test signal	R/W	0
6:0	Reserved	Write as 0, ignore on read	R	0

Notes:

1. *For collision test, the “enable loopback mode” bit must also be set to ensure that collision traffic is not imposed on the network.*
2. *R/W = Read/Write; R = Read only.*

HPR1: HomePNA PHY Status Register (Register 1)

Table 18. HPR1: HomePNA PHY Status Register (Register 1)

Bits	Name	Description	Read/Write	Default Value (hex)
15	100BASE-T4	0 = PHY not able to perform 100BASE-T4	R	0
14	100BASE-X Full-Duplex	0 = PHY not able to perform Full-Duplex 100BASE-X	R	0
13	100BASE-X Half-Duplex	0 = PHY not able to perform Half-Duplex 100BASE-X	R	0
12	10 Mbps Full-Duplex	0 = PHY not able to perform 10 Mbps in Full-Duplex	R	0
11	10 Mbps Half-Duplex	1 = PHY able to perform 10 Mbps in Half-Duplex	R	1
10:7	Reserved	Reads will produce undefined results	R	X
6	Management Frame Preamble Suppression	1 = PHY will accept management frames with Preamble suppressed 0 = PHY will not accept management frames with Preamble suppressed	R	1
5	Auto-Negotiation Complete	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed	R	0
4	Remote Fault	1 = Remote fault detected 0 = Normal operation	R	0
3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	R	0
2	Link Status	1 = Link is up 0 = Link is down This bit will be RESET (latched low and re-enabled on Read).	R	0
1	Jabber Detect	1 = Jabber condition detected 0 = Normal operation	R	0
0	Extended Capability	1 = Extended Register capability 0 = Basic Register Set capability	R	1

HPR2 and HPR3: HomePNA PHY ID Registers (Registers 2 and 3)

Table 19. HPR2: HomePNA PHY ID Register (Register 2)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:0	PHY_ID MSB (31-16)	Most significant bytes of the PHY_ID (Bits 3-18)	R	0000

Table 20. HPR3: HomePNA PHY ID Register (Register 3)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:10	PHY_ID LSB (15-10)	IEEE Address (Bits 19-24)	R	1A
9:4	PHY_ID LSB (9-4)	Manufacturer's Model Number	R	39
3:0	PHY_ID LSB (3-0)	Revision Number	R	1 (rev. A.1) 2 (rev. A.2) 3 (rev. A.3)

HPR4: HomePNA PHY Auto-Negotiation Advertisement Register (Register 4)

This register contains the advertised ability of the Am79C901A device. The purpose of this register is to advertise the technology ability to the link partner device. When this register is modified, Restart Auto-Negotiation (Register 0, bit 9) must be enabled to guarantee the change is implemented.

Table 21. HPR4: HomePNA PHY Auto-Negotiation Advertisement Register (Register 4)

Bits	Name	Description	Read/Write	Default Value (hex)
15	Next Page	When set, the device wishes to engage in next page exchange. If cleared, the device does not wish to engage in next page exchange.	R	0
14	Reserved		R	0
13	Remote Fault	When set, a remote fault bit is inserted into the base link code word during the Auto-Negotiation process. When cleared, the base link code work will have the bit position for remote fault as cleared.	R	0
12:11	Reserved		R	0
10	PAUSE	This bit should be set if the PAUSE capability is to be advertised.	R	0
9	Reserved		R	0
8	Full-Duplex 100BASE-TX	This bit advertises Full-Duplex capability. When set, Full-Duplex capability is advertised. When cleared, Full-Duplex capability is not advertised.	R	0
7	Half-Duplex 100BASE-TX	This bit advertises Half-Duplex capability for the Auto-Negotiation process. Setting this bit advertises Half-Duplex capability. Clearing this bit does not advertise Half-Duplex capability.	R	0
6	Full-Duplex 10BASE-T	This bit advertises Full-Duplex capability. When set, Full-Duplex capability is advertised. When cleared, Full-Duplex capability is not advertised.	R	0
5	Half-Duplex 10BASE-T	This bit advertises Half-Duplex capability for the Auto-Negotiation process. Setting this bit advertises Half-Duplex capability. Clearing this bit does not advertise Half-Duplex capability.	R	1
4:0	Selector Field	The Am79C901A device is an IEEE 802.3 compliant device.	R	01

HPR5: HomePNA PHY Auto-Negotiation Link Partner Ability Register (Register 5)

The Auto-Negotiation Link Partner Ability Register is Read Only. The register contains the advertised ability of the link partner. The bit definitions represent the received link code word. This register contains either the base page or the link partner's next pages. The values contained in these registers are only valid once Auto-Negotiation has successfully completed, as indicated by bit 5 in HPR1, or if the Next Page exchange is used, after the Page Received (bit 1 of HPR6) has been set to logic one.

Table 22. HPR5: HomePNA PHY Auto-Negotiation Link Partner Ability Register - Base Page Format (Register 5)

Bits	Name	Description	Read/Write	Default Value (hex)
15	Next Page	Link partner next page request	R	0
14	Acknowledge	Link partner acknowledgment	R	0
13	Remote Fault	Link partner remote fault request	R	0
12:5	Technology Ability	Link partner technology ability field	R	0
4:0	Selector Field	Link partner selector field	R	0

Table 23. HPR5: HomePNA PHY Auto-Negotiation Link Partner Ability Register - Next Page Format (Register 5)

Bits	Name	Description	Read/Write	Default Value (hex)
15	Next Page	Link partner next page request	R	0
14	Acknowledge	Link partner acknowledgment	R	0
13	Message Page	Link partner message page request	R	0
12	Acknowledge 2	1 = Link partner can comply with the request 0 = Link partner cannot comply with the request	R	0
11	Toggle	Link partner toggle bit	R	0
10:0	Message Field	Link partner's message code	R	0

HPR6: HomePNA PHY Auto-Negotiation Expansion Register (Register 6)

The Auto-Negotiation Expansion Register provides additional information that aids the Auto-Negotiation process. The Auto-Negotiation Expansion Register bits are Read Only.

Table 24. HPR6: HomePNA PHY Auto-Negotiation Expansion Register (Register 6)

Bits	Name	Description	Read/Write	Default Value (hex)
15:5	Reserved		R	0
4	Parallel Detection Fault	1 = Parallel detection fault 0 = No parallel detection fault	R	0
3	Link Partner Next Page Able	1 = Link partner is next page able 0 = Link partner is not next page able	R	0
2	Next Page Able	1 = Am79C901A device channel is next page able 0 = Am79C901A device channel is not next page able	R	0
1	Page Received	1 = A new page has been received 0 = A new page has not been received	R	0
0	Link Partner Auto-Negotiation Able	1 = Link partner is Auto-Negotiation able 0 = Link partner is not Auto-Negotiation able	R	0

HPR7: HomePNA PHY Auto-Negotiation Next Page Register (Register 7)

The Auto-Negotiation Next Page Register contains the next page link code word to be transmitted. On power-up the default value of 0x2001 represents a message page with the message code set to null.

Table 25. HPR7: HomePNA PHY Auto-Negotiation Next Page Register (Register 7)

Bits	Name	Description	Read/Write	Default Value (hex)
15	Next Page	Am79C901A device channel next page request	R	0
14	Reserved		R	0
13	Message Page	Am79C901A device channel message page request	R	0
12	Acknowledge 2	1 = Am79C901A device channel can comply with the request 0 = Am79C901A device channel cannot comply with the request	R	0
11	Toggle	Am79C901A device channel toggle bit	R	0
10:0	Message Field	Message code field	R	000

Reserved Registers: HPR8 - HPR15

These registers should be ignored when read and should not be written to at any time.

HPR16: HomePNA PHY Control Register (Register 16)

Table 26. HPR16: HomePNA PHY Control Register (Register 16)

Bits	Name	Description	Read/ Write	Default Value (hex)
15	Remote Command	1 = Ignore Remote Commands 0 = Normal operation	R/W	0
14:13	Reserved	Reads will produce undefined results. Should be written as 0.	R/W	XX
12	SQE_TEST Disable	1 = Disables the SQE heartbeat which occurs after each transmission. 0 = The heartbeat assertion occurs on the COL pin approximately 1-5 µs after transmission and for a duration of 1 µs.	R/W	0
11	Command Low Power	1 = Command low power 0 = Normal operation	R/W	0
10	Command High Power	1 = Command high power 0 = Normal operation	R/W	0
9	Command Low Speed	1 = Command low speed 0 = Normal operation	R/W	0
8	Command High Speed	1 = Command high speed 0 = Normal operation	R/W	0
7	Disable AID Negotiation	1 = Disable AID negotiation 0 = Normal operation	R/W	0
6	Clear PHY-Event Counter	1 = Clear PHY event counter 0 = Normal operation **Self clearing after ~100 ns	R/W	0
5	Disable Squelch adaptation	1 = Disable Squelch adaptation 0 = Normal operation	R/W	0
4	Power Down	1 = Power down 0 = Normal operation (This bit is controlled by the HPR0, bit 11)	R	0
3	Reserved	Reads will produce undefined results	R	X
2	High Speed	1 = Device is currently in High speed 0 = Device is currently in Low speed	R/W	1
1	High Power	1 = Device is currently in High power 0 = Device is currently in Low power	R/W	0
0	Reserved	Reads will produce undefined results	R/W	X

Note: *Writes to bits 1 and 2 will affect speed and power on node only.*

HPR17: HomePNA PHY Status/Control Register (Register 17)

The HomePNA PHY Status/Control Register provides information regarding the global aspects of the operation of the PHY.

Table 27. HPR17: HomePNA PHY Status/Control Register (Register 17)

Bits	Name	Description	Read/Write	Default Value (hex)
15:13	Reserved	Test control bits. Reads will produce undefined results. Should be written as 0.	R	00
12	any1Home_ Disable	1 = any1Home Link packet disabled 0 = any1Home Link packet enabled	R/W	0
11:8	Reserved	Test control bits. Reads will produce undefined results. Should be written as 0.	R	3
7	Reserved	Test control bit. Reads will produce undefined results. Should be written as 0.	R	0
6	Received_Power	1 = Last packet received, was sent at High Power 0 = Last packet received, was sent at Low Power	R	0
5	Received_Speed	1 = Last packet received, was sent at High Speed 0 = Last packet received, was sent at Low Speed	R	0
4	Received_Ver	1 = Last packet received, was sent at Version XX 0 = Last packet received, was sent at Version 0	R	0
3:0	Reserved	Test control bits. Reads will produce undefined results. Should be written as 0.	R	X

HPR18 and HPR19: HomePNA PHY TxCOMM Registers (Registers 18 and 19)

Table 28. HPR18 and HPR19: HomePNA PHY TxCOMM Registers (Registers 18 and 19)

Bits	Name	Description	Read/Write	Default Value (hex)
15:0	PHY_TX_COMM (4)	The 32-bit preamble transmitted on the HomePNA PHY. HPR18 contains the high word and HPR19 the low word.	R/W	0000

The 32-bit transmitted data field is to be used for out-of-band communication between PHY management entities. No protocol for out-of-band management has been defined. Accessing the low word causes the PHY to send all-0 PCOMs until the high word has been accessed. Once accessed, the next transmitted packet will cause this register's contents to be shifted out in the PCOM field of the transmitted packet. Upon transmission, this register will read back as all 0s. A non-null transmitted PCOM will set the TxPCOM Ready bit in the Event Status Register (HPR26). An access to any of the two TxPCOM words will clear the TxPCOM Ready bit in the ISTAT register.

HPR20 and HPR21: HomePNA PHY RxCOMM Registers (Registers 20 and 21)

Table 29. HPR20 and HPR21: HomePNA PHY RxCOMM Registers (Registers 20 and 21)

Bits	Name	Description	Read/Write	Default Value (hex)
15:0	PHY_RX_COMM (4)	The 32-bit preamble received by the HomePNA PHY. HPR20 contains the high word and HPR21 the low word.	R	0000

The 32-bit received data field to be used for out-of-band communication between PHY management entities. No protocol for out-of-band management has been defined. Accessing the low word of the register is sufficient to ensure that subsequently received packets will not overwrite the register contents. A non-null received PCOM will set the RxPCOM Valid bit of the Event Status Register (HPR26). Accessing the high word of the register clears this bit and allows overwriting of the register by subsequent received packets.

HPR22: HomePNA PHY AID Register (Register 22)

Table 30. HPR22: HomePNA PHY AID Register (Register 22)

Bits	Name	Description	Read/Write	Default Value (hex)
15:8	PHY_AID	The Access ID of this PHY. If PHY_Control Disable AID Negotiation is set, then writes to this bit will have no effect.	R/W	00
7:0	Noise Events	An 8-bit counter that records the number of noise events detected. Overflows are held as FFh. Can be cleared by setting bit 6 of HPR16.	R/W	00

The PHY's AID address is used for collision detection. Unless bit 7 of the CONTROL register is set, the PHY is assured to select a unique AID address. Addresses above EFh are reserved. Address FFh is defined to indicate a remote command.

HPR23: HomePNA PHY Noise Control Register (Register 23)

Table 31. HPR23: HomePNA PHY Noise Control Register (Register 23)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:8	Noise Floor	If the input NOISE measurement (HPR25, bits 15:8) exceeds the PEAK measurement (HPR25, bits 7:0), this value is loaded into the NOISE Level register HPR25, bits 15:8.	R/W	03
7:0	Noise Ceiling	If the input NOISE measurement (HPR25, bits 15:8) exceeds the PEAK measurement (HPR25, bits 7:0), this value is loaded into the NOISE Level register HPR25, bits 7:0.	R/W	FF

HPR24: HomePNA PHY Noise Control 2 Register (Register 24)

Table 32. HPR24: HomePNA PHY Noise Control 2 Register (Register 24)

Bits	Name	Description	Read/ Write	Default Value
15:8	Noise Attack	Sets the attack characteristics of the NOISE algorithm. High nibble sets number of noise events needed to raise the NOISE level immediately, while the low nibble is the number of noise events needed to raise the level at the end of an 870 ms period.	R/W	F4
7:0	Reserved	Reads will produce undefined results.	R	XX

HPR25: HomePNA PHY Noise Statistics Register (Register 25)

Table 33. HPR25: HomePNA PHY Noise Statistics Register (Register 25)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:8	Noise Level	This is the digital value of the SLICE_LVL_NOISE output. It is effectively a measure of the noise level on the wire and tracks noise by counting the number of false triggers of the NOISE comparator in an 800 ms window. When auto-adaptation is enabled (bit 5 of the PHY_Control Register is false), this register is updated with the current NOISE count every 50 ns. When adaptation is disabled, this register may be written to and is used to generate both the SLICE_LVL_NOISE and SLICE_LVL_DATA signals.	R/W	03
7:0	Peak Level	This is a measurement of the peak level of the last valid (non-collision) AID received.	R/W	FF

HPR26: HomePNA PHY Event Status Register (Register 26)

Table 34. HPR26: HomePNA PHY Event Status Register (Register 26)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:10	Reserved		R	0
9	RxPCOM	Indicates a valid RxPCOM. An access to the RxCOM MSB Register 18 will clear this bit.	R	0
8	TxPCOM	Indicates a valid TxPCOM. Any access to the TxCOM registers (Registers 20 and 21) will clear this bit.	R	0
7:4	Reserved	Reads will produce undefined results. Should be written as 0.	R	X
3	Packet Received	Status is cleared by writing a 0.	R/W	0
2	Packet Transmitted	Status is cleared by writing a 0.	R/W	0
1	Remote Command Received	A valid remote command was received. Status is cleared by writing a 0.	R/W	0
0	Remote Command Sent	A remote command has been sent. Status is cleared by writing a 0.	R/W	0

HPR27: HomePNA PHY AID Control Register (Register 27)

The HomePNA AID Control Register reports the state of each event source. Any bit may be written and so facilitate software-stimulated event testing.

Table 35. HPR27: HomePNA PHY AID Control Register (Register 27)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:8	AID_INTERVAL	This value defines the number of TCLKs (116.6 ns) separating AID symbols.	R/W	14
7:0	AID_ISBI	This value defines the number of TCLKs (116.6 ns) separating AID symbol 0.	R/W	40

HPR28: HomePNA PHY ISBI Control Register (Register 28)

Table 36. HPR28: HomePNA PHY ISBI Control Register (Register 28)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:8	ISBI_SLOW	This value defines the number of TCLKs (116.6 ns) separating data pulses for Symbol 0 in low-speed mode.	R/W	2C
7:0	ISBI_FAST	This value defines the number of TCLKs (116.6 ns) separating data pulses for Symbol 0 in high-speed mode.	R/W	1C

HPR29: HomePNA PHY TX Control Register (Register 29)

Table 37. HPR29: HomePNA PHY TX Control Register (Register 29)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:8	TX_PULSE_WIDTH	This value defines the duration of a transmit pulse in OSC cycles (16.7 ns). This will effectively determine the transmit spectrum of the PHY.	R/W	04
7:4	TX_PULSE_CYCLES_N	This value defines the number of pulses that will be driven onto the HRTXRX_N pin.	R/W	4
3:0	TX_PULSE_CYCLES_P	This value defines the number of pulses that will be driven onto the HRTXRX_P pin.	R/W	4

HPR30: HomePNA PHY Drive Level Control Register (Register 30)

Table 38. HPR30: HomePNA PHY Drive Level Control Register (Register 30)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:12	Reserved	Reserved. Must be written as 0. Read = X.	R	XX
11:6	High Level Control	Defines the drive level that will be utilized in the High Power mode.	R/W	15
5:0	Low Level Control	Defines the drive level that will be utilized in the Low Power mode.	R/W	09

HPR31: HomePNA PHY Analog Control Register (Register 31)

Table 39. HPR31: HomePNA PHY Analog Control Register (Register 31)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:11	Level_Adjust	Global output slope adjustment. These bits control the number of current sources enabled for transmit. Each bit represents a single current source. Thus 10101 enables three current sources as does 11100.	R/W	18
10:8	Reserved	Reserved. Must be written as 0.	R/W	0
7	Force_Link_Valid	1 = Link Status bit will be held valid 0 = Normal operation	R/W	0
6:0	Reserved	Reserved. Must be written as 0.	R/W	0

10BASE-T PHY Management Registers (TBRs)

The Am79C901A home networking device supports the MII basic register set and extended register set. Both sets of registers are accessible through the MII management interface or via the SPI interface. As specified in the IEEE standard, the basic register set-Status Register (Register 1). The extended register set consists of the Control Register (Register 0) and the consists of Registers 2 to 31 (decimal).

Table 40 lists all the 10BASE-T registers implemented in the device. All the reserved registers should not be written to, and reading them will return an undetermined value.

Table 40. 10BASE-T PHY Management Registers (TBRs)

Register Address	Symbol	Name	Basic/Extended	Default Value After H_RESET
0	TBR0	PHY Control Register	B	1500h
1	TBR1	PHY Status Register	B	1xx9h
2	TBR2	PHY Identifier Register	E	0000h
3	TBR3	PHY Identifier Register	E	6B71h
4	TBR4	Auto-Negotiation Advertisement Register	E	0061h
5	TBR5	Auto-Negotiation Link Partner Ability Register	E	0000h
6	TBR6	Auto-Negotiation Expansion Register	E	0004h
7	TBR7	Auto-Negotiation Next Page Register	E	2001h
8:15	TBR8-TBR15	Reserved	E	–
16	TBR16	Status and Enable Register	E	0000h
17	TBR17	PHY Control/Status Register	E	0001h
18	TBR18	Reserved	E	–
19	TBR19	PHY Management Extension Register	E	–
20:23	TBR20-TBR23	Reserved	E	–
24	TBR24	Summary Status Register	E	0000h
25:31	TBR25-TBR31	Reserved	E	–

TBR0: 10BASE-T PHY Control Register (Register 0)

Table 41. TBR0: 10BASE-T PHY Control Register (Register 0)

Bits	Name	Description	Read/Write (Note 1)	Default Value (hex)
15	Soft Reset (Note 2)	When write 1 = PHY software reset 0 = Normal operation When read 1 = Reset in process 0 = Reset done	R/W, SC	0
14	Enable Loopback Mode	1 = Loopback mode enable 0 = Loopback mode disable	R/W	0
13	Speed Selection (Note 3)	1 = 100 Mbps (not available) 0 = 10 Mbps	R	0
12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation 0 = Disable Auto-Negotiation	R/W	1
11	Power Down	1 = Power down 0 = Normal operation	R/W	0
10	Isolate (Note 4)	1 = Electrically isolates PHY from the MII/GPSI 0 = Normal operation	R/W	1
9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation 0 = Normal operation	R/W, SC	0
8	Duplex Mode (Note 3)	1 = Full-Duplex 0 = Half-Duplex	R/W	1
7	Collision Test (Note 5)	1 = Enable COL signal test 0 = Disable COL signal test	R/W	0
6:0	Reserved	Write as 0, ignore on read	R	0

Notes:

1. *R/W = Read/Write, SC = Self Clearing, R = Read only.*
2. *Soft Reset does not reset the PDX block. Refer to the Soft Reset section for details.*
3. *Bits 8 and 13 have no effect if Auto-Negotiation is enabled (Bit 12 = 1).*
4. *If the ISOL pin of the chip and the Isolate bit in Register 0 is 1, this bit will be set.*
5. *The “enable loopback mode” bit must also be set to ensure that collision traffic is not imposed on the network.*

TBR1: 10BASE-T Status Register (Register 1)

The Status Register identifies the physical and Auto-Negotiation capabilities of the local PHY. This register is read only; a write will have no effect. See Table 42.

Table 42. TBR1: 10BASE-T PHY Status Register (Register 1)

Bits	Name	Description	Read/Write (Note 1)	Default Value (hex)
15	100BASE-T4	1 = 100BASE-T4 able 0 = Not 100BASE-T4 able	R	0
14	100BASE-X Full-Duplex	1 = 100BASE-X full-duplex able 0 = Not 100BASE-X full-duplex able	R	0
13	100BASE-X Half-Duplex	1 = 100BASE-X half-duplex able 0 = Not 100BASE-X half-duplex able	R	0
12	10 Mbps Full-Duplex	1 = 10 Mbps full-duplex able 0 = Not 10 Mbps full-duplex able	R	1
11	10 Mbps Half-Duplex	1 = 10 Mbps half-duplex able 0 = Not 10 Mbps half-duplex able	R	1
10:7	Reserved	Ignore when read	R	X
6	Management Frame Preamble Suppression	1 = PHY can accept management (mgmt) frames with or without preamble 0 = PHY can only accept mgmt frames with preamble	R	1
5	Auto-Negotiation Complete	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed	R	0
4	Remote Fault	1 = Remote fault detected 0 = No remote fault detected	R, LH (Note 1)	0
3	Auto-Negotiation Ability	1 = PHY able to auto-negotiate, 0 = PHY not able to auto-negotiate	R	1
2	Link Status	1 = Link is up 0 = Link is down	R, LL (Note 1)	0
1	Jabber Detect	1 = Jabber condition detected 0 = No jabber condition detected	R	0
0	Extended Capability	1 = Extended register capabilities 0 = Basic register set capabilities only	R	1

Note:
1. LH = Latching High, LL = Latching Low.

TBR2 and TBR3: 10BASE-T PHY Identifier Register (Registers 2 and 3)

Registers 2 and 3 contain a unique PHY identifier, consisting of 22 bits of the organizationally unique IEEE identifier, a 6-bit manufacturer's model number, and a 4-bit manufacturer's revision number. The most significant bit of the PHY identifier is bit 15 of register 2; the least significant bit of the PHY identifier is bit 0 of register 3. Register 2, bit 15, corresponds to bit 3 of the IEEE identifier and register 2, bit 0, corresponds to bit 18 of the IEEE identifier. Register 3, bit 15, corresponds to bit 19 of the IEEE identifier and register 3, bit 10, corresponds to bit 24 of the IEEE identifier. Register 3, bits 9-4, contain the manufacturer's model number and bits 3-0 contain the manufacturer's revision number. These registers are shown in Table 43 and Table 44.

Table 43. TBR2: 10BASE-T PHY Identifier Register (Register 2)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:0	PHY_ID[31-16]	IEEE Address (bits 3-18); Register 2, bit 15 is MSB of PHY Identifier	R	0000

Table 44. TBR3: 10BASE-T PHY Identifier Register (Register 3)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:10	PHY_ID[15-10]	IEEE Address (bits 19-24)	R	1A
9:4	PHY_ID[9-4]	Manufacturer's Model Number (bits 5-0)	R	37
3:0	PHY_ID[3-0]	Revision Number (bits 3-0); Register 3, bit 0, is LSB of PHY Identifier	R	01

TBR4: 10BASE-T Auto-Negotiation Advertisement Register (Register 4)

This register contains the advertised ability of the Am79C901A home networking device. The purpose of this register is to advertise the technology ability to the link partner device. See Table 45.

When this register is modified, Restart Auto-Negotiation (Register 0, bit 9) must be enabled to guarantee the change is implemented.

Table 45. TBR4: 10BASE-T Auto-Negotiation Advertisement Register (Register 4)

Bits	Name	Description	Read/ Write	Default Value (hex)
15	Next Page	When set, the device wishes to engage in next page exchange. If cleared, the device does not wish to engage in next page exchange.	R/W	0
14	Reserved		R	0
13	Remote Fault	When set, a remote fault bit is inserted into the base link code word during the Auto-Negotiation process. When cleared, the base link code work will have the bit position for remote fault as cleared.	R/W	0
12:11	Reserved		R	0
10	PAUSE	This bit should be set if the PAUSE capability is to be advertised.	R/W	0
9	Reserved		R	0
8	Full-Duplex - 100BASE-TX	This bit advertises Full-Duplex capability. When set, Full-Duplex capability is advertised. When cleared, Full-Duplex capability is not advertised.	R	0
7	Half-Duplex - 100BASE-TX	This bit advertises Half-Duplex capability for the Auto-Negotiation process. Setting this bit advertises Half-Duplex capability. Clearing this bit does not advertise Half-Duplex capability.	R	0
6	Full-Duplex - 10BASE-T	This bit advertises Full-Duplex capability. When set, Full-Duplex capability is advertised. When cleared, Full-Duplex capability is not advertised.	R/W	1
5	Half-Duplex - 10BASE-T	This bit advertises Half-Duplex capability for the Auto-Negotiation process. Setting this bit advertises Half-Duplex capability. Clearing this bit does not advertise Half-Duplex capability.	R/W	1
4:0	Selector Field	The 10BASE-T PHY of the Am79C901A home networking device is an 802.3 compliant device.	R	01

TBR5: 10BASE-T Auto-Negotiation Link Partner Ability Register (Register 5)

The Auto-Negotiation Link Partner Ability Register is Read Only. The register contains the advertised ability of the link partner. The bit definitions represent the received link code word. This register contains either the base page or the link partner's next pages. The values contained in these registers are only valid once Auto-Negotiation has successfully completed, as indicated by bit 5 in TBR1, or if the Next Page exchange is used after the Page Received (TBR6, bit 1) has been set to logic one. See Table 46 and Table 47.

Table 46. TBR5: 10BASE-T Auto-Negotiation Link Partner Ability Register (Register 5) - Base Page Format

Bits	Name	Description	Read/ Write	Default Value (hex)
15	Next Page	Link partner next page request	R	0
14	Acknowledge	Link partner acknowledgment	R	0
13	Remote Fault	Link partner remote fault request	R	0
12:5	Technology Ability	Link partner technology ability field	R	0
4:0	Selector Field	Link partner selector field	R	0

Table 47. TBR5: 10BASE-T Auto-Negotiation Link Partner Ability Register (Register 5) - Next Page Format

Bits	Name	Description	Read/ Write	Default Value (hex)
15	Next Page	Link partner next page request	R	0
14	Acknowledge	Link partner acknowledgment	R	0
13	Message Page	Link partner message page request	R	0
12	Acknowledge 2	1 = Link partner can comply with the request 0 = Link partner cannot comply with the request	R	0
11	Toggle	Link partner toggle bit	R	0
10:0	Message Field	Link partner's message code	R	0

TBR6: 10BASE-T Auto-Negotiation Expansion Register (Register 6)

The Auto-Negotiation Expansion Register provides additional information which aids the Auto-Negotiation process. The Auto-Negotiation Expansion Register bits are Read Only. See Table 48.

Table 48. TBR6: 10BASE-T Auto-Negotiation Expansion Register (Register 6)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:5	Reserved		R	0
4	Parallel Detection Fault	1 = Parallel detection fault 0 = No parallel detection fault	R, LH	0
3	Link Partner Next Page Able	1 = Link partner is next page able 0 = Link partner is not next page able	R	0
2	Next Page Able	1 = Am79C901A device channel is next page able 0 = Am79C901A device channel is not next page able	R	1
1	Page Received	1 = A new page has been received 0 = A new page has not been received	R, LH	0
0	Link Partner ANEG Able	1 = Link partner is Auto-Negotiation able 0 = Link partner is not Auto-Negotiation able	R	0

TBR7: 10BASE-T Auto-Negotiation Next Page Register (Register 7)

The Auto-Negotiation Next Page Register contains the next page link code word to be transmitted. On power-up the default value of 2001h represents a message page with the message code set to null. See Table 49.

Table 49. TBR7: 10BASE-T Auto-Negotiation Next Page Register (Register 7)

Bits	Name	Description	Read/ Write	Default Value (hex)
15	Next Page	Am79C901A device channel next page request	R/W	0
14	Reserved		R	0
13	Message Page	Am79C901A device channel message page request	R/W	1
12	Acknowledge 2	1 = Am79C901A device channel can comply with the request 0 = Am79C901A device channel cannot comply with the request	R/W	0
11	Toggle	Am79C901A device channel toggle bit	R	0
10:0	Message Field	Message code field	R/W	001

Reserved Registers (Registers 8-15, 18, 20-23, and 25-31)

The Am79C901A device contains reserved registers at addresses 8-15, 18, 20-23, and 25-31. These registers should be ignored when read and should not be written to at any time.

TBR16: 10BASE-T Status and Enable Register (Register 16)

The status bits indicate when there is a change in the Link Status, Duplex Mode, Auto-Negotiation status, or Speed status. Register 16 contains the status and enable bits. The status is always updated whether or not the enable bits are set. When a status change occurs, the system will need to read this register to clear the status bits. See Table 50.

Table 50. TBR16: 10BASE-T Status and Enable Register (Register 16)

Bits	Name	Description	Read/ Write	Default Value (hex)
15:14	Reserved		R	0
13	Status Test Enable (Note 1)	1 = When this bit is set, setting bits 12:9 of this register will cause a condition that will set bits 4:1 accordingly. The effect is to test the register bits with a forced interrupt condition. 0 = Bits 4:1 are only set if the interrupt condition (if any bits in 12:9 are set) occurs.	R/W	0
12	Link Status Change Enable	1 = Link Status change enable 0 = This interrupt is masked	R/W	0
11	Duplex Mode Change Enable	1 = Duplex Mode change enable 0 = This interrupt is masked	R/W	0
10	Auto-Negotiation Change Enable	1 = Auto-Negotiation change enable 0 = This interrupt is masked	R/W	0
9	Speed Change Enable	1 = Speed change enable 0 = This interrupt is masked	R/W	0
8	Global Enable	1= Global interrupt enable 0 = This interrupt is masked	R/W	0
7:5	Reserved		R	0
4	Link Status Change	1 = Link Status has changed on a port 0 = No change in Link Status	R, LH	0
3	Duplex Mode Change	1 = Duplex Mode has changed on a port 0 = No change in Duplex mode	R, LH	0
2	Auto-Negotiation Change	1 = Auto-Negotiation status has changed on a port 0 = No change in Auto-Negotiation status	R, LH	0
1	Speed Change	1 = Speed status has changed on a port 0 = No change	R, LH	0
0	Global	1 = Indicates a change in status of any of the above interrupts 0 = Indicates no change in Interrupt status	R, LH	0

Note:
All bits, except bit 13, are cleared on read (COR). The register must be read twice to see if it has been cleared.

TBR17: 10BASE-T PHY Control/Status Register (Register 17)

This register is used to control the configuration of the 10 Mbps PHY of the Am79C901A home networking device. See Table 1.

Table 1. TBR17: 10BASE-T PHY Control/Status Register (Register 17)

Bits	Name	Description	Read/Write	Default Value (hex)
15:14	Reserved		R	00
13	Force Link Good Enable	1 = Link status forced to link up state 0 = Link status is determined by the device	R/W	0
12	Disable Link Pulse	1 = Link pulses sent from the 10BASE-T transmitter are suppressed 0 = Link pulse enabled (normal operation)	R/W	0
11	SQE_TEST Disable	1 = Disables the SQE heartbeat which occurs after each 10BASE-T transmission 0 = The heartbeat assertion occurs on the COL pin approximately 1 µs after transmission and for a duration of 1 µs	R/W	0
10	Reserved		R	0
9	Jabber Detect Disable	1 = Disable jabber detect 0 = Enable jabber detect	R/W	0
8:7	Reserved		R	00
6	Receive Polarity Reversed	1 = Receive polarity of the 10BASE-T receiver is reversed 0 = Receive polarity is correct	R	0
5	Auto Receive Polarity Correction Disable	1 = Polarity correction circuit is disabled for 10BASE-T 0 = Self correcting polarity circuit is enabled	R/W	0
4	Extended Distance Enable	1 = 10BASE-T receive squelch thresholds are reduced to allow reception of frames which are greater than 100 meters 0 = Squelch thresholds are set for standard distance of 100 meters	R/W	0
3	TX_DISABLE	1 = TX± outputs not active 0 = Transmit valid data	R/W	0
2	TX_CRS_EN	1 = CRS is asserted when transmit or receive medium is active 0 = CRS is asserted when receive medium is active	R/W	0
1	Reserved		R	0
0	PHY Isolated	1 = 10BASE-T PHY is isolated 0 = 10BASE-T PHY is enabled	R	1

Note: *For these loopback paths, the data is also transmitted out of the MDI pins (TX±).*

TBR19: 10BASE-T PHY Management Extension Register (Register 19)

Table 2 contains the PHY Management Extension Register (Register 19) bits.

Table 2. TBR19: 10BASE-T PHY Management Extension Register (Register 19)

Bits	Name	Description	Read/Write	Default Value (hex)
15:6	Reserved	Write as 0; ignore on read	R	0
5	Mgmt Frame Format	1 = Last management frame was invalid (opcode error, etc.) 0 = Last management frame was valid	R	0
4:0	PHY Address	PHY Address defaults to 000X1 X = Value on pin PHY_ADD (i.e., 00001 or 00011)	R	01/03

TBR24: 10BASE-T Summary Status Register (Register 24)

The Summary Status register is a global register containing status information. This register is Read Only and represents the most important data which a single register access can convey. The Summary Status register indicates the following: Link Status, Full-Duplex Status, Auto-Negotiation Alert, and Speed. See Table 3.

Table 3. TBR24: 10BASE-T Summary Status Register (Register 24)

Bits	Name	Description	Read/Write	Default Value (hex)
15:4	Reserved	Write as 0; Ignore on Read	R	0
3	Link Status	1 = Link Status is up 0 = Link Status is down	R	0
2	Full-Duplex	1 = Operating in Full-Duplex mode 0 = Operating in Half-Duplex mode	R	0
1	Auto-Negotiation Alert	1 = Auto-Negotiation status has changed 0 = Auto-Negotiation status unchanged	R	0
0	Speed	1 = Operating at 100 Mbps 0 = Operating at 10 Mbps	R	0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature (C). . . . . -65°C to +70°C

Ambient Temperature (I) . . . . . -65°C to +85°C

Supply Voltage
with respect to V_{SS} . . . . . –0.3 V to 3.63 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (TA) . . . . . .0°C to +70°C

Supply Voltages (V_{DD}) . . . . . 3.0 V to 3.6 V

All inputs within the range: . . . . . V_{SS} - 0.5 V to 5.5 V

Industrial (I) Devices

Temperature (TA) . . . . . -40°C to +85°C

Supply Voltages (V_{DD}) . . . . . 3.0 V to 3.6 V

All inputs within the range: . . . . . V_{SS} - 0.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
Digital I/O Voltage					
V_{IH}	Input HIGH Voltage		2.0		V
V_{IH5V}	Input HIGH voltage (5V)		2.0	D_{VDD} + 2.5	V
V_{IL}	Input LOW Voltage			0.8	V
V_{OL}	Output LOW Voltage	I_{OL1} = 4 mA I_{OL2} = 6 mA I_{OL3} = 12 mA		0.4	V
V_{OH}	Output HIGH Voltage (Notes 1, 2)	I_{OH1} = -4 mA I_{OH2} = -2 mA (Note 2)	2.4		V
V_{OUT}	Output Voltage on TX± (peak) (Note 8)		1.55	1.98	V
V_{DIFF}	Input Differential Squelch Assert on RX± (peak)		300	520	mV
V_{DIFF}	Input Differential De-Assert Voltage on RX± (peak)		150	300	mV
Digital I/O Current					
I_{OZ}	Output Leakage Current (Note 3)	0 V <V_{OUT} <V_{DD}	-10	10	µA
I_{IX}	Input Leakage Current (Note 4)	0 V < V_{IN} < V_{DD}	-10	10	µA
I_{IL}	Input LOW Current (Note 5)	V_{IN} = 0 V; V_{DD} = 3.6 V	-200	-10	µA
I_{IH}	Input HIGH Current (Note 5)	V_{IN} = 2.7 V; V_{DD} = 3.6 V	-50	10	µA
Power Supply Current					
I_{CC} (1 Mbps)	1 Mbps mode on TX± and RX±. Outputs driving load.	V_{DD}= Maximum Transmitting maximum packets at minimum IPG.		100	mA
I_{CC} (10 Mbps)	10BASE-T mode on TX± and RX±. Outputs driving load.	V_{DD} = Maximum Transmitting maximum packets at minimum IPG.		175	mA
I_{CC} (Static)	XCLK frequency = 0.	V_{DD} = Maximum		45	mA
I_{CC} (Idle)	Not transmitting.	V_{DD} = Maximum		75	mA
Pin Capacitance					
C_{IN}	Pin Capacitance	F_C = 1 MHz (Note 6)		10	pF
C_{CLK}	CLK Pin Capacitance	F_C = 1 MHz (Notes 6, 7)	5	12	pF
L_{PIN}	Pin Inductance	F_C = 1 MHz (Note 6)		20	nH

Notes:

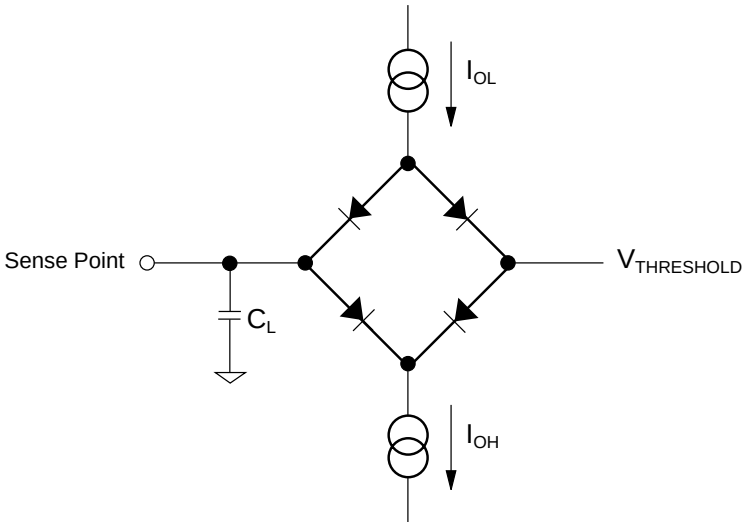
1. *V_{OH} does not apply to open-drain output pins.*
2. *I_{OH2} applies to all other outputs.*
3. *I_{OZ} applies to all output and bidirectional pins. Tests are performed at V_{IN} = 0 V and at V_{DD} only.*
4. *I_{IX} applies to all input pins except TDI, TCLK, and TMS pins.*
5. *I_{IL} and I_{IH} apply to the TDI, TCLK, and TMS pins.*
6. *Parameter not tested. Value determined by characterization.*
7. *C_{CLK} applies only to the CLK pin.*
8. *V_{OUT} reflects output levels prior to 1: √ 2 transformer state.*

SWITCHING WAVEFORMS
Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUITS



22304B-25

Figure 1. Normal and Tri-State Outputs

AC CHARACTERISTICS

GPSI

10BASE-T Transmit Timing (GPSI)

No.	Symbol	Parameter Description	Min	Max	Unit
1	t_S	TXDAT, TXEN setup time to TXCLK ↑ edge	10	–	ns
2	t_H	TXDAT, TXEN hold time from TXCLK ↑ edge	0	–	ns
3	t_{PD}	Transmit latency (TXEN sampled HIGH to 1st bit of data)	240	360	ns
4	t_{PD}	RXCRS assert from TXEN sampled HIGH	0	130	ns
5	t_{PD}	RXCRS de-assert from TXEN sampled LOW	0	130	ns
6	t_{PWL}	TXEN de-assertion time between packets (Note 1)	300	–	ns

Note: *Not tested.*

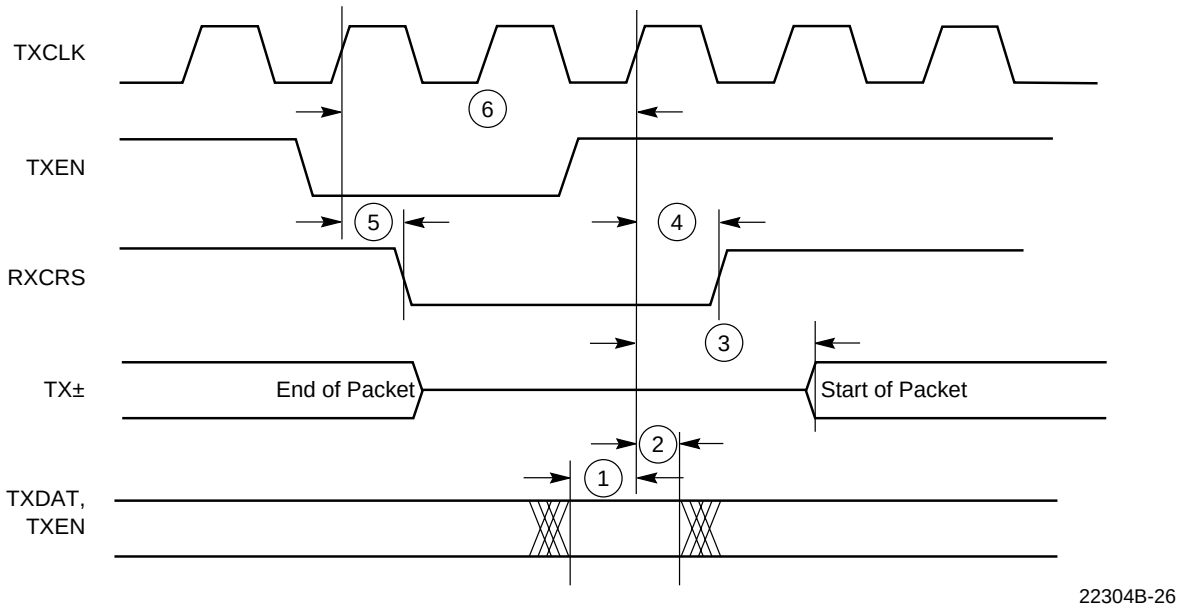
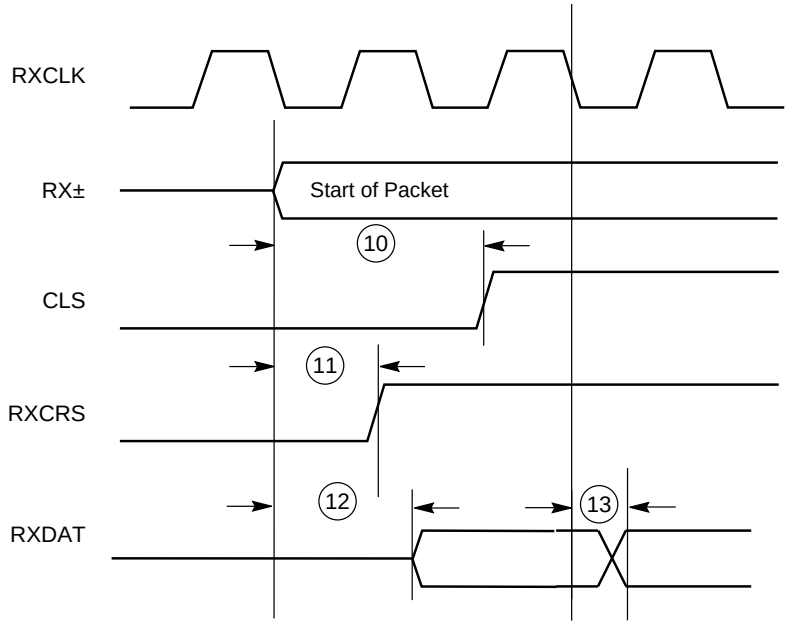


Figure 2. 10 Mbps Transmit Timing (GPSI)

AC CHARACTERISTICS (CONTINUED)

10BASE-T Receive Timing (GPSI)

No.	Symbol	Parameter Description	Min	Max	Unit
10	t_{PD}	CLS assert latency from SOP	200	300	ns
11	t_{PD}	RXCRS assert latency from SOP	200	300	ns
12	t_{PD}	Receive latency (SOP to RXDAT valid)	320	430	ns
13	t_{PD}	RXCLK ↓ edge to RXDAT transition	–	10	ns
14	t_{PD}	CLS de-assert latency from EOP	125	250	ns
15	t_{PD}	RXCRS de-assert latency from EOP	165	255	ns



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Figure 3. 10 Mbps Receive Start of Packet Timing (GPSI)

AC CHARACTERISTICS (CONTINUED)

10BASE-T Receive Timing (GPSI) (Continued)

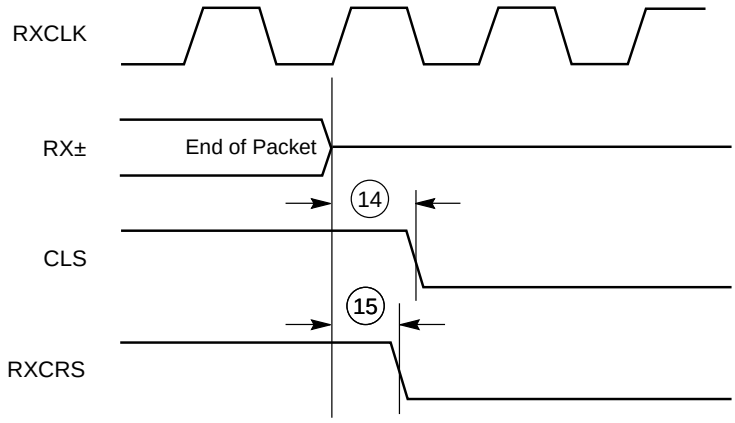


Figure 4. 10 Mbps Receive End of Packet Timing (GPSI)

10BASE-T Transmit Clock Timing (GPSI)

No.	Symbol	Parameter Description	Min	Max	Unit
18	t_{PER}	TXCLK period	99.99	100.01	ns
19	t_{PWH}	TXCLK pulse width HIGH	45	55	ns
20	t_{PWL}	TXCLK pulse width LOW	45	55	ns

10BASE-T Receive Clock Timing (GPSI)

No.	Symbol	Parameter Description	Min	Max	Unit
18	t_{PER}	RXCLK period	99.99	100.01	ns
19	t_{PWH}	RXCLK pulse width HIGH	45	55	ns
20	t_{PWL}	RXCLK pulse width LOW	45	55	ns

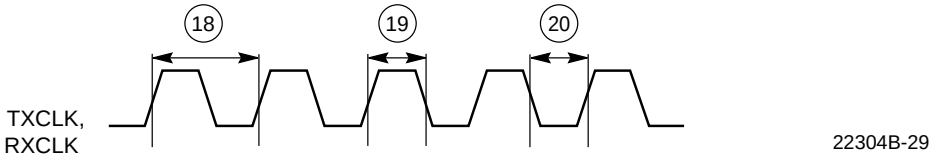


Figure 5. 10 Mbps Transmit and Receive Clock Timing (GPSI)

AC CHARACTERISTICS (CONTINUED)

1 Mbps HomePNA Transmit Timing (GPSI)

No.	Symbol	Parameter Description	Min	Max	Unit
23	t_S	TXDAT setup time to TXCLK ↑	12	–	ns
24	t_S	TXEN setup time to TXCLK ↓	10	–	ns
25	t_H	TXDAT hold time from TXCLK ↑	10	–	ns
26	t_H	TXEN hold time from TXCLK ↓	10	–	ns
27	t_{PD}	Transmit Latency (TXEN sampled HIGH to SYNC pulse (5 mV))	200	500	ns
28	t_{PD}	TXEN sampled HIGH to CLS active (Note 1)	–	120	µs

Note: *Not tested.*

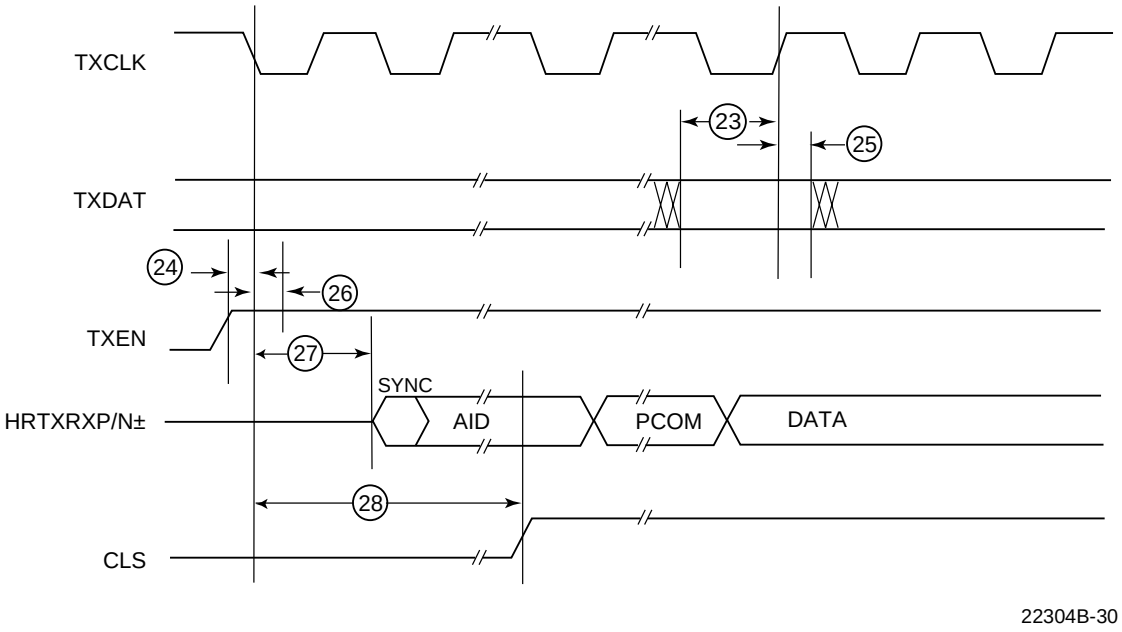


Figure 6. 1 Mbps HomePNA Transmit Timing (GPSI)

AC CHARACTERISTICS (CONTINUED)

1 Mbps HomePNA Receive Timing (GPSI)

No.	Symbol	Parameter Description	Min	Max	Unit
29	t_{PD}	RXCLK ↓ edge to RXDAT transition (Note 1)	0	10	ns
30	t_{PD}	SYNC pulse detected to RXCRS clocked as active by MAC (Note 1)	650	850	ns
31	t_{PD}	Last DATA pulse crosses noise slice level to RXCRS inactive (Note 1)	15.98	16.10	µs
32	t_{PD}	RXCRS inactive to CLS inactive clocked into MAC (Note 1)	–	200	ns

Note: *Not tested.*

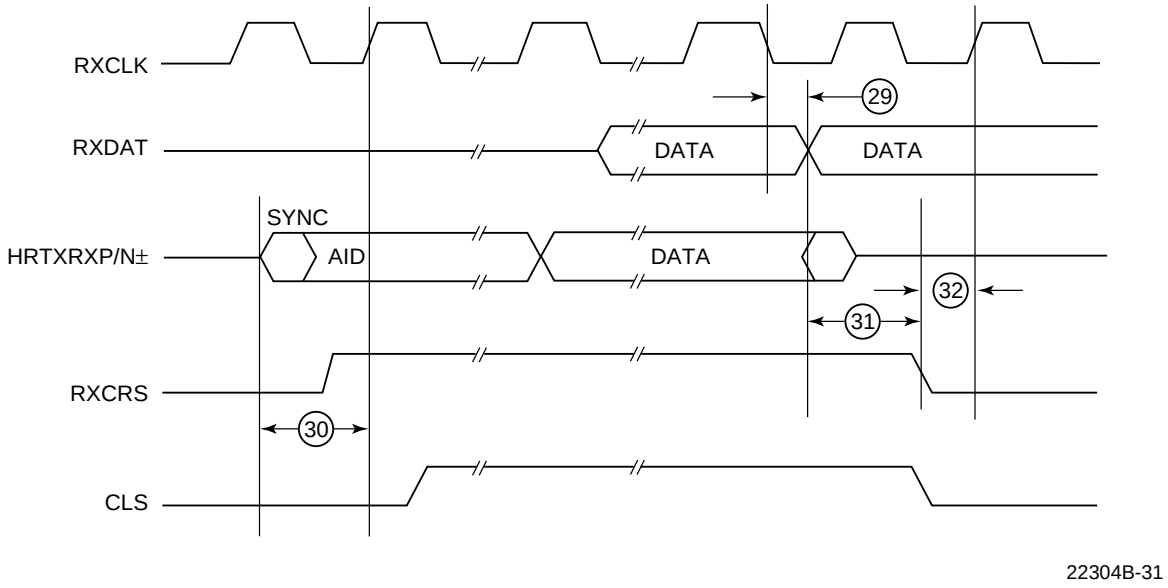


Figure 7. 1 Mbps HomePNA Receive Timing (GPSI)

AC CHARACTERISTICS (CONTINUED)

1 Mbps HomePNA Clock Timing (GPSI)

No.	Symbol	Parameter Description	Clock Period	Unit
Idle (excluding IPG time)				
35	t_{PER}	TXCLK, RXCLK period	583.3	ns
36	t_{PWH}	TXCLK, RXCLK pulse width HIGH	115.5	ns
37	t_{PWL}	TXCLK, RXCLK pulse width LOW	467.8	ns
Preamble (first 64 bits of TX MAC frame)				
35	t_{PER}	TXCLK, RXCLK period	233.3	ns
36	t_{PWH}	TXCLK, RXCLK pulse width HIGH	115.5	ns
37	t_{PWL}	TXCLK, RXCLK pulse width LOW	117.8	ns
Data (thoughtout the data phase)				
35	t_{PER}	TXCLK, RXCLK period	233.3 ns - 10 µs	
36	t_{PWH}	TXCLK, RXCLK pulse width HIGH	115.5	ns
37	t_{PWL}	TXCLK, RXCLK pulse width LOW	117.8 ns - 10 µs	
IPG (96 bit times following CRS falling edge)				
35	t_{PER}	TXCLK, RXCLK period	233.3	ns
36	t_{PWH}	TXCLK, RXCLK pulse width HIGH	115.5	ns
37	t_{PWL}	TXCLK, RXCLK pulse width LOW	117.8	ns

Note: *During AID interval, RXCLK and TXCLK stop for up to 140 µs.*

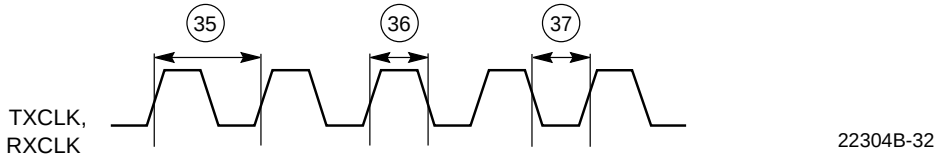


Figure 8. 1 Mbps HomePNA Clock Timing (GPSI)

AC CHARACTERISTICS (CONTINUED)

MII

10BASE-T Transmit Timing (MII)

No.	Symbol	Parameter Description	Min	Max	Unit
40	t_S	TXD, TX_EN setup time to TXCLK ↑ edge	10	–	ns
41	t_H	TXD, TX_EN hold time from TXCLK ↑ edge	0	–	ns
42	t_{PD}	Transmit latency (TX_EN sampled HIGH to 1st bit of data)	240	360	ns
43	t_{PD}	CRS assert from TX_EN sampled HIGH	0	430	ns
44	t_{PD}	CRS de-assert from TX_EN sampled LOW	0	430	ns
45	t_{PWL}	TX_EN de-assertion time between packets (Note 1)	1200	–	ns

Note: *Not tested*

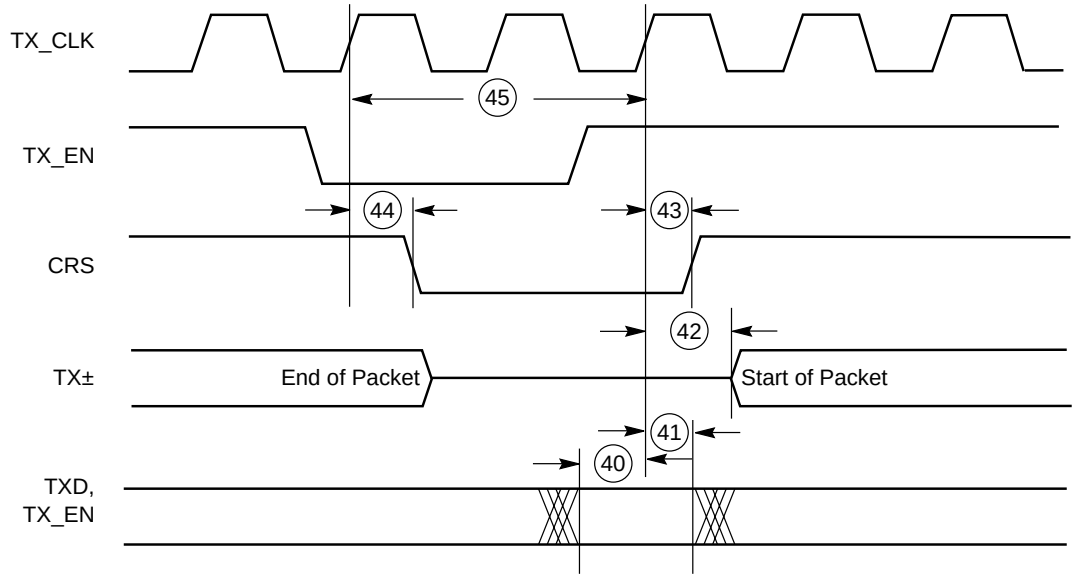


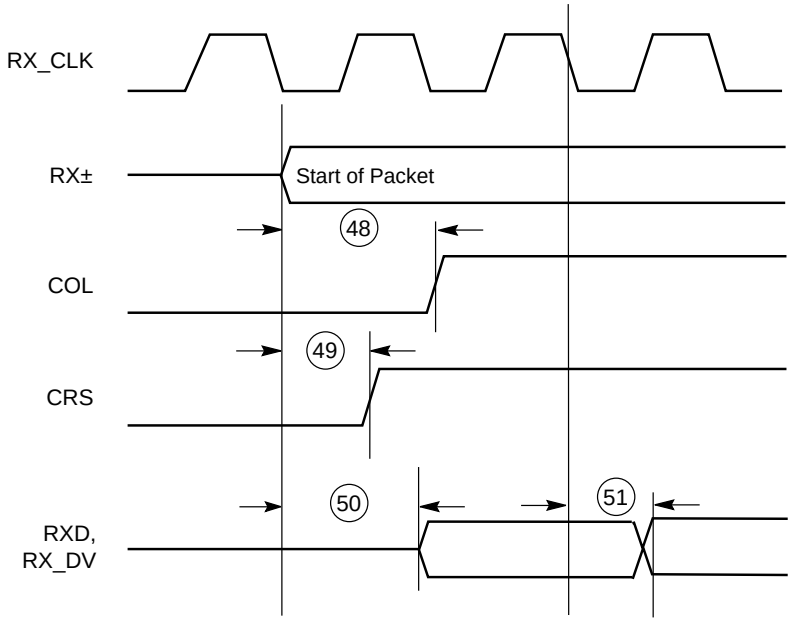
Figure 9. 10 Mbps Transmit Timing (MII)

AC CHARACTERISTICS (CONTINUED)

10BASE-T Receive Timing (MII)

No.	Symbol	Parameter Description	Min	Max	Unit
48	t_{PD}	COL assert latency from SOP	200	300	ns
49	t_{PD}	CRS assert latency from SOP	200	300	ns
50	t_{PD}	Receive latency (SOP to RXD, RX_DV valid) (Note 1)	625	1275	ns
51	t_{PD}	RX_CLK ↓ edge to RXD, RX_DV transition	–	10	ns
52	t_{PD}	RX_DV de-assert latency EOP	500	900	ns
53	t_{PD}	COL de-assert latency from EOP	100	700	ns
54	t_{PD}	CRS de-assert latency from EOP	500	900	ns

Note: *RXD not tested.*



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Figure 10. 10 Mbps Receive Start of Packet Timing (MII)

AC CHARACTERISTICS (CONTINUED)

10BASE-T Receive Timing (MII) (Continued)

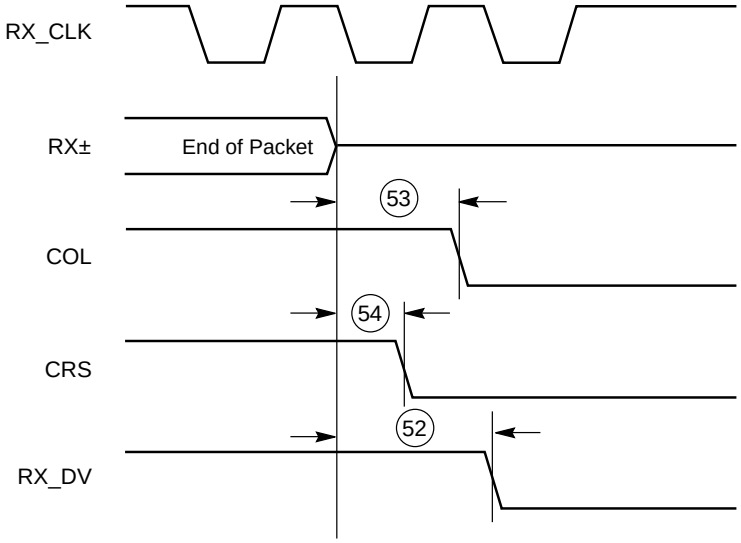


Figure 11. 10 Mbps Receive End of Packet Timing (MII)

AC CHARACTERISTICS (CONTINUED)

10BASE-T Transmit Clock Timing (MII)

No.	Symbol	Parameter Description	Min	Max	Unit
57	t_{PER}	TX_CLK period	399.6	400.4	ns
58	t_{PWH}	TX_CLK pulse width HIGH	180	220	ns
59	t_{PWL}	TX_CLK pulse width LOW	180	220	ns

10BASE-T Receive Clock Timing (MII)

No.	Symbol	Parameter Description	Min	Max	Unit
57	t_{PER}	RX_CLK period	399.6	400.4	ns
58	t_{PWH}	RX_CLK pulse width HIGH	180	220	ns
59	t_{PWL}	RX_CLK pulse width LOW	180	220	ns

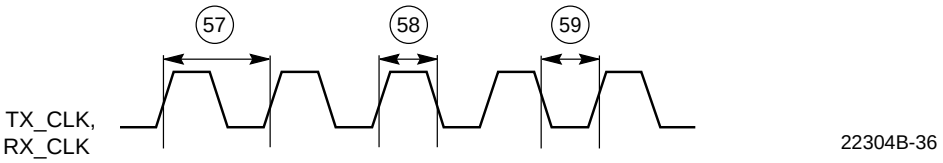


Figure 12. 10 Mbps Transmit and Receive Clock Timing (MII)

AC CHARACTERISTICS (CONTINUED)

1 Mbps HomePNA Transmit Timing (MII)

No.	Symbol	Parameter Description	Min	Max	Unit
62	t_S	TXD, TX_EN setup time to TX_CLK ↑ edge	10	–	ns
63	t_H	TXD, TX_EN hold time from TX_CLK ↑ edge	10	–	ns
64	t_{PD}	Transmit Latency (TX_EN sampled HIGH to SYNC pulse (5 mV))	200	500	ns
65	t_{PD}	TX_EN sampled HIGH to COL active (Note 1)	–	120	µs

Note: *Not tested.*

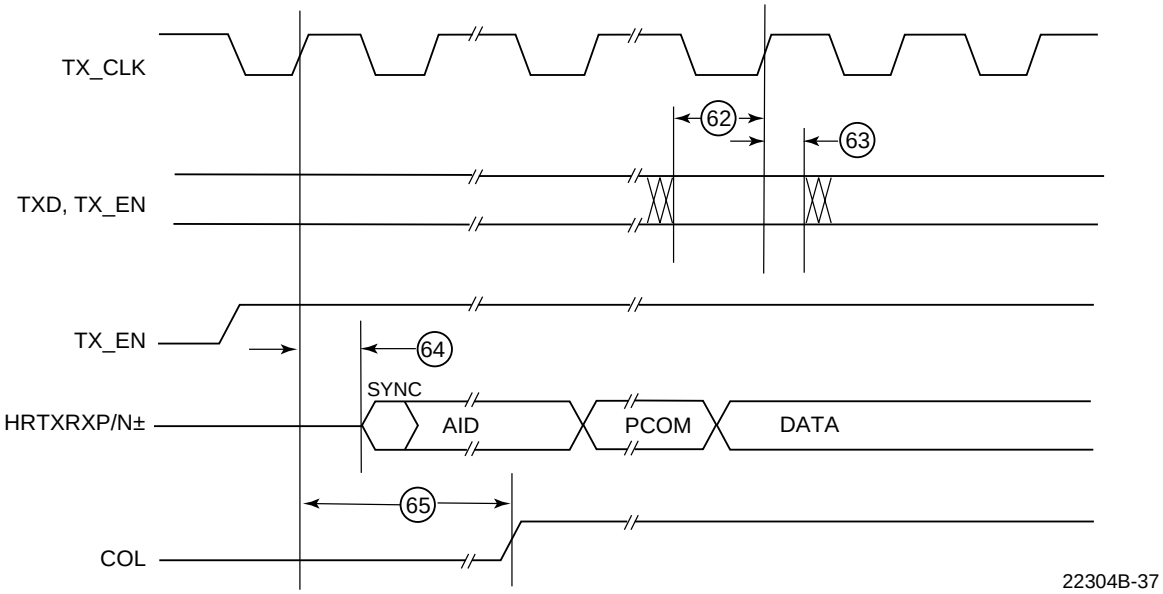


Figure 13. 1 Mbps HomePNA Transmit Timing (MII)

AC CHARACTERISTICS (CONTINUED)

1 Mbps HomePNA Receive Timing (MII)

No.	Symbol	Parameter Description	Min	Max	Unit
68	t_{PD}	RX_CLK ↓ edge to RXD, RX_DV transitions (Note 1)	0	10	ns
69	t_{PD}	SYNC pulse detected to CRS clocked as active by MAC (Note 1)	650	850	ns
70	t_{PD}	Last DATA pulse crosses data slice level to CRS inactive (Note 1)	15.98	16.10	µs
71	t_{PD}	CRS inactive to COL inactive clocked into MAC (Note 1)	–	200	ns

Note: *Not tested.*

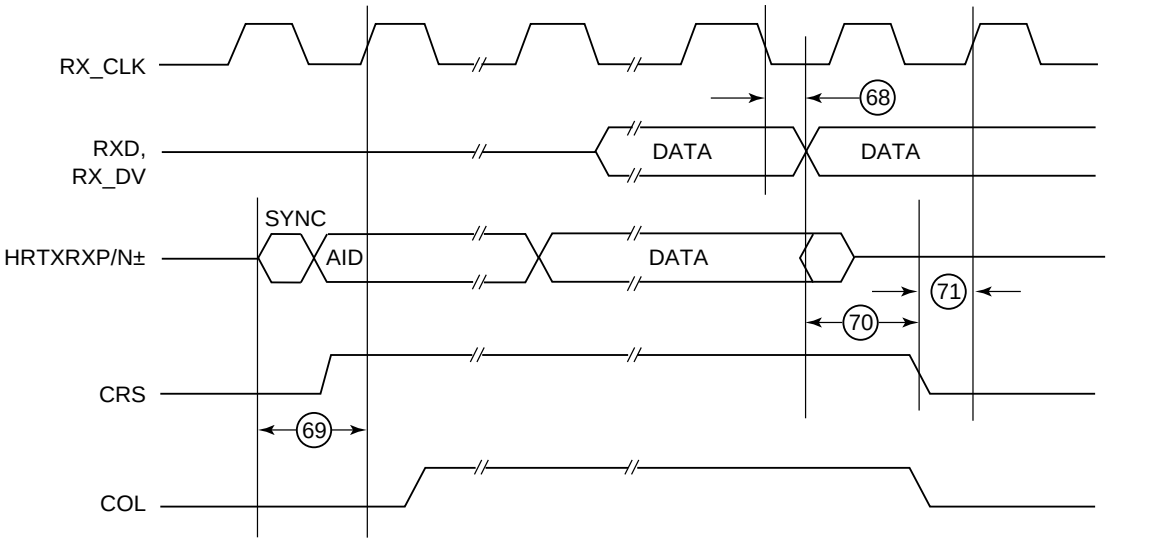


Figure 14. 1 Mbps HomePNA Receive Timing (MII)

AC CHARACTERISTICS (CONTINUED)

1 Mbps HomePNA Clock Timing (MII)

No.	Symbol	Parameter Description	Clock Period	Unit
Idle (excluding IPG time)				
74	t_{PER}	TX_CLK, RX_CLK period	2333.34	ns
75	t_{PWH}	TX_CLK, RX_CLK pulse width HIGH	1165	ns
76	t_{PWL}	TX_CLK, RX_CLK pulse width LOW	1168	ns
Preamble (first 64 bits of TX MAC frame)				
74	t_{PER}	TX_CLK, RX_CLK period	933.33	ns
75	t_{PWH}	TX_CLK, RX_CLK pulse width HIGH	466	ns
76	t_{PWL}	TX_CLK, RX_CLK pulse width LOW	467	ns
Data (throughout the data phase)				
74	t_{PER}	TX_CLK, RX_CLK period	933 ns - 40 µs	
75	t_{PWH}	TX_CLK, RX_CLK pulse width HIGH	466 ns - 40 µs	
76	t_{PWL}	TX_CLK, RX_CLK pulse width LOW	467 ns - 40 µs	
IPG (96 bit times following CRS falling edge)				
74	t_{PER}	TX_CLK, RX_CLK period	933.33	ns
75	t_{PWH}	TX_CLK, RX_CLK pulse width HIGH	466	ns
76	t_{PWL}	TX_CLK, RX_CLK pulse width LOW	467	ns

Note: *During AID interval, RX_CLK and TX_CLK stop for up to 140 µs.*

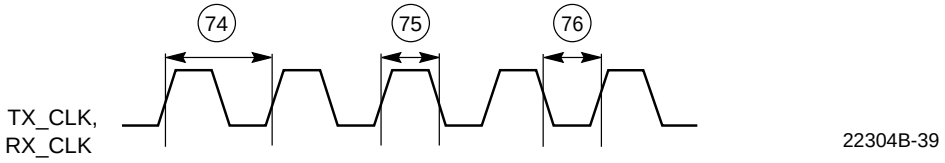


Figure 15. 1 Mbps HomePNA Clock Timing (MII)

AC CHARACTERISTICS (CONTINUED)

MDC/MDIO

No.	Symbol	Parameter Description	Min	Max	Unit
79	t_{PER}	MDC period	400	–	ns
80	t_{PWH}	MDC pulse width HIGH	160	–	ns
81	t_{PWL}	MDC pulse width LOW	160	–	ns
82	t_{PD}	MDIO output delay from MDC ↑ edge	0	300	ns
83	t_S	MDIO input setup time to MDC ↑ edge	8	–	ns
84	t_H	MDIO input hold time from MDC ↑ edge	8	–	ns
85	t_Z	MDC to high impedance	5	40	ns

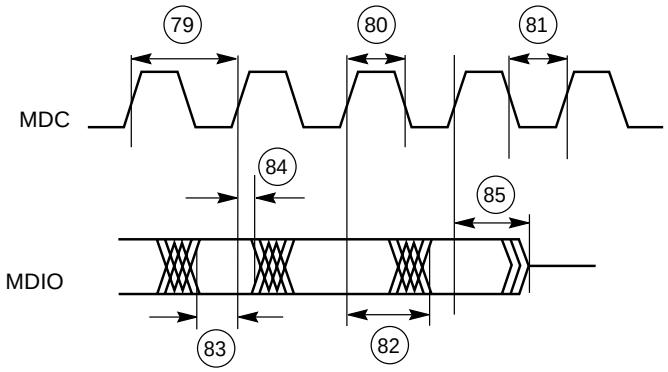
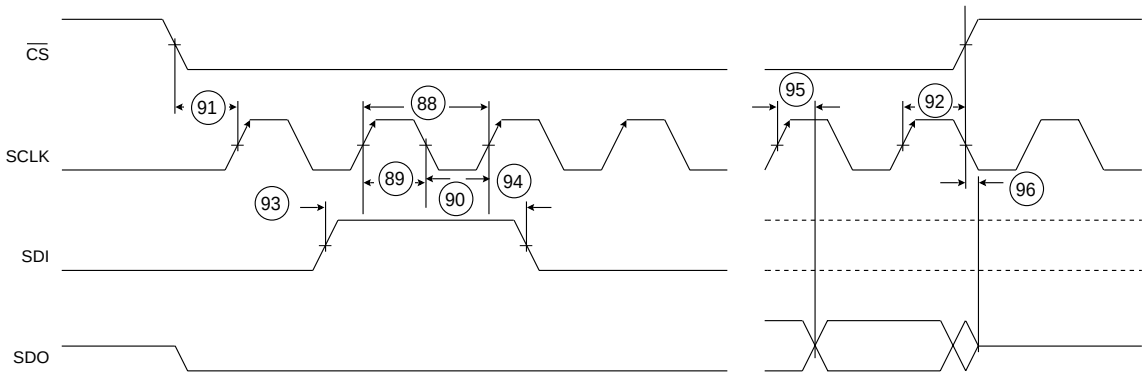


Figure 16. MII Management Timing

AC CHARACTERISTICS (CONTINUED)

SPI

No.	Parameter Symbol	Parameter Name	Min	Max	Unit
88	t_{PW}	SCLK period	400	–	ns
89	t_{PWH}	SCLK Min pulse HIGH	160	–	ns
90	t_{PWL}	SCLK Min pulse LOW	160	–	ns
91	t_S	$\overline{CS}$ ↓ setup to SCLK ↑	8	–	ns
92	t_H	$\overline{CS}$ ↑ hold to SCLK ↑	25	–	ns
93	t_S	SDI setup to SCLK ↑	8	–	ns
94	t_H	SDI hold to SCLK ↑	0	–	ns
95	t_{PD}	SCLK ↑ to DO valid	0	25	ns
96	t_{PZD}	$\overline{CS}$ ↑ to DO Hi Z	–	50	ns



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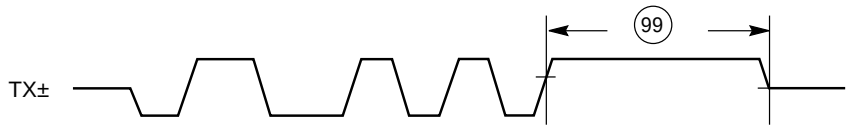
Figure 17. SPI Timing

AC CHARACTERISTICS (CONTINUED)

10BASE-T PMD

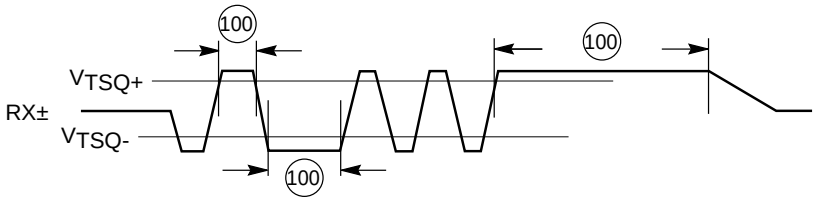
No.	Symbol	Parameter Description	Test Conditions	Min	Max	Unit
99	t_{TETD}	Transmit End of Transmit Data		250	375	ns
100	t_{PWKRD}	RX± Pulse Width Maintain/Turn Off Threshold	$\|V_{IN}\| > \|V_{THS}\|$ (Note 1)	136	200	ns

Note: *RX± pulses narrower than t_{PWDRD} (min) will maintain internal Carrier Sense on. RX± pulses wider than t_{PWKRD} (max) will turn internal Carrier Sense off.*



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Figure 18. 10 Mbps Transmit (TX±) Timing Diagram



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Figure 19. 10 Mbps Receive (RX±) Timing Diagram

AC CHARACTERISTICS (CONTINUED)

1 Mbps HomePNA Analog

No.	Parameter Symbol	Parameter Name	Conditions	Typical	Units
103	t_{PW}	Pulse Width		133	ns
104	t_{PWH}	Pulse Width HIGH		67	ns
105	t_{PWL}	Pulse Width LOW		67	ns
106	t_{VMAXp}	Maximum Voltage (positive)	Low Power High Power	1.00 2.00	V
107	t_{VMAXn}	Maximum Voltage (negative)	Low Power High Power	1.00 2.00	V

Notes:

1. *All registers at default values and V_{CC} = 3.3 V, 25°C.*
2. *Measurements across HRTXTXP and HRTXTXN, differentially measured, with a 50 Ω resistive load.*

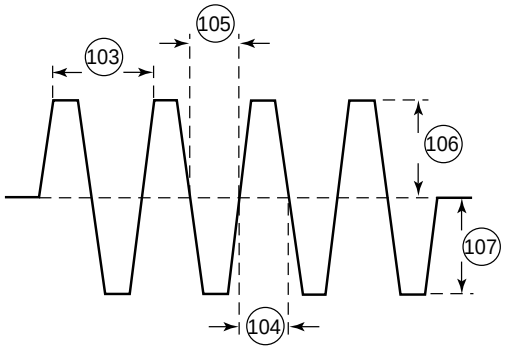


Figure 20. HomePNA PHY AC Waveform

AC CHARACTERISTICS (CONTINUED)

JTAG

No.	Parameter Symbol	Parameter Name	Min	Max	Unit
110	t_{PER}	TCK Period	100	–	ns
111	t_{PWH}	TCK HIGH Time	45	–	ns
112	t_{PWL}	TCK LOW Time	45	–	ns
113	t_S	TDI, TMS Setup Time	8	–	ns
114	t_H	TDI, TMS Hold Time	10	–	ns
115	t_{PD}	TDO Valid Delay	3	30	ns
116	t_{PD}	TDO Float Delay	–	50	ns

Note: *1. Not tested; parameter guaranteed by design characterization.*

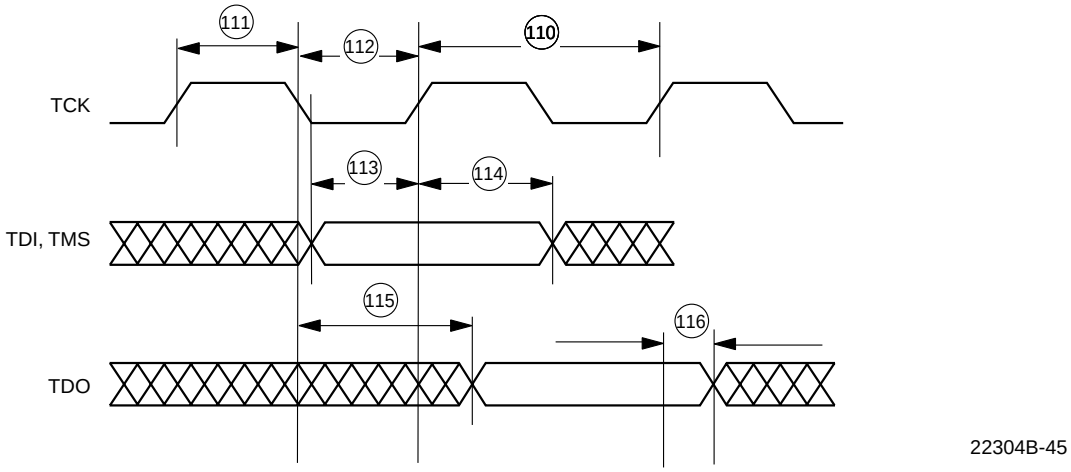
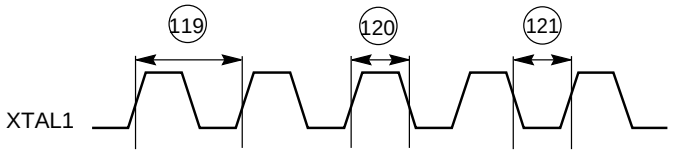


Figure 21. JTAG (IEEE 1149.1) Test Signal Timing

AC CHARACTERISTICS (CONCLUDED)

External Clock (XTAL1)

No.	Symbol	Parameter Description	Min	Max	Unit
119	t_{PER}	Cycle time	16.665	16.669	ns
120	t_{PWH}	Cycle HIGH time	0.4 x T_{CYCLE}	0.6 x T_{CYCLE}	ns
121	t_{PWL}	Cycle LOW time	0.4 x T_{CYCLE}	0.6 x T_{CYCLE}	ns



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Figure 22. External Clock Timing

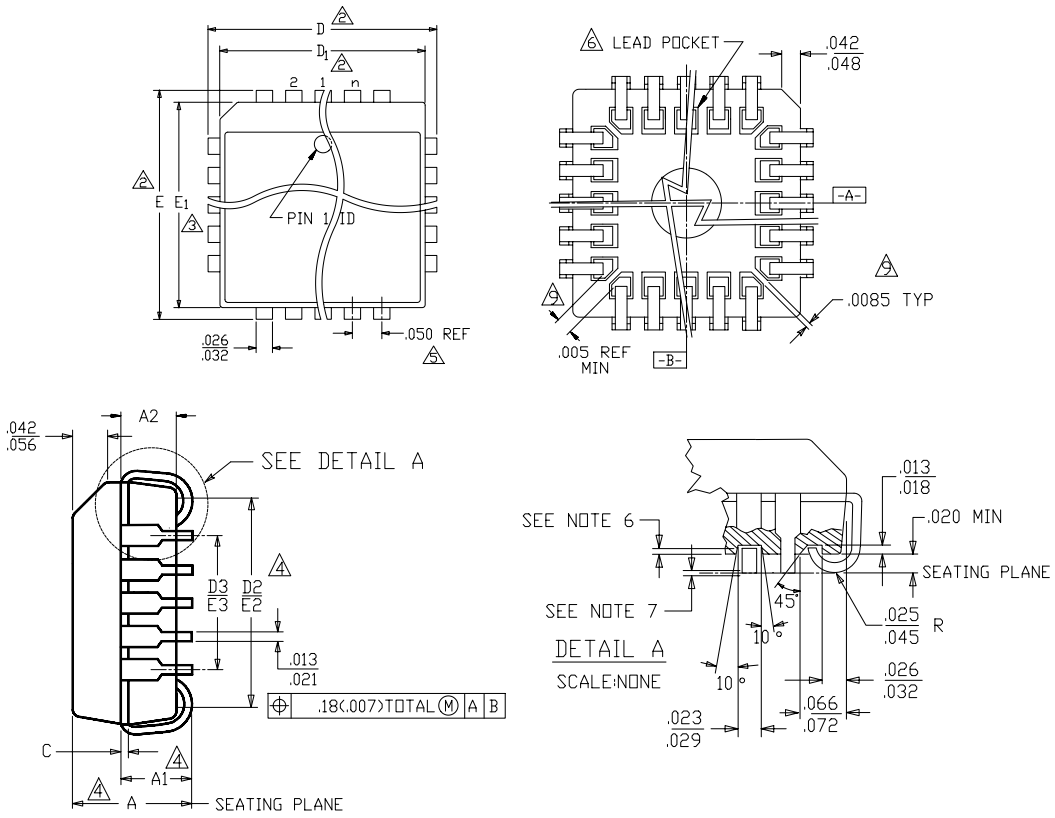
Reset

Symbol	Parameter Description	Min	Max	Unit
t_{PW}	RESET ↓ to RESET ↑	5000	–	ns

PHYSICAL DIMENSIONS*

PL 068

Plastic Leaded Chip Carrier (measured in inches)



PACKAGE	PL68	
JEDEC	MO-047(B)AE	
SYMBOL	MIN	MAX
A	.165	.180
A1	.090	.130
A2	.062	.083
D	.985	.995
D1	.950	.956
D2	.890	.930
D3	.800	REF
E	.985	.995
E1	.950	.956
E2	.890	.930
E3	.800	REF
C	.007	.013

NOTES: (UNLESS OTHERWISE SPECIFIED)

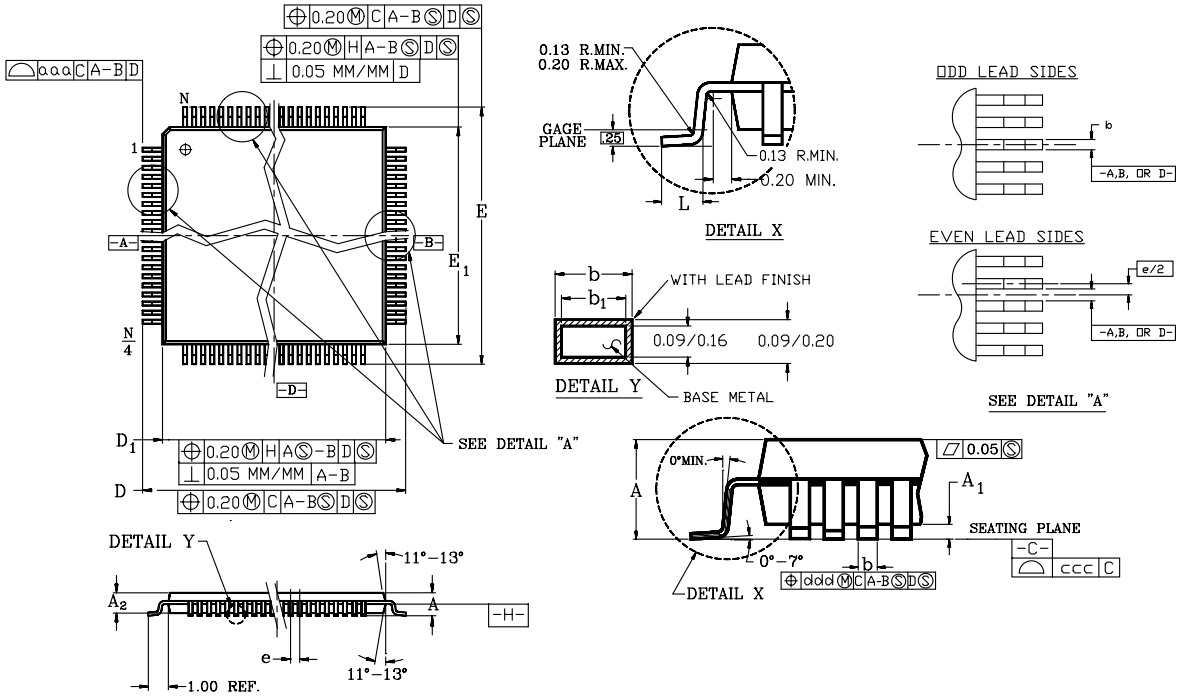
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010 INCH
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005 INCH.
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004 INCH AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045 INCH ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

PQT 80

Thin Plastic Quad Flat Pack (measured in millimeters)



PACKAGE	PQT 80		
JEDEC	MO-136 (B) AM		
SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	14.00 BSC		
D1	12.00 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
N	80		
e	0.50 BASIC		
b	0.17	0.22	0.27
b1	0.16	0.20	0.23
ccc	—	—	0.08
ddd	—	—	0.08
aaa	—	—	0.20

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD–TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06–500) 1– 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65–0.80 COPLANARITY IS MEASURED PER SPECIFICATION 06–500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165 mm.
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–136, MS–026.

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

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