Am42BDS640AG

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **26445** Revision **B** Amendment **0** Issue Date **November I, 2002**

PRELIMINARY

Am42BDS640AG

Stacked Multi-Chip Package (MCP) Flash Memory and SRAM

Am29BDS640G 64 Megabit (4 M x 16-Bit) CMOS 1.8 Volt-only, Simultaneous Operation, Burst Mode Flash Memory and 16 Mbit (1 M x 16-Bit) Static RAM

DISTINCTIVE CHARACTERISTICS

MCP Features

- **Power supply voltage of 1.65 to 1.95 volt**
- **High performance**
  - Access time as fast as 70 ns
- **Package**
  - 93-Ball FBGA
- **Operating Temperature**
  - –40°C to +85°C

Flash Memory Features

ARCHITECTURAL ADVANTAGES

- **Single 1.8 volt read, program and erase (1.65 to 1.95 volt)**
- **Manufactured on 0.17 µm process technology**
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
  - Four bank architecture: 16Mb/16Mb/16Mb/16Mb
- **Programmable Burst Interface**
  - 2 Modes of Burst Read Operation
  - Linear Burst: 8, 16, and 32 words with wrap-around
  - Continuous Sequential Burst
- **Sector Architecture**
  - Eight 8 Kword sectors and one hundred twenty-six 32 Kword sectors
  - Banks A and D each contain four 8 Kword sectors and thirty-one 32 Kword sectors; Banks B and C each contain thirty-two 32 Kword sectors
  - Eight 8 Kword boot sectors, four at the top of the address range, and four at the bottom of the address range
- **Minimum 1 million erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARCTERISTICS

- **Read access times at 54/40 MHz**
  - Burst access times of 13.5/20 ns @ 30 pF at industrial temperature range
  - Asynchronous random access times of 70 ns (at 30 pF)
  - Synchronous latency of 87.5/95 ns
- **Power dissipation (typical values, C_L = 30 pF)**
  - Burst Mode Read: 10 mA
  - Simultaneous Operation: 25 mA
  - Program/Erase: 15 mA
  - Standby mode: 0.2 µA

HARDWARE FEATURES

- **Software command sector locking**
- **Handshaking: host monitors operations via RDY output**
- **Hardware reset input (RESET#)**
- **WP# input**
  - Write protect (WP#) function protects sectors 0, 1 (bottom boot) or sectors 132 and 133 (top boot), regardless of sector protect status
- **ACC input: Acceleration function reduces programming time; all sectors locked when ACC = V_{IL}**
- **CMOS compatible inputs, CMOS compatible outputs**
- **Low V_{CC} write inhibit**

SOFTWARE FEATURES

- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
- **Data# Polling and toggle bits**
- **Erase Suspend/Resume**
  - Suspends or resumes an erase operation in one sector to read data from, or program data to, other sectors
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

SRAM Features

- **Power dissipation**
  - Operating: 3 mA maximum
  - Standby: 15 µA maximum
- **CE1s# and CE2s Chip Select**
- **Power down features using CE1s# and CE2s**
- **Data retention supply voltage: 1.0 to 2.2 volt**
- **Byte data control: LB#s (DQ7–DQ0), UB#s (DQ15–DQ8)**

This document contains information on a product under development at Advanced Micro Devices. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication# **26445** Rev: **B** Amendment/**0**
Issue Date: **November 1, 2002**

GENERAL DESCRIPTION

The Am29BDS640G is a 64 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory device, organized as 4,194,304 words of 16 bits each. This device uses a single V_{CC} of 1.65 to 1.95 V to read, program, and erase the memory array. A 12.0-volt V_{ID} may be used for faster program performance if desired. The device can also be programmed in standard EPROM programmers.

At 54 MHz, the device provides a burst access of 13.5 ns at 30 pF with a latency of 87.5 ns at 30 pF. At 40 MHz, the device provides a burst access of 20 ns at 30 pF with a latency of 95 ns at 30 pF. The device operates within the industrial temperature range of -40°C to +85°C. The device is offered in a 93-ball FBGA package.

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is divided as shown in the following table:

Bank	Quantity	Size
A	4	8 Kwords
	31	32 Kwords
B	32	32 Kwords
C	32	32 Kwords
D	31	32 Kwords
	4	8 Kwords

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The burst read mode feature gives system designers flexibility in the interface to the device. The user can preset the burst length and wrap through the same memory space, or read the flash array in continuous mode.

The clock polarity feature provides system designers a choice of active clock edges, either rising or falling. The active clock edge initiates burst accesses and determines when data will be output.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a program or erase operation is complete by using the device status bit DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. The **sector lock/unlock command sequence** disables or re-enables both program and erase operations in any sector. When at V_{IL}, **WP#** locks sectors 0 and 1 (bottom boot device) or sectors 132 and 133 (top boot device).

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

TABLE OF CONTENTS

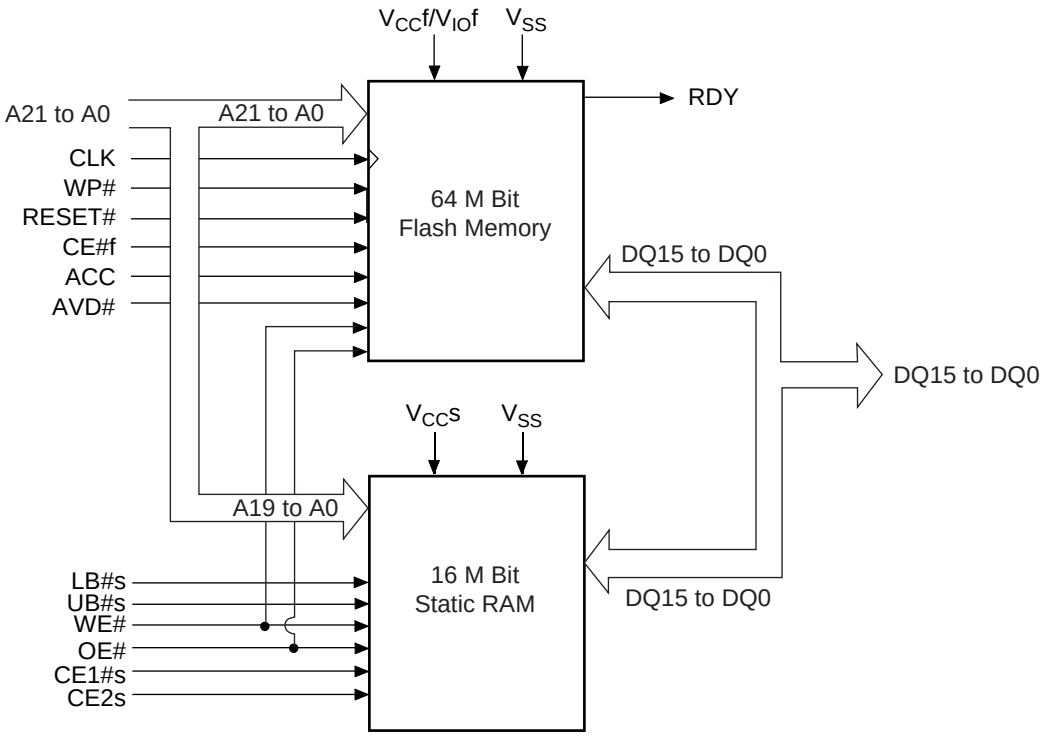
Product Selector Guide 5
MCP Block Diagram 5
Flash Memory Block Diagram 6
Flash Memory Simultaneous Operation Diagram 7
Connection Diagram 8
Special Package Handling Instructions 8
Pin Description 9
Logic Symbol 9
Ordering Information 10
MCP Device Bus Operations 11
Table 1. Device Bus Operations 12
Flash Device Bus Operations 13
Requirements for Asynchronous Read Operation (Non-Burst) 13
Requirements for Synchronous (Burst) Read Operation 13
8-, 16-, and 32-Word Linear Burst with Wrap Around 13
Table 2. Burst Address Groups 13
Burst Mode Configuration Register 14
Reduced Wait-State Handshaking Option 14
Simultaneous Read/Write Operations with Zero Latency 14
Writing Commands/Command Sequences 14
Accelerated Program Operation 14
Autoselect Functions 15
Standby Mode 15
Automatic Sleep Mode 15
RESET#: Hardware Reset Input 15
Output Disable Mode 15
Hardware Data Protection 15
Write Protect (WP#) 16
Low V_{CC} Write Inhibit 16
Write Pulse “Glitch” Protection 16
Logical Inhibit 16
Power-Up Write Inhibit 16
Common Flash Memory Interface (CFI) 16
Table 3. CFI Query Identification String 16
System Interface String 17
Table 5. Device Geometry Definition 17
Table 6. Primary Vendor-Specific Extended Query 18
Table 7. Sector Address Table 19
Flash Command Definitions 23
Reading Array Data 23
Set Burst Mode Configuration Register Command Sequence 23
Figure 1. Synchronous/Asynchronous State Diagram 23
Read Mode Setting 23
Programmable Wait State Configuration 23
Table 8. Programmable Wait State Settings 24
Handshaking Option 24
Table 9. Initial Access Codes 24
Standard Handshaking Operation 24
Table 10. Wait States for Standard Handshaking 24
Burst Read Mode Configuration 24
Table 11. Burst Read Mode Settings 25
Burst Active Clock Edge Configuration 25
RDY Configuration 25
Configuration Register 25
Table 12. Burst Mode Configuration Register 25
Sector Lock/Unlock Command Sequence 25
Reset Command 25
Autoselect Command Sequence 26
Table 13. Device IDs 26
Program Command Sequence 26
Unlock Bypass Command Sequence 27
Figure 2. Erase Operation 27
Chip Erase Command Sequence 27
Sector Erase Command Sequence 28
Erase Suspend/Erase Resume Commands 28
Figure 3. Program Operation 29
Command Definitions 30
Table 14. Command Definitions 30
Flash Write Operation Status 31
DQ7: Data# Polling 31
Figure 4. Data# Polling Algorithm 31
RDY: Ready 32
DQ6: Toggle Bit I 32
Figure 5. Toggle Bit Algorithm 32
DQ2: Toggle Bit II 32
Table 15. DQ6 and DQ2 Indications 33
Reading Toggle Bits DQ6/DQ2 33
DQ5: Exceeded Timing Limits 33
DQ3: Sector Erase Timer 34
Table 16. Write Operation Status 34
Absolute Maximum Ratings 35
Figure 6. Maximum Negative Overshoot Waveform 35
Figure 7. Maximum Positive Overshoot Waveform 35
Operating Ranges 35
Flash DC Characteristics 36
SRAM DC and Operating Characteristics 37
Test Conditions 38
Figure 8. Test Setup 38
Table 17. Test Specifications 38
Key to Switching Waveforms 38
Figure 9. Input Waveforms and Measurement Levels 38
AC Characteristics 39
SRAM CE#s Timing 39
Figure 10. Timing Diagram for Alternating Between SRAM and Flash 39
Synchronous/Burst Read 40
Figure 11. CLK Synchronous Burst Mode Read (rising active CLK) 41
Figure 12. CLK Synchronous Burst Mode Read (Falling Active Clock) 42
Figure 13. Synchronous Burst Mode Read 43
Figure 14. 8-word Linear Burst with Wrap Around 43
Figure 15. Burst with RDY Set One Cycle Before Data 44
Figure 16. Reduced Wait-State Handshaking Burst Mode Read Starting at an Even Address 45
Figure 17. Reduced Wait-State Handshaking Burst Mode Read Starting at an Odd Address 46
Asynchronous Read 47
Figure 18. Asynchronous Mode Read with Latched Addresses 47
Figure 19. Asynchronous Mode Read 48
Figure 20. Reset Timings 49
Erase/Program Operations 50
Figure 21. Asynchronous Program Operation Timings 51
Figure 22. Alternate Asynchronous Program Operation Timings 52
Figure 23. Synchronous Program Operation Timings 53

Figure 24. Alternate Synchronous Program Operation Timings 54
Figure 25. Chip/Sector Erase Command Sequence 55
Figure 26. Accelerated Unlock Bypass Programming Timing 56
Figure 27. Data# Polling Timings (During Embedded Algorithm) ... 57
Figure 28. Toggle Bit Timings (During Embedded Algorithm) 57
Figure 29. Synchronous Data Polling Timings/Toggle Bit Timings . 58
Figure 30. Latency with Boundary Crossing 59
Figure 31. Latency with Boundary Crossing into Program/Erase Bank 60
Figure 32. Example of Wait States Insertion (Standard Handshaking Device) 61
Figure 33. Back-to-Back Read/Write Cycle Timings 62
SRAM AC Characteristics 63
Read Cycle 63
Figure 34. SRAM Read Cycle—Address Controlled 63
Figure 35. SRAM Read Cycle 64
Write Cycle 65
Figure 36. SRAM Write Cycle—WE# Control 65
Figure 37. SRAM Write Cycle—CE1#s Control 66
Figure 38. SRAM Write Cycle—UB#s and LB#s Control 67
Flash Erase And Programming Performance . 68
Flash Latchup Characteristics. 68
Package Pin Capacitance 68
Flash Data Retention 68
SRAM Data Retention 69
Figure 39. CE1#s Controlled Data Retention Mode 69
Figure 40. CE2s Controlled Data Retention Mode 69
Physical Dimensions 70
FSC093—93-Ball Fine-Pitch Grid Array 8 x 11.6 mm 70
Revision Summary 71
Revision A (May 20, 2002) 71

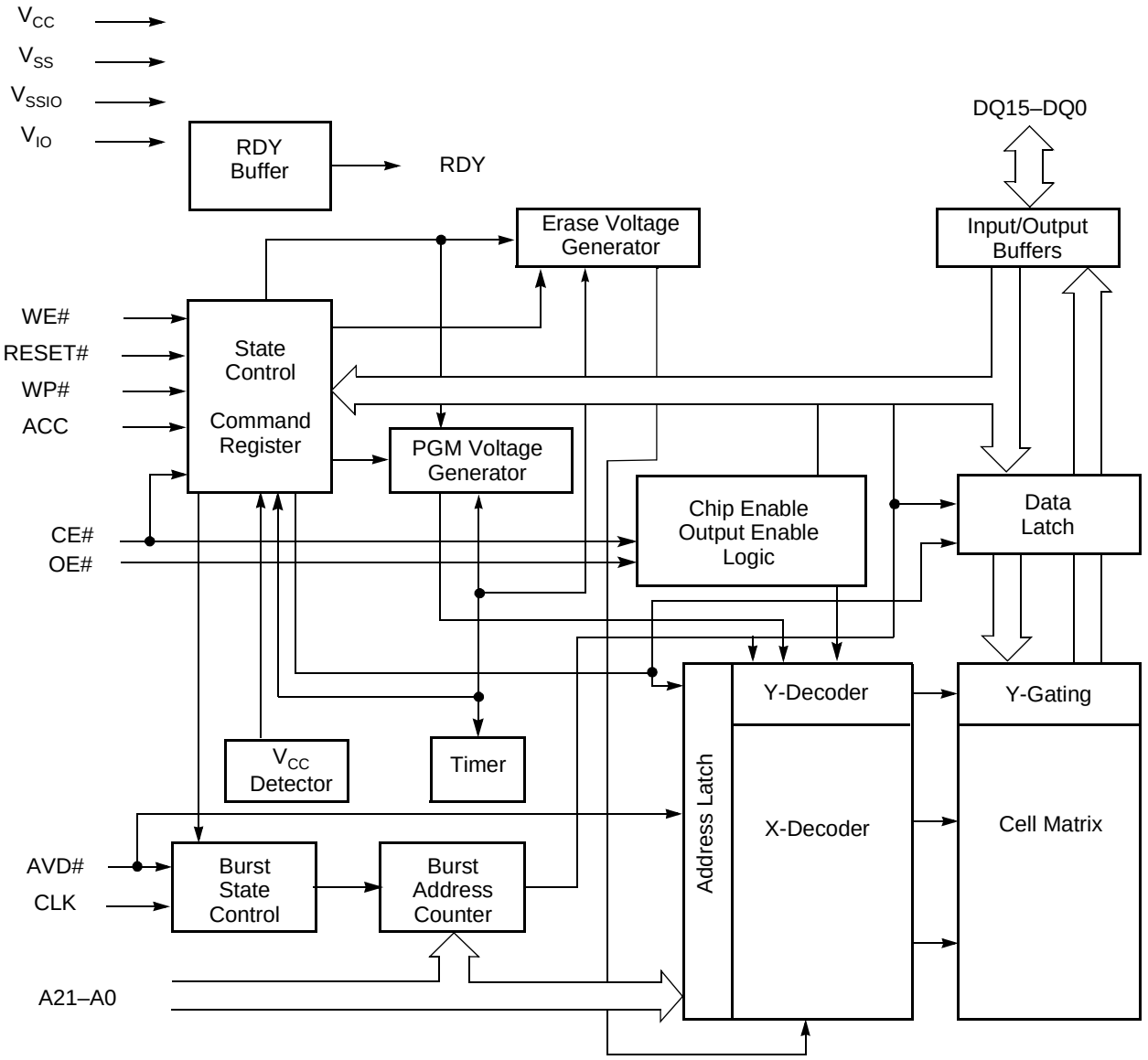
PRODUCT SELECTOR GUIDE

Part Number		Am42BDS640AG	
Burst Frequency		54 MHz	40 MHz
Speed Option	V_{CC}, V_{IO} = 1.65 – 1.95 V	D8, D9	C8, C9
Flash	Max Initial Synchronous Access Time, ns (t_{IACC}) Reduced Wait-state Handshaking: Even Address	87.5	95
	Max Initial Synchronous Access Time, ns (t_{IACC}) Reduced Wait-state Handshaking: Odd Address; or Standard Handshaking	106	120
	Max Burst Access Time, ns (t_{BACC})	13.5	20
	Max Asynchronous Access Time, ns (t_{ACC})	70	85
	Max CE# Access, ns (t_{CE})		
	Max OE# Access, ns (t_{OE})	13.5	20
SRAM	Max Access Time, ns (t_{ACC})	70	85
	Max CE# Access, ns (t_{CE})		
	Max OE# Access, ns (t_{OE})	35	40

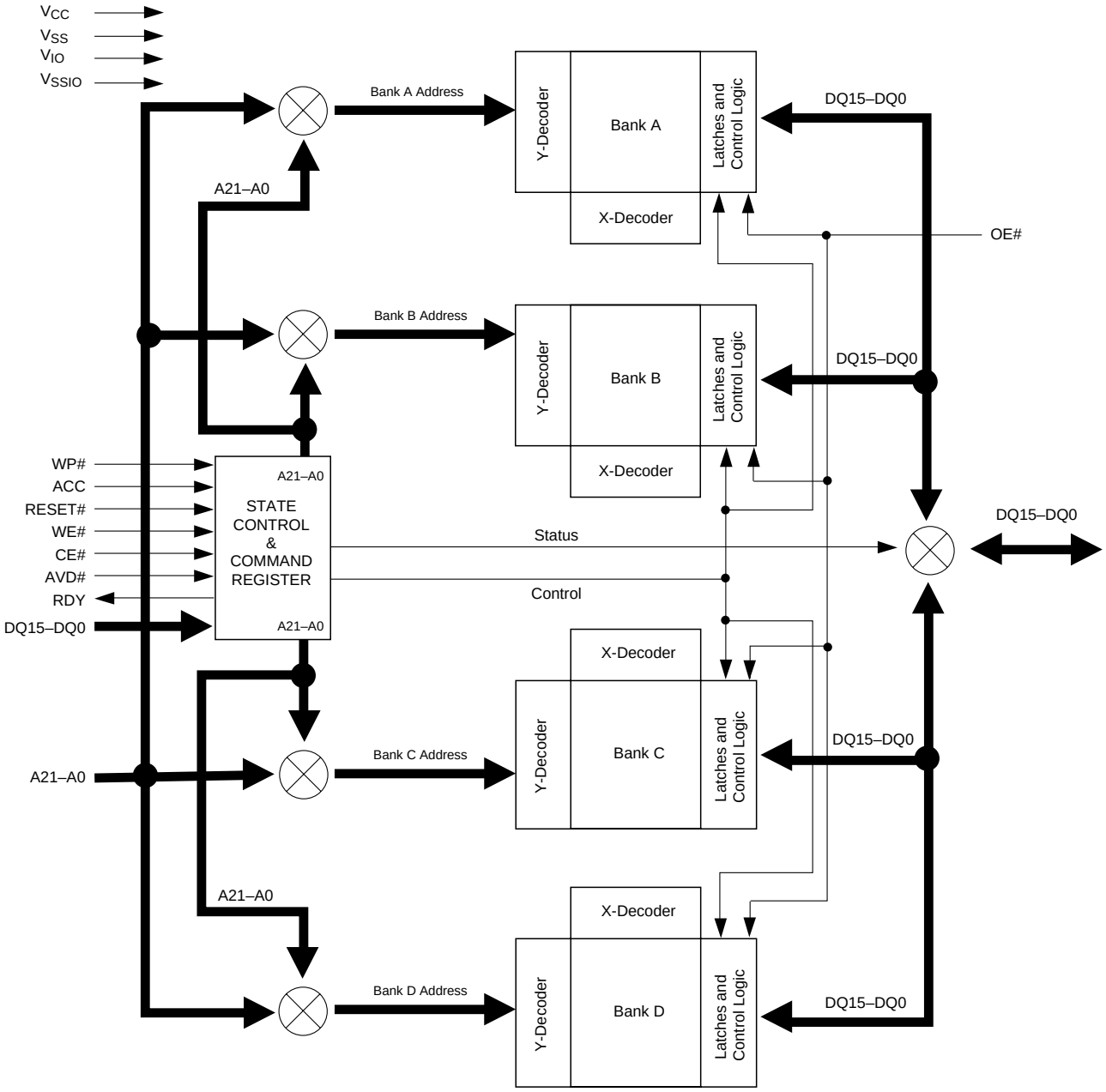
MCP BLOCK DIAGRAM



FLASH MEMORY BLOCK DIAGRAM

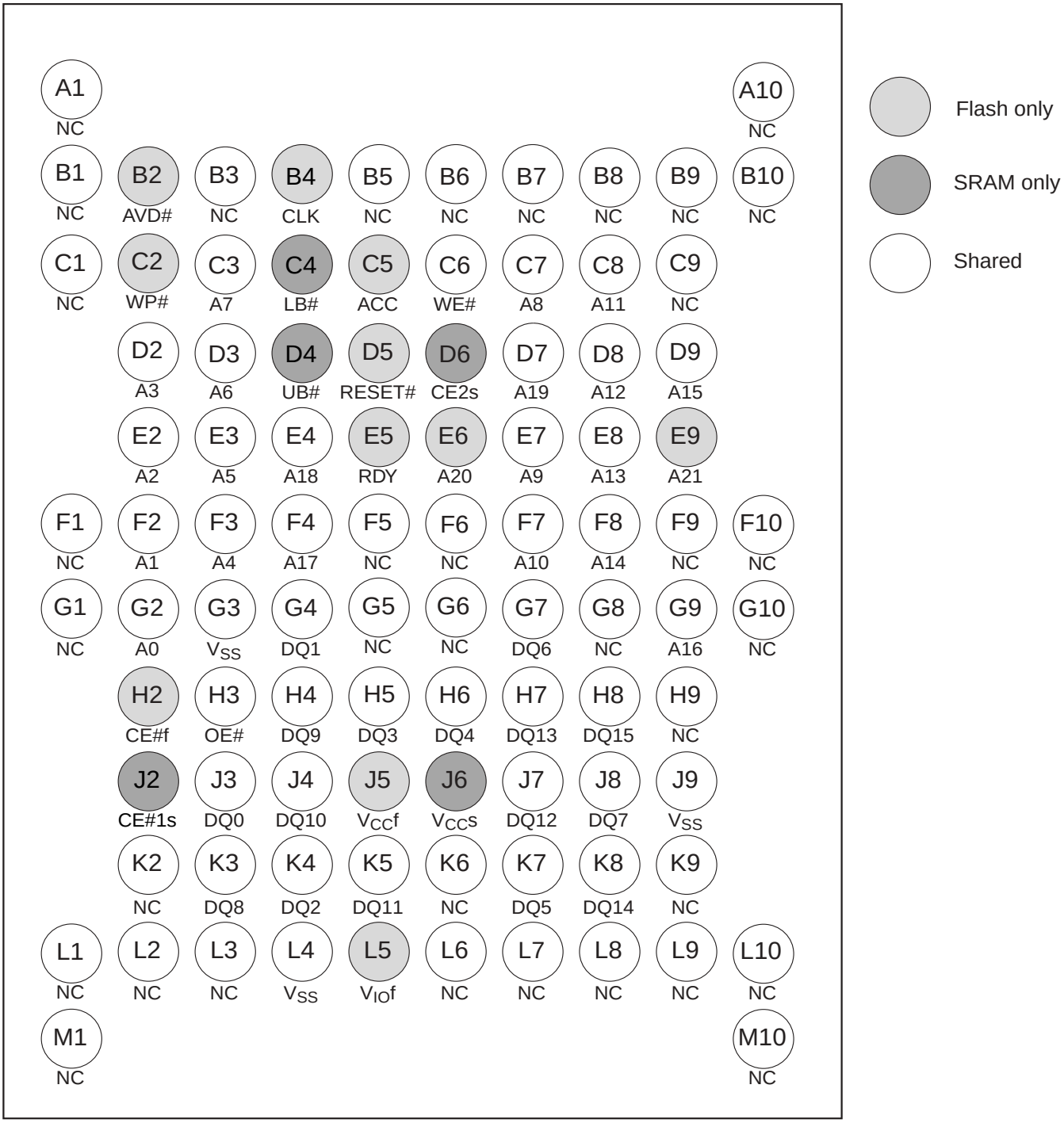


FLASH MEMORY SIMULTANEOUS OPERATION DIAGRAM



CONNECTION DIAGRAM

93-Ball FBGA
Top View



Note: *$V_{IO}f$ must be tied to $V_{CC}f$.*

Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, BGA, PLCC, PDIP, SSOP). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A19–A0 = 20 Address Inputs (Common)

A21–A20 = 2 Address Inputs (Flash)

DQ15–DQ0 = 16 Data Inputs/Outputs (Common)

CE#f = Chip Enable (Flash)

CE1#s = Chip Enable 1 (SRAM)

CE2s = Chip Enable 2 (SRAM)

OE# = Output Enable (Common)

WE# = Write Enable (Common)

UB#s = Upper Byte Control (SRAM)

LB#s = Lower Byte Control (SRAM)

RESET# = Hardware Reset Pin, Active Low

V_{CC}f = Flash 1.8 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

V_{IO}f = Input & Output Buffer Power Supply must be tied to V_{CC}f.

V_{CC}s = SRAM Power Supply

V_{SS} = Device Ground (Common)

NC = Pin Not Connected Internally

RDY = Ready output; indicates the status of the Burst read. Low = data not valid at expected time. High = data valid.

CLK = CLK is not required in asynchronous mode. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter.

AVD# = Address Valid input. Indicates to device that the valid address is present on the address inputs (A21–A0).

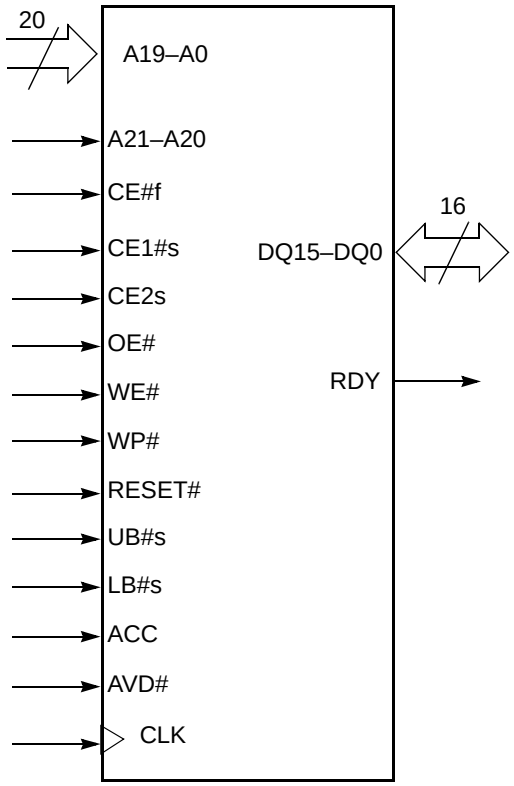
Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.

High = device ignores address inputs

WP# = Hardware write protect input. At V_{IL}, disables program and erase functions in the two outermost sectors. Should be at V_{IH} for all other conditions.

ACC = At V_{ID}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, locks all sectors. Should be at V_{IH} for all other conditions.

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:

Am42BDS640 A G T D 8 I T

TAPE AND REEL
T = 7 inches
S = 13 inches

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

V_{IO} AND HANDSHAKING FEATURES
8 = 1.8 V V_{IO}, reduced wait-state handshaking
9 = 1.8 V V_{IO}, standard handshaking

CLOCK RATE/ASYNCHRONOUS SPEED/SRAM SPEED
D = 54 MHz/70 ns/70 ns
C = 40 MHz/85 ns/85 ns

BOOT SECTOR
T = Top Boot Sector
B = Bottom Boot Sector

PROCESS TECHNOLOGY
G = 0.17 µm

SRAM DEVICE DENSITY
A = 16 Mbits

AMD DEVICE NUMBER/DESCRIPTION
Am42BDS640AG
Stacked Multi-Chip Package (MCP) Flash Memory and SRAM
Am29BDS640G 64 Megabit (4 M x 16-Bit) CMOS 1.8 Volt-only, Simultaneous Operation, Burst Mode Flash Memory and 16 Mbit (1 M x 16-Bit) Static RAM
93-Ball Fine-pitch Ball Grid Array Package, 8.0 x 11.6 mm, 0.8 mm ball pitch (FSC093)

Valid Combinations				
Order Number		**Package Marking**	**Burst Frequency (MHz)**	**V_{IO} Range**
Am42BDS640AGTD8I Am42BDS640AGBD8I	T, S	M42000004Y M42000004Z	54	1.65 – 1.95 V
Am42BDS640AGTD9I Am42BDS640AGBD9I		M420000050 M420000051		
Am42BDS640AGTC8I Am42BDS640AGBC8I		M420000052 M420000053	40	
Am42BDS640AGTC9I Am42BDS640AGBC9I		M420000054 M420000055		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MCP DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#f	CE1#s (Note 3)	CE2s (Note 3)	OE#	WE#	A [21–0]	DQ [15–8]	DQ [7–0]	LB#s (Note 4)	UB#s (Note 4)	RESET#	CLK	AVD#
Asynchronous Read from Flash, Addresses Latched	L	H	L	L	H	A_{IN}	I/O		X	X	H	X	↑
Asynchronous Read from Flash, Addresses Steady State	L	H	L	L	H	A_{IN}	I/O		X	X	H	X	L
Asynchronous Write to Flash	L	H	L	H	L	A_{IN}	I/O		X	X	H	X	L
Synchronous Write to Flash	L	H	L	H	L	A_{IN}	I/O		X	X	H	X	↑
CE# Standby	H	H	L	X	X	Hi-Z	Hi-Z		X	X	H	X	X
Output Disable	L	H	L	H	H	Hi-Z	Hi-Z	Hi-Z	L	X	H	X	X
		H	L						X	L			
Hardware Reset	X	H	L	X	X	Hi-Z	Hi-Z	Hi-Z	X	X	L	X	X
Read from SRAM	H	L	H	L	H	A_{IN}	D_{OUT}	D_{OUT}	L	L	H	X	X
							D_{OUT}	Hi-Z	H	L			
							Hi-Z	D_{OUT}	L	H			
Wirte to SRAM	H	L	H	X	L	A_{IN}	D_{IN}	D_{IN}	L	L	H	X	X
							D_{IN}	Hi-Z	H	L			
							HI-Z	D_{IN}	L	H			
Flash Burst Read Operations													
Load Starting Burst Address	L	H	L	X	H	Addr In	X		X	X	H	↑	↓
Advance Burst to next address with appropriate Data presented on the Data Bus	L	H	L	L	H	HIGH Z	Burst Data Out		X	X	H	↑	H
Terminate current Burst read cycle	H	H	L	X	H	Hi-Z	Hi-Z		X	X	H	↑	X
Terminate current Burst read cycle via RESET#	X	H	L	X	H	Hi-Z	Hi-Z		X	X	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	H	L	X	H	Hi-Z	I/O		X	X	H	↑	↓

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 9–11 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

↑ = Active edge of CLK, ⊓ = Pulse Low, ⊔ = Rising edge of Pulse Low

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Either CE1#s = V_{IH} or CE2s = V_{IL} will disable the SRAM. If one of these conditions is true, the other CE input is don't care.*
4. *X = Don't care or open LB#s or UB#s.*
5. *Default edge of CLK is the rising edge.*
6. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Lock/Unlock Command Sequence"section.*
7. *If ACC = V_{HH}, all sectors will be protected.*
8. *If WP# = V_{IL}, sectors 0,1 (bottom boot) or sectors 132, 133 (top boot) are protected. If WP# = V_{IH}, the protection applied to the aforementioned sectors depends on whether they were last protected or unprotected using the method described in "Sector Lock/Unlock Command Sequence". Note that WP# must not be left floating or unconnected.*

FLASH DEVICE BUS OPERATIONS

Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must first assert a valid address on A21–A0, while driving AVD# and CE# to V_{IL}. WE# should remain at V_{IH}. The rising edge of AVD# latches the address. The data will appear on DQ15–DQ0. Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Requirements for Synchronous (Burst) Read Operation

The device is capable of continuous sequential burst operation and linear burst operation of a preset length. When the device first powers up, it is enabled for asynchronous read operation.

Prior to entering burst mode, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst access, what mode of burst operation is desired, which edge of the clock will be the active clock edge, and how the RDY signal will transition with valid data. The system would then write the burst mode configuration register command sequence. See "Set Burst Mode Configuration Register Command Sequence" and "Flash Command Definitions" for further details.

Once the system has written the "Set Burst Mode Configuration Register" command sequence, the device is enabled for synchronous reads only.

The initial word is output t_{IACC} after the active edge of the first CLK cycle. Subsequent words are output t_{BACC} after the active edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has a fixed internal address boundary that occurs every 64 words, starting at address 00003Fh. During the time the device is outputting data at this fixed internal address boundary (address 00003Fh, 00007Fh, 0000BFh, etc.), a two cycle latency occurs before data appears for the next address (address 000040h, 000080h, 0000C0h, etc.). The RDY output indicates this condition to the system by pulsing low. For standard handshaking devices, there is no two cycle latency between 3Fh and 40h (or multiple thereof). See Table 10.

For reduced wait-state handshaking devices, if the address latched is 3Dh (or 64 multiple), an additional cycle latency occurs prior to the initial access. If the address latched is 3Eh (or 64 multiple) two additional cycle latency occurs prior to the initial access and the 2 cycle latency between 3Fh and 40h (or 64 multiple) will not occur. For 3Fh latched addresses (or 64 multiple) three additional cycle latency occurs prior to the initial access and the 2 cycle latency between 3Fh and 40h (or 64 multiple) will not occur.

The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system drives CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 1, "Device Bus Operations," on page 12.

If the host system crosses the bank boundary while reading in burst mode, and the device is not programming or erasing, a two-cycle latency will occur as described above in the subsequent bank. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

8-, 16-, and 32-Word Linear Burst with Wrap Around

The remaining three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 2.)

Table 2. Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h, ...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh, ...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh, ...

As an example: if the starting address in the 8-word mode is 39h, the address range to be read would be 38-3Fh, and the burst sequence would be

39-3A-3B-3C-3D-3E-3F-38h-etc. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 64 words; thus, no wait states are inserted (except during the initial access).**

The RDY pin indicates when data is valid on the bus. The devices can wrap through a maximum of 128 words of data (8 words up to 16 times, 16 words up to 8 times, or 32 words up to 4 times) before requiring a new synchronous access (latching of a new address).

Burst Mode Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active.

Reduced Wait-State Handshaking Option

The device can be equipped with a reduced wait-state handshaking feature that allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the programmable wait state configuration to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

The presence of the reduced wait-state handshaking feature may be verified by writing the autoselect command sequence to the device. See “Autoselect Command Sequence” for details.

For optimal burst mode performance on devices without the reduced wait-state handshaking option, the host system must set the appropriate number of wait states in the flash device depending on clock frequency and the presence of a boundary crossing. See “Set Burst Mode Configuration Register Command Sequence” section on page 23 section for more information. The device will automatically delay RDY and data by one additional clock cycle when the starting address is odd.

The autoselect function allows the host system to determine whether the flash device is enabled for reduced wait-state handshaking. See the “Autoselect Command Sequence” section for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 33, “Back-to-Back Read/Write Cycle Timings,” on page 62 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

Writing Commands/Command Sequences

The device has the capability of performing an asynchronous or synchronous write operation. During a synchronous write operation, to write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data. During an asynchronous write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address, command, and data. The asynchronous and synchronous programing operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 8, “Programmable Wait State Settings,” on page 24 indicates the address space that each sector occupies. The device address space is divided into four banks: Banks B and C contain only 32 Kword sectors, while Banks A and D contain both 8 Kword boot sectors in addition to 32 Kword sectors. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” is the address bits required to uniquely select a sector.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. ACC is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{ID} on this input, the device automatically enters the aforementioned Unlock Bypass

mode and uses the higher voltage on the input to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{ID} from the ACC input returns the device to normal operation. Note that sectors must be unlocked prior to raising ACC to V_{ID}. *Note that the ACC pin must not be at V_{ID} for operations other than accelerated programming, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result*.

When at V_{IL}, ACC locks all sectors. ACC should be at V_{IH} for all other conditions.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Autoselect mode may only be entered and used when in the asynchronous read mode. Refer to the "Autoselect Command Sequence" section on page 26 section for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at $V_{CC} \pm 0.2$ V. The device requires standard access time (t_{CE}) for read access, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. While in asynchronous mode, the device automatically enables this mode when addresses remain stable for t_{ACC} + 60 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. While in synchronous mode, the device automatically enables this mode when either the first active CLK edge occurs after t_{ACC} or the CLK runs slower than 5MHz. Note that a new burst operation is required to provide new data.

I_{CC4} in the "Flash DC Characteristics" section on page 36 represents the automatic sleep mode current specification.

RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.2$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.2$ V, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the device requires a time of t_{READY} (during Embedded Algorithms) before the device is ready to read data again. If RESET# is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 20, "Reset Timings," on page 49 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 14, "Command Definitions," on page 30 for command definitions).

The device offers two types of data protection at the sector level:

- The sector lock/unlock command sequence disables or re-enables both program and erase operations in any sector.

- When WP# is at V_{IL}, sectors 0 and 1 (bottom boot) or sectors 132 and 133 (top boot) are locked.
- When ACC is at V_{IL}, all sectors are locked.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Write Protect (WP#)

The Write Protect (WP#) input provides a hardware method of protecting data without using V_{ID}.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in sectors 0 and 1 (bottom boot) or sectors 132 and 133 (top boot).

If the system asserts V_{IH} on the WP# pin, the device reverts to whether the two outermost 8K Byte boot sectors were last set to be protected or unprotected.

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 3-6. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 3-6. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the AMD site at the following URL: http://www.amd.com/us-en/FlashMemory/TechnicalResources/0,,37_1693_1780_1834^1955,00.html. Alternatively, contact an AMD representative for copies of these documents.

Table 3. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)

19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 4. System Interface String

Addresses	Data	Description
1Bh	0017h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0004h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0004h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 5. Device Geometry Definition

Addresses	Data	Description
27h	0017h	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0003h 0000h 0040h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	007Dh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	0003h 0000h 0040h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 6. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0004h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Technology (Bits 5-2) 0001 = 0.17 µm
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0005h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	0063h	Simultaneous Operation Number of Sectors in all banks except boot block
4Bh	0001h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	00xxh	Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device
50h	0000h	Program Suspend. 00h = not supported
57h	0004h	Bank Organization: X = Number of banks
58h	0023h	Bank A Region Information. X = Number of sectors in bank
59h	0020h	Bank B Region Information. X = Number of sectors in bank
5Ah	0020h	Bank C Region Information. X = Number of sectors in bank
5Bh	0023h	Bank D Region Information. X = Number of sectors in bank

Table 7. Sector Address Table

	Sector	Sector Size	(x16) Address Range
Bank D	SA0	8 Kwords	000000h-001FFFh
	SA1	8 Kwords	002000h-003FFFh
	SA2	8 Kwords	004000h-005FFFh
	SA3	8 Kwords	006000h-007FFFh
	SA4	32 Kwords	008000h-00FFFFh
	SA5	32 Kwords	010000h-017FFFh
	SA6	32 Kwords	018000h-01FFFFh
	SA7	32 Kwords	020000h-027FFFh
	SA8	32 Kwords	028000h-02FFFFh
	SA9	32 Kwords	030000h-037FFFh
	SA10	32 Kwords	038000h-03FFFFh
	SA11	32 Kwords	040000h-047FFFh
	SA12	32 Kwords	048000h-04FFFFh
	SA13	32 Kwords	050000h-057FFFh
	SA14	32 Kwords	058000h-05FFFFh
	SA15	32 Kwords	060000h-067FFFh
	SA16	32 Kwords	068000h-06FFFFh
	SA17	32 Kwords	070000h-077FFFh
	SA18	32 Kwords	078000h-07FFFFh
	SA19	32 Kwords	080000h-087FFFh
	SA20	32 Kwords	088000h-08FFFFh
	SA21	32 Kwords	090000h-097FFFh
	SA22	32 Kwords	098000h-09FFFFh
	SA23	32 Kwords	0A0000h-0A7FFFh
	SA24	32 Kwords	0A8000h-0AFFFFh
	SA25	32 Kwords	0B0000h-0B7FFFh
	SA26	32 Kwords	0B8000h-0BFFFFh
	SA27	32 Kwords	0C0000h-0C7FFFh
	SA28	32 Kwords	0C8000h-0CFFFFh
	SA29	32 Kwords	0D0000h-0D7FFFh
	SA30	32 Kwords	0D8000h-0DFFFFh
	SA31	32 Kwords	0E0000h-0E7FFFh
	SA32	32 Kwords	0E8000h-0EFFFFh
	SA33	32 Kwords	0F0000h-0F7FFFh
	SA34	32 Kwords	0F8000h-0FFFFFh

Table 7. Sector Address Table (Continued)

	Sector	Sector Size	(x16) Address Range
Bank C	SA35	32 Kwords	100000h-107FFFh
	SA36	32 Kwords	108000h-10FFFFh
	SA37	32 Kwords	110000h-117FFFh
	SA38	32 Kwords	118000h-11FFFFh
	SA39	32 Kwords	120000h-127FFFh
	SA40	32 Kwords	128000h-12FFFFh
	SA41	32 Kwords	130000h-137FFFh
	SA42	32 Kwords	138000h-13FFFFh
	SA43	32 Kwords	140000h-147FFFh
	SA44	32 Kwords	148000h-14FFFFh
	SA45	32 Kwords	150000h-157FFFh
	SA46	32 Kwords	158000h-15FFFFh
	SA47	32 Kwords	160000h-167FFFh
	SA48	32 Kwords	168000h-16FFFFh
	SA49	32 Kwords	170000h-177FFFh
	SA50	32 Kwords	178000h-17FFFFh
	SA51	32 Kwords	180000h-187FFFh
	SA52	32 Kwords	188000h-18FFFFh
	SA53	32 Kwords	190000h-197FFFh
	SA54	32 Kwords	198000h-19FFFFh
	SA55	32 Kwords	1A0000h-1A7FFFh
	SA56	32 Kwords	1A8000h-1AFFFFh
	SA57	32 Kwords	1B0000h-1B7FFFh
	SA58	32 Kwords	1B8000h-1BFFFFh
	SA59	32 Kwords	1C0000h-1C7FFFh
	SA60	32 Kwords	1C8000h-1CFFFFh
	SA61	32 Kwords	1D0000h-1D7FFFh
	SA62	32 Kwords	1D8000h-1DFFFFh
	SA63	32 Kwords	1E0000h-1E7FFFh
	SA64	32 Kwords	1E8000h-1EFFFFh
	SA65	32 Kwords	1F0000h-1F7FFFh
	SA66	32 Kwords	1F8000h-1FFFFFh

Table 7. Sector Address Table (Continued)

	Sector	Sector Size	(x16) Address Range
Bank B	SA67	32 Kwords	200000h-207FFFh
	SA68	32 Kwords	208000h-20FFFFh
	SA69	32 Kwords	210000h-217FFFh
	SA70	32 Kwords	218000h-21FFFFh
	SA71	32 Kwords	220000h-227FFFh
	SA72	32 Kwords	228000h-22FFFFh
	SA73	32 Kwords	230000h-237FFFh
	SA74	32 Kwords	238000h-23FFFFh
	SA75	32 Kwords	240000h-247FFFh
	SA76	32 Kwords	248000h-24FFFFh
	SA77	32 Kwords	250000h-257FFFh
	SA78	32 Kwords	258000h-25FFFFh
	SA79	32 Kwords	260000h-267FFFh
	SA80	32 Kwords	268000h-26FFFFh
	SA81	32 Kwords	270000h-277FFFh
	SA82	32 Kwords	278000h-27FFFFh
	SA83	32 Kwords	280000h-287FFFh
	SA84	32 Kwords	288000h-28FFFFh
	SA85	32 Kwords	290000h-297FFFh
	SA86	32 Kwords	298000h-29FFFFh
	SA87	32 Kwords	2A0000h-2A7FFFh
	SA88	32 Kwords	2A8000h-2AFFFFh
	SA89	32 Kwords	2B0000h-2B7FFFh
	SA90	32 Kwords	2B8000h-2BFFFFh
	SA91	32 Kwords	2C0000h-2C7FFFh
	SA92	32 Kwords	2C8000h-2CFFFFh
	SA93	32 Kwords	2D0000h-2D7FFFh
	SA94	32 Kwords	2D8000h-2DFFFFh
	SA95	32 Kwords	2E0000h-2E7FFFh
	SA96	32 Kwords	2E8000h-2EFFFFh
	SA97	32 Kwords	2F0000h-2F7FFFh
	SA98	32 Kwords	2F8000h-2FFFFFh

Table 7. Sector Address Table (Continued)

	Sector	Sector Size	(x16) Address Range
Bank A	SA99	32K words	300000h-307FFFh
	SA100	32K words	308000h-30FFFFh
	SA101	32K words	310000h-317FFFh
	SA102	32K words	318000h-31FFFFh
	SA103	32K words	320000h-327FFFh
	SA104	32K words	328000h-32FFFFh
	SA105	32K words	330000h-337FFFh
	SA106	32K words	338000h-33FFFFh
	SA107	32K words	340000h-347FFFh
	SA108	32K words	348000h-34FFFFh
	SA109	32K words	350000h-357FFFh
	SA110	32K words	358000h-35FFFFh
	SA111	32K words	360000h-367FFFh
	SA112	32K words	368000h-36FFFFh
	SA113	32K words	370000h-377FFFh
	SA114	32K words	378000h-37FFFFh
	SA115	32K words	380000h-387FFFh
	SA116	32K words	388000h-38FFFFh
	SA117	32K words	390000h-397FFFh
	SA118	32K words	398000h-39FFFFh
	SA119	32K words	3A0000h-3A7FFFh
	SA120	32K words	3A8000h-3AFFFFh
	SA121	32K words	3B0000h-3B7FFFh
	SA122	32K words	3B8000h-3BFFFFh
	SA123	32K words	3C0000h-3C7FFFh
	SA124	32K words	3C8000h-3CFFFFh
	SA125	32K words	3D0000h-3D7FFFh
	SA126	32K words	3D8000h-3DFFFFh
	SA127	32K words	3E0000h-3E7FFFh
	SA128	32K words	3E8000h-3EFFFFh
	SA129	32K words	3F0000h-3F7FFFh
	SA130	8K words	3F8000h-3F9FFFh
	SA131	8K words	3FA000h-3FBFFFh
	SA132	8K words	3FC000h-3FDFFFh
	SA133	8K words	3FE000h-3FFFFFh

FLASH COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 14, "Command Definitions," on page 30 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the "Erase Suspend/Erase Resume Commands" section on page 28 section for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the "Reset Command" section on page 25 section for more information.

See also "Requirements for Asynchronous Read Operation (Non-Burst)" and "Requirements for Synchronous (Burst) Read Operation" sections for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figures 11, 13, and 18 show the timings.

Set Burst Mode Configuration Register Command Sequence

The device uses a burst mode configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active. The burst mode configuration register must be set before the device will enter burst mode.

The burst mode configuration register is loaded with a three-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C0h, address bits A11–A0 should be 555h, and address bits A19–A12 set the code to be latched. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The burst mode configuration register can not be changed during device operations (program, erase, or sector lock).

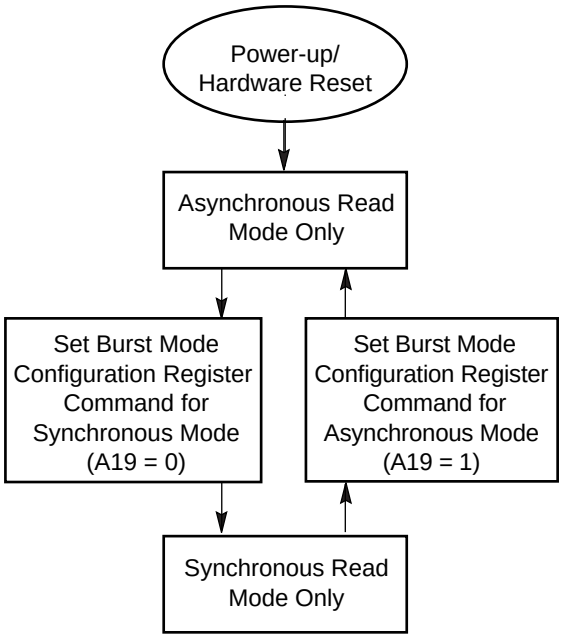


Figure 1. Synchronous/Asynchronous State Diagram

Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations. Address A19 determines this setting: "1' for asynchronous mode, "0" for synchronous mode.

Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. Address bits A14–A12 determine the setting (see Table 8).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 8. Programmable Wait State Settings

A14	A13	A12	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7

Notes:

1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY will default to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*
3. *Assumes even address.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

Handshaking Option

If the device is equipped with reduced wait-state handshaking, the host system should set address bits A14–A12 to 010 for a clock frequency of 40 MHz or to 011 for a clock frequency of 54 MHz for the system/device to execute at maximum speed.

Table 9 describes the typical number of clock cycles (wait states) for various conditions.

Table 9. Initial Access Codes

System Frequency Range	Even Initial Addr.	Odd Initial Addr.	Even Initial Addr. with Boundary*	Odd Initial Addr. with Boundary*	Device Speed Rating
6–11 MHz	2	2	3	4	40 MHz
12–23 MHz	2	3	4	5	
24–33 MHz	3	4	5	6	
34–40 MHz	4	5	6	7	
40–47 MHz	4	5	6	7	54 MHz
48–54 MHz	5	6	7	8	

** In the 8-, 16- and 32-word burst read modes, the address pointer does not cross 64-word boundaries (addresses which are multiples of 3Fh).*

The autoselect function allows the host system to determine whether the flash device is enabled for reduced wait-state handshaking. See the “Autoselect Command Sequence” section for more information.

Standard Handshaking Operation

For optimal burst mode performance on devices with standard handshaking, the host system must set the appropriate number of wait states in the flash device depending on the clock frequency.

Table 10 describes the typical number of clock cycles (wait states) for various conditions with A14–A12 set to 101.

Table 10. Wait States for Standard Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low
	40/54 MHz
Initial address is even	7
Initial address is odd	7
Initial address is even, and is at boundary crossing*	7
Initial address is odd, and is at boundary crossing*	7

** In the 8-, 16- and 32-word burst read modes, the address pointer does not cross 64-word boundaries (addresses which are multiples of 3Fh).*

Burst Read Mode Configuration

The device supports four different burst read modes: continuous mode, and 8, 16, and 32 word linear wrap around modes. A continuous sequence begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear burst with wrap around begins on the starting burst address written to the device and then proceeds until the next 8 word boundary. The address pointer then returns to the first word of the boundary, wrapping back to the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 11 shows the address bits and settings for the four burst read modes.

Table 11. Burst Read Mode Settings

Burst Modes	Address Bits	
	A16	A15
Continuous	0	0
8-word linear wrap around	0	1
16-word linear wrap around	1	0
32-word linear wrap around	1	1

Note: *Upon power-up or hardware reset the default setting is continuous.*

Burst Active Clock Edge Configuration

By default, the device will deliver data on the rising edge of the clock after the initial synchronous access time. Subsequent outputs will also be on the following rising edges, barring any delays. The device can be set so that the falling clock edge is active for all synchronous accesses. Address bit A17 determines this setting; “1” for rising active, “0” for falling active.

RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determines this setting; “1” for RDY active with data, “0” for RDY active one clock cycle before valid data.

Configuration Register

Table 12 shows the address bits that determine the configuration register settings for various device functions.

Table 12. Burst Mode Configuration Register

Address BIt	Function	Settings (Binary)
A19	Set Device Read Mode	0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Mode (default)
A18	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
A17	Clock	0 = Burst starts and data is output on the falling edge of CLK 1 = Burst starts and data is output on the rising edge of CLK (default)
A16	Burst Read Mode	00 = Continuous (default) 01 = 8-word linear with wrap around 10 = 16-word linear with wrap around 11 = 32-word linear with wrap around
A15		
A14	Programmable Wait State	000 = Data is valid on the 2nd active CLK edge after AVD# transition to V_{IH} 001 = Data is valid on the 3rd active CLK edge after AVD# transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after AVD# transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after AVD# transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after AVD# transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after AVD# transition to V_{IH} (default)
A13		
A12		

Note:*Device will be in the default state upon power-up or hardware reset.*

Sector Lock/Unlock Command Sequence

The sector lock/unlock command sequence allows the system to determine which sectors are protected from accidental writes. When the device is first powered up, all sectors are locked. To unlock a sector, the system must write the sector lock/unlock command sequence. Two cycles are first written: addresses are don’t care and data is 60h. During the third cycle, the sector address (SLA) and unlock command (60h) is written, while specifying with address A6 whether that sector should be locked (A6 = V_{IL}) or unlocked (A6 = V_{IH}). After the third cycle, the system can continue to lock or unlock additional cycles, or exit the sequence by writing F0h (reset command).

Note that the last two outermost boot sectors can be locked by taking the WP# signal to V_{IL}.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don’t cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which

the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins (prior to the third cycle). This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

The reset command is used to exit the sector lock/unlock sequence.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 14, “Command Definitions,” on page 30 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. No subsequent data will be made available if the autoselect data is read in synchronous mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address, and SA represents the sector address. The device ID is read in three cycles.

Table 13. Device IDs

Description	Address	Read Data
Manufacturer ID	(BA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	227Eh
Device ID, Word 2, Top Boot	(BA) + 0Eh	2204h (1.8 V V_{IO})
Device ID, Word 2, Bottom Boot	(BA) + 0Eh	2224h (1.8 V V_{IO})
Device ID, Word 3	(BA) + 0Fh	2201h
Sector Block Lock/Unlock	(SA) + 02h	0001 (locked), 0000 (unlocked)
Handshaking	(BA) + 03h	43h (reduced wait-state), 42h (standard)

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 14 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the “Flash Write Operation Status” section on page 31 section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from “0” back to a “1.” Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bit to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

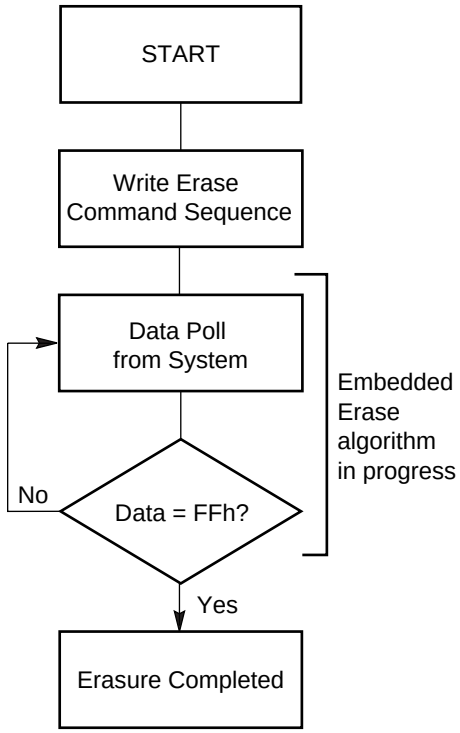
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to primarily program to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. The host system may also initiate the chip erase and sector erase sequences in the unlock bypass mode. The erase command sequences are four cycles in length instead of six cycles. Table 14, "Command Definitions," on page 30 shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Unlock Bypass Program, Unlock Bypass Sector Erase, Unlock Bypass Chip Erase, and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

The device offers accelerated program operations through the ACC input. When the system asserts V_{ID} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC input to accelerate the operation.

Figure 2 illustrates the algorithm for the program operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 21, "Asynchronous Program Operation Timings," on page 51 for timing diagrams.



Notes:

1. *See Table 14 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 2. Erase Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 14, "Command Definitions," on page 30 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to the "Flash Write Operation Status" section on page 31 section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the chip erase command sequence while the device is in the unlock bypass mode. The command sequence is two cycles cycles in length instead of six cycles. See Table 14 for details on the unlock bypass command sequences.

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters and timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 14 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than 35 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See “DQ3: Sector Erase Timer” section on page 34.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing bank. Refer to the “Flash Write Operation Status” section on page 31 section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the sector erase command sequence while the device is in the unlock bypass mode. The command sequence is four cycles cycles in length instead of six cycles.

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters and timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

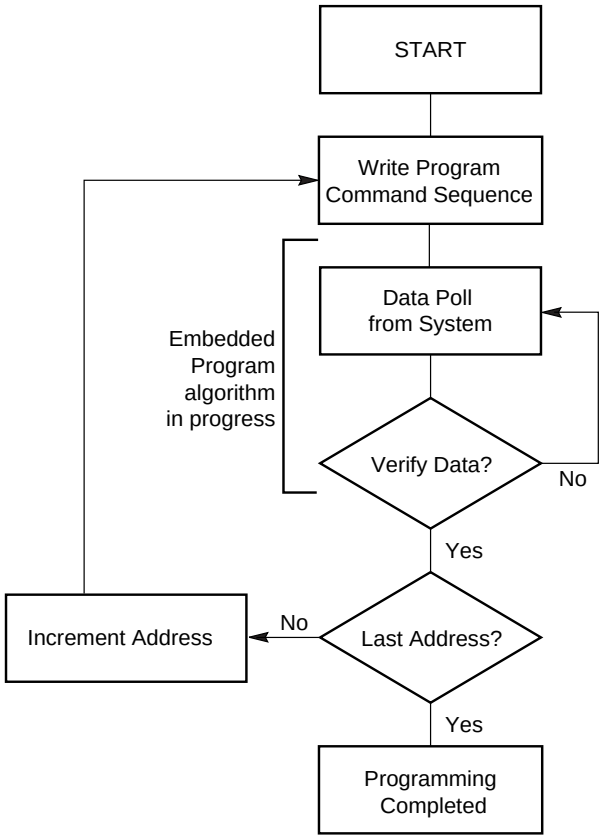
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to the "Flash Write Operation Status" section on page 31 section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the "Autoselect Functions" section on page 15 and "Autoselect Command Sequence" section on page 26 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Note: *See Table 14 for program command sequence.*

Figure 3. Program Operation

Command Definitions

Table 14. Command Definitions

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (6)		1	RA	RD										
Reset (7)		1	XXX	F0										
Autoselect (8)	Manufacturer ID	4	555	AA	2AA	55	(BA)555	90	(BA)X00	0001				
	Device ID (9)	6	555	AA	2AA	55	(BA)555	90	(BA)X01	227E	(BA) X0E	(Note 9)	(BA) X0F	2201
	Sector Lock Verify (10)	4	555	AA	2AA	55	(SA)555	90	(SA)X02	0000/0001				
	Handshaking Option (11)	4	555	AA	2AA	55	(BA)555	90	(BA)X03	0042/0043				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (12)		2	XXX	A0	PA	PD								
Unlock Bypass Sector Erase (12)		2	XXX	80	SA	30								
Unlock Bypass Chip Erase (12)		2	XXX	80	XXX	10								
Unlock Bypass Reset (13)		2	BA	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (14)		1	BA	B0										
Erase Resume (15)		1	BA	30										
Sector Lock/Unlock		3	XXX	60	XXX	60	SLA	60						
Set Burst Mode Configuration Register (16)		3	555	AA	2AA	55	(CR)555	C0						
CFI Query (17)		1	55	98										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the rising edge of the AVD# pulse.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# pulse.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A21–A14 uniquely select any sector.

BA = Address of the bank (A21, A20) that is being switched to autoselect mode, is in bypass mode, or is being erased.

SLA = Address of the sector to be locked. Set sector address (SA) and either A6 = 1 for unlocked or A6 = 0 for locked.

CR = Configuration Register address bits A19–A12.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A21–A12 are don't cares.*
6. *No unlock or command cycles required when bank is reading array data.*
7. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information) or performing sector lock/unlock.*
8. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
9. *The data in the fifth cycle is 2204h for top boot, 2224h for bottom boot.*
10. *The data is 0000h for an unlocked sector and 0001h for a locked sector*
11. *The data is 0043h for reduced wait-state handshaking and 0042h standard handshaking.*
12. *The Unlock Bypass command sequence is required prior to this command sequence.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
16. *See "Set Burst Mode Configuration Register Command Sequence" for details.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

FLASH WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 16, "Write Operation Status," on page 34 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

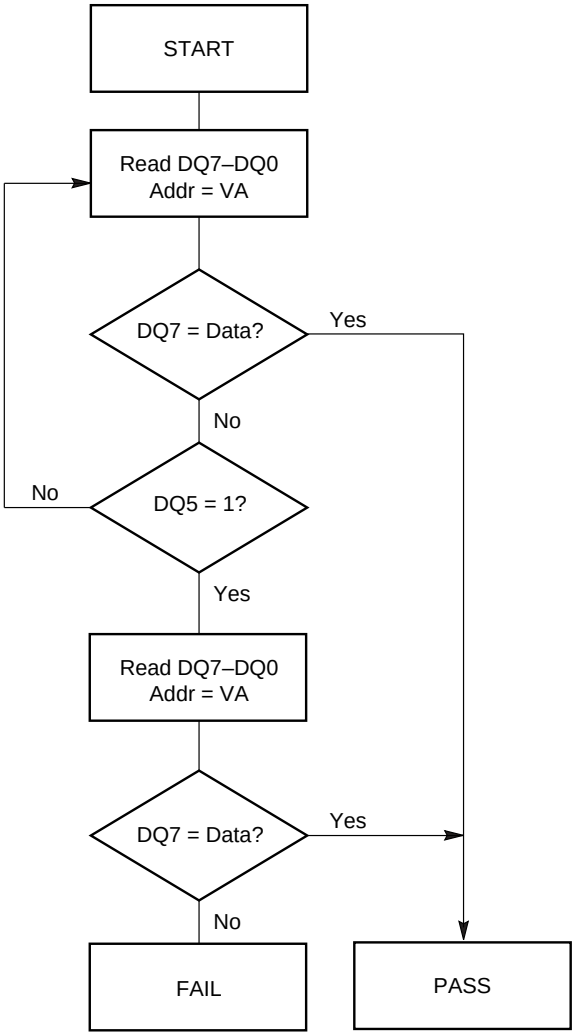
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 will appear on successive read cycles.

Table 16 shows the outputs for Data# Polling on DQ7. Figure 3 shows the Data# Polling algorithm. Figure 27, "Data# Polling Timings (During Embedded Algorithm)," on page 57 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 4. Data# Polling Algorithm

RDY: Ready

The RDY is a dedicated output that, by default, indicates (when at logic low) the system should wait 1 clock cycle before expecting the next word of data. Using the RDY Configuration Command Sequence, RDY can be set so that a logic low indicates the system should wait 2 clock cycles before expecting valid data.

RDY functions only while reading data in burst mode. The following conditions cause the RDY output to be low: during the initial access (in burst mode), and after the boundary that occurs every 64 words beginning with the 64th address, 3Fh.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

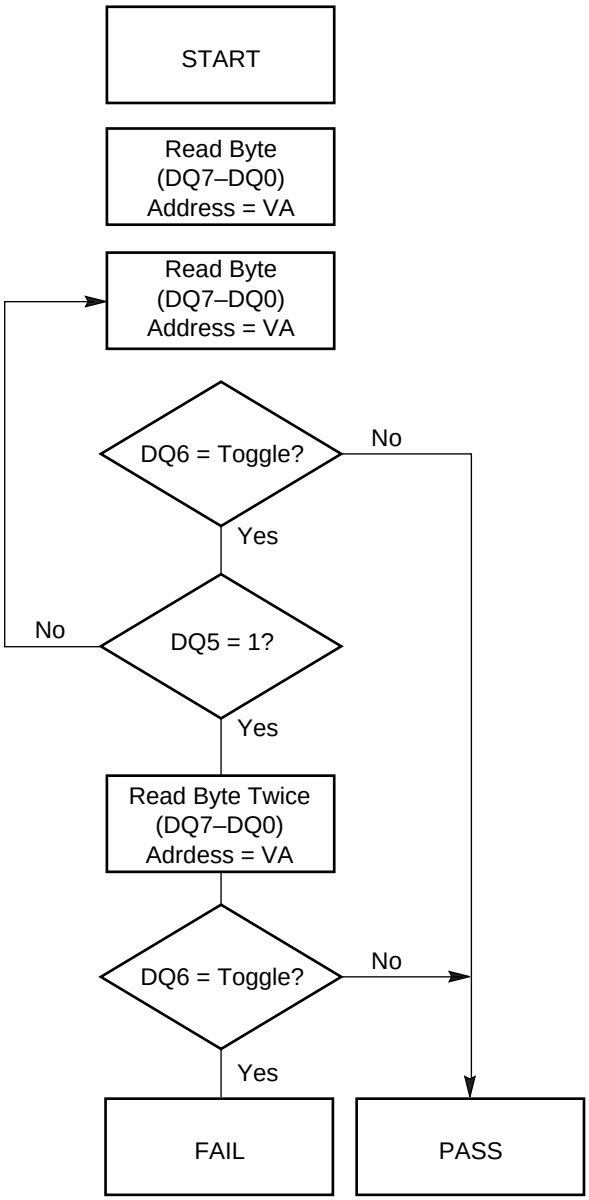
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 ms after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: Figure 4 (toggle bit flowchart), DQ6: Toggle Bit I (description), Figure 28, “Toggle Bit Timings (During Embedded Algorithm),” on page 57 (toggle bit timing diagram), and Table 15, “DQ6 and DQ2 Indications,” on page 33.



Note: *The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.*

Figure 5. Toggle Bit Algorithm

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit

II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 15 to compare outputs for DQ2 and DQ6.

See the following for additional information: Figure 5, "Toggle Bit Algorithm," on page 32, See "DQ6: Toggle Bit I" on page 32., Figure 28, "Toggle Bit Timings (During Embedded Algorithm)," on page 57, and Table 15, "DQ6 and DQ2 Indications," on page 33.

Table 15. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 4 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 4).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 16 shows the status of DQ3 relative to the other status bits.

Table 16. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
Erase Suspend Mode	Erase-Suspend-Read (Note 4)	Erase Suspended Sector	1	No toggle	0	N/A	Toggle
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A

Notes:

1. *DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*
4. *The system may read either asynchronously or synchronously (burst) while in erase suspend. RDY will function exactly as in non-erase-suspended mode.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground:
All Inputs and I/Os except
as noted below (Note 1). . . . . –0.5 V to V_{IO} + 0.5 V

V_{CC}f/V_{CC}s (Note 1) . . . . . –0.5 V to +2.5 V

V_{IO} . . . . . –0.5 V to +1.95 V

ACC . . . . . –0.5 V to +12.5 V

Output Short Circuit Current (Note 3) . . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns during voltage transitions inputs might overshoot to V_{CC} +0.5 V for periods up to 20 ns. See Figure 6. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 7.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

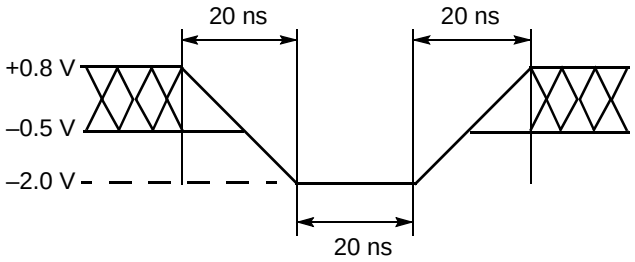


Figure 6. Maximum Negative Overshoot Waveform

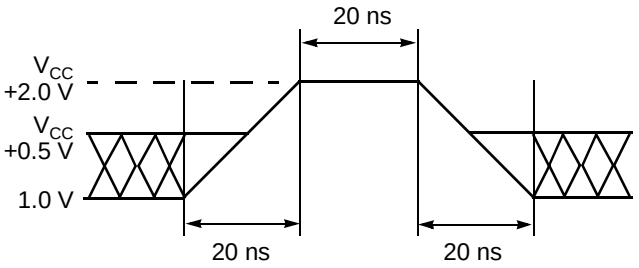


Figure 7. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Supply Voltages

V_{CC} Supply Voltages . . . . . +1.65 V to +1.95 V

V_{IO} Supply Voltages:
$V_{IO} \leq V_{CC}$ . . . . . +1.65 V to +1.95 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

FLASH DC CHARACTERISTICS

CMOS Compatible

Parameter	Description	Test Conditions (Note 1)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{CCB}	V_{CC} Active Burst Read Current	CE# = V_{IL}, OE# = V_{IL}, WE# = V_{IH}			10	20	mA
I_{IO1}	V_{IO} Active Read Current	V_{IO} = 1.8 V, CE# = V_{IL}, OE# = V_{IL}, WE# = V_{IH}			15	30	mA
I_{IO2}	V_{IO} Non-active Output	V_{IO} = 1.8 V, OE# = V_{IH}			0.2	10	µA
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	5 MHz		12	16	mA
			1 MHz		3.5	5	mA
I_{CC2}	V_{CC} Active Write Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, $V_{PP} = V_{IH}$			15	40	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	CE# = RESET# = V_{CC} ± 0.2 V			0.2	10	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			0.2	10	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IH}			25	60	mA
I_{ACC}	Accelerated Program Current (Note 5)	CE# = V_{IL}, OE# = V_{IH}, V_{ACC} = 12.0 ± 0.5 V	V_{ACC}		7	15	mA
			V_{CC}		5	10	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.8 V		–0.5		0.2	V
V_{IH}	Input High Voltage	V_{IO} = 1.8 V		V_{IO} – 0.2		V_{IO} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$, $V_{IO} = V_{IO\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$, $V_{IO} = V_{IO\ min}$		V_{IO} – 0.1			V
V_{ID}	Voltage for Accelerated Program			11.5		12.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Note:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 60 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Total current during accelerated programming is the sum of V_{ACC} and V_{CC} currents.*

SRAM DC AND OPERATING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	–1.0		1.0	µA
I_{LO}	Output Leakage Current	CE1#s = V_{IH}, CE2s = V_{IL} or OE# = V_{IH} or WE# = V_{IL}, V_{IO}= V_{SS} to V_{CC}	–1.0		1.0	µA
I_{CC}	Operating Power Supply Current	I_{IO} = 0 mA, CE1#s = V_{IL}, CE2s = WE# = V_{IH}, V_{IN} = V_{IH} or V_{IL}			5	mA
$I_{CC1}s$	Average Operating Current	Cycle time = 1 µs, 100% duty, I_{IO} = 0 mA, CE1#s ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V		1	3	mA
$I_{CC2}s$	Average Operating Current	Cycle time = Min., I_{IO} = 0 mA, 100% duty, CE1#s = V_{IL}, CE2s = V_{IH}, V_{IN} = V_{IL} = or V_{IH}		8	25	mA
V_{OL}	Output Low Voltage	I_{OL} = 0.1 mA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	1.4			V
I_{SB1}	Standby Current (CMOS)	CE1#s ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V (CE1#s controlled) or CE2 ≤ 0.2 V (CE2s controlled), CIOs = V_{SS} or V_{CC}, Other input = 0 ~ V_{CC}			15	µA
V_{IL}	Input Low Voltage		–0.2 (Note 2)		0.4	V
V_{IH}	Input High Voltage		1.4		V_{CC}+0.2 (Note 3)	V

Notes:

1. *Typical values measured at V_{CC} = 2.0 V, T_A = 25°C. Not 100% tested.*
2. *Undershoot is –1.0 V when pulse width ≤ 20 ns.*
3. *Overshoot is V_{CC} + 1.0 V when pulse width ≤ 20 ns.*
4. *Overshoot and undershoot are sampled, not 100% tested.*

TEST CONDITIONS

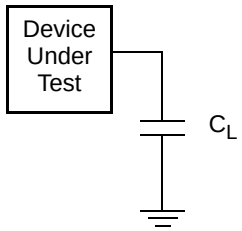
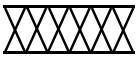


Figure 8. Test Setup

Table 17. Test Specifications

Test Condition	All speed options	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

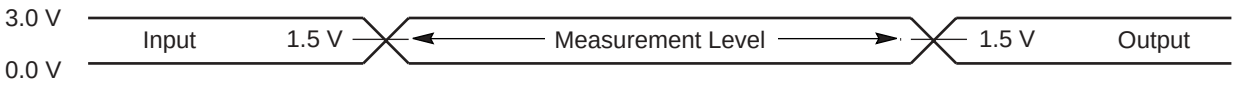


Figure 9. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

SRAM CE#s Timing

Parameter		Description	Test Setup		All Speeds	Unit
JEDEC	Std					
—	t_{CCR}	CE#s Recover Time	—	Min	0	ns

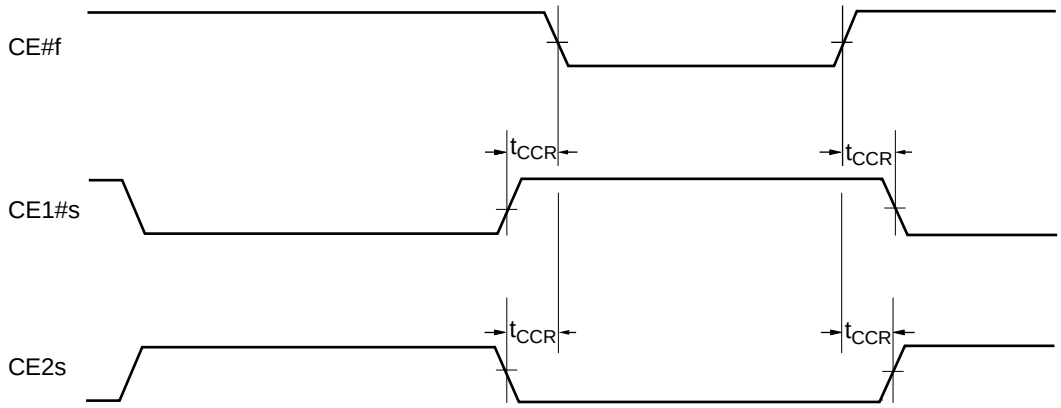


Figure 10. Timing Diagram for Alternating Between SRAM and Flash

FLASH AC CHARACTERISTICS

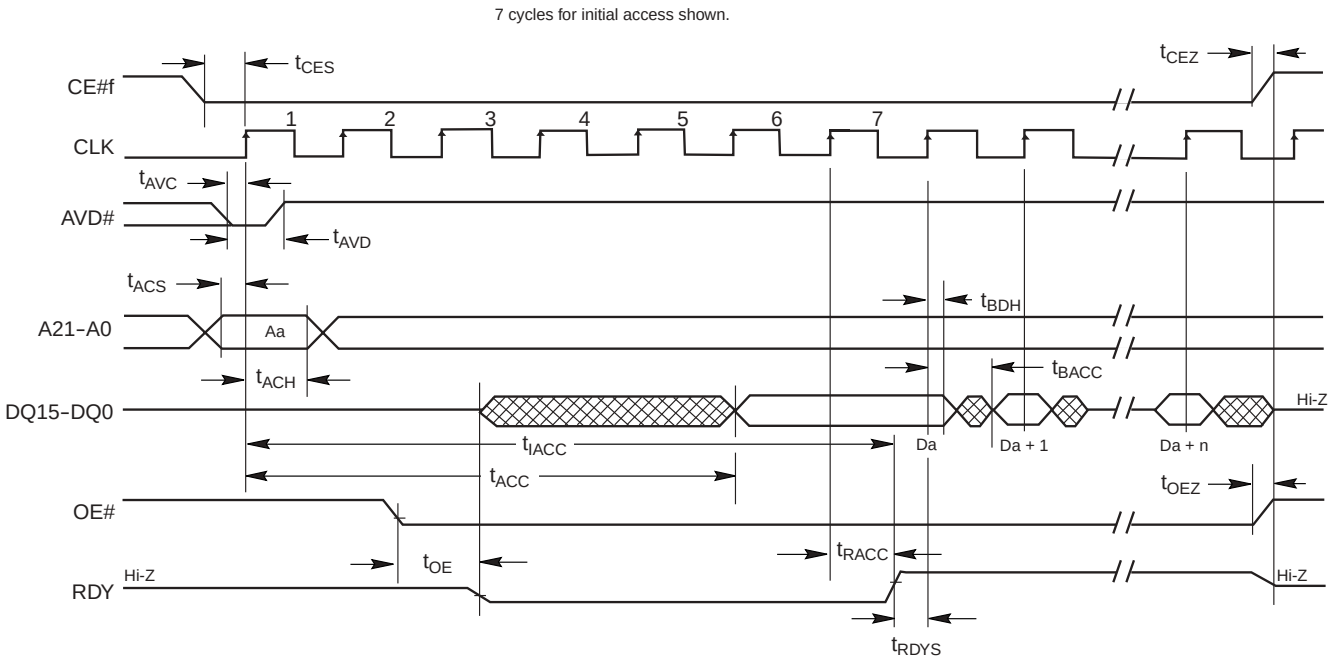
Synchronous/Burst Read

Parameter		Description		D8 (54 MHz)	C8 (40 MHz)	Unit
JEDEC	Standard					
	t_{IACC}	Latency (Even Address in Reduced Wait-State Handshaking Mode)	Max	87.5	95	ns
Parameter		**Description**		**D8, D9 (54 MHz)**	**C8, C9 (40 MHz)**	**Unit**
JEDEC	**Standard**					
	t_{IACC}	Latency—(Odd Address in Handshaking mode or Standard Handshaking)	Max	106	120	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	13.5	20	ns
	t_{ACS}	Address Setup Time to CLK (Note 1)	Min	5		ns
	t_{ACH}	Address Hold Time from CLK (Note 1)	Min	7		ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Max	4		ns
	t_{OE}	Output Enable to Output Valid	Max	13.5	20	ns
	t_{CEZ}	Chip Enable to High Z	Max	10		ns
	t_{OEZ}	Output Enable to High Z	Max	10		ns
	t_{CES}	CE# Setup Time to CLK	Min	5		ns
	t_{RDYS}	RDY Setup Time to CLK	Min	5		ns
	t_{RACC}	Ready Access Time from CLK	Max	13.5	20	ns
	t_{AAS}	Address Setup Time to AVD# (Note 1)	Min	5		ns
	t_{AAH}	Address Hold Time to AVD# (Note 1)	Min	7		ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0		ns
	t_{AVC}	AVD# Low to CLK	Min	5		ns
	t_{AVD}	AVD# Pulse	Min	12		ns
	t_{ACC}	Access Time	Max	70		ns

Note:

1. Addresses are latched on the first of either the active edge of CLK or the rising edge of AVD#.

AC CHARACTERISTICS

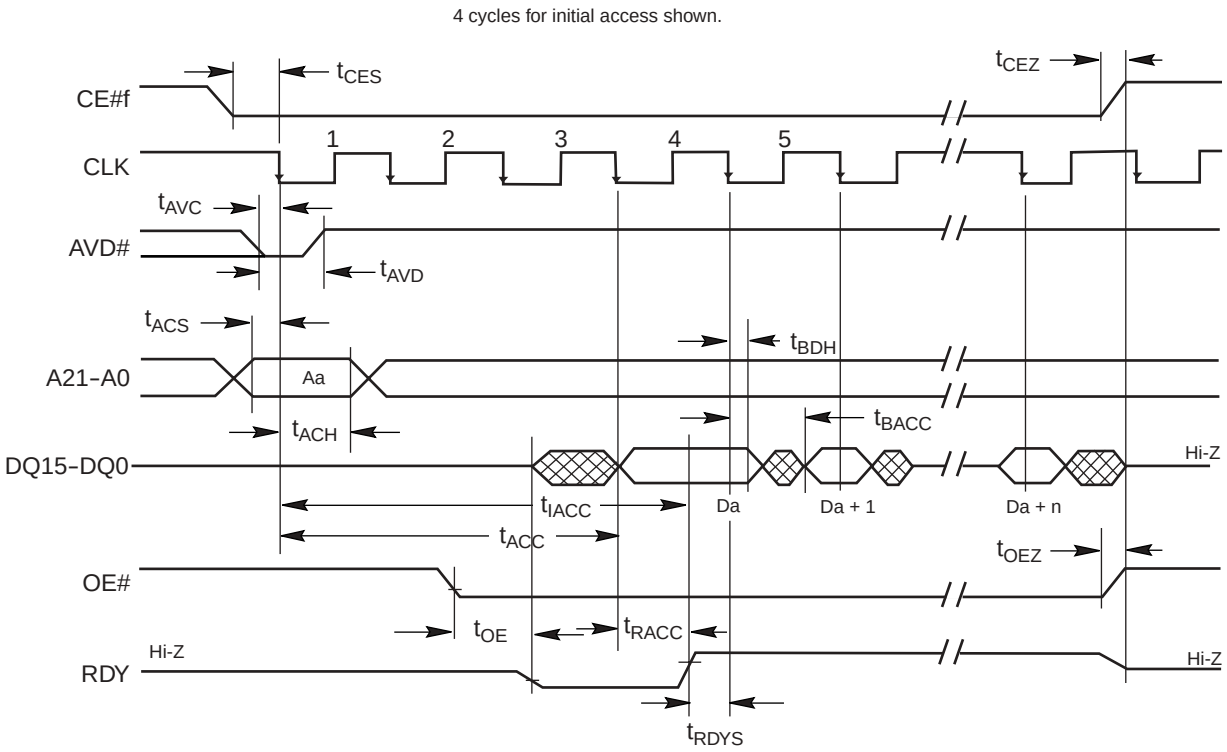


Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles.*
2. *If any burst address occurs at a 64-word boundary, one additional clock cycle is inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

Figure 11. CLK Synchronous Burst Mode Read (rising active CLK)

AC CHARACTERISTICS

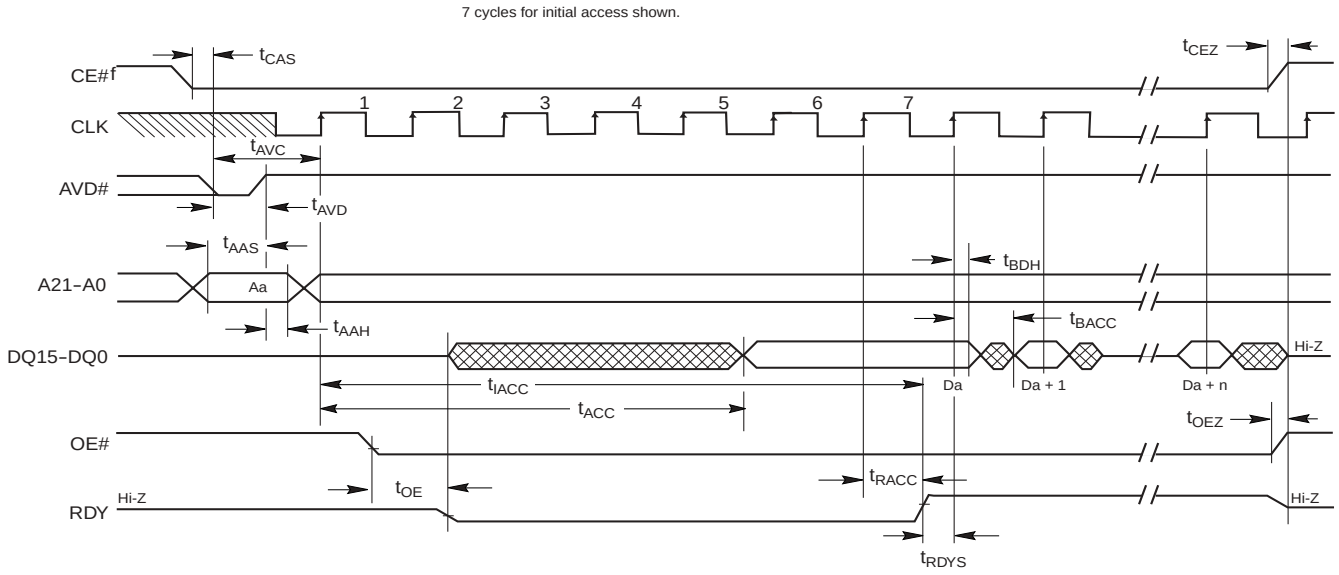


Notes:

1. *Figure shows total number of wait states set to four cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active falling edge.*
2. *If any burst address occurs at a 64-word boundary, one additional clock cycle is inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*
4. *A17 = 0.*

Figure 12. CLK Synchronous Burst Mode Read (Falling Active Clock)

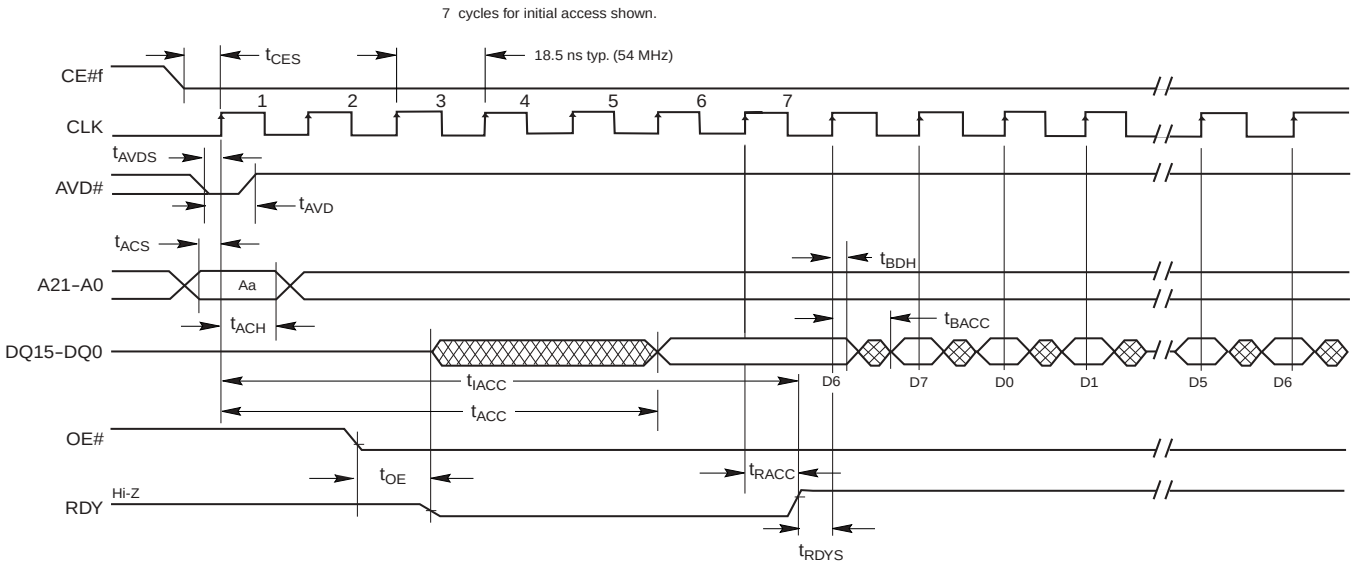
AC CHARACTERISTICS



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, one additional clock cycle is inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*
4. *A17 = 1.*

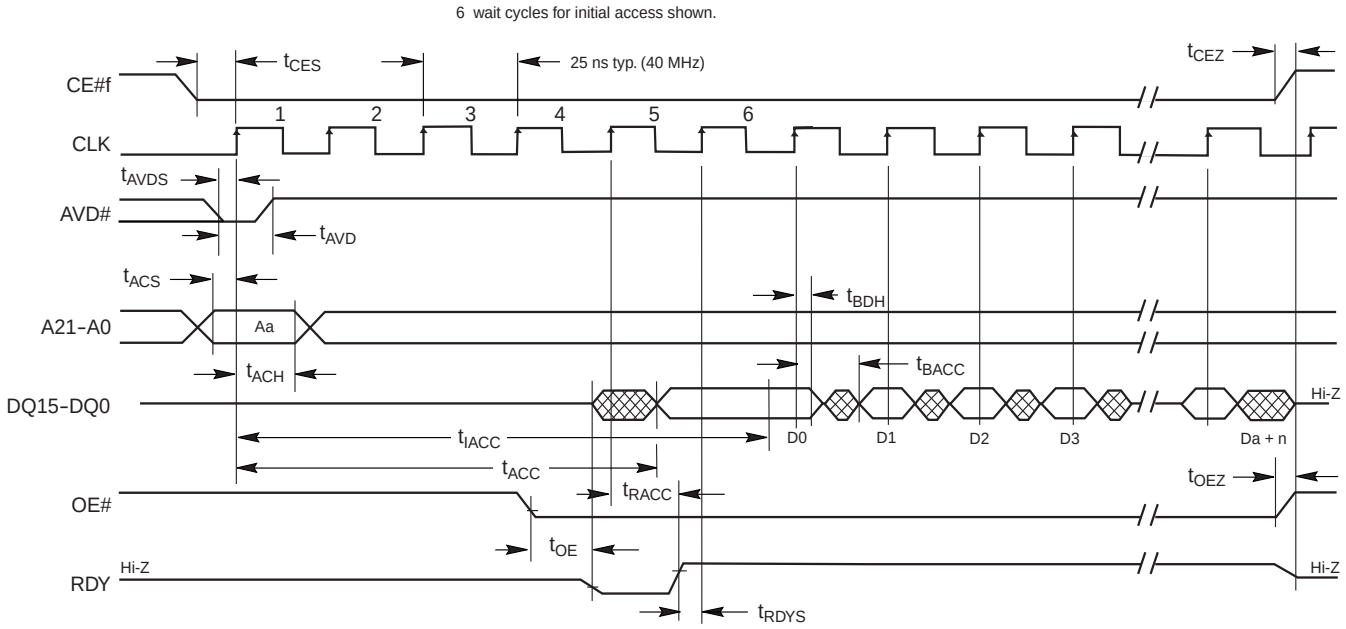
Figure 13. Synchronous Burst Mode Read



Note: *Figure assumes 7 wait states for initial access, 54 MHz clock, and automatic detect synchronous read. D0–D7 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Data will wrap around within the 8 words non-stop unless the RESET# is asserted low, or AVD# latches in another address. Starting address in figure is the 7th address in range (A6). See "Requirements for Synchronous (Burst) Read Operation". The Set Configuration Register command sequence has been written with A18=1; device will output RDY with valid data.*

Figure 14. 8-word Linear Burst with Wrap Around

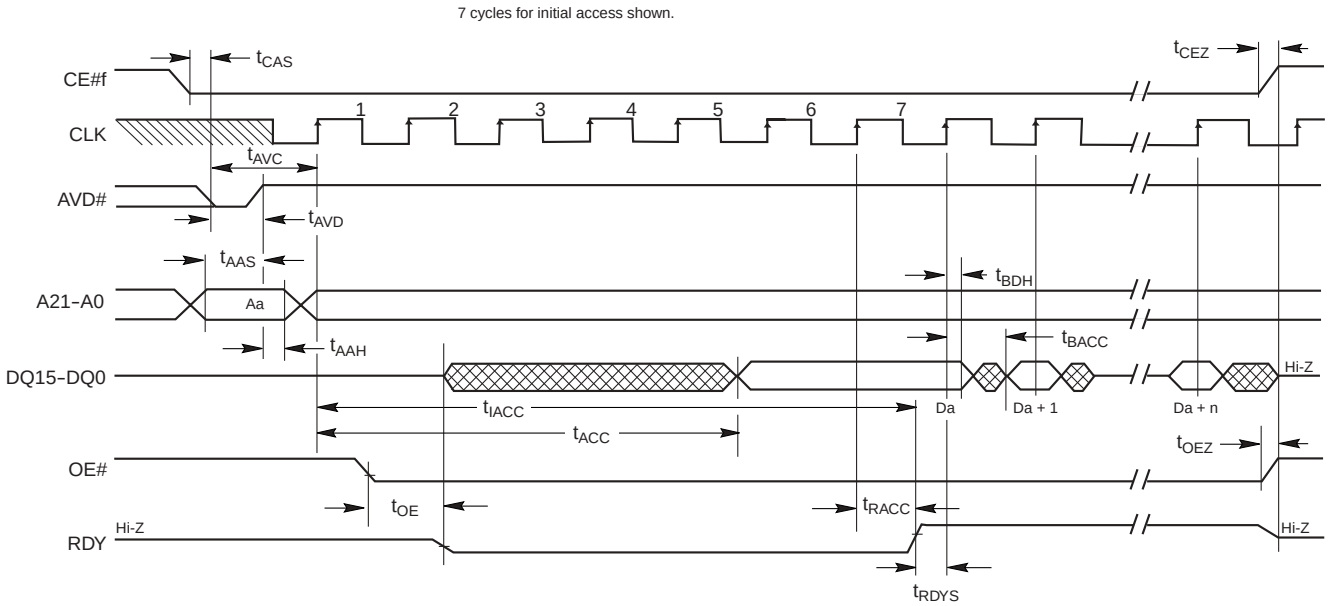
AC CHARACTERISTICS



Note: *Figure assumes 6 wait states for initial access, 40 MHz clock, and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY one cycle before valid data.*

Figure 15. Burst with RDY Set One Cycle Before Data

AC CHARACTERISTICS



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, one additional clock cycle is inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*
4. *This waveform represents a synchronous burst mode, the device will also operate in reduced wait-state handshaking under a CLK synchronous burst mode.*

Figure 16. Reduced Wait-State Handshaking Burst Mode Read Starting at an Even Address

AC CHARACTERISTICS

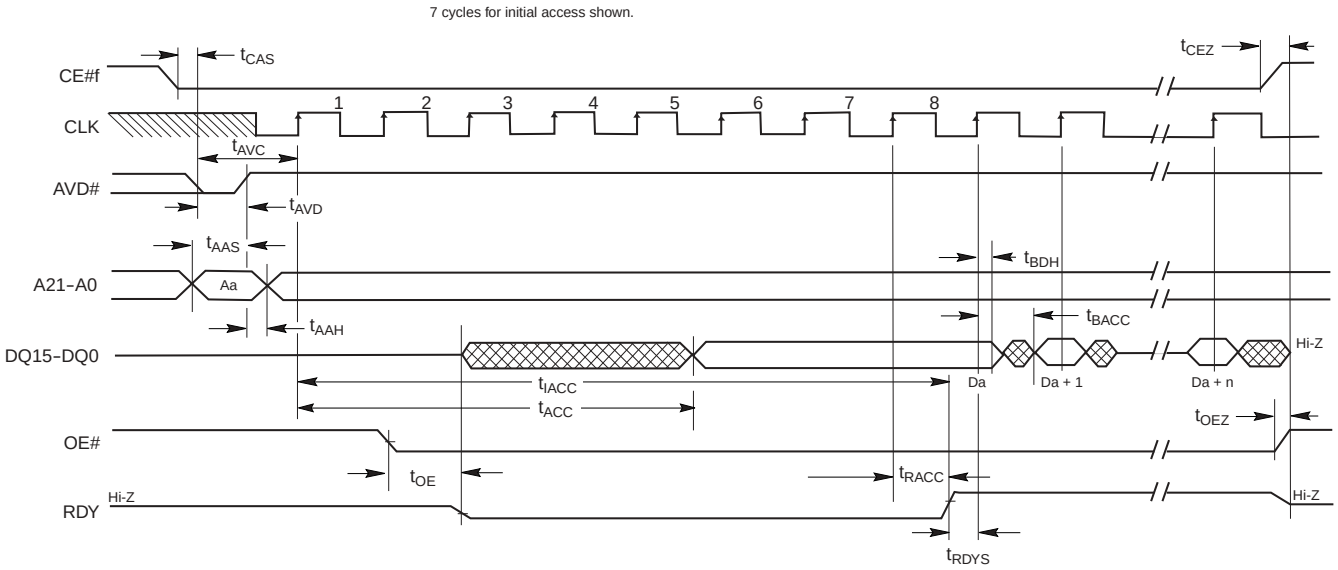


Figure 17. Reduced Wait-State Handshaking Burst Mode Read Starting at an Odd Address

Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, one additional clock cycle is inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*
4. *This waveform represents a synchronous burst mode, the device will also operate in reduced wait-state handshaking under a CLK synchronous burst mode.*

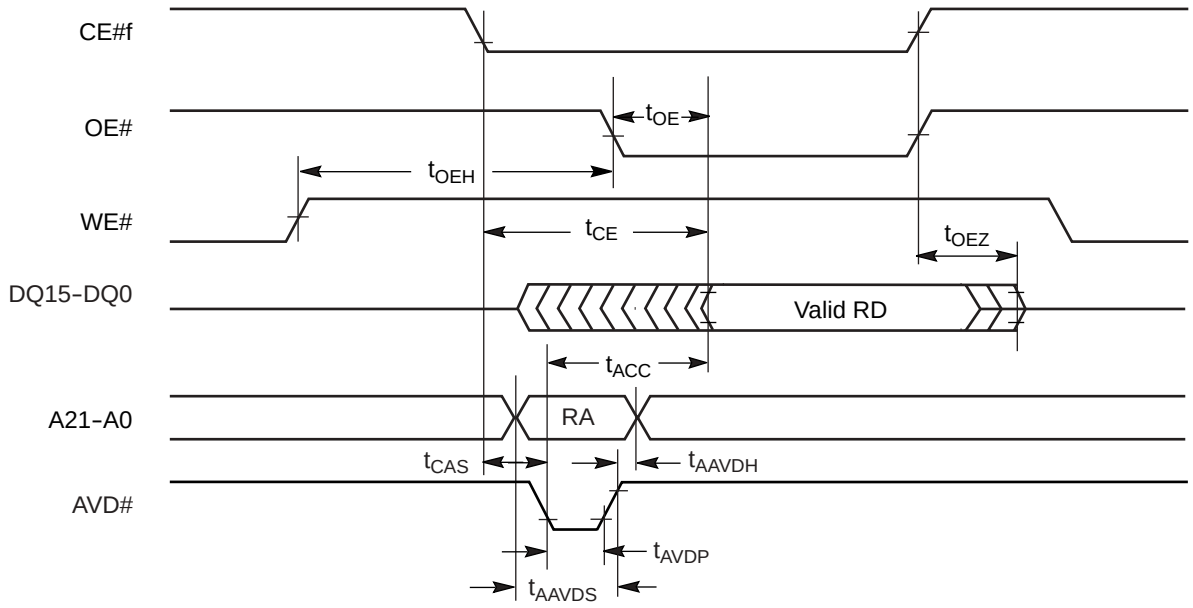
AC CHARACTERISTICS

Asynchronous Read

Parameter		Description			D8, D9 (54 MHz)	C8, C9 (40 MHz)	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	70	85	ns
	t_{ACC}	Asynchronous Access Time (Note 1)		Max	70	85	ns
	t_{AVDP}	AVD# Low Time		Min	12		ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	5		ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	7		ns
	t_{OE}	Output Enable to Output Valid		Max	13.5	20	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	10		ns
	t_{OEZ}	Output Enable to High Z (Note 2)		Max	10	10.5	ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0		ns

Notes:

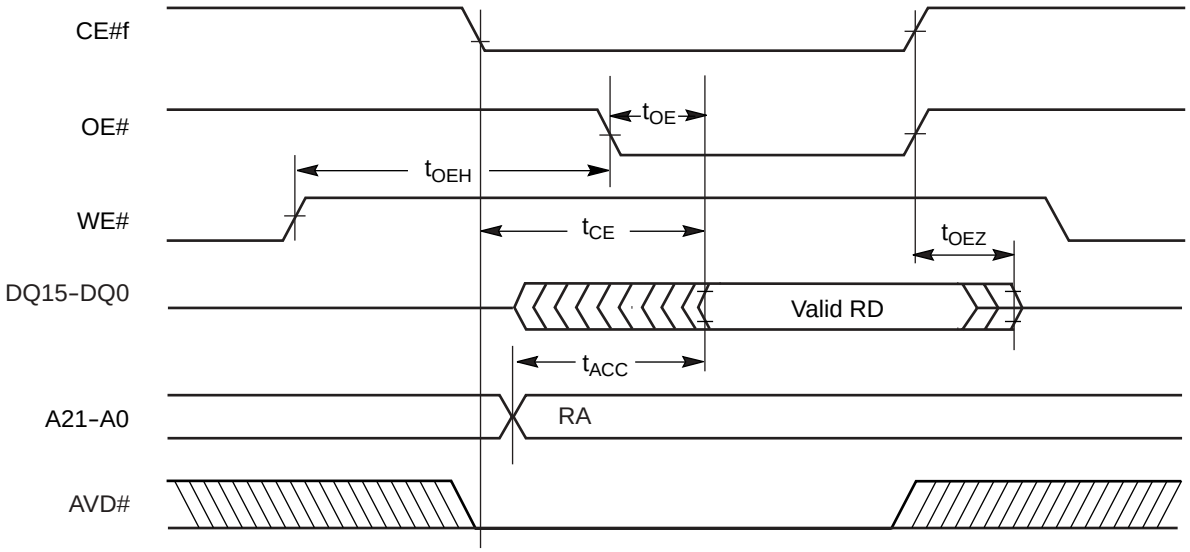
1. *Asynchronous Access Time is from the last of either stable addresses or the falling edge of AVD#.*
2. *Not 100% tested.*



Note: *RA = Read Address, RD = Read Data.*

Figure 18. Asynchronous Mode Read with Latched Addresses

AC CHARACTERISTICS



Note: *RA = Read Address, RD = Read Data.*

Figure 19. Asynchronous Mode Read

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Readyw}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	35	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

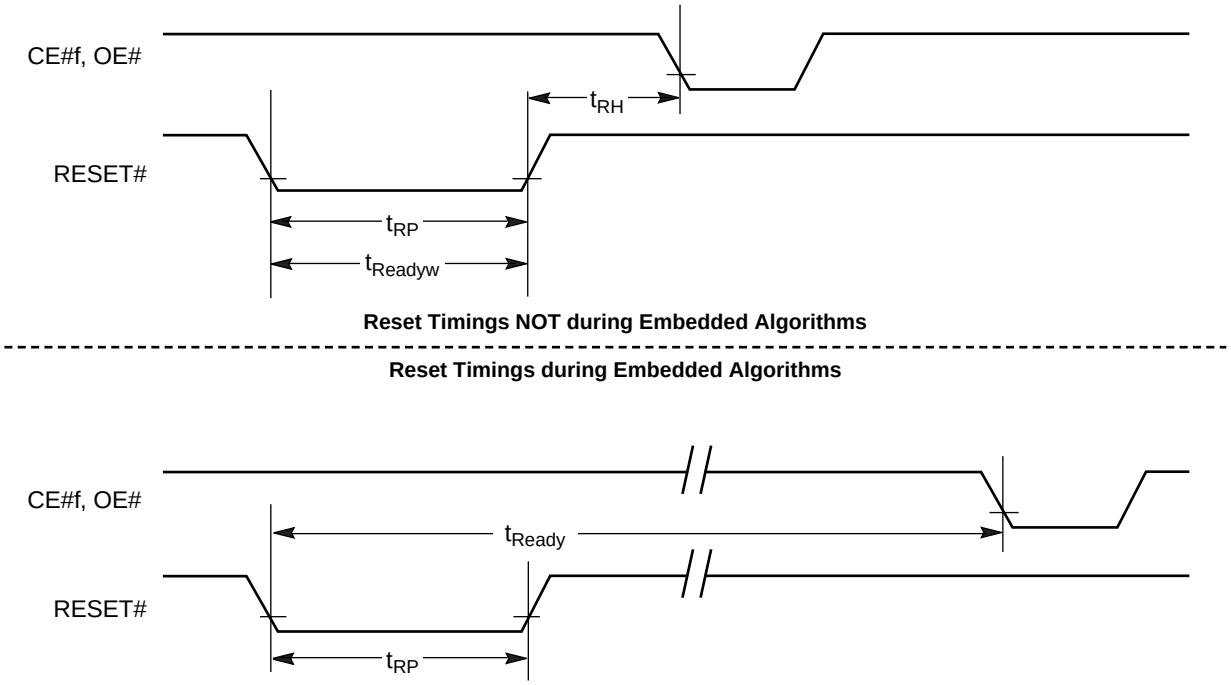


Figure 20. Reset Timings

AC CHARACTERISTICS

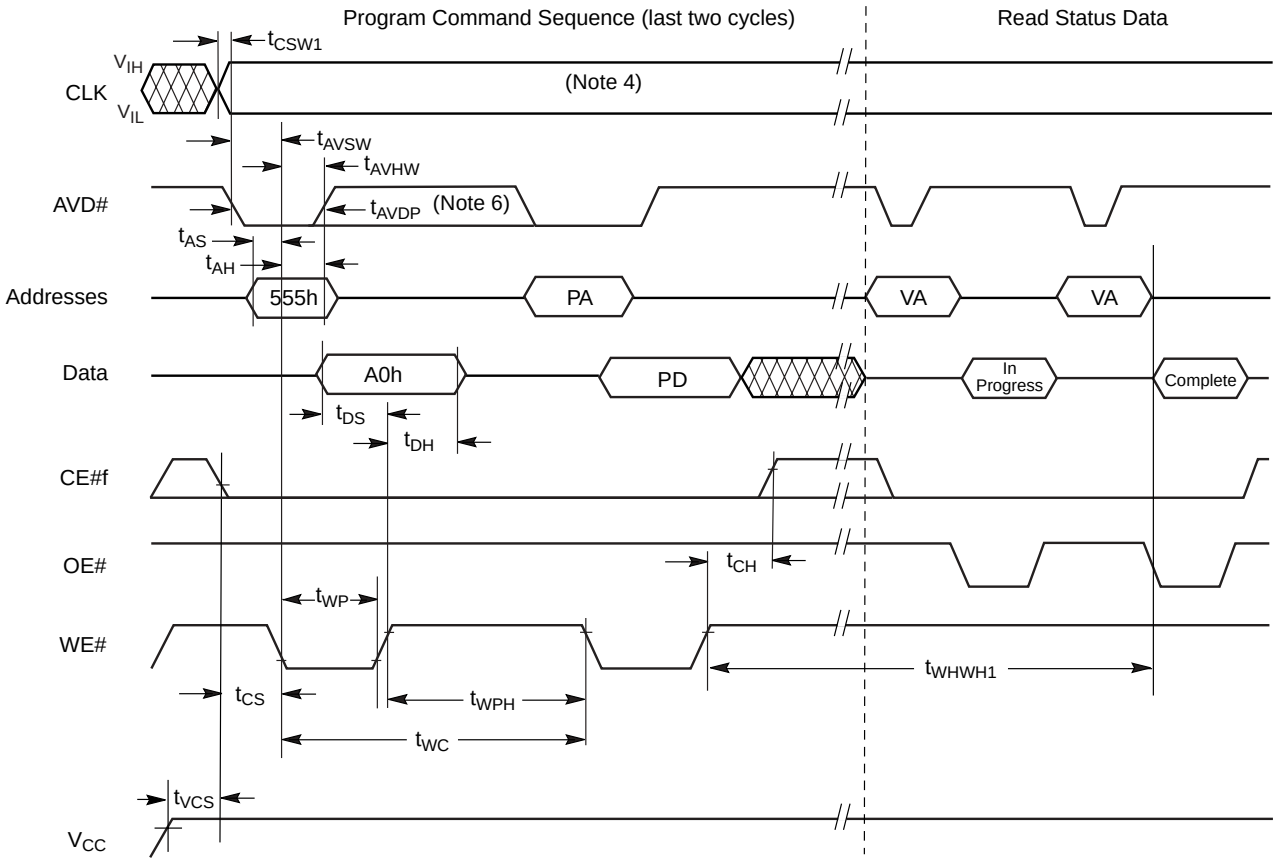
Erase/Program Operations

Parameter		Description			All Speed Options	Unit
JEDEC	Standard					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	80	ns
t_{AVWL}	t_{AS}	Address Setup Time (Note 2)	Synchronous	Min	5	ns
			Asynchronous		0	
t_{WLAX}	t_{AH}	Address Hold Time (Note 2)	Synchronous	Min	7	ns
			Asynchronous		45	
	t_{ACS}	Address Setup Time to CLK (Note 2)		Min	5	ns
	t_{ACH}	Address Hold Time to CLK (Note 2)		Min	7	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0	ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 3)		Typ	8	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 3)		Typ	2.5	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 3, 4)		Typ	0.2	sec
		Chip Erase Operation (Notes 3, 4)			26.8	
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500	ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1	µs
	t_{VCS}	V_{CC} Setup Time		Min	50	µs
	t_{CSW1}	Clock Setup Time to WE# (Asynchronous)		Min	5	ns
	t_{CSW2}	Clock Setup Time to WE# (Synchronous)		Min	1	ns
	t_{CHW}	Clock Hold Time from WE#		Min	1	ns
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	0	ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	5	ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	5	ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	5	ns
	t_{AVDP}	AVD# Low Time		Min	12	ns

Notes:

1. *Not 100% tested.*
2. *In asynchronous timing, addresses are latched on the falling edge of WE#. In synchronous mode, addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
3. *See the "Flash Erase And Programming Performance" section for more information.*
4. *Does not include the preprogramming time.*

AC CHARACTERISTICS

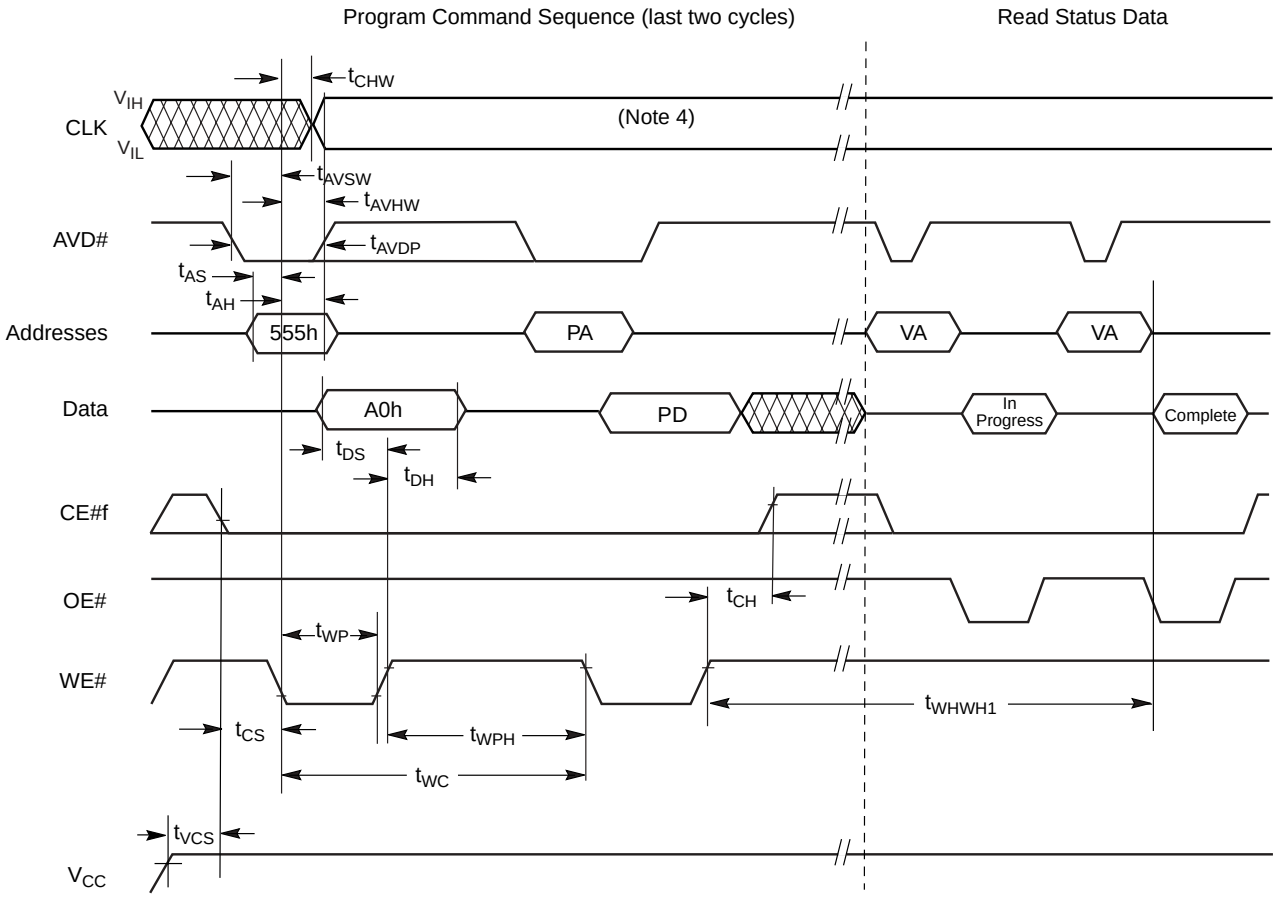


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.*
6. *AVD# must toggle during command sequence if CLK is at V_{IH}.*

Figure 21. Asynchronous Program Operation Timings

AC CHARACTERISTICS

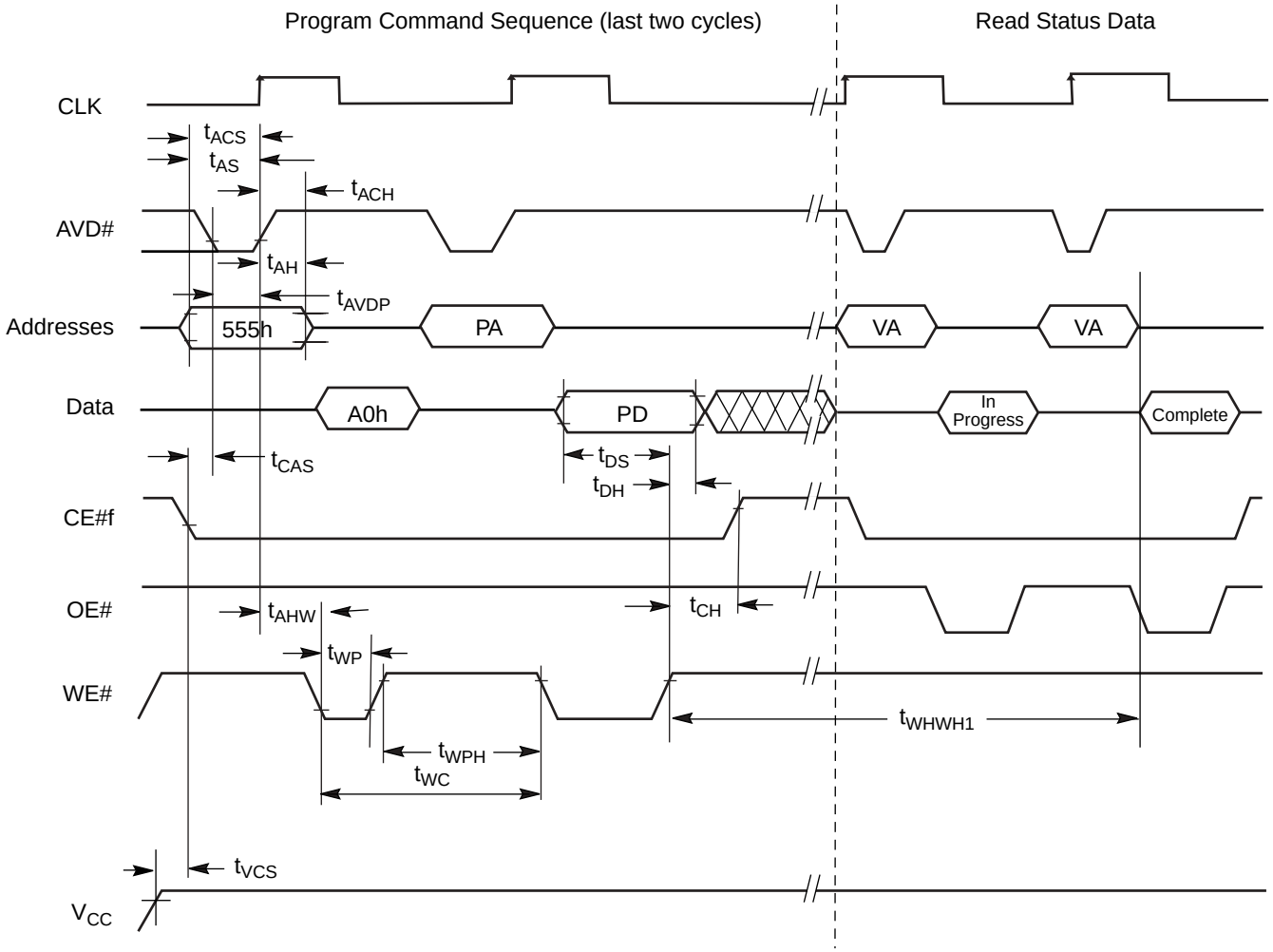


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.*
6. *AVD# must toggle during command sequence if CLK is at V_{IH}.*

Figure 22. Alternate Asynchronous Program Operation Timings

AC CHARACTERISTICS

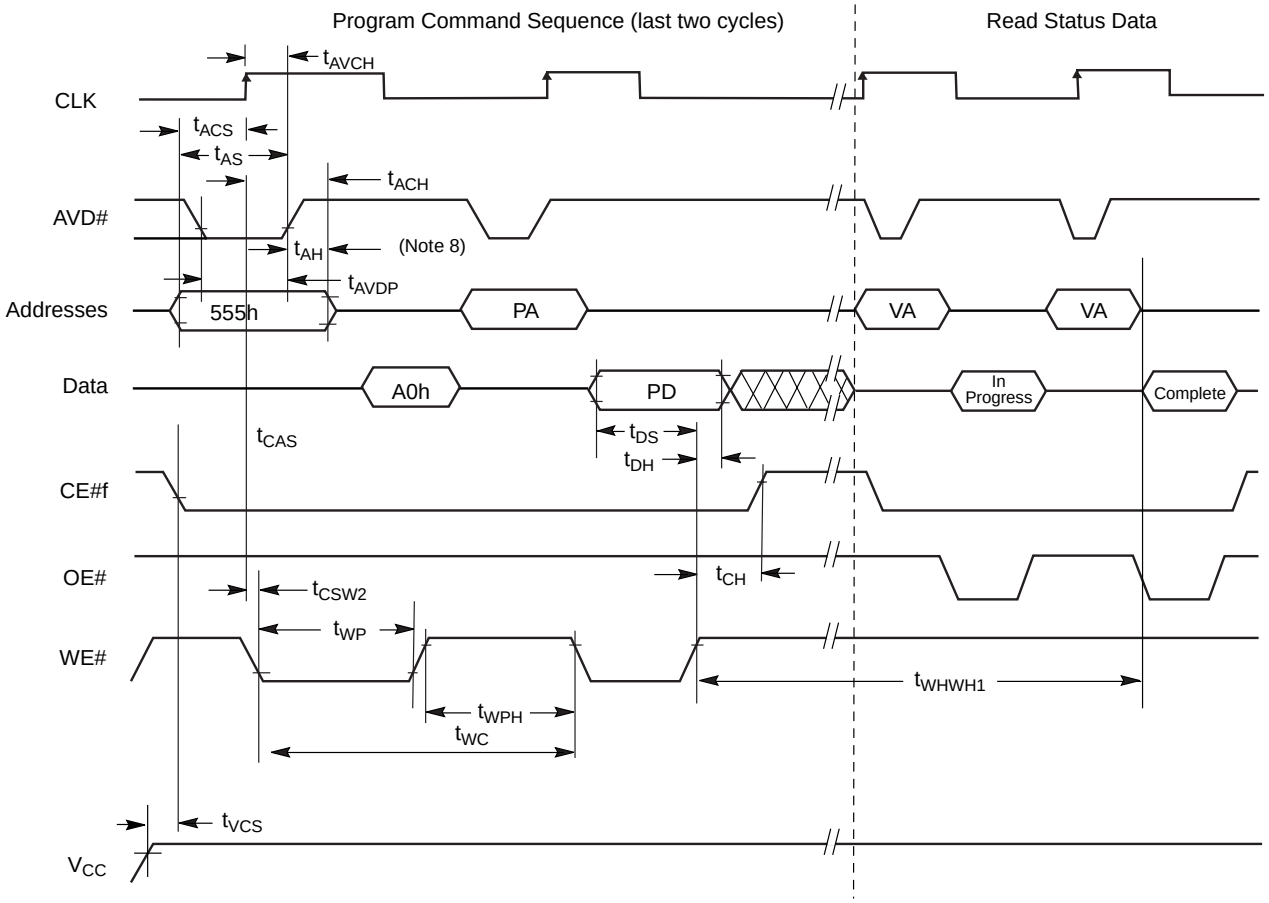


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CS# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.*
7. *CLK must not have an active edge while WE# is at V_{IL}.*
8. *AVD# must toggle during command sequence unlock cycles.*

Figure 23. Synchronous Program Operation Timings

AC CHARACTERISTICS



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CS# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.*
7. *AVD# must toggle during command sequence unlock cycles.*
8. *t_{AH} = 45 ns.*
9. *CLK must not have an active edge while WE# is at V_{IL}.*

Figure 24. Alternate Synchronous Program Operation Timings

AC CHARACTERISTICS

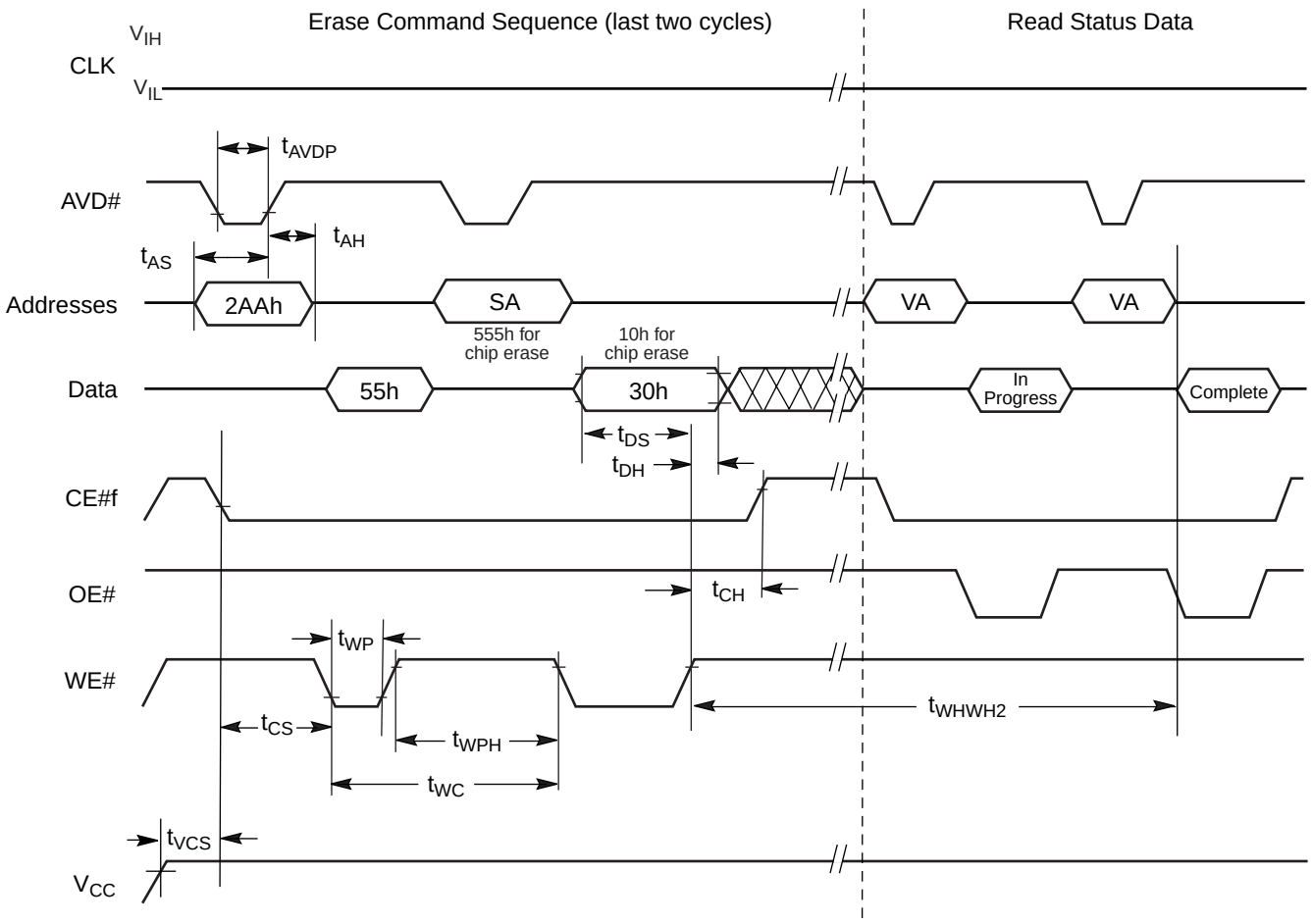
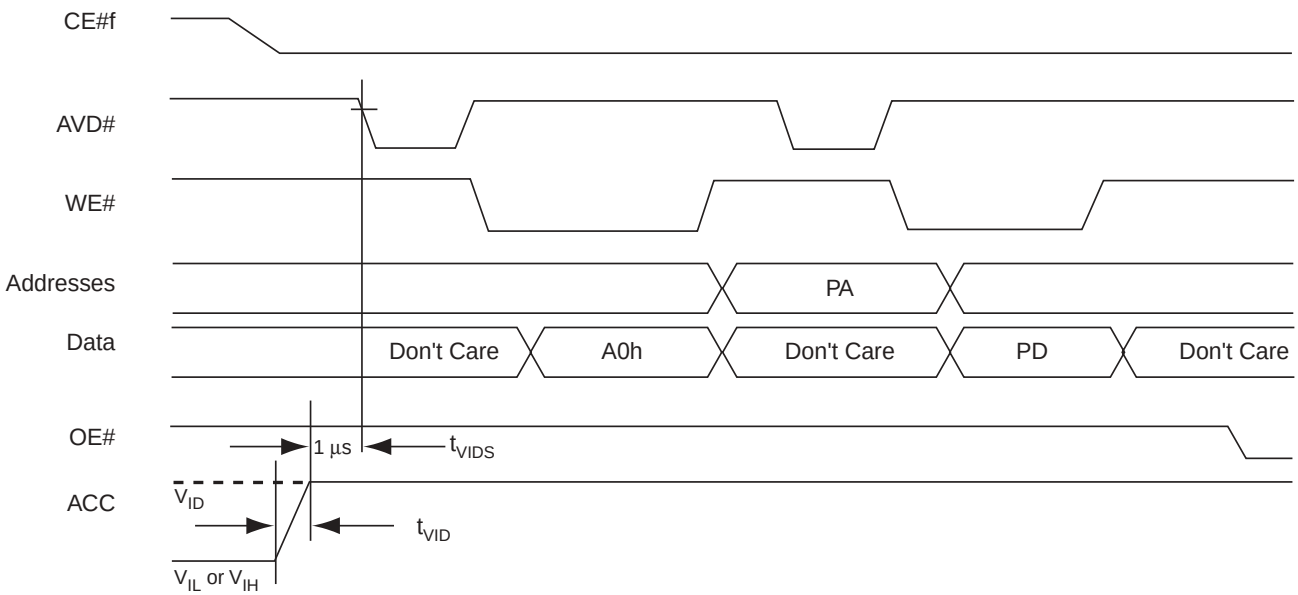


Figure 25. Chip/Sector Erase Command Sequence

Notes:

1. *SA is the sector address for Sector Erase.*
2. *Address bits A21–A12 are don't cares during unlock cycles in the command sequence.*

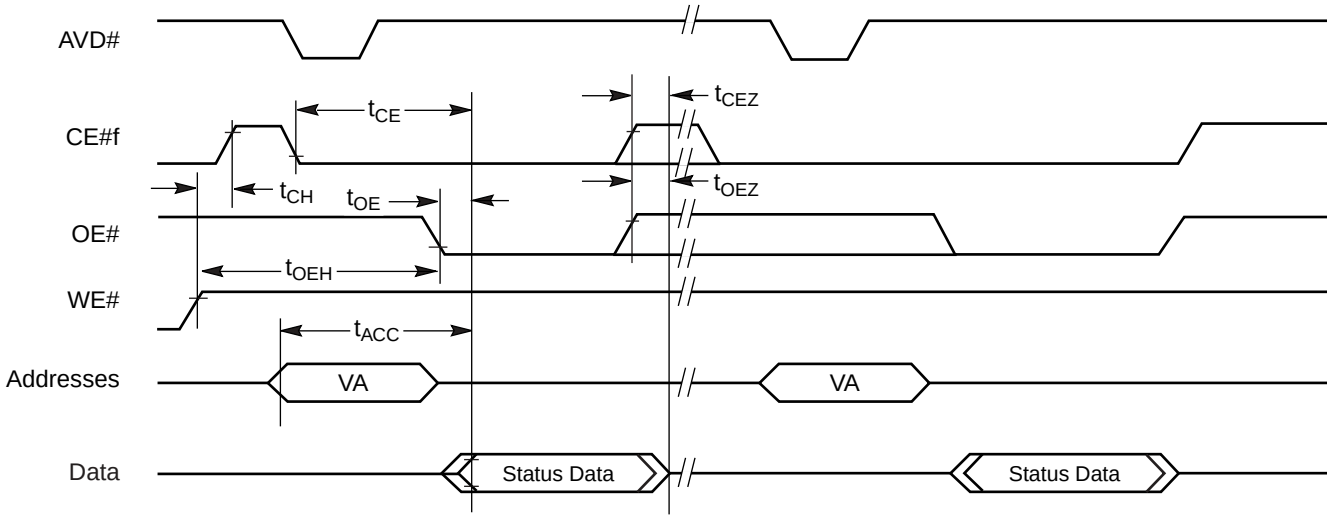
AC CHARACTERISTICS



Note: *Use setup and hold times from conventional program operation.*

Figure 26. Accelerated Unlock Bypass Programming Timing

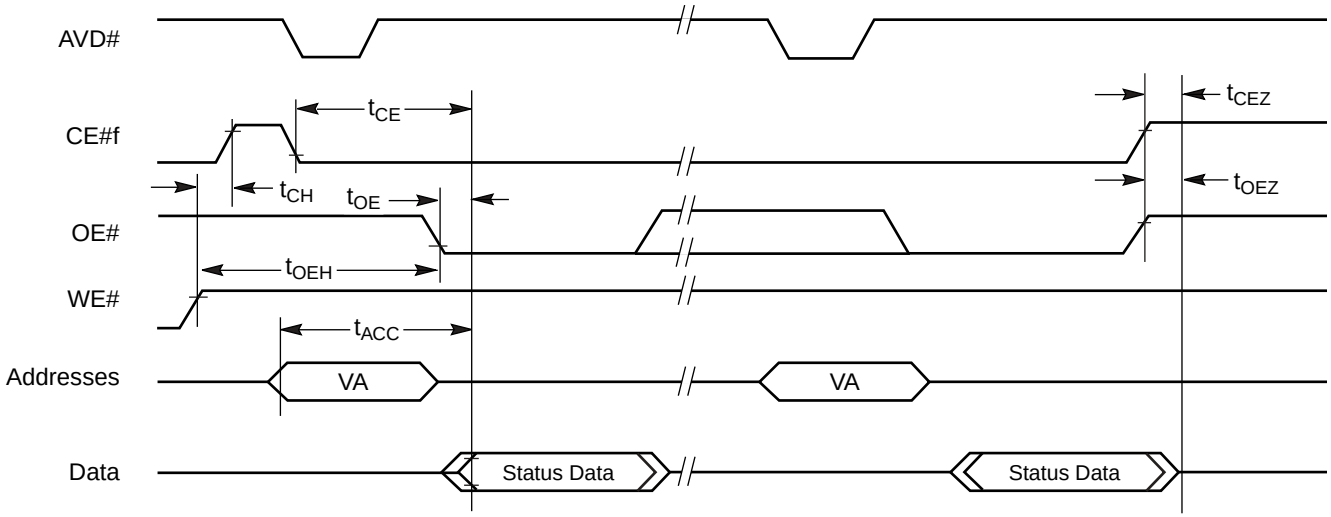
AC CHARACTERISTICS



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*
3. *AVD# must toggle between data reads.*

Figure 27. Data# Polling Timings (During Embedded Algorithm)

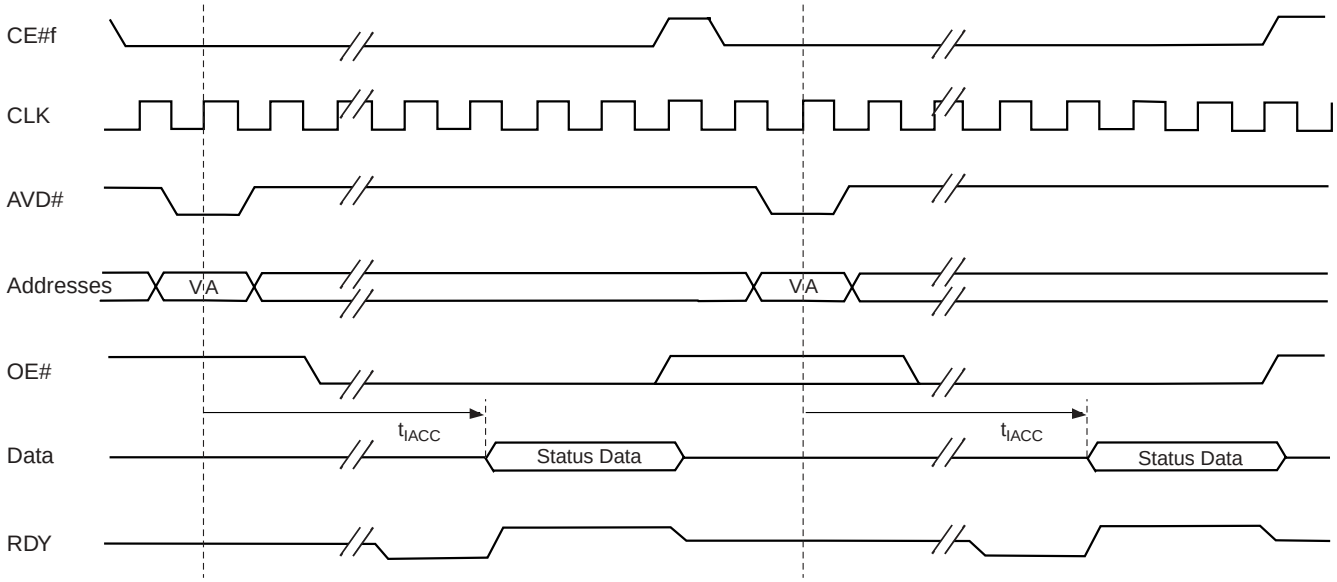


Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *AVD# must toggle between data reads.*

Figure 28. Toggle Bit Timings (During Embedded Algorithm)

AC CHARACTERISTICS

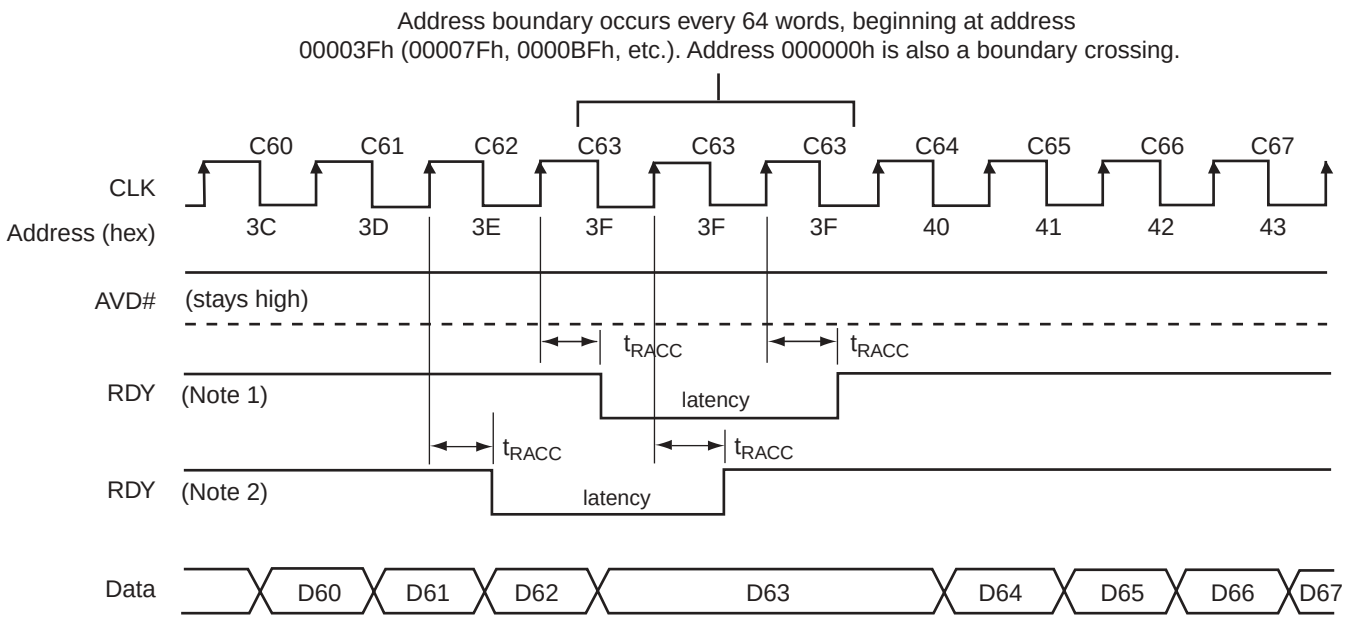


Notes:

1. *The timings are similar to synchronous read timings.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *RDY is active with data (A18 = 0 in the Burst Mode Configuration Register). When A18 = 1 in the Burst Mode Configuration Register, RDY is active one clock cycle before data.*
4. *AVD# must toggle between data reads.*

Figure 29. Synchronous Data Polling Timings/Toggle Bit Timings

AC CHARACTERISTICS)

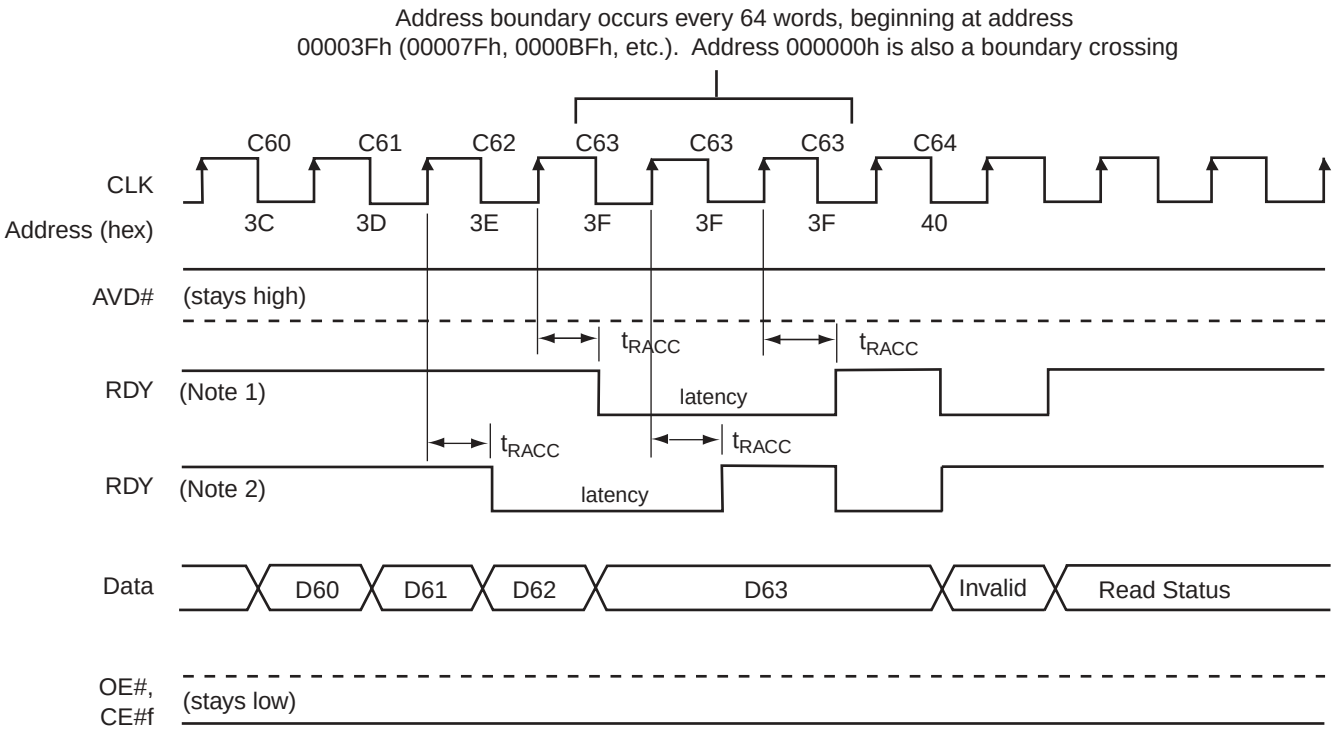


Notes:

1. *RDY active with data (A18 = 0 in the Burst Mode Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Burst Mode Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device not crossing a bank in the process of performing an erase or program.*

Figure 30. Latency with Boundary Crossing

AC CHARACTERISTICS

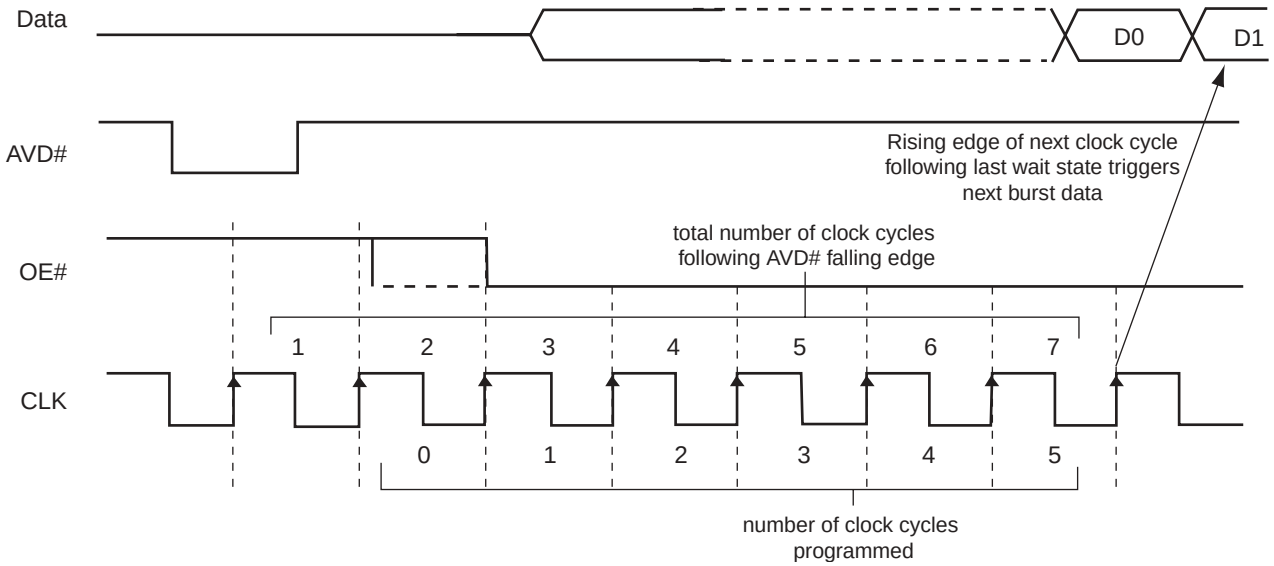


Notes:

1. *RDY active with data (A18 = 0 in the Burst Mode Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Burst Mode Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device crossing a bank in the process of performing an erase or program.*

Figure 31. Latency with Boundary Crossing into Program/Erase Bank

AC CHARACTERISTICS

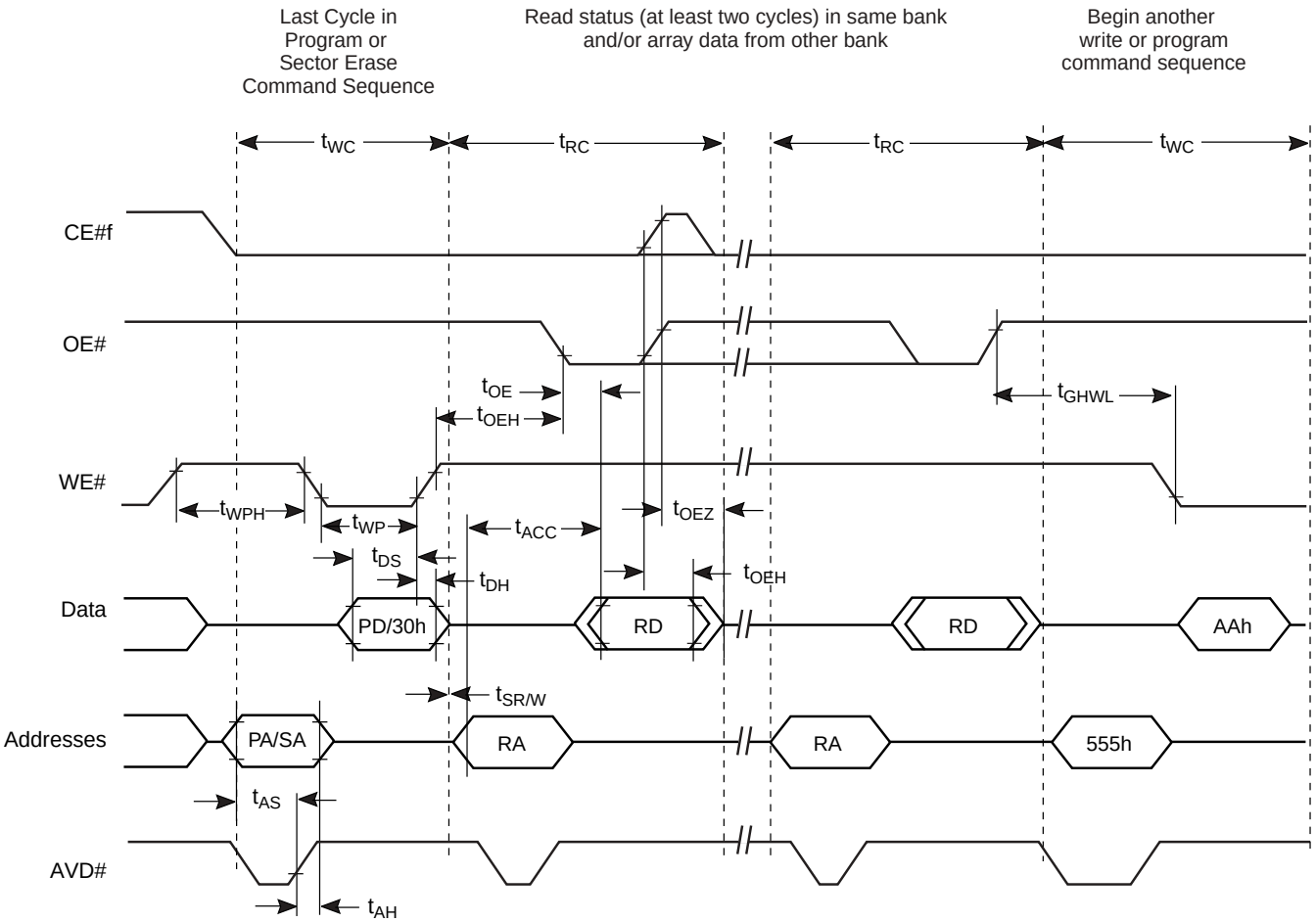


Wait State Decoding Addresses:
A14, A13, A12 = "101" ⇒ 5 programmed, 7 total
A14, A13, A12 = "100" ⇒ 4 programmed, 6 total
A14, A13, A12 = "011" ⇒ 3 programmed, 5 total
A14, A13, A12 = "010" ⇒ 2 programmed, 4 total
A14, A13, A12 = "001" ⇒ 1 programmed, 3 total
A14, A13, A12 = "000" ⇒ 0 programmed, 2 total

Note: *Figure assumes address D0 is not at an address boundary, active clock edge is rising, and wait state is set to "101".*

Figure 32. Example of Wait States Insertion (Standard Handshaking Device)

AC CHARACTERISTICS



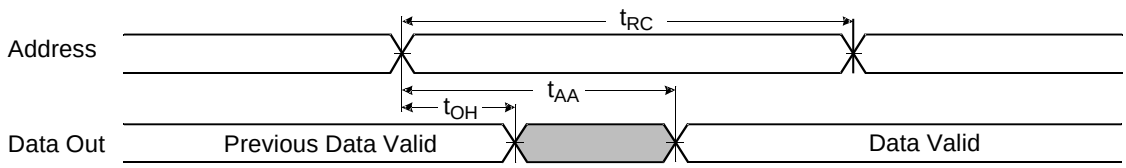
Note: *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

Figure 33. Back-to-Back Read/Write Cycle Timings

SRAM AC CHARACTERISTICS

Read Cycle

Parameter Symbol	Description		D8, D9 (54 MHz)	C8, C9 (40 MHz)	Unit
t_{RC}	Read Cycle Time	Min	70	85	ns
t_{AA}	Address Access Time	Max	70	85	ns
t_{CO1}, t_{CO2}	Chip Enable to Output	Max	70	85	ns
t_{OE}	Output Enable Access Time	Max	35	40	ns
t_{BA}	LB#s, UB#s to Access Time	Max	70	85	ns
t_{LZ1}, t_{LZ2}	Chip Enable (CE1#s Low and CE2s High) to Low-Z Output	Min	10		ns
t_{BLZ}	UB#, LB# Enable to Low-Z Output	Min	10		ns
t_{OLZ}	Output Enable to Low-Z Output	Min	5		ns
t_{HZ1}, t_{HZ2}	Chip Disable to High-Z Output	Max	25		ns
t_{BHZ}	UB#s, LB#s Disable to High-Z Output	Max	25		ns
t_{OHZ}	Output Disable to High-Z Output	Max	25		ns
t_{OH}	Output Data Hold from Address Change	Min	10		ns



Note: *CE1#s = OE# = V_{IL}, CE2s = WE# = V_{IH}, UB#s and/or LB#s = V_{IL}*

Figure 34. SRAM Read Cycle—Address Controlled

SRAM AC CHARACTERISTICS

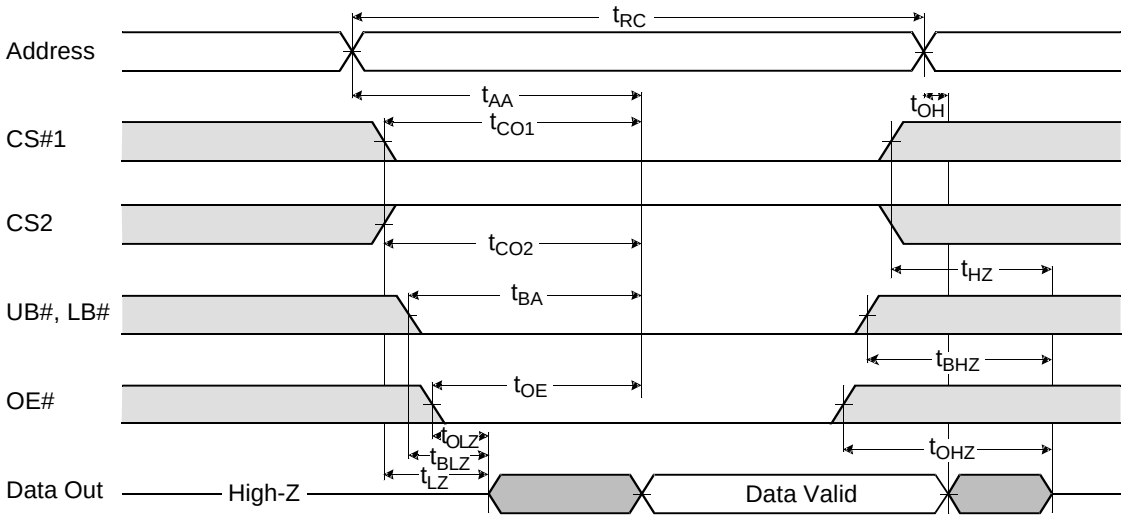


Figure 35. SRAM Read Cycle

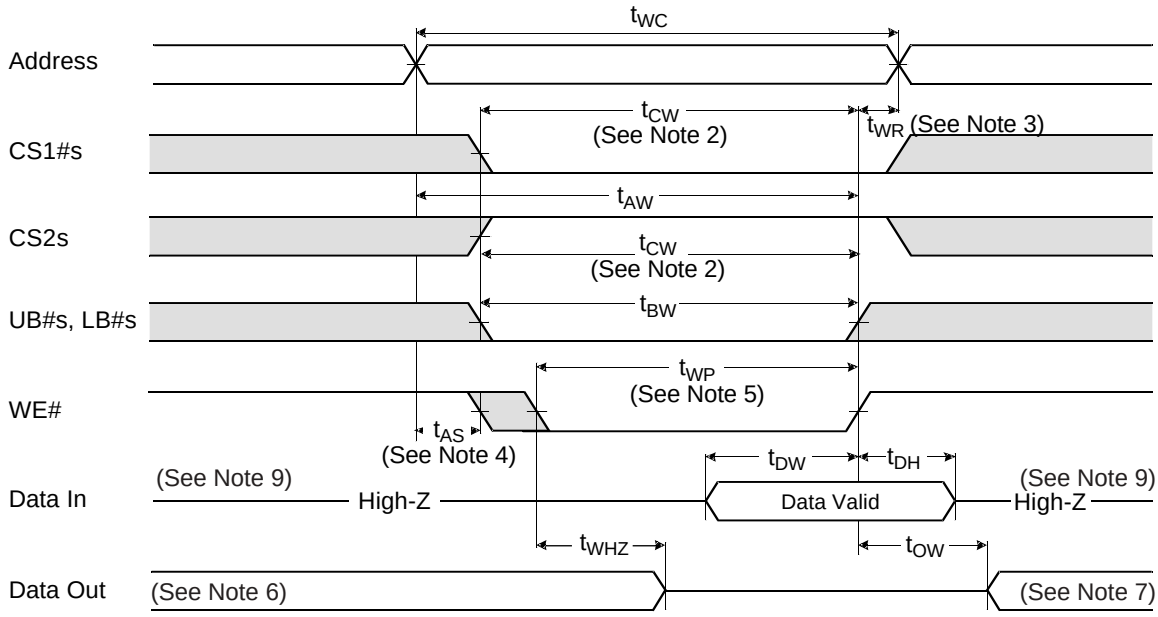
Notes:

1. *WE# = V_{IH}.*
2. *t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
3. *At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device interconnection.*

SRAM AC CHARACTERISTICS

Write Cycle

Parameter Symbol	Description		D8, D9 (54 MHz)	C8, C9 (40 MHz)	Unit
t_{WC}	Write Cycle Time	Min	70	85	ns
t_{Cw}	Chip Enable to End of Write	Min	60	70	ns
t_{AS}	Address Setup Time	Min	0		ns
t_{AW}	Address Valid to End of Write	Min	60	70	ns
t_{BW}	UB#s, LB#s to End of Write	Min	60	70	ns
t_{WP}	Write Pulse Time	Min	50	60	ns
t_{WR}	Write Recovery Time	Min	0		ns
t_{WHZ}	Write to Output High-Z	Min	0		ns
		Max	20		
t_{DW}	Data to Write Time Overlap	Min	30		ns
t_{DH}	Data Hold from Write Time	Min	0		ns
t_{OW}	End Write to Output Low-Z	min	5		ns

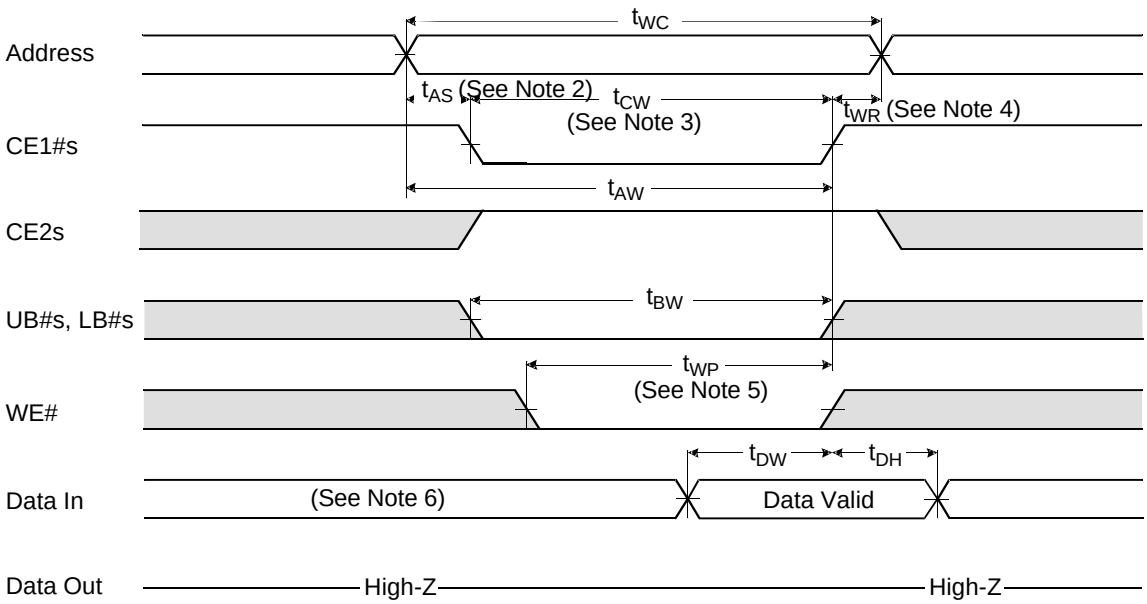


Notes:

1. *WE# controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 36. SRAM Write Cycle—WE# Control

SRAM AC CHARACTERISTICS

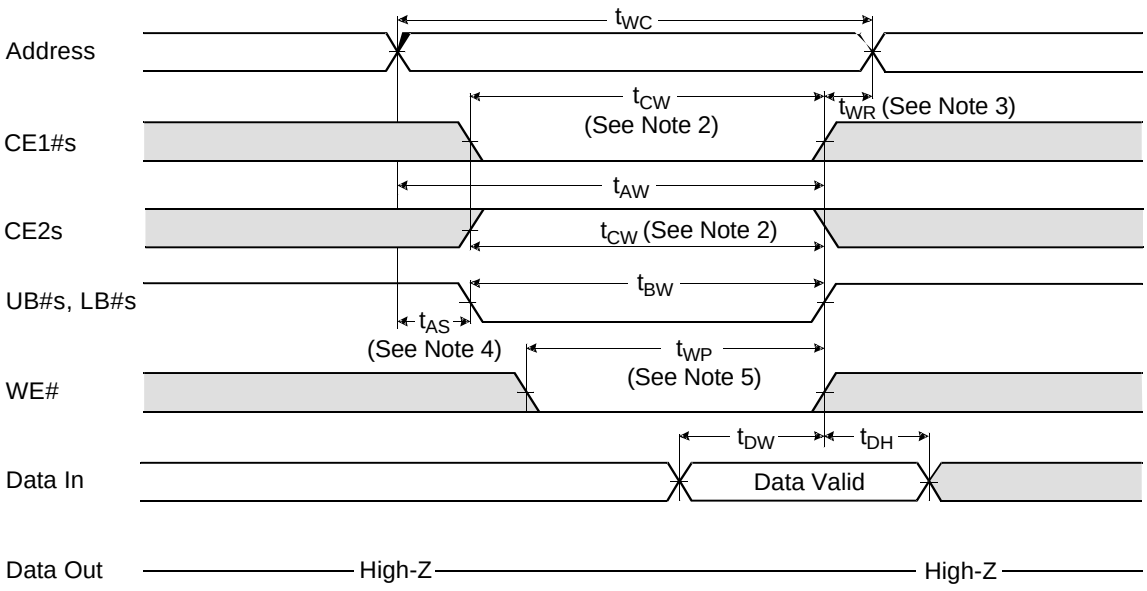


Notes:

1. *CE1#s controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 37. SRAM Write Cycle—CE1#s Control

SRAM AC CHARACTERISTICS



Notes:

1. *UB#s and LB#s controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 38. SRAM Write Cycle—UB#s and LB#s Control

FLASH ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time (32 Kword or 8 Kword)	0.4	5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	54		sec	
Word Program Time	11.5	210	µs	Excludes system level overhead (Note 5)
Accelerated Word Program Time	4	120	µs	
Chip Program Time (Note 3)	48	144	sec	
Accelerated Chip Program Time	16	48	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 2.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.8 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 14 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

FLASH LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

PACKAGE PIN CAPACITANCE

Parameter Symbol	Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	11	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	16	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	14	16	pF
C_{IN3}	WP#/ACC Pin Capacitance	V_{IN} = 0	17	20	pF

Note: *Test conditions T_A = 25°C, f = 1.0 MHz.*

FLASH DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

SRAM DATA RETENTION

Parameter Symbol	Parameter Description	Test Setup	Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	CS1#s ≥ V_{CC} – 0.2 V (Note 1)	1.0		2.2	V
I_{DR}	Data Retention Current	V_{CC} = 1.2 V, CE1#s ≥ V_{CC} – 0.2 V (Note 1)		1.0 (Note 2)	8	µA
t_{SDR}	Data Retention Set-Up Time	See data retention waveforms	0			ns
t_{RDR}	Recovery Time		t_{RC}			ns

Notes:

1. *CE1#s ≥ V_{CC} – 0.2 V, CE2s ≥ V_{CC} – 0.2 V (CE1#s controlled) or CE2s ≤ 0.2 V (CE2s controlled).*
2. *Typical values are not 100% tested.*

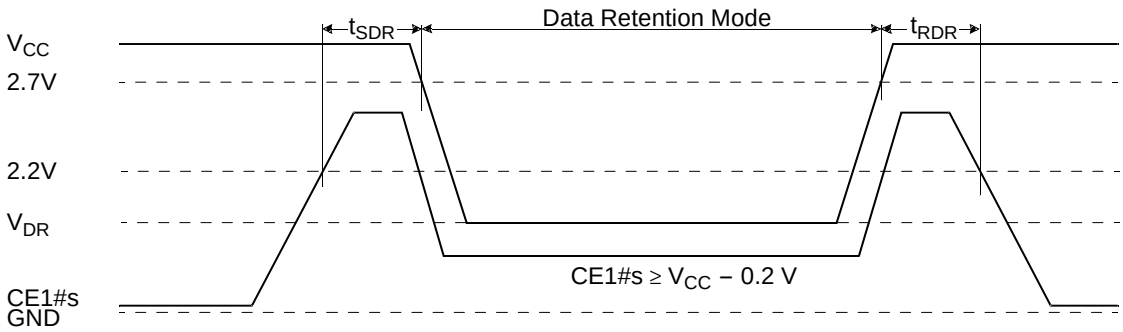


Figure 39. CE1#s Controlled Data Retention Mode

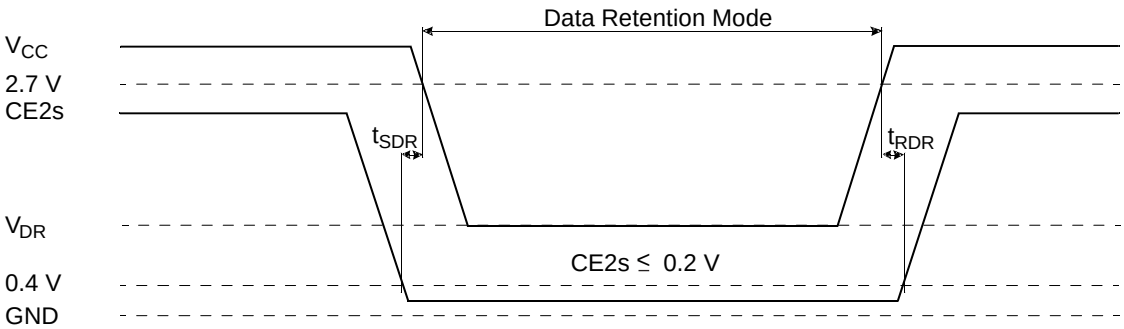
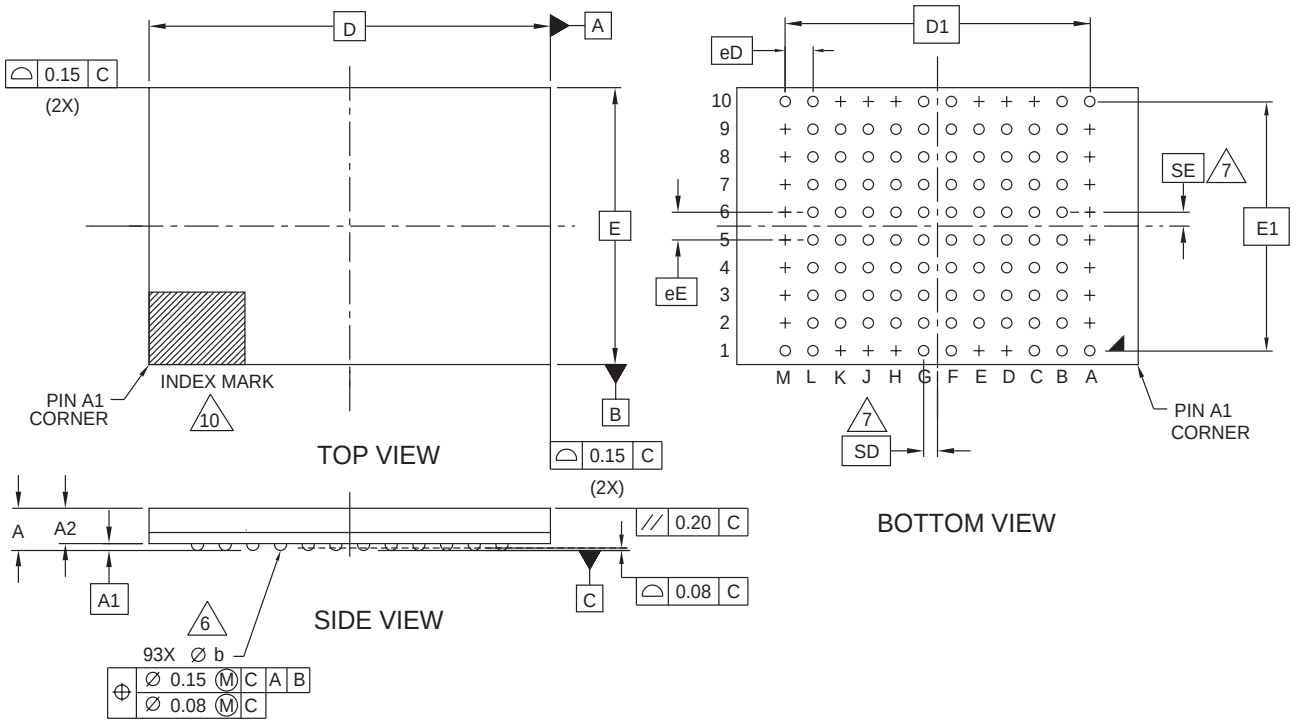


Figure 40. CE2s Controlled Data Retention Mode

PHYSICAL DIMENSIONS

FSC093—93-Ball Fine-Pitch Grid Array 8 x 11.6 mm



PACKAGE	FSC 093			NOTE
JEDEC	N/A			
	8.00 mm x 11.60 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	---	---	1.40	PROFILE
A1	0.25	---	---	BALL HEIGHT
A2	1.00	---	1.10	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		93		BALL COUNT
øb	0.30	0.35	0.40	BALL DIAMETER
eE		0.80 BSC		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD/SE		0.40 BSC		SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 C10,D1,D10,E1,E10,H1,H10 J1,J10,K1,K10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALL

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTION OR OTHER MEANS.

3187\38.14A

REVISION SUMMARY

Revision A (May 20, 2002)

Initial release.

Revision B (November 1, 2002)

Global

Renamed Non-Handshaking to Standard Handshaking.

Renamed Handshaking Enabled to Reduced Wait-state Handshaking.

Product Selector Guide

Revised with renamed speed options and added Synchronous Access Time with Reduced Wait-state Handshaking.

Added Asynchronous Access Time

Ordering Information

Revised with global changes

Revised Valid Combinations with updated ordering information.

Trademarks

Copyright © 2002 Advanced Micro Devices, Inc. All rights reserved.

AMD, the AMD logo, and combinations thereof are registered trademarks of Advanced Micro Devices, Inc.

ExpressFlash is a trademark of Advanced Micro Devices, Inc.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.