# Am29SLI60C

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

## Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

## Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

## For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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# Am29SL160C

## 16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 1.8 Volt-only Super Low Voltage Flash Memory

## DISTINCTIVE CHARACTERISTICS

### ARCHITECTURAL ADVANTAGES

- **Secured Silicon (SecSi) Sector: 256-byte sector**
  - — *Factory locked and identifiable:* 16 bytes available for secure, random factory Electronic Serial Number; verifiable as factory locked through autoselect function. ExpressFlash option allows entire sector to be available for factory-secured data
  - — *Customer lockable:* Customer may program own custom data. Once locked, data cannot be changed
- **Zero Power Operation**
  - — Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero
- **Package options**
  - — 48-ball FBGA
  - — 48-pin TSOP
- **Top or bottom boot block**
- **Manufactured on 0.32 µm process technology**
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash standard

### PERFORMANCE CHARACTERISTICS

- **High performance**
  - — Access time as fast 90 ns
  - — Program time: 8 µs/word typical using Accelerate
- **Ultra low power consumption (typical values)**
  - — 1 mA active read current at 1 MHz
  - — 5 mA active read current at 5 MHz
  - — 1 µA in standby or automatic sleep mode
- **Minimum 1 million erase cycles guaranteed per sector**
- **20 Year data retention at 125°C**
  - — Reliable operation for the life of the system

### SOFTWARE FEATURES

- **Supports Common Flash Memory Interface (CFI)**
- **Erase Suspend/Erase Resume**
  - — Suspends erase operations to allow programming in same bank
- **Data# Polling and Toggle Bits**
  - — Provides a software method of detecting the status of program or erase cycles
- **Unlock Bypass Program command**
  - — Reduces overall programming time when issuing multiple program command sequences

### HARDWARE FEATURES

- **Any combination of sectors can be erased**
- **Ready/Busy# output (RY/BY#)**
  - — Hardware method for detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - — Hardware method of resetting the internal state machine to reading array data
- **WP#/ACC input pin**
  - — Write protect (WP#) function allows protection of two outermost boot sectors, regardless of sector protect status
  - — Acceleration (ACC) function accelerates program timing
- **Sector protection**
  - — Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - — Temporary Sector Unprotect allows changing data in protected sectors in-system

This Data Sheet states AMD's current specifications regarding the Products described herein. This Data Sheet may be revised by subsequent versions or modifications due to changes in technical specifications.

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Issue Date: **November 1, 2004**

## GENERAL DESCRIPTION

The Am29SL160C is a 16 Mbit, 1.8 V volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The data appears on DQ0–DQ15. The device is offered in 48-pin TSOP and 48-ball FBGA packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed and erased in-system with a single 1.8 volt $V_{CC}$ supply. No $V_{PP}$ is required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The standard device offers access times of 90, 100, 120, or 150 ns, allowing microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 1.8 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle completes, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

**Hardware data protection** measures include a low $V_{CC}$ detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This is achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses are stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

# TABLE OF CONTENTS

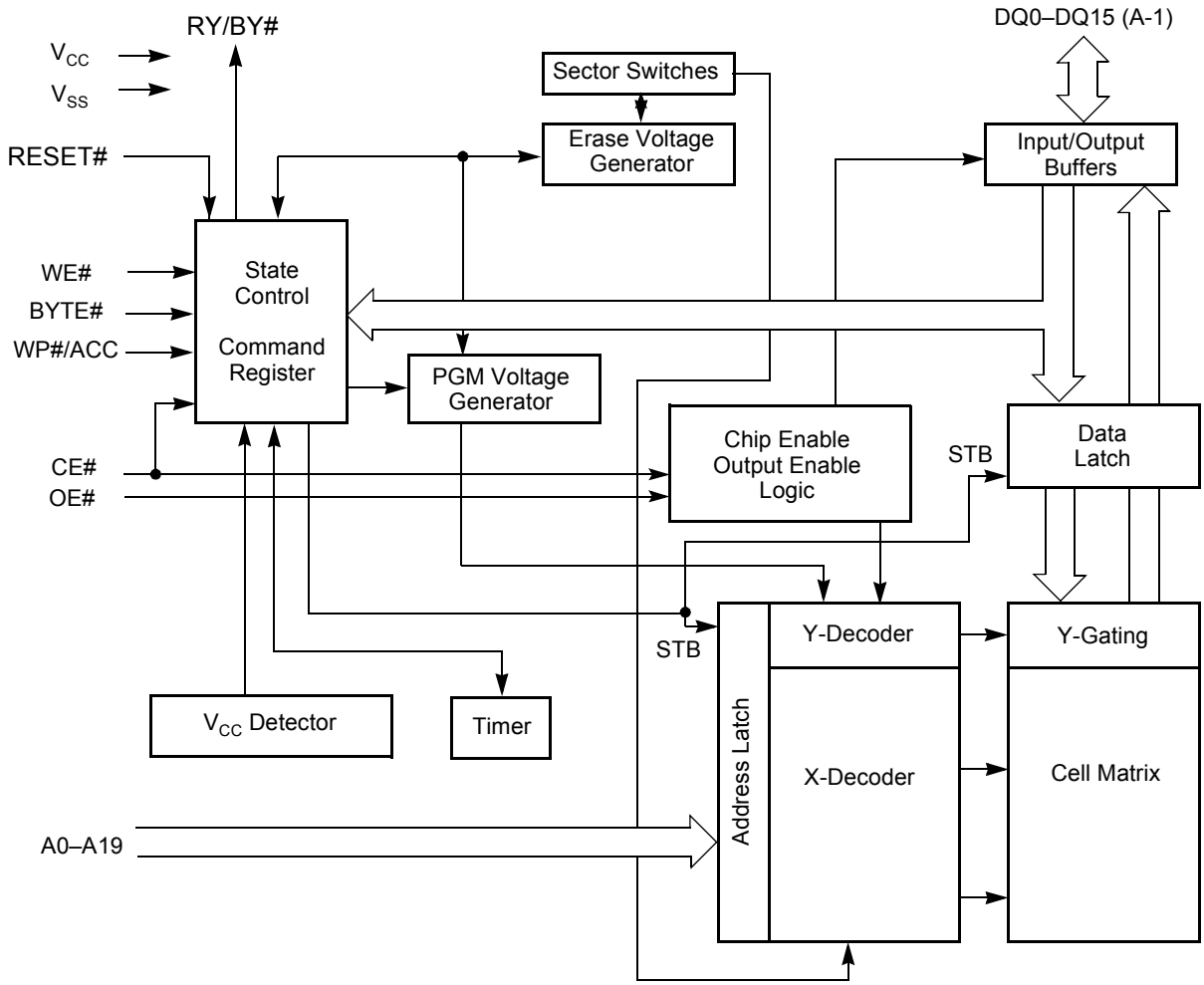

**Product Selector Guide . . . . . 6**
**Block Diagram . . . . . 6**
**Connection Diagrams . . . . . 7**
Special Handling Instructions for FBGA Packages . . . . . 8
**Pin Configuration . . . . . 9**
**Logic Symbol . . . . . 9**
**Ordering Information . . . . . 10**
Table 1. Am29SL160C Device Bus Operations . . . . . 11
Word/Byte Configuration . . . . . 11
Requirements for Reading Array Data . . . . . 11
Writing Commands/Command Sequences . . . . . 12
Accelerated Program Operation . . . . . 12
Program and Erase Operation Status . . . . . 12
Standby Mode . . . . . 12
Automatic Sleep Mode . . . . . 12
RESET#: Hardware Reset Pin . . . . . 12
Output Disable Mode . . . . . 13
Table 2. Am29SL160CT Top Boot Sector Architecture . . . . . 14
Table 3. Am29SL160CB Bottom Boot Sector Architecture . . . . . 15
Autoselect Mode . . . . . 16
Table 4. Am29SL160C Autoselect Codes (High Voltage Method) . . 16
Sector/Sector Block Protection and Unprotection . . . . . 17
Table 5. Top Boot Sector/Sector Block Addresses for Protection/Unprotection . . . . . 17
Table 6. Bottom Boot Sector/Sector Block Addresses for Protection/Unprotection . . . . . 17
Write Protect (WP#) . . . . . 18
Temporary Sector Unprotect . . . . . 18
Figure 1. In-System Sector Protect/Unprotect Algorithms . . . . . 19
Figure 2. Temporary Sector Unprotect Operation . . . . . 20
Secured Silicon (SecSi) Sector Flash Memory Region . . . . . 20
Table 7. SecSi Sector Addresses . . . . . 20
Hardware Data Protection . . . . . 20
Low $V_{CC}$ Write Inhibit . . . . . 20
Write Pulse “Glitch” Protection . . . . . 20
Logical Inhibit . . . . . 20
Power-Up Write Inhibit . . . . . 20
**Common Flash Memory Interface (CFI) . . . . . 21**
Table 8. CFI Query Identification String . . . . . 21
Table 9. System Interface String . . . . . 22
Table 10. Device Geometry Definition . . . . . 22
Table 11. Primary Vendor-Specific Extended Query . . . . . 23
**Command Definitions . . . . . 23**
Reading Array Data . . . . . 23
Reset Command . . . . . 23
Autoselect Command Sequence . . . . . 24
Enter SecSi Sector/Exit SecSi Sector Command Sequence . . 24
Word/Byte Program Command Sequence . . . . . 24
Unlock Bypass Command Sequence . . . . . 24
Figure 3. Program Operation . . . . . 25
Chip Erase Command Sequence . . . . . 26
Sector Erase Command Sequence . . . . . 26
Erase Suspend/Erase Resume Commands . . . . . 26
Figure 4. Erase Operation . . . . . 27
Command Definitions . . . . . 28
Table 12. Am29SL160C Command Definitions . . . . . 28
**Write Operation Status . . . . . 29**
DQ7: Data# Polling . . . . . 29
Figure 5. Data# Polling Algorithm . . . . . 29
RY/BY#: Ready/Busy# . . . . . 30
DQ6: Toggle Bit I . . . . . 30
DQ2: Toggle Bit II . . . . . 30
Reading Toggle Bits DQ6/DQ2 . . . . . 30
DQ5: Exceeded Timing Limits . . . . . 31
DQ3: Sector Erase Timer . . . . . 31
Figure 6. Toggle Bit Algorithm . . . . . 31
Table 13. Write Operation Status . . . . . 32
**Absolute Maximum Ratings . . . . . 33**
Figure 7. Maximum Negative Overshoot Waveform . . . . . 33
Figure 8. Maximum Positive Overshoot Waveform . . . . . 33
**Operating Ranges . . . . . 33**
**DC Characteristics . . . . . 34**
Figure 9. $I_{CC1}$ Current vs. Time (Showing Active and Automatic Sleep Currents) . . . . . 35
Figure 10. Typical $I_{CC1}$ vs. Frequency . . . . . 35
**Test Conditions . . . . . 36**
Figure 11. Test Setup . . . . . 36
Table 14. Test Specifications . . . . . 36
Figure 12. Input Waveforms and Measurement Levels . . . . . 36
**AC Characteristics . . . . . 37**
Read Operations . . . . . 37
Figure 13. Read Operations Timings . . . . . 37
Hardware Reset (RESET#) . . . . . 38
Figure 14. RESET# Timings . . . . . 38
Word/Byte Configuration (BYTE#) . . . . . 39
Figure 15. BYTE# Timings for Read Operations . . . . . 39
Figure 16. BYTE# Timings for Write Operations . . . . . 39
Erase/Program Operations . . . . . 40
Figure 17. Program Operation Timings . . . . . 41
Figure 18. Chip/Sector Erase Operation Timings . . . . . 42
Figure 19. Data# Polling Timings (During Embedded Algorithms) . 43
Figure 20. Toggle Bit Timings (During Embedded Algorithms) . . . . . 43
Figure 21. DQ2 vs. DQ6 . . . . . 44
Figure 22. Temporary Sector Unprotect Timing Diagram . . . . . 44
Figure 23. Accelerated Program Timing Diagram . . . . . 45
Figure 24. Sector Protect/Unprotect Timing Diagram . . . . . 45
Figure 25. Alternate CE# Controlled Write Operation Timings . . . . . 47
**Erase And Programming Performance . . . . . 48**
**Latchup Characteristics . . . . . 48**
**TSOP Pin Capacitance . . . . . 48**
**Data Retention . . . . . 48**
**Physical Dimensions* . . . . . 49**
TS 048—48-Pin Standard TSOP . . . . . 49
FBC048—48-Ball Fine-Pitch Ball Grid Array (FBGA) 8 x 9 mm package . . . . . 50
**Revision Summary . . . . . 51**

## PRODUCT SELECTOR GUIDE

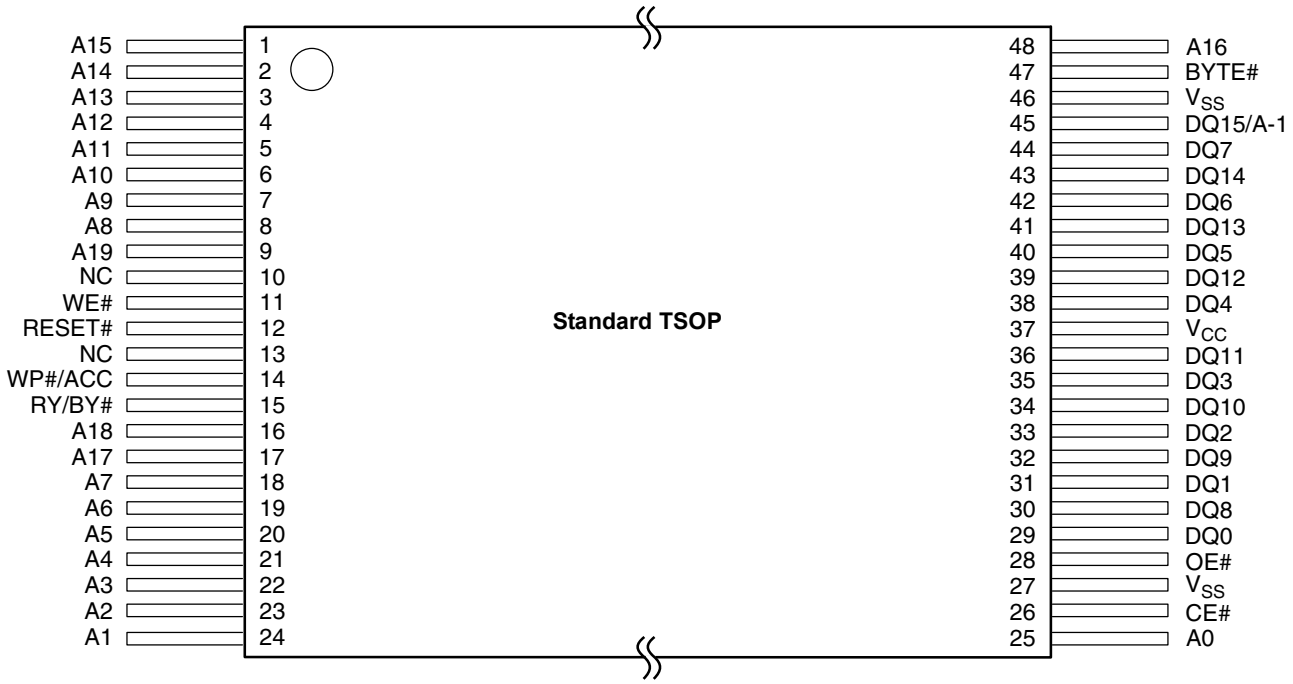
| Family Part Number | Am29SL160C | | | |
|---|---|---|---|---|
| Speed Options | **-90** | **-100** | **-120** | **-150** |
| Max access time, ns ($t_{ACC}$) | 90 | 100 | 120 | 150 |
| Max CE# access time, ns ($t_{CE}$) | 90 | 100 | 120 | 150 |
| Max OE# access time, ns ($t_{OE}$) | 35 | 35 | 50 | 65 |

***Note:*** *See "AC Characteristics" for full specifications.*

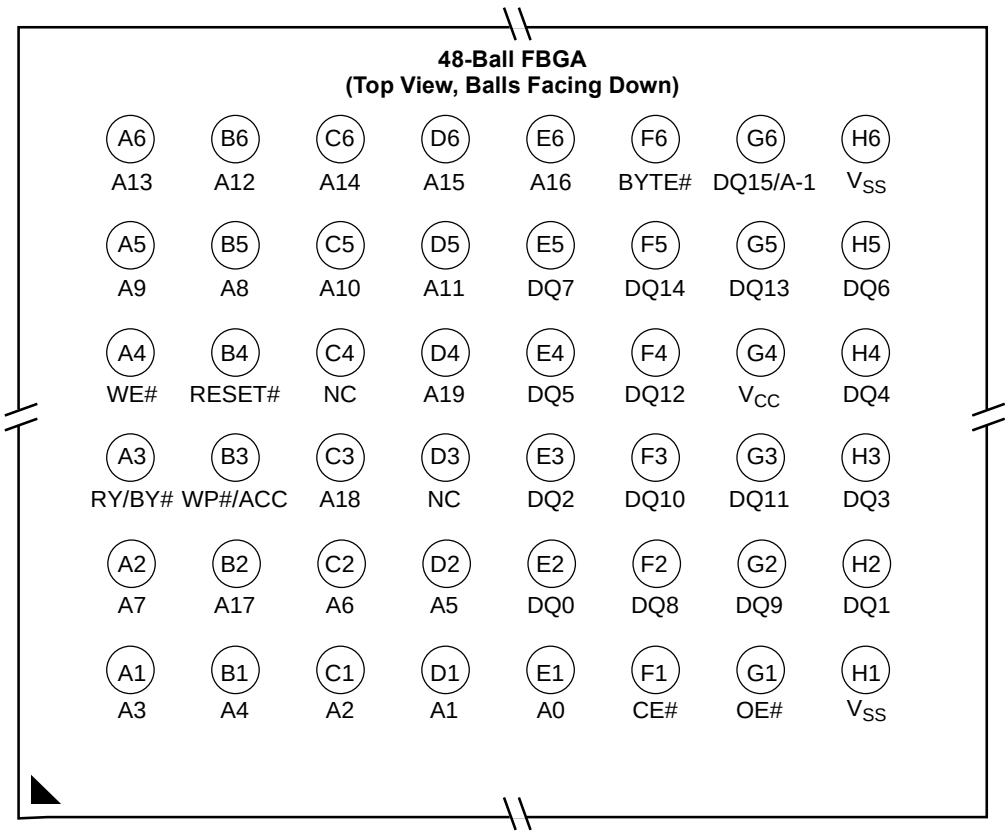
## BLOCK DIAGRAM



## CONNECTION DIAGRAMS



## CONNECTION DIAGRAMS (Continued)




### Special Handling Instructions for FBGA Packages

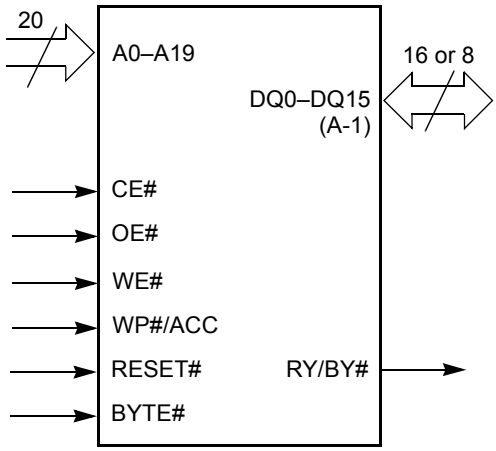
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

## PIN CONFIGURATION

| | | |
|---|---|---|
| A0–A19 | = | 20 addresses |
| DQ0–DQ14 | = | 15 data inputs/outputs |
| DQ15/A-1 | = | DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode) |
| CE# | = | Chip enable |
| OE# | = | Output enable |
| WE# | = | Write enable |
| WP#/ACC | = | Hardware write protect/acceleration pin |
| RESET# | = | Hardware reset pin, active low |
| BYTE# | = | Selects 8-bit or 16-bit mode |
| RY/BY# | = | Ready/Busy# output |
| $V_{CC}$ | = | 1.8–2.2 V single power supply |
| $V_{SS}$ | = | Device ground |
| NC | = | Pin not connected internally |

## LOGIC SYMBOL



## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

**Am29SL160C T -90 E C N**

**STANDARD PROCESSING**
N = SecSi Sector factory-locked with random ESN
(Contact an AMD representative for more information)

**TEMPERATURE RANGE**
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)
D = Commercial (0°C to +70°C) with PB-free Package
F = Industrial (-40°C to +85°C) with PB-free Package
F = Extended (-55°C to +125°C) with PB-free Package

**PACKAGE TYPE**
E = 48-Pin Thin Small Outline Package (TSOP)
Standard Pinout (TS 048)
WC=48-ball Fine-Pitch Ball Grid Array (FBGA)
0.80 mm pitch, 8 x 9 mm package (FBC048)

**SPEED OPTION**
See Product Selector Guide and Valid Combinations

**BOOT CODE SECTOR ARCHITECTURE**
T = Top sector
B = Bottom sector

**DEVICE NUMBER/DESCRIPTION**
Am29SL160C
16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS Flash Memory
1.8 Volt-only Read, Program, and Erase

| Valid Combinations for TSOP Packages | |
|---|---|
| AM29SL160CT-90, AM29SL160CB-90 | EC, EI<br>ED, EF |
| AM29SL160CT-100, AM29SL160CB-100 | |
| AM29SL160CT-120, AM29SL160CB-120 | |
| AM29SL160CT-150, AM29SL160CB-150 | |

| Valid Combinations for FBGA Packages | | | |
|---|---|---|---|
| **Order Number** | | **Package Marking** | |
| AM29SL160CT-90, AM29SL160CB-90 | WCC, WCI<br>WCD, WCF | A160CT90V, A160CB90V | C, I,<br>D, F |
| AM29SL160CT-100, AM29SL160CB-100 | | A160CT10V, A160CB10V | |
| AM29SL160CT-120, AM29SL160CB-120 | | A160CT12V, A160CB12V | |
| AM29SL160CT-150, AM29SL160CB-150 | | A160CT15V, A160CB15V | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

**Table 1. Am29SL160C Device Bus Operations**

| Operation | CE# | OE# | WE# | RESET# | WP#/ACC | Addresses (Note 1) | DQ0–DQ7 | DQ8–DQ15 | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | BYTE# = $V_{IH}$ | BYTE# = $V_{IL}$ |
| Read | L | L | H | H | X | $A_{IN}$ | $D_{OUT}$ | $D_{OUT}$ | DQ8–DQ14 = High-Z, DQ15 = A-1 |
| Write (Program/Erase) | L | H | L | H | (Note 3) | $A_{IN}$ | $D_{IN}$ | $D_{IN}$ | |
| Standby | $V_{CC}$ ± 0.2 V | X | X | $V_{CC}$ ± 0.2 V | X | X | High-Z | High-Z | High-Z |
| Output Disable | L | H | H | H | X | X | High-Z | High-Z | High-Z |
| Reset | X | X | X | L | X | X | High-Z | High-Z | High-Z |
| Sector Protect (Note 2) | L | H | L | $V_{ID}$ | X | Sector Address, A6 = L, A1 = H, A0 = L | $D_{IN}$ | X | X |
| Sector Unprotect (Note 2) | L | H | L | $V_{ID}$ | (Note 3) | Sector Address, A6 = H, A1 = H, A0 = L | $D_{IN}$ | X | X |
| Temporary Sector Unprotect | X | X | X | $V_{ID}$ | (Note 3) | $A_{IN}$ | $D_{IN}$ | $D_{IN}$ | High-Z |

***Legend:***

*L = Logic Low = $V_{IL}$, H = Logic High = $V_{IH}$, $V_{ID}$ = 10 ± 1.0 V, $V_{HH}$ = 10 ± 0.5 V, X = Don't Care, $A_{IN}$ = Address In, $D_{IN}$ = Data In, $D_{OUT}$ = Data Out*

***Notes:***

1. *Addresses are A19:A0 in word mode (BYTE# = $V_{IH}$), A19:A-1 in byte mode (BYTE# = $V_{IL}$).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See "Sector/Sector Block Protection and Unprotection" on page 17.*
3. *If WP#/ACC = $V_{IL}$, the two outermost boot sectors are protected. If WP#/ACC = $V_{IH}$, the two outermost boot sectors are protected or unprotected as previously set by the system. If WP#/ACC = $V_{HH}$, all sectors, including the two outermost boot sectors, are unprotected.*

### Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

### Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to $V_{IL}$. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at $V_{IH}$. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array

data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" on page 23 for more information. Refer to the AC table for timing specifications and to Figure 13, on page 37 for the timing diagram. $I_{CC1}$ in the DC Characteristics table represents the active current specification for reading array data.

## Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to $V_{IL}$, and OE# to $V_{IH}$.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to "Word/Byte Configuration" on page 11 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word/Byte Program Command Sequence" on page 24 contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2, on page 14 and Table 3, on page 15 indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Command Definitions" on page 23 contains details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to "Autoselect Mode" on page 16 and "Autoselect Command Sequence" on page 24 for more information.

$I_{CC2}$ in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" on page 37 contains timing specification tables and timing diagrams for write operations.

## Accelerated Program Operation

The device offers accelerated program operation through the ACC function, which is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster in-system programming of the device during the system production process.

If the system asserts $V_{HH}$ on the pin, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing $V_{HH}$ from the WP#/ACC pin returns the device to normal operation.

## Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and $I_{CC}$ read specifications apply. Refer to "Write Operation Status" on page 29 for more information, and to "AC Characteristics" on page 37 for timing diagrams.

## Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.2$ V. (Note that this is a more restricted voltage range than $V_{IH}$.) If CE# and RESET# are held at $V_{IH}$, but not within $V_{CC} \pm 0.2$ V, the device is in the standby mode, but the standby current is greater. The device requires standard access time ($t_{CE}$) for read access when the device is in either of these standby modes, before it is ready to read data.

The device also enters the standby mode when the RESET# pin is driven low. Refer to "RESET#: Hardware Reset Pin" on page 12.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

$I_{CC3}$ in the DC Characteristics table represents the standby current specification.

## Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC}$ + 50 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. $I_{CC4}$ in the DC Characteristics table represents the automatic sleep mode current specification.

## RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the

RESET# pin is driven low for at least a period of $t_{RP}$, the device **immediately terminates** any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.2$ V, the device draws CMOS standby current ($I_{CC4}$). If RESET# is held at $V_{IL}$ but not within $V_{SS} \pm 0.2$ V, the standby current is greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of $t_{READY}$ (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of $t_{READY}$ (not during Embedded Algorithms). The system can read data $t_{RH}$ after the RESET# pin returns to $V_{IH}$.

Refer to “AC Characteristics” on page 37 for RESET# parameters and to “RESET# Timings” on page 38 for the timing diagram.

## Output Disable Mode

When the OE# input is at $V_{IH}$, output from the device is disabled. The output pins are placed in the high impedance state.

## Table 2. Am29SL160CT Top Boot Sector Architecture

| Sector | Sector Address | | | | | | | | Sector Size (Kbytes/Kwords) | Address Range (in Hexadecimal | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | Byte Mode (x8) | Word Mode (x16) |
| SA0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 000000h–00FFFFh | 00000h–07FFFh |
| SA1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 010000h–01FFFFh | 08000h–0FFFFh |
| SA2 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 020000h–02FFFFh | 10000h–17FFFh |
| SA3 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 030000h–03FFFFh | 18000h–1FFFFh |
| SA4 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 040000h–04FFFFh | 20000h–27FFFh |
| SA5 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 050000h–05FFFFh | 28000h–2FFFFh |
| SA6 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 060000h–06FFFFh | 30000h–37FFFh |
| SA7 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 070000h–07FFFFh | 38000h–3FFFFh |
| SA8 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 080000h–08FFFFh | 40000h–47FFFh |
| SA9 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 090000h–09FFFFh | 48000h–4FFFFh |
| SA10 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 0A0000h–0AFFFFh | 50000h–57FFFh |
| SA11 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 0B0000h–0BFFFFh | 58000h–5FFFFh |
| SA12 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 0C0000h–0CFFFFh | 60000h–67FFFh |
| SA13 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 0D0000h–0DFFFFh | 68000h–6FFFFh |
| SA14 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 0E0000h–0EFFFFh | 70000h–77FFFh |
| SA15 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 0F0000h–0FFFFFh | 78000h–7FFFFh |
| SA16 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 100000h–10FFFFh | 80000h–87FFFh |
| SA17 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 110000h–11FFFFh | 88000h–8FFFFh |
| SA18 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 120000h–12FFFFh | 90000h–97FFFh |
| SA19 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 130000h–13FFFFh | 98000h–9FFFFh |
| SA20 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 140000h–14FFFFh | A0000h–A7FFFh |
| SA21 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 150000h–15FFFFh | A8000h–AFFFFh |
| SA22 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 160000h–16FFFFh | B0000h–B7FFFh |
| SA23 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 170000h–17FFFFh | B8000h–BFFFFh |
| SA24 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 180000h–18FFFFh | C0000h–C7FFFh |
| SA25 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 190000h–19FFFFh | C8000h–CFFFFh |
| SA26 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 1A0000h–1AFFFFh | D0000h–D7FFFh |
| SA27 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 1B0000h–1BFFFFh | D8000h–DFFFFh |
| SA28 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 1C0000h–1CFFFFh | E0000h–E7FFFh |
| SA29 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 1D0000h–1DFFFFh | E8000h–EFFFFh |
| SA30 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 1E0000h–1EFFFFh | F0000h–F7FFFh |
| SA31 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 8/4 | 1F0000h–1F1FFFh | F8000h–F8FFFh |
| SA32 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 8/4 | 1F2000h–1F3FFFh | F9000h–F9FFFh |
| SA33 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 8/4 | 1F4000h–1F5FFFh | FA000h–FAFFFh |
| SA34 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 8/4 | 1F6000h–1F7FFFh | FB000h–FBFFFh |
| SA35 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 8/4 | 1F8000h–1F9FFFh | FC0004–FCFFFh |
| SA36 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 8/4 | 1FA000h–1FBFFFh | FD000h–FDFFFh |
| SA37 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8/4 | 1FC000h–1DFFFFh | FE000h–FEFFFh |
| SA38 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8/4 | 1FE000h–1FFFFFh | FF000h–FFFFFh |

***Note:*** *Address range is A19:A-1 in byte mode and A19:A0 in word mode. See "Word/Byte Configuration" section for more information.*

**Table 3. Am29SL160CB Bottom Boot Sector Architecture**

| Sector | Sector Address | | | | | | | | Sector Size (Kbytes/Kwords) | Address Range (in hexadecimal) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | Byte Mode (x8) | Word Mode (x16) |
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8/4 | 000000h–001FFFh | 00000h–00FFFh |
| SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 8/4 | 002000h–003FFFh | 01000h–01FFFh |
| SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 8/4 | 004000h–005FFFh | 02000h–02FFFh |
| SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 8/4 | 006000h–07FFFFh | 03000h–03FFFh |
| SA4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8/4 | 008000h–009FFFh | 04000h–04FFFh |
| SA5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 8/4 | 00A000h–00BFFFh | 05000h–05FFFh |
| SA6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 8/4 | 00C000h–00DFFFh | 06000h–06FFFh |
| SA7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 8/4 | 00E000h–00FFFFh | 07000h–07FFFh |
| SA8 | 0 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 010000h–01FFFFh | 08000h–0FFFFh |
| SA9 | 0 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 020000h–02FFFFh | 10000h–17FFFh |
| SA10 | 0 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 030000h–03FFFFh | 18000h–1FFFFh |
| SA11 | 0 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 040000h–04FFFFh | 20000h–27FFFh |
| SA12 | 0 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 050000h–05FFFFh | 28000h–2FFFFh |
| SA13 | 0 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 060000h–06FFFFh | 30000h–37FFFh |
| SA14 | 0 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 070000h–07FFFFh | 38000h–3FFFFh |
| SA15 | 0 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 080000h–08FFFFh | 40000h–47FFFh |
| SA16 | 0 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 090000h–09FFFFh | 48000h–4FFFFh |
| SA17 | 0 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 0A0000h–0AFFFFh | 50000h–57FFFh |
| SA18 | 0 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 0B0000h–0BFFFFh | 58000h–5FFFFh |
| SA19 | 0 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 0C0000h–0CFFFFh | 60000h–67FFFh |
| SA20 | 0 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 0D0000h–0DFFFFh | 68000h–6FFFFh |
| SA21 | 0 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 0E0000h–0EFFFFh | 70000h–77FFFh |
| SA22 | 0 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 0F0000h–0FFFFFh | 78000h–7FFFFh |
| SA23 | 1 | 0 | 0 | 0 | 0 | X | X | X | 64/32 | 100000h–10FFFFh | 80000h–87FFFh |
| SA24 | 1 | 0 | 0 | 0 | 1 | X | X | X | 64/32 | 110000h–11FFFFh | 88000h–8FFFFh |
| SA25 | 1 | 0 | 0 | 1 | 0 | X | X | X | 64/32 | 120000h–12FFFFh | 90000h–97FFFh |
| SA26 | 1 | 0 | 0 | 1 | 1 | X | X | X | 64/32 | 130000h–13FFFFh | 98000h–9FFFFh |
| SA27 | 1 | 0 | 1 | 0 | 0 | X | X | X | 64/32 | 140000h–14FFFFh | A0000h–A7FFFh |
| SA28 | 1 | 0 | 1 | 0 | 1 | X | X | X | 64/32 | 150000h–15FFFFh | A8000h–AFFFFh |
| SA29 | 1 | 0 | 1 | 1 | 0 | X | X | X | 64/32 | 160000h–16FFFFh | B0000h–B7FFFh |
| SA30 | 1 | 0 | 1 | 1 | 1 | X | X | X | 64/32 | 170000h–17FFFFh | B8000h–BFFFFh |
| SA31 | 1 | 1 | 0 | 0 | 0 | X | X | X | 64/32 | 180000h–18FFFFh | C0000h–C7FFFh |
| SA32 | 1 | 1 | 0 | 0 | 1 | X | X | X | 64/32 | 190000h–19FFFFh | C8000h–CFFFFh |
| SA33 | 1 | 1 | 0 | 1 | 0 | X | X | X | 64/32 | 1A0000h–1AFFFFh | D0000h–D7FFFh |
| SA34 | 1 | 1 | 0 | 1 | 1 | X | X | X | 64/32 | 1B0000h–1BFFFFh | D8000h–DFFFFh |
| SA35 | 1 | 1 | 1 | 0 | 0 | X | X | X | 64/32 | 1C0000h–1CFFFFh | E0000h–E7FFFh |
| SA36 | 1 | 1 | 1 | 0 | 1 | X | X | X | 64/32 | 1D0000h–1DFFFFh | E8000h–EFFFFh |
| SA37 | 1 | 1 | 1 | 1 | 0 | X | X | X | 64/32 | 1E0000h–1EFFFFh | F0000h–F7FFFh |
| SA38 | 1 | 1 | 1 | 1 | 1 | X | X | X | 64/32 | 1F0000h–1FFFFFh | F8000h–FFFFFh |

***Note:*** *Address range is A19:A-1 in byte mode and A19:A0 in word mode. See "Word/Byte Configuration" section for more information.*

## Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires $V_{ID}$ on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Tables 2 and 3). Table 4 shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 12, on page 28. This method does not require $V_{ID}$. See "Command Definitions" on page 23 for details on using the autoselect mode.

**Table 4. Am29SL160C Autoselect Codes (High Voltage Method)**

| Description | Mode | CE# | OE# | WE# | A19 to A12 | A11 to A10 | A9 | A8 to A7 | A6 | A5 to A2 | A1 | A0 | DQ8 to DQ15 | DQ7 to DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer ID: AMD | | L | L | H | X | X | $V_{ID}$ | X | L | X | L | L | X | 01h |
| Device ID: Am29SL160CT (Top Boot Block) | Word | L | L | H | X | X | $V_{ID}$ | X | L | X | L | H | 22h | E4 |
| | Byte | L | L | H | | | | | | | | | X | E4 |
| Device ID: Am29SL160CB (Bottom Boot Block) | Word | L | L | H | X | X | $V_{ID}$ | X | L | X | L | H | 22h | E7 |
| | Byte | L | L | H | | | | | | | | | X | E7 |
| Sector Protection Verification | | L | L | H | SA | X | $V_{ID}$ | X | L | X | H | L | X | 01h (protected) |
| | | | | | | | | | | | | | X | 00h (unprotected) |
| SecSi Sector Indicator bit (DQ7) | | L | L | H | SA | X | $V_{ID}$ | X | L | X | H | H | X | 81h (factory locked) |

*L = Logic Low = $V_{IL}$, H = Logic High = $V_{IH}$, SA = Sector Address, X = Don't care.*

***Note:*** *Outputs for data bits DQ8–DQ15 are for BYTE#=$V_{IH}$. DQ8–DQ15 are don't care when BYTE#=$V_{IL}$.*

## Sector/Sector Block Protection and Unprotection

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 5 and Table 6).

**Table 5. Top Boot Sector/Sector Block Addresses for Protection/Unprotection**

| Sector / Sector Block | A19–A12 | Sector / Sector Block Size |
|---|---|---|
| SA0 | 00000XXX | 64 Kbytes |
| SA1-SA3 | 00001XXX, 00010XXX, 00011XXX | 192 (3x64) Kbytes |
| SA4-SA7 | 001XXXXX | 256 (4x64) Kbytes |
| SA8-SA11 | 010XXXXX | 256 (4x64) Kbytes |
| SA12-SA15 | 011XXXXX | 256 (4x64) Kbytes |
| SA16-SA19 | 100XXXXX | 256 (4x64) Kbytes |
| SA20-SA23 | 101XXXXX | 256 (4x64) Kbytes |
| SA24-SA27 | 110XXXXX | 256 (4x64) Kbytes |
| SA28-SA30 | 11100XXX, 11101XXX, 11110XXX | 192 (3x64) Kbytes |
| SA31 | 11111000 | 8 Kbytes |
| SA32 | 11111001 | 8 Kbytes |
| SA33 | 11111010 | 8 Kbytes |
| SA34 | 11111011 | 8 Kbytes |
| SA35 | 11111100 | 8 Kbytes |
| SA36 | 11111101 | 8 Kbytes |
| SA37 | 11111110 | 8 Kbytes |
| SA38 | 11111111 | 8 Kbytes |

**Table 6. Bottom Boot Sector/Sector Block Addresses for Protection/Unprotection**

| Sector / Sector Block | A19–A12 | Sector / Sector Block Size |
|---|---|---|
| SA38 | 11111XXX | 64 Kbytes |
| SA37-SA35 | 11110XXX, 11101XXX, 11100XXX | 192 (3x64) Kbytes |
| SA34-SA31 | 110XXXXX | 256 (4x64) Kbytes |
| SA30-SA27 | 101XXXXX | 256 (4x64) Kbytes |
| SA26-SA23 | 100XXXXX | 256 (4x64) Kbytes |
| SA22-SA19 | 011XXXXX | 256 (4x64) Kbytes |
| SA18-SA15 | 010XXXXX | 256 (4x64) Kbytes |
| SA14-SA11 | 001XXXXX | 256 (4x64) Kbytes |
| SA10-SA8 | 00001XXX, 00010XXX, 00011XXX | 192 (3x64) Kbytes |
| SA7 | 00000111 | 8 Kbytes |
| SA6 | 00000110 | 8 Kbytes |
| SA5 | 00000101 | 8 Kbytes |
| SA4 | 00000100 | 8 Kbytes |
| SA3 | 00000011 | 8 Kbytes |
| SA2 | 00000010 | 8 Kbytes |
| SA1 | 00000001 | 8 Kbytes |
| SA0 | 00000000 | 8 Kbytes |

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection is implemented via two methods.

The primary method requires $V_{ID}$ on the RESET# pin only, and is implemented either in-system or via programming equipment. Figure 1, on page 19 shows the algorithms and Figure 24, on page 45 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment requires $V_{ID}$ on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only AMD flash devices. Publication number 21622 contains further details. Contact an AMD representative to request the document containing further details.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" on page 16 for details.

## Write Protect (WP#)

The write protect function provides a hardware method of protecting certain boot sectors without using $V_{ID}$. This function is one of two provided by the WP#/ACC pin.

If the system asserts $V_{IL}$ on the WP#/ACC pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection" on page 17. The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts $V_{IH}$ on the WP#/ACC pin, the device reverts to whether the two outermost 8 Kbyte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection" on page 17.

Note that if the system asserts $V_{HH}$ on the WP#/ACC pin, all sectors, including the two outermost sectors, are unprotected. $V_{HH}$ is intended for accelerated in-system programming of the device during system production. It is advisable, therefore, not to assert $V_{HH}$ on this pin after the system has been placed in the field for use. If faster programming is desired, the system may use the unlock bypass program command sequence.

## Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to $V_{ID}$. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once $V_{ID}$ is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 2, on page 20 shows the algorithm, and Figure 22, on page 44 shows the timing diagrams, for this feature.

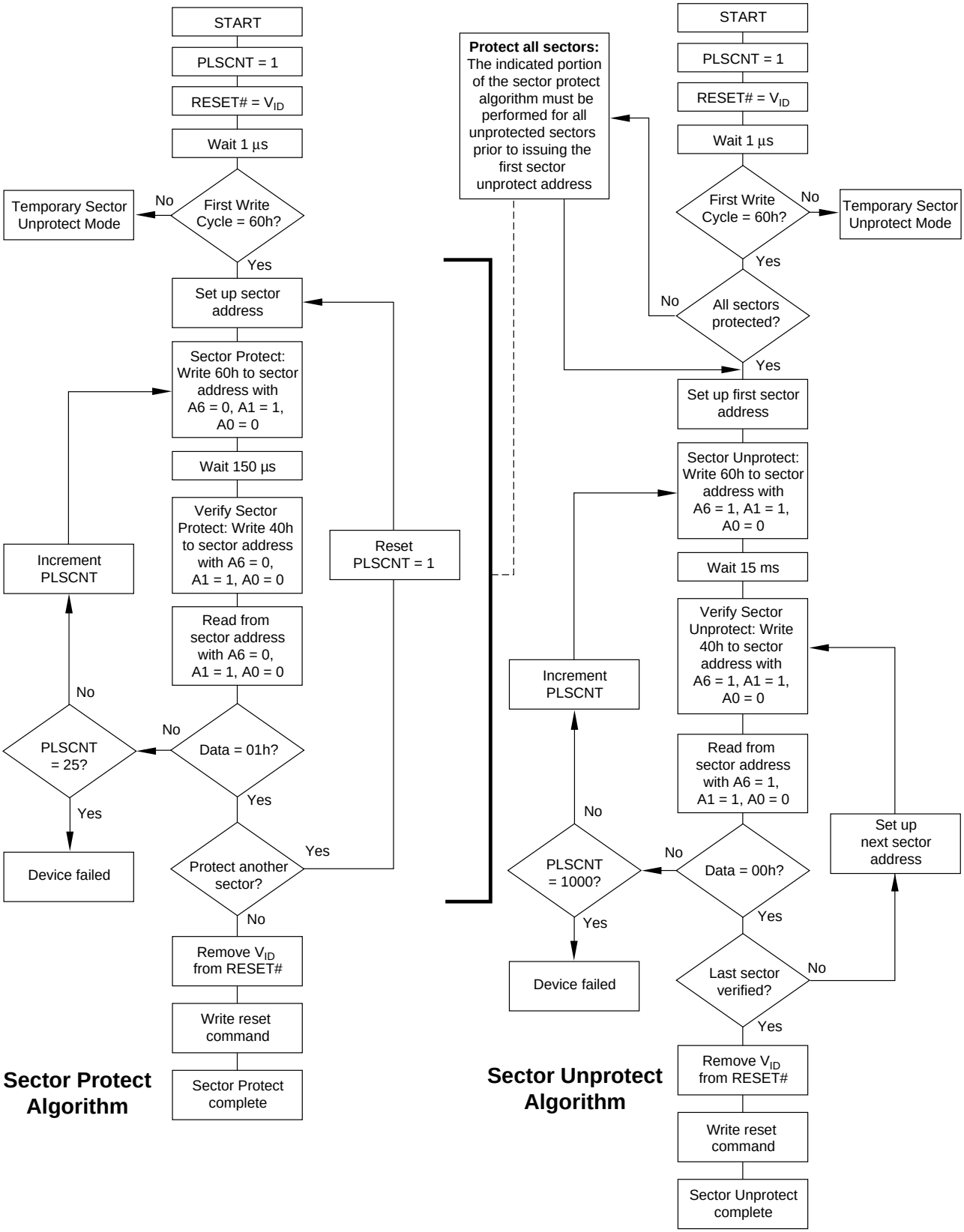
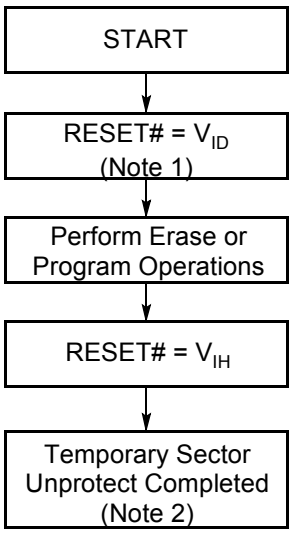



**Figure 1. In-System Sector Protect/Unprotect Algorithms**




***Notes:***

1. *All protected sectors unprotected. (If WP#/ACC = $V_{IL}$, the outermost sectors remain protected)*
2. *All previously protected sectors are protected once again.*

**Figure 2. Temporary Sector Unprotect Operation**

## Secured Silicon (SecSi) Sector Flash Memory Region

The Secured Silicon (SecSi) Sector is a flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector in this device is 256 bytes in length. The device contains a SecSi Sector indicator bit that allows the system to determine whether or not the SecSi Sector was factory locked. This indicator bit is permanently set at the factory and cannot be changed, which prevents a factory-locked part from being cloned.

AMD offers this device only with the SecSi Sector factory serialized and locked. The first sixteen bytes of the SecSi Sector contain a random ESN. To utilize the remainder SecSi Sector space, customers must provide their code to AMD through AMD's Express Flash service. The factory will program and permanently protect the SecSi Sector (in addition to programming and protecting the remainder of the device as required).

The system can read the SecSi Sector by writing the Enter SecSi Sector command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence" on page 24). Table 7, on page 20 shows the layout for the SecSi Sector.

**Table 7. SecSi Sector Addresses**

| Description | Address Range | |
|---|---|---|
| | Word Mode (x16) | Byte Mode (x8) |
| 16-byte random ESN | 00–07h | 000–00Fh |
| User-defined code or factory erased (all 1s) | 08–7Fh | 010–0FFh |

The device continues to read from the SecSi Sector until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

## Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 12, on page 28 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during $V_{CC}$ power-up and power-down transitions, or from system noise.

### Low $V_{CC}$ Write Inhibit

When $V_{CC}$ is less than $V_{LKO}$, the device does not accept any write cycles. This protects data during $V_{CC}$ power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until $V_{CC}$ is greater than $V_{LKO}$. The system must provide the proper signals to the control pins to prevent unintentional writes when $V_{CC}$ is greater than $V_{LKO}$.

### Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

### Logical Inhibit

Write cycles are inhibited by holding any one of OE# = $V_{IL}$, CE# = $V_{IH}$ or WE# = $V_{IH}$. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

### Power-Up Write Inhibit

If WE# = CE# = $V_{IL}$ and OE# = $V_{IH}$ during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

## COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 8, on page 21 to Table 11, on page 23. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 8, on page 21 to Table 11, on page 23. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact an AMD representative for copies of these documents.

**Table 8. CFI Query Identification String**

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 10h<br>11h<br>12h | 20h<br>22h<br>24h | 0051h<br>0052h<br>0059h | Query Unique ASCII string “QRY” |
| 13h<br>14h | 26h<br>28h | 0002h<br>0000h | Primary OEM Command Set |
| 15h<br>16h | 2Ah<br>2Ch | 0040h<br>0000h | Address for Primary Extended Table |
| 17h<br>18h | 2Eh<br>30h | 0000h<br>0000h | Alternate OEM Command Set (00h = none exists) |
| 19h<br>1Ah | 32h<br>34h | 0000h<br>0000h | Address for Alternate OEM Extended Table (00h = none exists) |

### Table 9. System Interface String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 1Bh | 36h | 0018h | $V_{CC}$ Min. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Ch | 38h | 0022h | $V_{CC}$ Max. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Dh | 3Ah | 0000h | $V_{PP}$ Min. voltage (00h = no $V_{PP}$ pin present) |
| 1Eh | 3Ch | 0000h | $V_{PP}$ Max. voltage (00h = no $V_{PP}$ pin present) |
| 1Fh | 3Eh | 0004h | Typical timeout per single byte/word write $2^N$ µs |
| 20h | 40h | 0000h | Typical timeout for Min. size buffer write $2^N$ µs (00h = not supported) |
| 21h | 42h | 000Ah | Typical timeout per individual block erase $2^N$ ms |
| 22h | 44h | 0000h | Typical timeout for full chip erase $2^N$ ms (00h = not supported) |
| 23h | 46h | 0005h | Max. timeout for byte/word write $2^N$ times typical |
| 24h | 48h | 0000h | Max. timeout for buffer write $2^N$ times typical |
| 25h | 4Ah | 0004h | Max. timeout per individual block erase $2^N$ times typical |
| 26h | 4Ch | 0000h | Max. timeout for full chip erase $2^N$ times typical (00h = not supported) |

### Table 10. Device Geometry Definition

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 27h | 4Eh | 0015h | Device Size = $2^N$ byte |
| 28h<br>29h | 50h<br>52h | 0002h<br>0000h | Flash Device Interface description (refer to CFI publication 100) |
| 2Ah<br>2Bh | 54h<br>56h | 0000h<br>0000h | Max. number of bytes in multi-byte write = $2^N$<br>(00h = not supported) |
| 2Ch | 58h | 0002h | Number of Erase Block Regions within device |
| 2Dh<br>2Eh<br>2Fh<br>30h | 5Ah<br>5Ch<br>5Eh<br>60h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 1 Information<br>(refer to the CFI specification or CFI publication 100) |
| 31h<br>32h<br>33h<br>34h | 62h<br>64h<br>66h<br>68h | 001Eh<br>0000h<br>0000h<br>0001h | Erase Block Region 2 Information |
| 35h<br>36h<br>37h<br>38h | 6Ah<br>6Ch<br>6Eh<br>70h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 3 Information |
| 39h<br>3Ah<br>3Bh<br>3Ch | 72h<br>74h<br>76h<br>78h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 4 Information |

**Table 11. Primary Vendor-Specific Extended Query**

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 40h<br>41h<br>42h | 80h<br>82h<br>84h | 0050h<br>0052h<br>0049h | Query-unique ASCII string “PRI” |
| 43h | 86h | 0031h | Major version number, ASCII |
| 44h | 88h | 0030h | Minor version number, ASCII |
| 45h | 8Ah | 0000h | Address Sensitive Unlock<br>0 = Required, 1 = Not Required |
| 46h | 8Ch | 0002h | Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 8Eh | 0001h | Sector Protect<br>0 = Not Supported, X = Number of sectors in per group |
| 48h | 90h | 0001h | Sector Temporary Unprotect<br>00 = Not Supported, 01 = Supported |
| 49h | 92h | 0004h | Sector Protect/Unprotect scheme<br>01 = 29F040 mode, 02 = 29F016 mode,<br>03 = 29F400 mode, 04 = 29LV800A mode |
| 4Ah | 94h | 0000h | Simultaneous Operation<br>00 = Not Supported, 01 = Supported |
| 4Bh | 96h | 0000h | Burst Mode Type<br>00 = Not Supported, 01 = Supported |
| 4Ch | 98h | 0000h | Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |

## COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 12, on page 28 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in “AC Characteristics” on page 37.

### Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See “Erase Suspend/Erase Resume Commands” on page 26 for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See “Reset Command”, next.

See also “Requirements for Reading Array Data” on page 11 for more information. The  table provides the read parameters, and Figure 13, on page 37 shows the timing diagram.

### Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don’t care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence

before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

See "AC Characteristics" on page 37 for parameters, and to Figure 14, on page 38 for the timing diagram.

## Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 12, on page 28 shows the address and data requirements. This method is an alternative to that shown in Table 4, on page 16, which is intended for PROM programmers and requires $V_{ID}$ on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address 01h in word mode (or 02h in byte mode) returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table 2, on page 14 and Table 3, on page 15 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

## Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, sixteen-byte electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi command sequence. The Exit SecSi command sequence returns the device to normal operation. Table 12, on page 28 shows the address and data requirements for both command sequences. See also "Secured Silicon (SecSi) Sector Flash Memory Region" on page 20 for further information.

## Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 12, on page 28 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See "Write Operation Status" on page 29 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device resets to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read shows that the data is still "0". Only erase operations can convert a "0" to a "1".

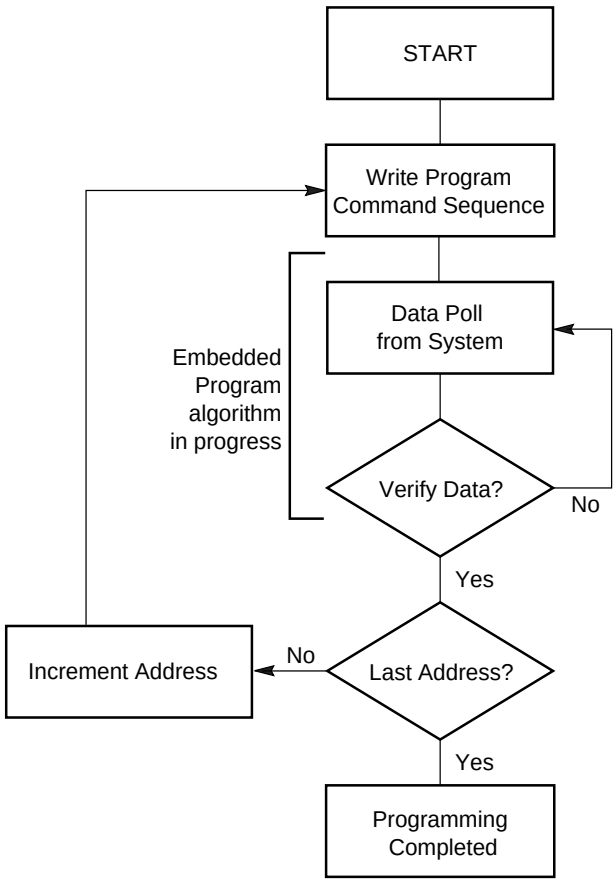
### Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 12, on page 28 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't cares. The device then returns to reading array data.

The device offers accelerated program operations through the WP#/ACC pin. This function is intended only to speed in-system programming of the device during system production. When the system asserts $V_{HH}$ on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. Note that the WP#/ACC pin must not be at $V_{HH}$ for any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Figure 3 illustrates the algorithm for the program operation. See "Erase/Program Operations" on page 40 for parameters, and Figure 17, on page 41 for timing diagrams.




***Note:*** *See Table 12, on page 28 for program command sequence.*

**Figure 3. Program Operation**

## Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 12, on page 28 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See "Write Operation Status" on page 29 for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 4, on page 27 illustrates the algorithm for the erase operation. See "Erase/Program Operations" on page 40 for parameters, and Figure 18, on page 42 for timing diagrams.

## Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 12, on page 28 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts are re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See "DQ3: Sector Erase Timer" on page 31.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to "Write Operation Status" on page 29 for information on these status bits.)

Figure 4, on page 27 illustrates the algorithm for the erase operation. Refer to the "Erase/Program Operations" on page 40 for parameters, and to Figure 18, on page 42 for timing diagrams.

## Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

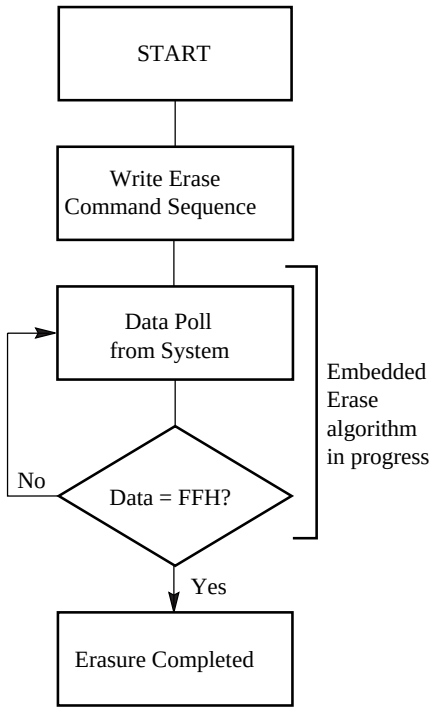
When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation is suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” on page 29 for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” on page 29 for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” on page 24 for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device resumes erasing.




***Notes:***

1. *See Table 12, on page 28 for erase command sequence.*
2. *See “DQ3: Sector Erase Timer” on page 31 for more information.*

**Figure 4. Erase Operation**

## Command Definitions

### Table 12. Am29SL160C Command Definitions

| Command Sequence (Note 1) | | | Cycles | Bus Cycles (Notes 2–5) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | |
| | | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read (Note 6) | | | 1 | RA | RD | | | | | | | | | | |
| Reset (Note 7) | | | 1 | XXX | F0 | | | | | | | | | | |
| Autoselect (Note 8) | Manufacturer ID | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X00 | 01 | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | |
| | Device ID (Top Boot/Bottom Boot) | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X01 | 22E4/ 22E7 | | | | |
| | | Byte | | AAA | | 555 | | AAA | | X02 | E4/E7 | | | | |
| | SecSi Sector Factory Protect | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X03 | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | X06 | | | | | |
| | Sector Protect Verify (Note 9) | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | (SA)X02 | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | (SA)X04 | | | | | |
| Enter SecSi Sector Region | | Word | 3 | 555 | AA | 2AA | 55 | 555 | 88 | | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | |
| Exit SecSi Sector Region | | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | XXX | 00 | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | |
| Program | | Word | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | |
| Unlock Bypass | | Word | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | |
| Unlock Bypass Program (Note 10) | | | 2 | XXX | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Reset (Note 11) | | | 2 | BA | 90 | XXX | 00 | | | | | | | | |
| Chip Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| | | Byte | | AAA | | 555 | | AAA | | AAA | | 555 | | AAA | |
| Sector Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 |
| | | Byte | | AAA | | 555 | | AAA | | AAA | | 555 | | | |
| Erase Suspend (Note 12) | | | 1 | BA | B0 | | | | | | | | | | |
| Erase Resume (Note 13) | | | 1 | BA | 30 | | | | | | | | | | |
| CFI Query (Note 14) | | Word | 1 | 55 | 98 | | | | | | | | | | |
| | | Byte | | AA | | | | | | | | | | | |

***Legend:***

*X = Don't care*

*RA = Address of the memory location to be read.*

*RD = Data read from location RA during read operation.*

*PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.*

*PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.*

*SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19–A12 uniquely select any sector.*

***Notes:***

1. *See Table 1, on page 11 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't cares in byte mode.*
5. *Unless otherwise noted, address bits A19–A11 are don't cares.*
6. *No unlock or command cycles required when in read mode.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when in the autoselect mode, or if DQ5 goes high (while providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to the read mode when in the unlock bypass mode.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
13. *The Erase Resume command is valid only during the Erase Suspend mode.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

## WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 13, on page 32 and the following subsections describe the functions of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an embedded program or erase operation is in progress or is completed.

### DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

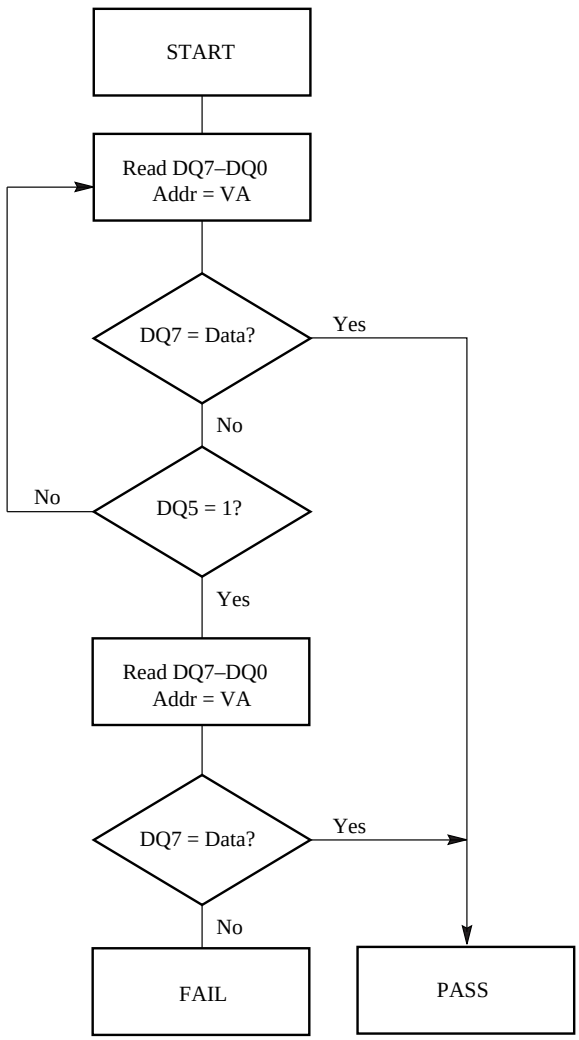
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 changes from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 19, on page 43, Data# Polling Timings (During Embedded Algorithms), in the “AC Characteristics” section illustrates this.

Table 13, on page 32 shows the outputs for Data# Polling on DQ7. Figure 5, on page 29 shows the Data# Polling algorithm.




***Notes:***

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

**Figure 5. Data# Polling Algorithm**

## RY/BY#: Ready/Busy#

RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to $V_{CC}$.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 13, on page 32 shows the outputs for RY/BY#. Figure 14, on page 38, Figure 17, on page 41 and Figure 18, on page 42 shows RY/BY# for reset, program, and erase operations, respectively.

## DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle (The system may use either OE# or CE# to control the read cycles). When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on "DQ7: Data# Polling" on page 29).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 13, on page 32 shows the outputs for Toggle Bit I on DQ6. Figure 6, on page 31 shows the toggle bit algorithm. Figure 20, on page 43 shows the toggle bit timing diagrams. Figure 21, on page 44 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on "DQ2: Toggle Bit II".

## DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ2 with each OE# or CE# read cycle.

DQ2 toggles when the system reads at addresses within those sectors that were selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 13, on page 32 to compare outputs for DQ2 and DQ6.

Figure 6, on page 31 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the "DQ6: Toggle Bit I" subsection. Figure 20, on page 43 shows the toggle bit timing diagram. Figure 21, on page 44 shows the differences between DQ2 and DQ6 in graphical form.

## Reading Toggle Bits DQ6/DQ2

Refer to Figure 6, on page 31 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device successfully completed the program or erase operation. If it is still toggling, the

device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 is not high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

## DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

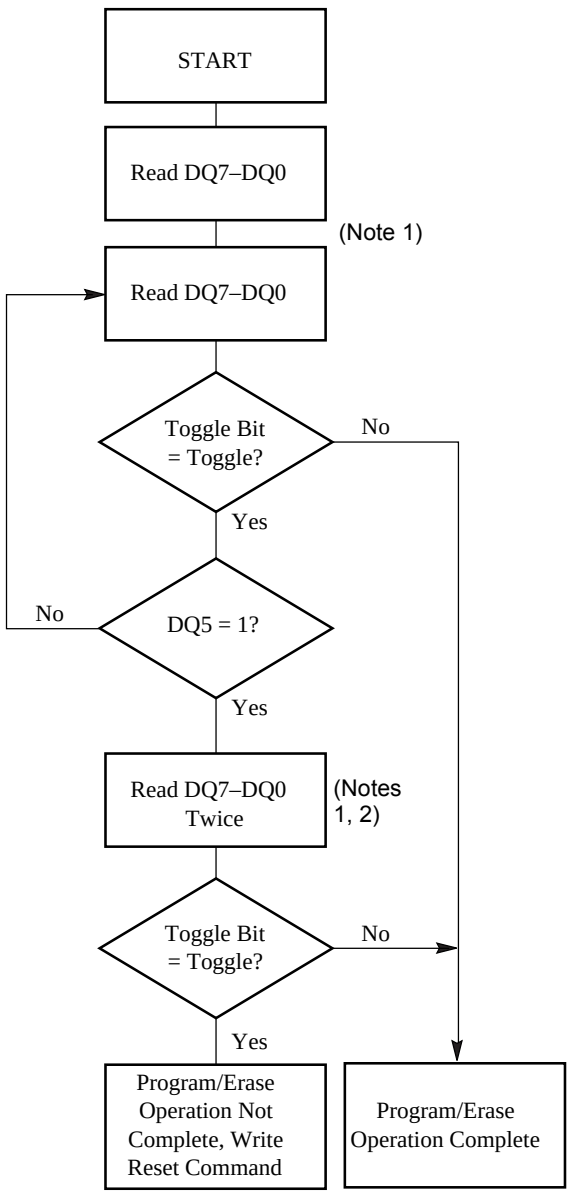
The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation exceeds the timing limits, DQ5 produces a “1.”

Under both these conditions, the system must issue the reset command to return the device to reading array data.

## DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation began. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1.” If the time between additional sector erase commands from the system are assumed to be less than 50 µs, the system need not monitor DQ3. See also the “Sector Erase Command Sequence” on page 26.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device accepted the command sequence, and then read DQ3. If DQ3 is “1”, the internally controlled erase cycle started; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0”, the device accepts additional sector erase commands. To ensure the command is accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 13, on page 32 shows the outputs for DQ3.




***Notes:***

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to “1”. See text.*

**Figure 6. Toggle Bit Algorithm**

**Table 13. Write Operation Status**

| Operation | | DQ7 (Note 2) | DQ6 | DQ5 (Note 1) | DQ3 | DQ2 (Note 2) | RY/BY# |
|---|---|---|---|---|---|---|---|
| Standard Mode | Embedded Program Algorithm | DQ7# | Toggle | 0 | N/A | No toggle | 0 |
| | Embedded Erase Algorithm | 0 | Toggle | 0 | 1 | Toggle | 0 |
| Erase Suspend Mode | Reading within Erase Suspended Sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| | Reading within Non-Erase Suspended Sector | Data | Data | Data | Data | Data | 1 |
| | Erase-Suspend-Program | DQ7# | Toggle | 0 | N/A | N/A | 0 |

***Notes:***

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation exceeds the maximum timing limits. See "DQ5: Exceeded Timing Limits" on page 31 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

$V_{CC}$ (Note 1). . . . . –0.5 V to +2.5 V

A9, OE#,
and RESET# (Note 2) . . . . . –0.5 V to +11.0 V

All other pins (Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Output Short Circuit Current (Note 3) . . . . . 100 mA

***Notes:***

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/O pins is $V_{CC}$ +0.5 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}$ +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9 is +11.0 V which may overshoot to +12.5 V for periods up to 20 ns. Maximum DC input voltage on pin WP#/ACC is +10.0 V which may overshoot to +11.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

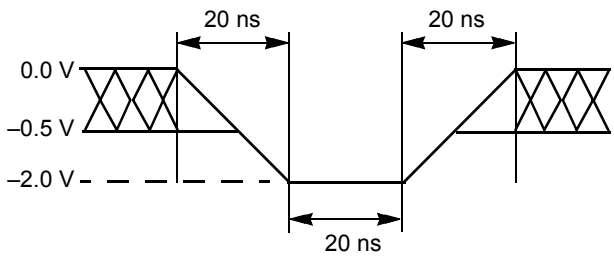



**Figure 7. Maximum Negative Overshoot Waveform**

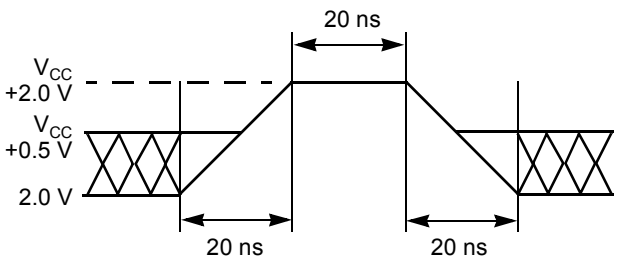



**Figure 8. Maximum Positive Overshoot Waveform**

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ($T_A$) . . . . . 0°C to +70°C

### Industrial (I) Devices

Ambient Temperature ($T_A$) . . . . . –40°C to +85°C

### $V_{CC}$ Supply Voltages

$V_{CC}$, all speed options . . . . . +1.8 V to +2.2 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS

### CMOS Compatible

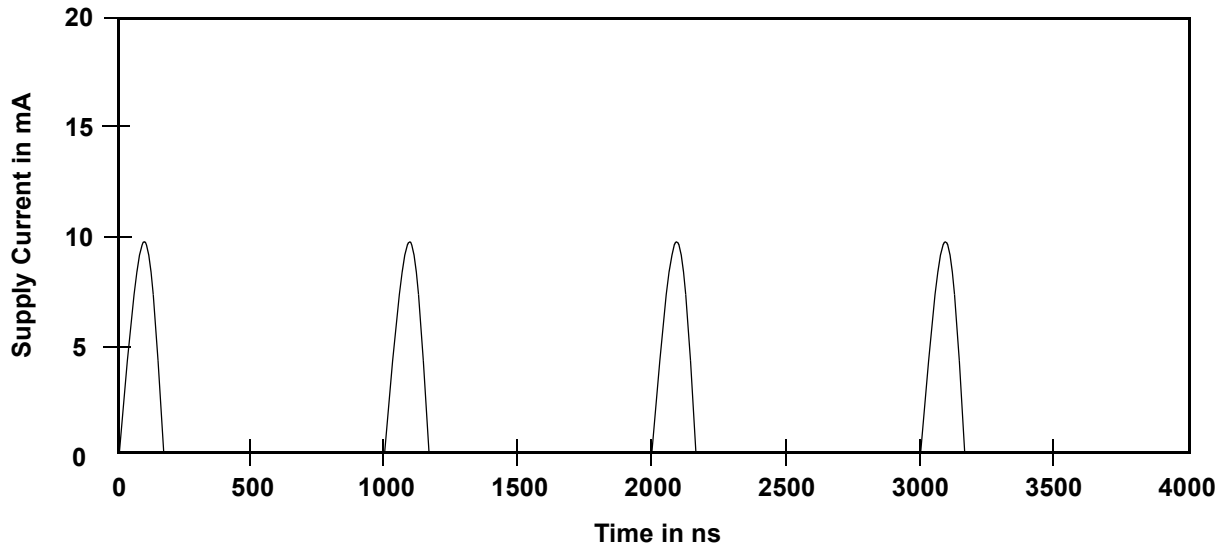
| Parameter | Description | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC\ max}$ | | | | ±1.0 | µA |
| $I_{LIT}$ | A9 Input Load Current | $V_{CC} = V_{CC\ max}$; A9 = 11.0 V | | | | 35 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC\ max}$ | | | | ±1.0 | µA |
| $I_{CC1}$ | $V_{CC}$ Active Read Current (Notes 1, 2) | CE# = $V_{IL}$, OE# = $V_{IH}$, Byte Mode | 5 MHz | | 5 | 10 | mA |
| | | | 1 MHz | | 1 | 3 | |
| | | CE# = $V_{IL}$, OE# = $V_{IH}$, Word Mode | 5 MHz | | 5 | 10 | |
| | | | 1 MHz | | 1 | 3 | |
| $I_{CC2}$ | $V_{CC}$ Active Write Current (Notes 2, 3, 5) | CE# = $V_{IL}$, OE# = $V_{IH}$ | | | 20 | 30 | mA |
| $I_{CC3}$ | $V_{CC}$ Standby Current (Note 2) | CE#, RESET# = $V_{CC}$±0.2 V | | | 1 | 5 | µA |
| $I_{CC4}$ | $V_{CC}$ Reset Current (Note 2) | RESET# = $V_{SS}$ ± 0.2 V | | | 1 | 5 | µA |
| $I_{CC5}$ | Automatic Sleep Mode (Notes 2, 3) | $V_{IH} = V_{CC}$ ± 0.2 V; $V_{IL} = V_{SS}$ ± 0.2 V | | | 1 | 5 | µA |
| $V_{IL}$ | Input Low Voltage | | | –0.5 | | 0.2 x $V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage | | | 0.8 x $V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| $V_{HH}$ | Voltage for WP#/ACC Sector Protect/Unprotect and Program Acceleration | | | 8.5 | | 9.5 | V |
| $V_{ID}$ | Voltage for Autoselect and Temporary Sector Unprotect | $V_{CC}$ = 2.0 V | | 9.0 | | 11.0 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100 µA, $V_{CC} = V_{CC\ min}$ | | | | 0.1 | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –100 µA, $V_{CC} = V_{CC\ min}$ | | $V_{CC}$–0.1 | | | |
| $V_{LKO}$ | Low $V_{CC}$ Lock-Out Voltage (Note 4) | | | 1.2 | | 1.5 | V |

***Notes:***

1. *The $I_{CC}$ current listed is typically less than 1 mA/MHz, with OE# at $V_{IL}$. Typical $V_{CC}$ is 2.0 V.*
2. *The maximum $I_{CC}$ specifications are tested with $V_{CC} = V_{CC}max$.*
3. *$I_{CC}$ active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for $t_{ACC}$ + 50 ns.*
5. *Not 100% tested.*

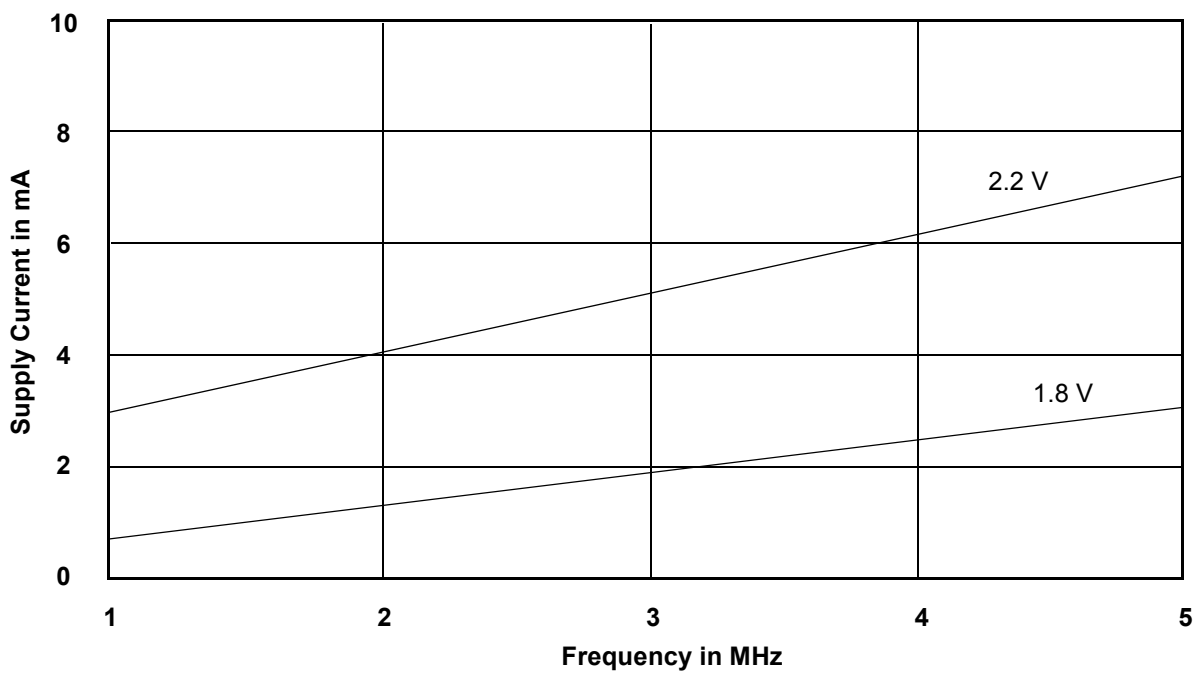
## DC CHARACTERISTICS (Continued)

### Zero Power Flash




***Note:*** *Addresses are switching at 1 MHz*

**Figure 9. $I_{CC1}$ Current vs. Time (Showing Active and Automatic Sleep Currents)**




***Note:*** *T = 25 °C*

**Figure 10. Typical $I_{CC1}$ vs. Frequency**

## TEST CONDITIONS

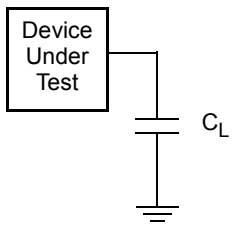



**Figure 11. Test Setup**

**Table 14. Test Specifications**

| Test Condition | -90, -100 | -120, -150 | Unit |
|---|---|---|---|
| Output Load | 1 TTL gate | | |
| Output Load Capacitance, $C_L$ (including jig capacitance) | 30 | 100 | pF |
| Input Rise and Fall Times | 5 | | ns |
| Input Pulse Levels | 0.0–2.0 | | V |
| Input timing measurement reference levels | 1.0 | | V |
| Output timing measurement reference levels | 1.0 | | V |

## Key To Switching Waveforms

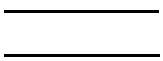
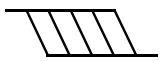
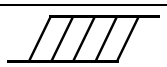
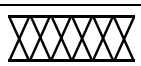
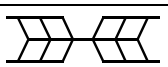
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Steady | |
|  | Changing from H to L | |
|  | Changing from L to H | |
|  | Don't Care, Any Change Permitted | Changing, State Unknown |
|  | Does Not Apply | Center Line is High Impedance State (High Z) |




**Figure 12. Input Waveforms and Measurement Levels**

## AC CHARACTERISTICS

### Read Operations

| Parameter | | Description | | Test Setup | | Speed Option | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std | | | | | -90 | -100 | -120 | -150 | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time (Note 1) | | | Min | 90 | 100 | 120 | 150 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | | CE# = $V_{IL}$<br>OE# = $V_{IL}$ | Max | 90 | 100 | 120 | 150 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | | OE# = $V_{IL}$ | Max | 90 | 100 | 120 | 150 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | | Max | 35 | 35 | 50 | 65 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z (Note 1) | | | Max | 16 | | | | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z (Note 1) | | | Max | 16 | | | | ns |
| | $t_{OEH}$ | Output Enable Hold Time (Note 1) | Read | | Min | 0 | | | | ns |
| | | | Toggle and Data# Polling | | Min | 30 | | | | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1) | | | Min | 0 | | | | ns |

***Notes:***

1. *Not 100% tested.*
2. *See Figure 11, on page 36 and Table 14, on page 36 for test specifications.*

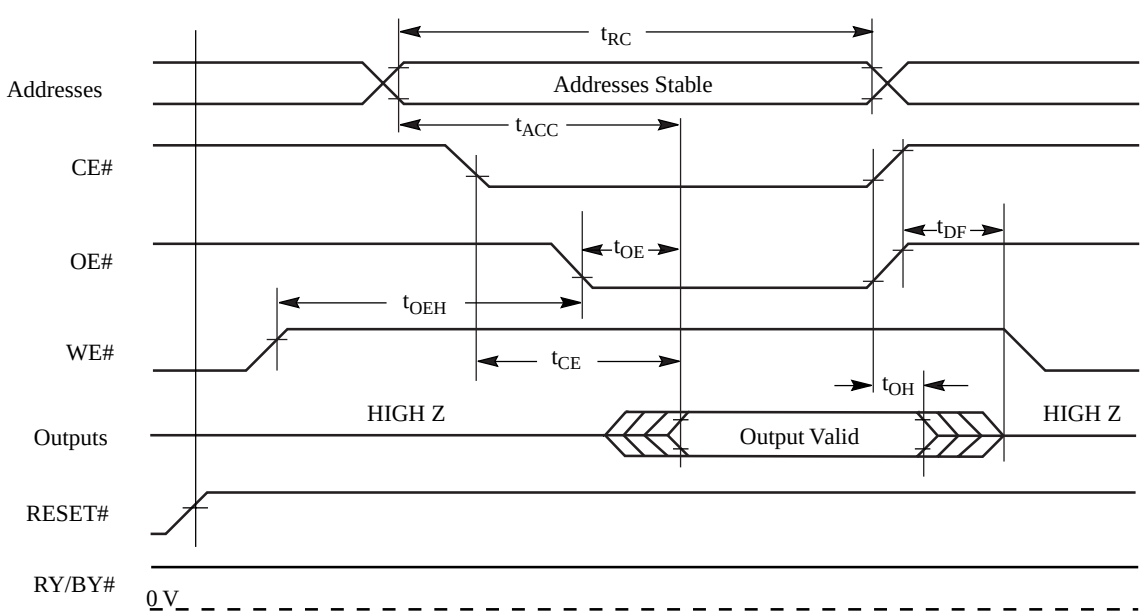



**Figure 13. Read Operations Timings**

## AC CHARACTERISTICS

### Hardware Reset (RESET#)

| Parameter | | Description | Test Setup | | All Speed Options | Unit |
|---|---|---|---|---|---|---|
| JEDEC | Std | | | | | |
| | $t_{READY}$ | RESET# Pin Low (During Embedded Algorithms) to Read or Write (see Note) | | Max | 20 | µs |
| | $t_{READY}$ | RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (see Note) | | Max | 500 | ns |
| | $t_{RP}$ | RESET# Pulse Width | | Min | 500 | ns |
| | $t_{RH}$ | RESET# High Time Before Read (see Note) | | Min | 200 | ns |
| | $t_{RB}$ | RY/BY# Recovery Time | | Min | 0 | ns |

***Note:*** *Not 100% tested.*

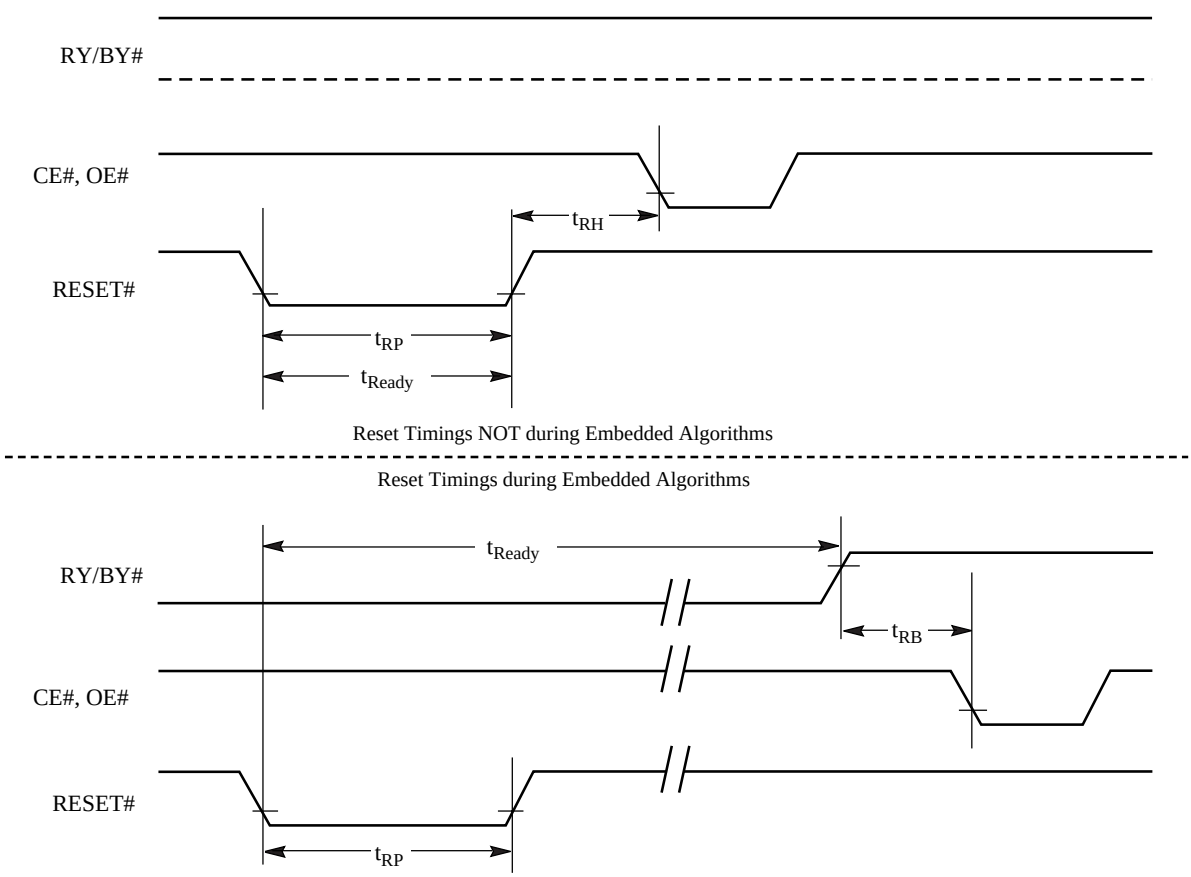



**Figure 14. RESET# Timings**

## AC CHARACTERISTICS

### Word/Byte Configuration (BYTE#)

| Parameter | | Description | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| JEDEC | Std | | | -90 | -100 | -120 | -150 | |
| | $t_{ELFL}/t_{ELFH}$ | CE# to BYTE# Switching Low or High | Max | 10 | | | | ns |
| | $t_{FLQZ}$ | BYTE# Switching Low to Output HIGH Z | Max | 50 | 50 | 60 | 60 | ns |
| | $t_{FHQV}$ | BYTE# Switching High to Output Active | Min | 90 | 100 | 120 | 150 | ns |

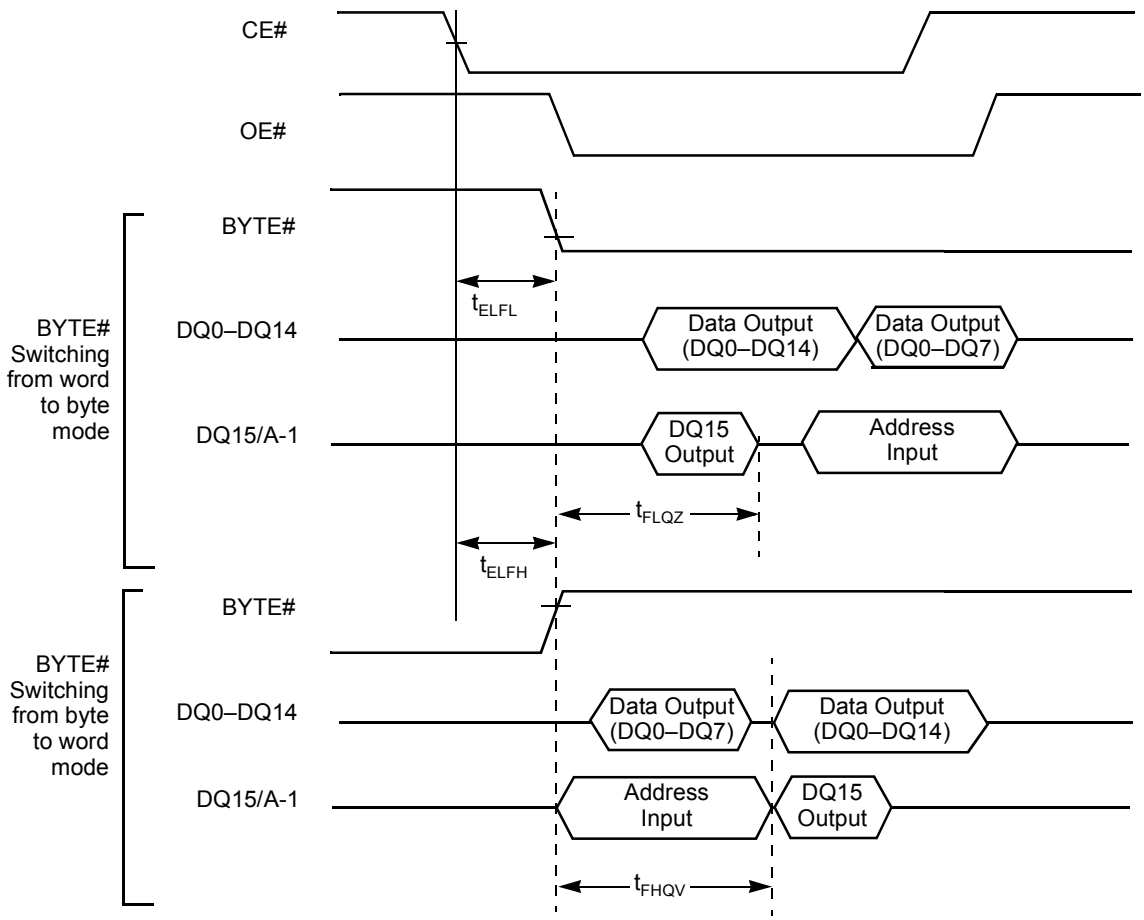
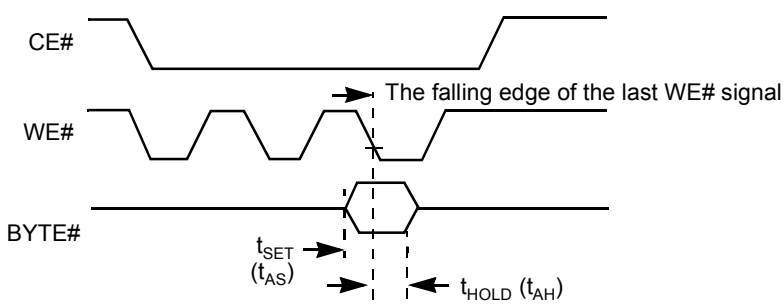



**Figure 15. BYTE# Timings for Read Operations**




***Note:*** *Refer to the Erase/Program Operations table for $t_{AS}$ and $t_{AH}$ specifications.*

**Figure 16. BYTE# Timings for Write Operations**

## AC CHARACTERISTICS

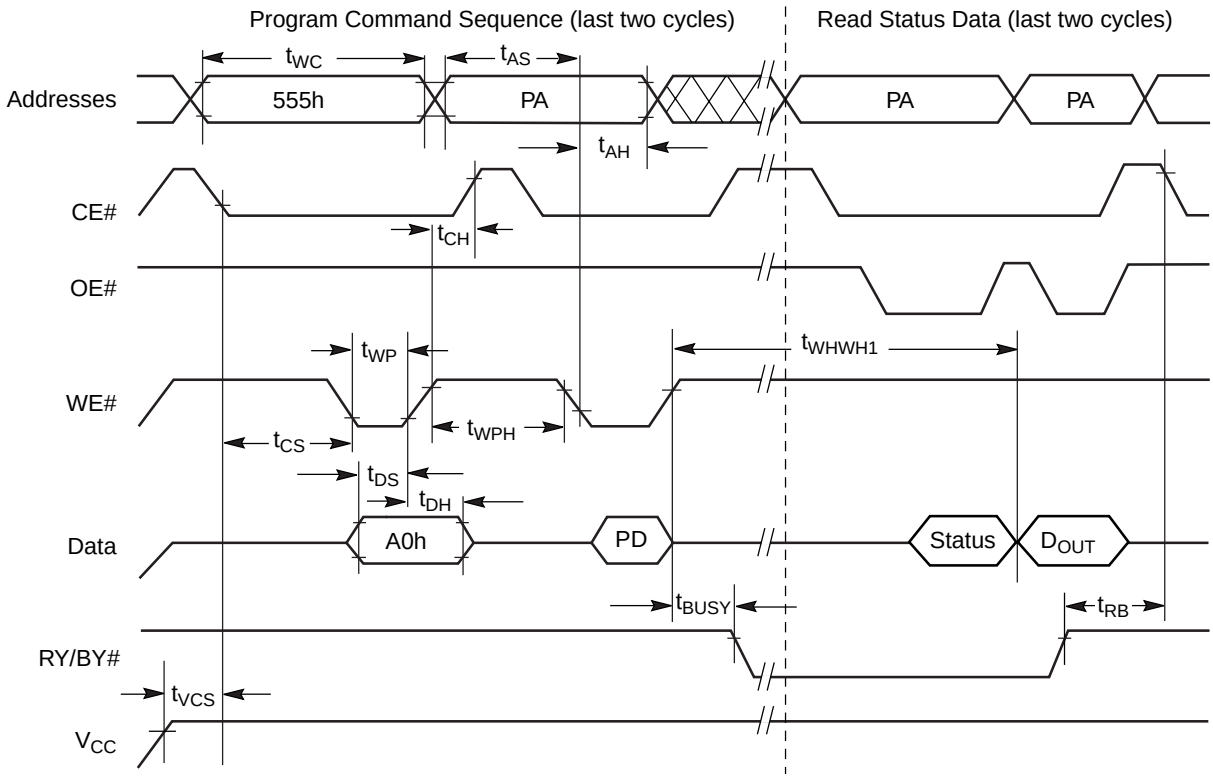
### Erase/Program Operations

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std | | | | -90 | -100 | -120 | -150 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 90 | 100 | 120 | 150 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | | Min | 50 | 50 | 60 | 70 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | Min | 50 | 50 | 60 | 70 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup Time | | Min | 0 | | | | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold Time | | Min | 0 | | | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | Min | 50 | 50 | 60 | 70 | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation (Notes 1, 2) | Byte | Typ | 10 | | | | µs |
| | | | Word | Typ | 12 | | | | |
| | | Accelerated Program Operation, Byte or Word (Note 2) | | Typ | 8 | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Notes 1, 2) | | Typ | 2 | | | | sec |
| | $t_{VCS}$ | $V_{CC}$ Setup Time | | Min | 50 | | | | µs |
| | $t_{RB}$ | Recovery Time from RY/BY# | | Min | 0 | | | | ns |
| | $t_{BUSY}$ | Program/Erase Valid to RY/BY# Delay | | Min | 200 | | | | ns |

***Notes:***

1. *Not 100% tested.*
2. *See "Erase And Programming Performance" on page 48 for more information.*

## AC CHARACTERISTICS

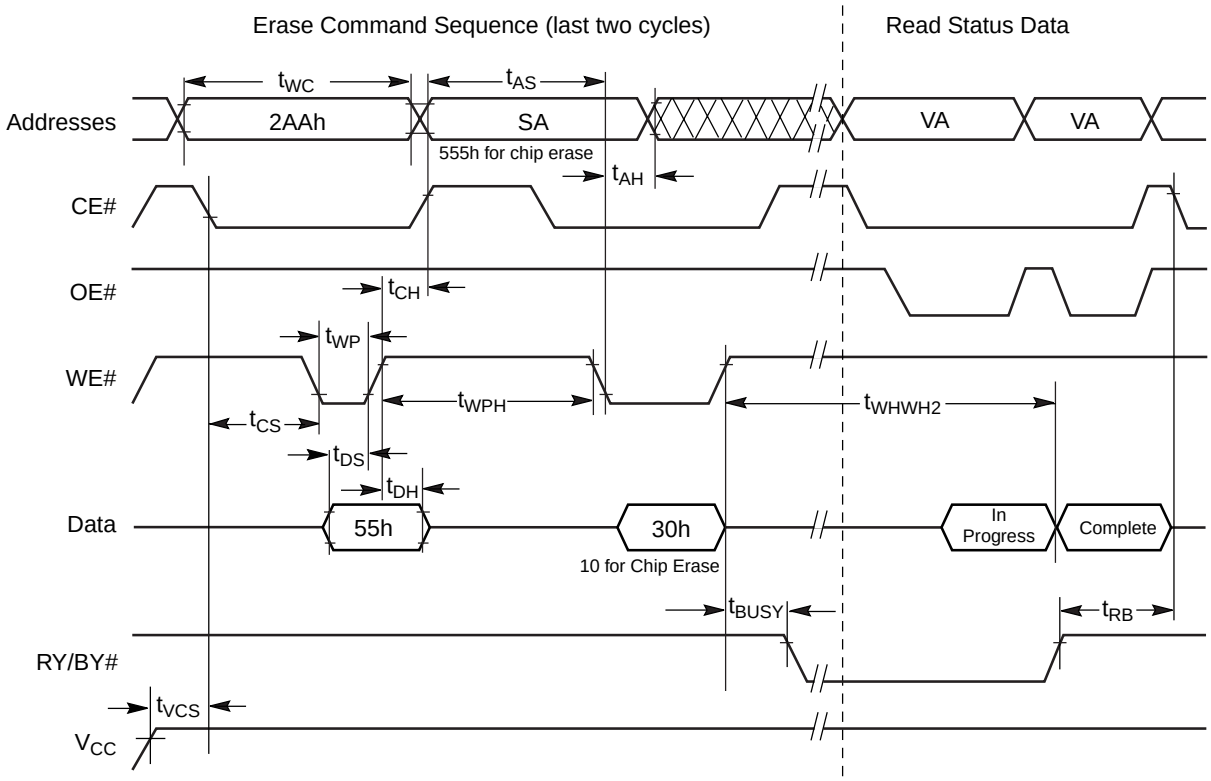



***Notes:***

1. *PA = program address, PD = program data, $D_{OUT}$ is the true data at the program address.*
2. *Illustration shows device in word mode.*

**Figure 17. Program Operation Timings**

## AC CHARACTERISTICS

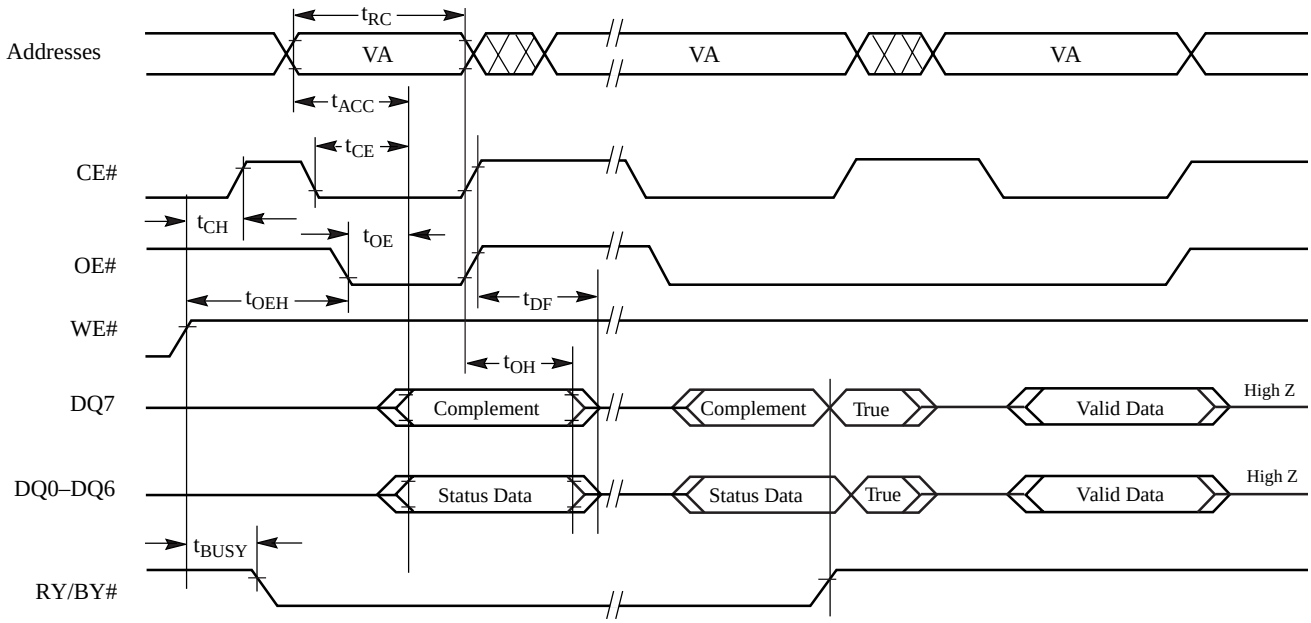



***Notes:***

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*
2. *Illustration shows device in word mode.*

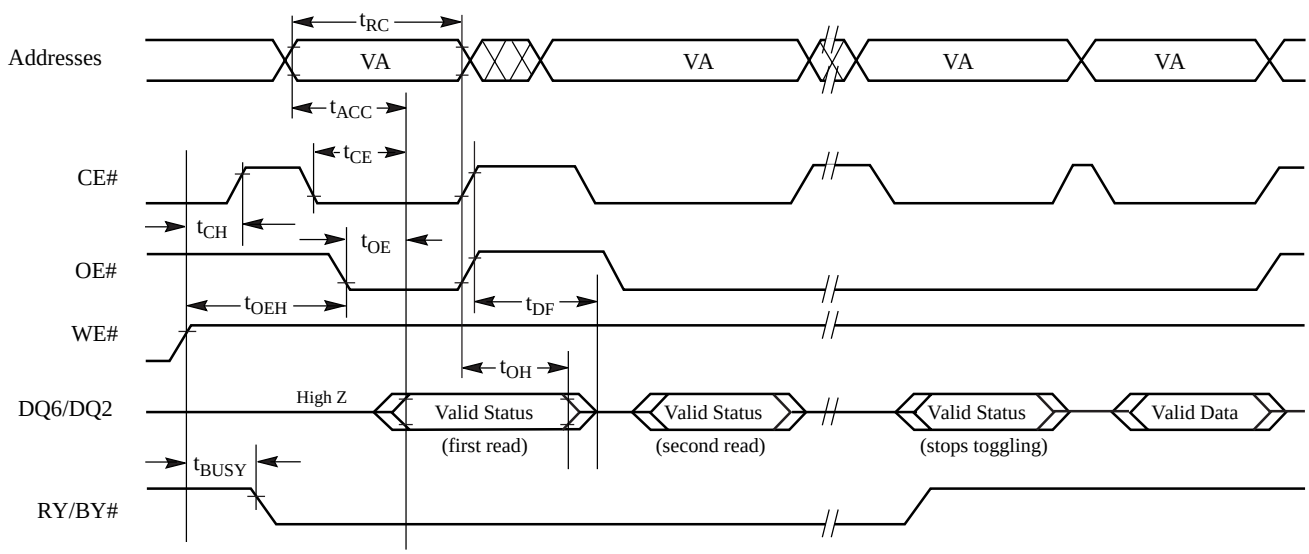
**Figure 18. Chip/Sector Erase Operation Timings**

## AC CHARACTERISTICS




***Note:*** *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

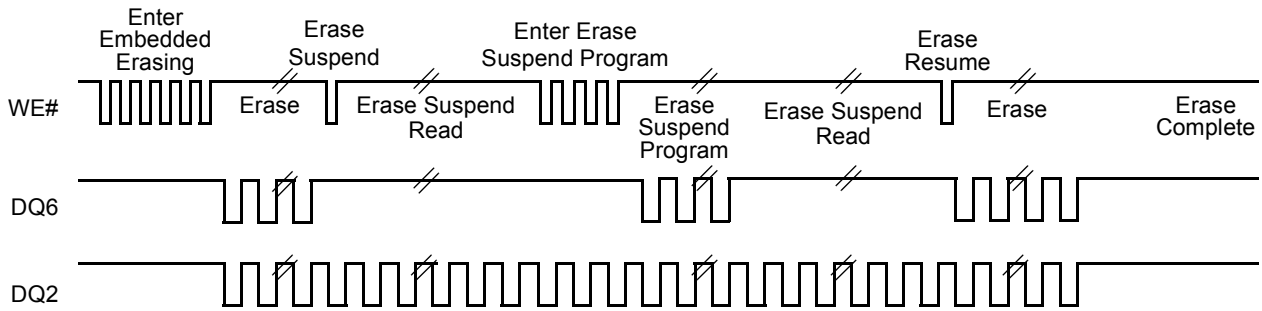
**Figure 19. Data# Polling Timings (During Embedded Algorithms)**




***Note:*** *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

**Figure 20. Toggle Bit Timings (During Embedded Algorithms)**

## AC CHARACTERISTICS




***Note:*** *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

**Figure 21. DQ2 vs. DQ6**

## Temporary Sector Unprotect

| Parameter | | Description | | All Speed Options | Unit |
|---|---|---|---|---|---|
| JEDEC | Std | | | | |
| | $t_{VIDR}$ | $V_{ID}$ Rise and Fall Time | Min | 500 | ns |
| | $t_{VHH}$ | $V_{HH}$ Rise and Fall Time | Min | 500 | ns |
| | $t_{RSP}$ | RESET# Setup Time for Temporary Sector Unprotect | Min | 4 | µs |

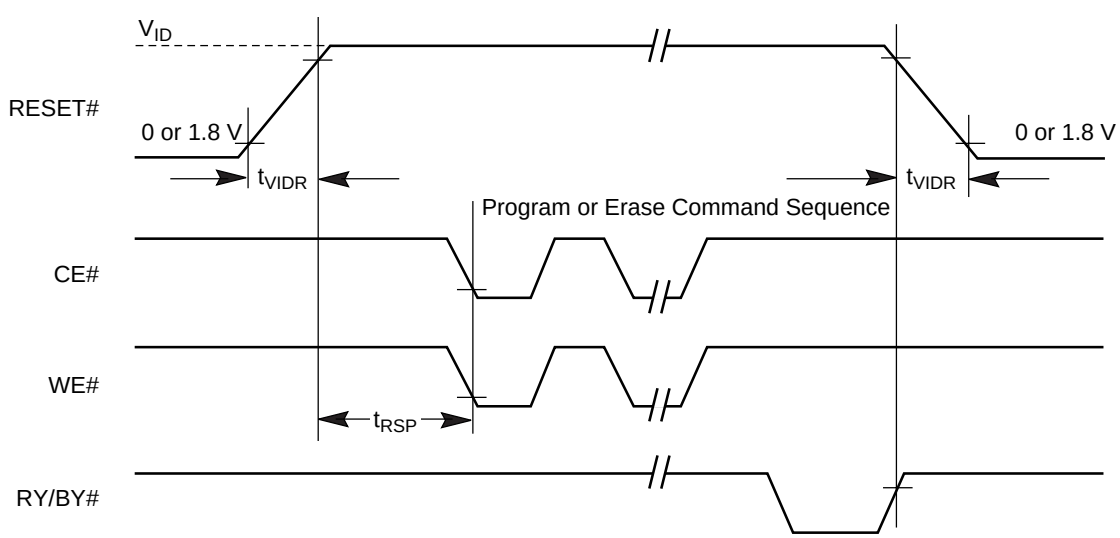



**Figure 22. Temporary Sector Unprotect Timing Diagram**

## AC CHARACTERISTICS

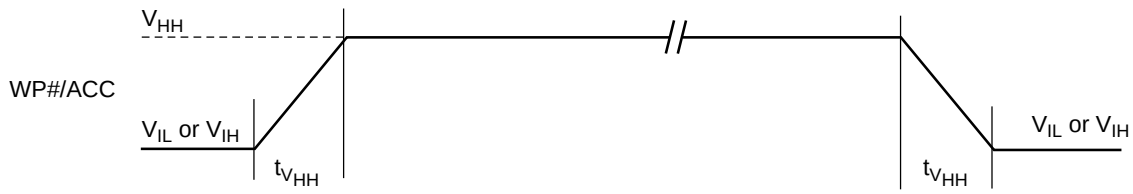
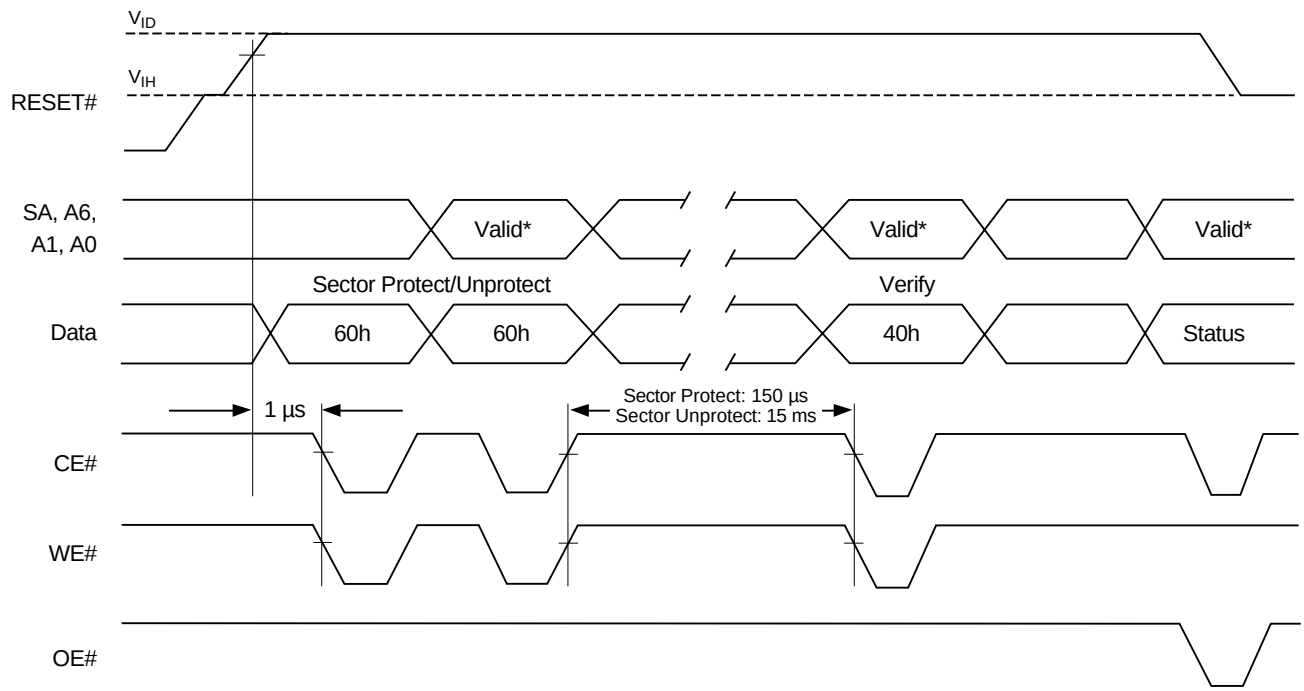



**Figure 23. Accelerated Program Timing Diagram**




* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

**Figure 24. Sector Protect/Unprotect Timing Diagram**

## AC CHARACTERISTICS

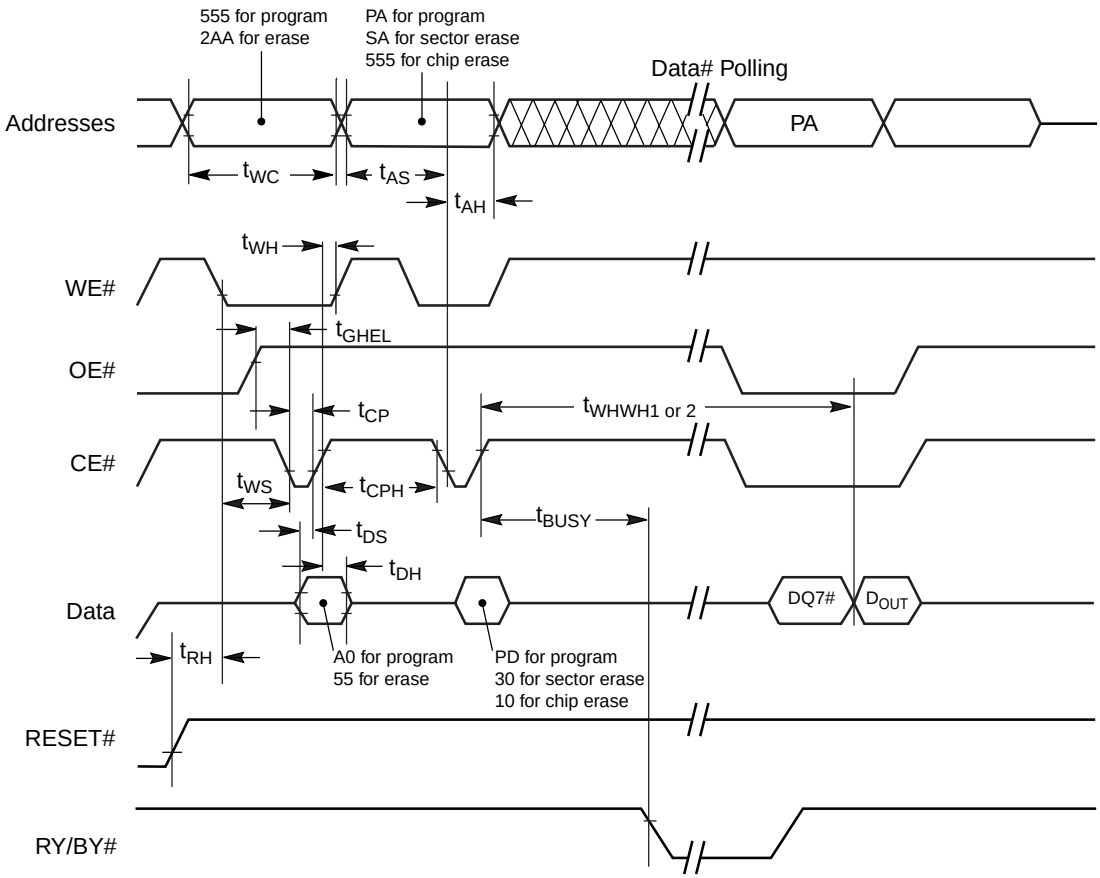
### Alternate CE# Controlled Erase/Program Operations

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std | | | | -90 | -100 | -120 | -150 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 90 | 100 | 120 | 150 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | | Min | 50 | 50 | 60 | 70 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | | Min | 50 | 50 | 60 | 70 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup Time | | Min | 0 | | | | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold Time | | Min | 0 | | | | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | | Min | 50 | 50 | 60 | 70 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | CE# Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation (Notes 1, 2) | Byte | Typ | 10 | | | | µs |
| | | | Word | Typ | 12 | | | | |
| | | Accelerated Program Operation, Byte or Word (Note 2) | | Typ | 8 | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Notes 1, 2) | | Typ | 2 | | | | sec |

***Notes:***

1. *Not 100% tested.*
2. *See "Erase And Programming Performance" on page 48 for more information.*

## AC CHARACTERISTICS




***Notes:***

1. *PA = program address, PD = program data, DQ7# = complement of the data written, $D_{OUT}$ = data written*
2. *Figure indicates the last two bus cycles of command sequence.*
3. *Word mode address used as an example.*

**Figure 25. Alternate CE# Controlled Write Operation Timings**

## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | | Typ (Note 1) | Max (Note 2) | Unit | Comments |
|---|---|---|---|---|---|
| Sector Erase Time | | 2 | 15 | s | Excludes 00h programming prior to erasure (Note 4) |
| Chip Erase Time | | 70 | | s | |
| Byte Programming Time | | 10 | 300 | µs | Excludes system level overhead (Note 5) |
| Word Programming Time | | 12 | 360 | µs | |
| Accelerated Program Time, Word/Byte | | 8 | 240 | µs | |
| Chip Programming Time (Note 3) | Byte Mode | 20 | 160 | s | |
| | Word Mode | 14 | 120 | s | |

***Notes:***

1. *Typical program and erase times assume the following conditions: 25°C, 2.0 V $V_{CC}$, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, $V_{CC}$ = 1.8 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 12, on page 28 for further information on command definitions.*
6. *The device has a minimum guaranteed erase and program cycle endurance of 1,000,000 cycles.*

## LATCHUP CHARACTERISTICS

| Description | Min | Max |
|---|---|---|
| Input voltage with respect to $V_{SS}$ on all pins except I/O pins (including A9, OE#, and RESET#) | –1.0 V | 11.0 V |
| Input voltage with respect to $V_{SS}$ on all I/O pins | –0.5 V | $V_{CC}$ + 0.5 V |
| $V_{CC}$ Current | –100 mA | +100 mA |

*Includes all pins except $V_{CC}$. Test conditions: $V_{CC}$ = 1.8 V, one pin at a time.*

## TSOP PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 7.5 | 9 | pF |

***Notes:***

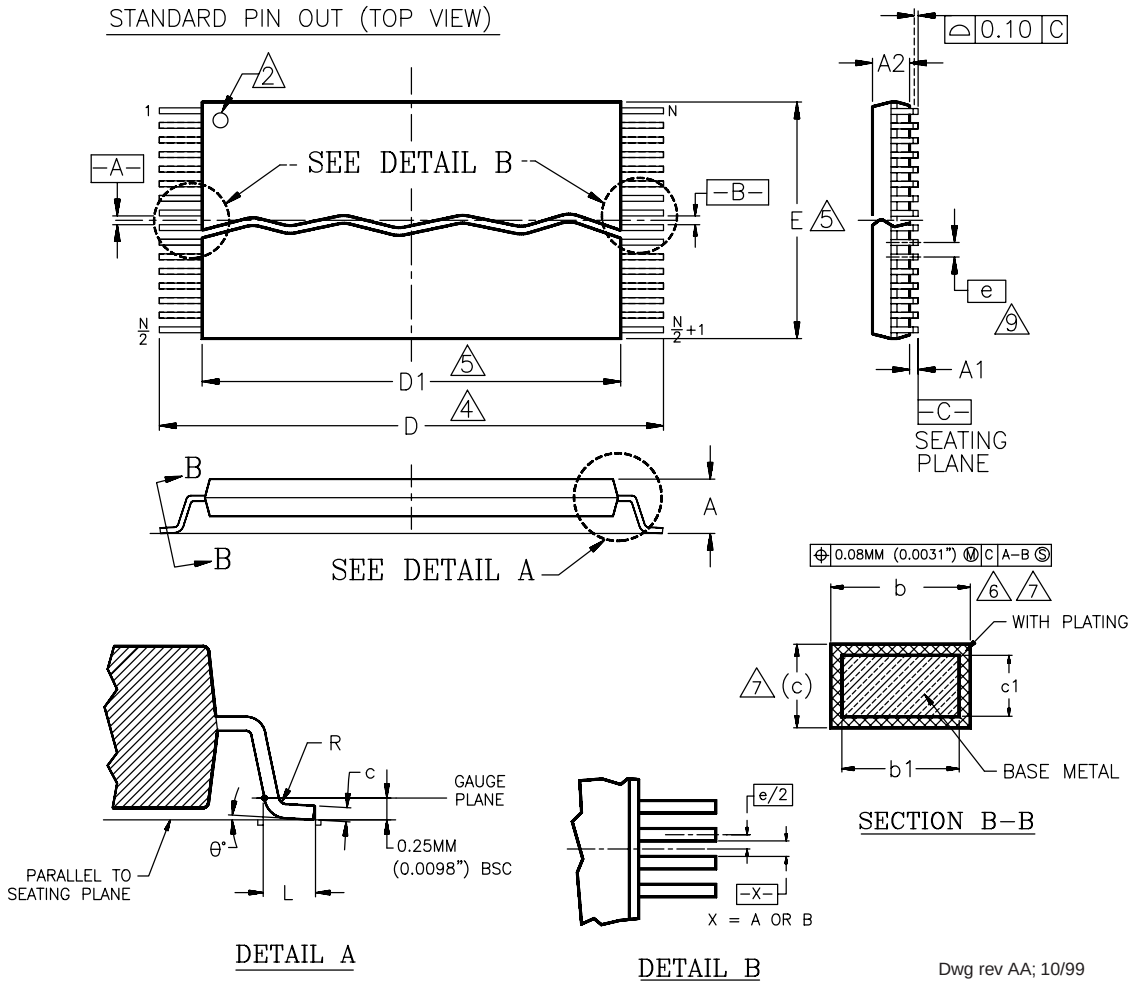
1. *Sampled, not 100% tested.*
2. *Test conditions $T_A$ = 25°C, f = 1.0 MHz.*

## DATA RETENTION

| Parameter | Test Conditions | Min | Unit |
|---|---|---|---|
| Minimum Pattern Data Retention Time | 150°C | 10 | Years |
| | 125°C | 20 | Years |

## PHYSICAL DIMENSIONS*

### TS 048—48-Pin Standard TSOP




| Package | TS 048 | | |
|---|---|---|---|
| Jedec | MO-142 (B) DD | | |
| Symbol | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.30 | 18.40 | 18.50 |
| E | 11.90 | 12.00 | 12.10 |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | 3° | 5° |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

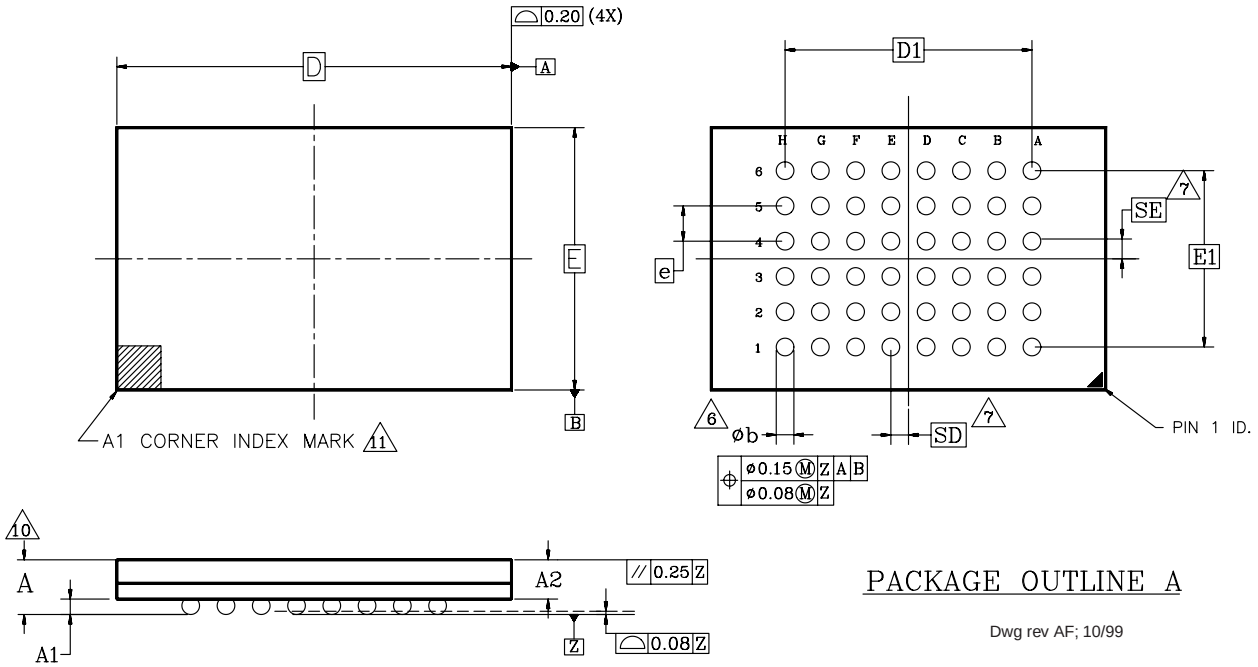
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

## PHYSICAL DIMENSIONS

### FBC048—48-Ball Fine-Pitch Ball Grid Array (FBGA)
### 8 x 9 mm package




PACKAGE OUTLINE A

Dwg rev AF; 10/99

| PACKAGE | FBC 048 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| | 8.00mmx9.00mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | — | — | 1.20 | OVERALL THICKNESS |
| A1 | 0.20 | — | — | BALL HEIGHT |
| A2 | 0.84 | — | 0.94 | BODY THICKNESS |
| D | 9.00 BSC | | | BODY SIZE |
| E | 8.00 BSC | | | BODY SIZE |
| D1 | 5.60 BSC | | | BALL FOOTPRINT |
| E1 | 4.00 BSC | | | BALL FOOTPRINT |
| MD | 8 | | | ROW MATRIX SIZE D DIRECTION |
| ME | 6 | | | ROW MATRIX SIZE E DIRECTION |
| N | 48 | | | TOTAL BALL COUNT |
| b | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| e | 0.80 BSC | | | BALL PITCH |
| SD / SE | 0.40 BSC | | | SOLDER BALL PLACEMENT |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.
11. A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

# REVISION SUMMARY

## Revision A (December 1998)

Initial release.

## Revision A+1 (January 1999)

### Distinctive Characteristics

*WP#/ACC pin:* In the third subbullet, deleted reference to increased erase performance.

### Device Bus Operations

*Accelerated Program and Erase Operations:* Deleted all references to accelerated erase.

*Sector/Sector Block Protection and Unprotection:* Changed section name and text to include tables and references to sector block protection and unprotection.

### AC Characteristics

*Accelerated Program Timing Diagram:* Deleted reference in title to accelerated erase.

## Revision A+2 (March 23, 1999)

### Connection Diagrams

Corrected the TSOP pinout on pins 13 and 14.

## Revision A+3 (April 12, 1999)

### Global

Modified the description of accelerated programming to emphasize that it is intended only to speed in-system programming of the device during the system production process.

### Distinctive Characteristics

*Secured Silicon (SecSi) Sector bullet:* Added the 8-byte unique serial number to description.

### Device Bus Operations table

Modified Note 3 to indicate sector protection behavior when $V_{IH}$ is asserted on WP#/ACC. Applied Note 3 to the WP#/ACC column for write operations.

### Ordering Information

Added the “N” designator to the optional processing section.

### Secured Silicon (SecSi) Sector Flash Memory Region

Modified explanatory text to indicate that devices now have an 8-byte unique ESN in addition to the 16-byte random ESN. Added table for address range clarification.

## Revision A+4 (May 14, 1999)

### Global

Deleted all references to the unique ESN.

## Revision A+5 (July 23, 1999)

### Global

Added 90 ns speed option.

## Revision A+6 (September 1, 1999)

### AC Characteristics

*Hardware Reset (RESET#) table:* Deleted $t_{RPD}$ specification. *Erase/Program Operations table:* Deleted $t_{OES}$ specification.

## Revision A+7 (September 7, 1999)

### Distinctive Characteristics

*Ultra low power consumption bullet:* Corrected values to match those in the DC Characteristics table.

### AC Characteristics

*Alternate CE# Controlled Erase/Program Operations:* Deleted $t_{OES}$ specification.

## Revision B (December 14, 1999)

### AC Characteristics—Figure 17. Program Operations Timing and Figure 18. Chip/Sector Erase Operations

Deleted $t_{GHWL}$ and changed OE# waveform to start at high.

### Physical Dimensions

Replaced figures with more detailed illustrations.

## Revision C (February 21, 2000)

Removed “Advance Information” designation from data sheet. Data sheet parameters are now stable; only speed, package, and temperature range combinations are expected to change in future revisions.

### Device Bus Operations table

Changed standby voltage specification to $V_{CC}$ ± 0.2 V.

### Standby Mode

Changed standby voltage specification to $V_{CC}$ ± 0.2 V.

### DC Characteristics table

Changed test conditions for $I_{CC3}$, $I_{CC4}$, $I_{CC5}$ to $V_{CC}$ ± 0.2 V.

## Revision C+1 (November 14, 2000)

### Global

Added dash to speed options and OPNs. Added table of contents.

### AC Characteristics—Read Operations

Changed $t_{DF}$ to 16 ns for all speeds.

## Revision C+2 (June 11, 2002)

### Secured Silicon (SecSi) Sector Flash Memory Region

Deleted reference to A-1 not being used in addressing, and to address bits that are don't cares. In Table 7, changed lower address bit for user-defined code to 08h (word mode) and 010h (byte mode).

## Revision C+3 (November 1, 2004)

### Global

Added Colophon.

Added reference links.

### Ordering Information

Added temperature ranges for Pb-free Package

### Valid Combinations for TSOP Packages

Added ED, and EF combinations.

### Valid Combinations for FBGA Packages

Added WCD, and WCF to Order Number column, and added D, and F to Package Marking column.

***Colophon***

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