Am29PDLI29H

Data Sheet

RETIRED PRODUCT

This product has been retired and is not available for designs. For new and current designs, S29PL129J supersedes Am29PDL129H and is the factory-recommended migration path. Please refer to the S29PL129J datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with “Am” and “MBM”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number 26842 **Revision** B **Amendment** +3 **Issue Date** November 2, 2005

THIS PAGE LEFT INTENTIONALLY BLANK.

Am29PDL129H

128 Megabit (8 M x 16-Bit) CMOS 3.0 Volt-only, Page Mode Simultaneous Read/Write Flash Memory with Enhanced VersatileIO™ Control and Dual Chip Enable Inputs

This product has been retired and is not available for designs. For new and current designs, S29PL129J supersedes Am29PDL129H and is the factory-recommended migration path. Please refer to the S29PL129J datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **128 Mbit Page Mode device**
  - Page size of 8 words: Fast page read access from random locations within the page
- **Dual Chip Enable inputs**
  - Two CE# inputs control selection of each half of the memory space
- **Single power supply operation**
  - Full Voltage range: 2.7 to 3.6 volt read, erase, and program operations for battery-powered applications
- **Simultaneous Read/Write Operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- **FlexBank Architecture**
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank 1A: 48 Mbit (32 Kw x 96)
  - Bank 1B: 16 Mbit (4 Kw x 8 and 32 Kw x 31)
  - Bank 2A: 16 Mbit (4 Kw x 8 and 32 Kw x 31)
  - Bank 2B: 48 Mbit (32 Kw x 96)
- **Enhanced VersatileI/O™ (V_{IO}) Control**
  - Output voltage generated and input voltages tolerated on all control inputs and I/Os is determined by the voltage on the V_{IO} pin
  - V_{IO} options at 1.8 V and 3 V I/O
- **SecSi™ (Secured Silicon) Sector region**
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words
- **Both top and bottom boot blocks in one device**
- **Manufactured on 0.13 µm process technology**
- **20-year data retention at 125°C**
- **Minimum 1 million erase cycle guarantee per sector**

PERFORMANCE CHARACTERISTICS

- **High Performance**
  - Page access times as fast as 20 ns
  - Random access times as fast as 55 ns
- **Power consumption (typical values at 10 MHz)**
  - 45 mA active read current
  - 15 mA program/erase current
  - 1 µA typical standby mode current

SOFTWARE FEATURES

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F and Am29LV families
- **CFI (Common Flash Interface) complaint**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data
- **WP#/ACC (Write Protect/Acceleration) input**
  - At V_{IL}, hardware level protection for the first and last two 4K word sectors.
  - At V_{IH}, allows removal of sector protection
  - At V_{HH}, provides accelerated programming in a factory setting
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- **Package options**
  - 80-ball Fine-pitch BGA
  - Multi Chip Packages (MCP)

Publication Number: **26842** Rev: **B** Amendment/ **+3**
Issue Date: **November 2, 2005**

GENERAL DESCRIPTION

The Am29PDL129H is a 128 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 8 Mwords. The device is offered in an 80-ball Fine-pitch BGA package, and various multi-chip packages. The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V V_{PP} is not required for write or erase operations.

The device offers fast page access times of 20 to 30 ns, with corresponding random access times of 55 to 85 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE1#, CE2#), write enable (WE#) and output enable (OE#) controls. Dual Chip Enables allow access to two 64 Mbit partitions of the 128 Mbit memory space.

Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

Chip Enable Configuration	
CE1# Control	**CE2# Control**
Bank 1A 48 Mbit (32 Kw x 96)	**Bank 2A** 16 Mbit (4 Kw x 8 and 32 Kw x 31)
Bank 1B 16 Mbit (4 Kw x 8 and 32 Kw x 31)	**Bank 2B** 48 Mbit (32 Kw x 96)

Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V or 2.7 V to 3.3 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combined years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

Note: *The next-generation S29PL129J will have a different bank configuration, as follows:*

Chip Enable Configuration	
CE1# Control	**CE2# Control**
Bank 1A 16 Mbit (4 Kw x 8 and 32 Kw x 31)	**Bank 2A** 48 Mbit (32 Kw x 96)
Bank 1B 48 Mbit (32 Kw x 96)	**Bank 2B** 16 Mbit (4 Kw x 8 and 32 Kw x 31)

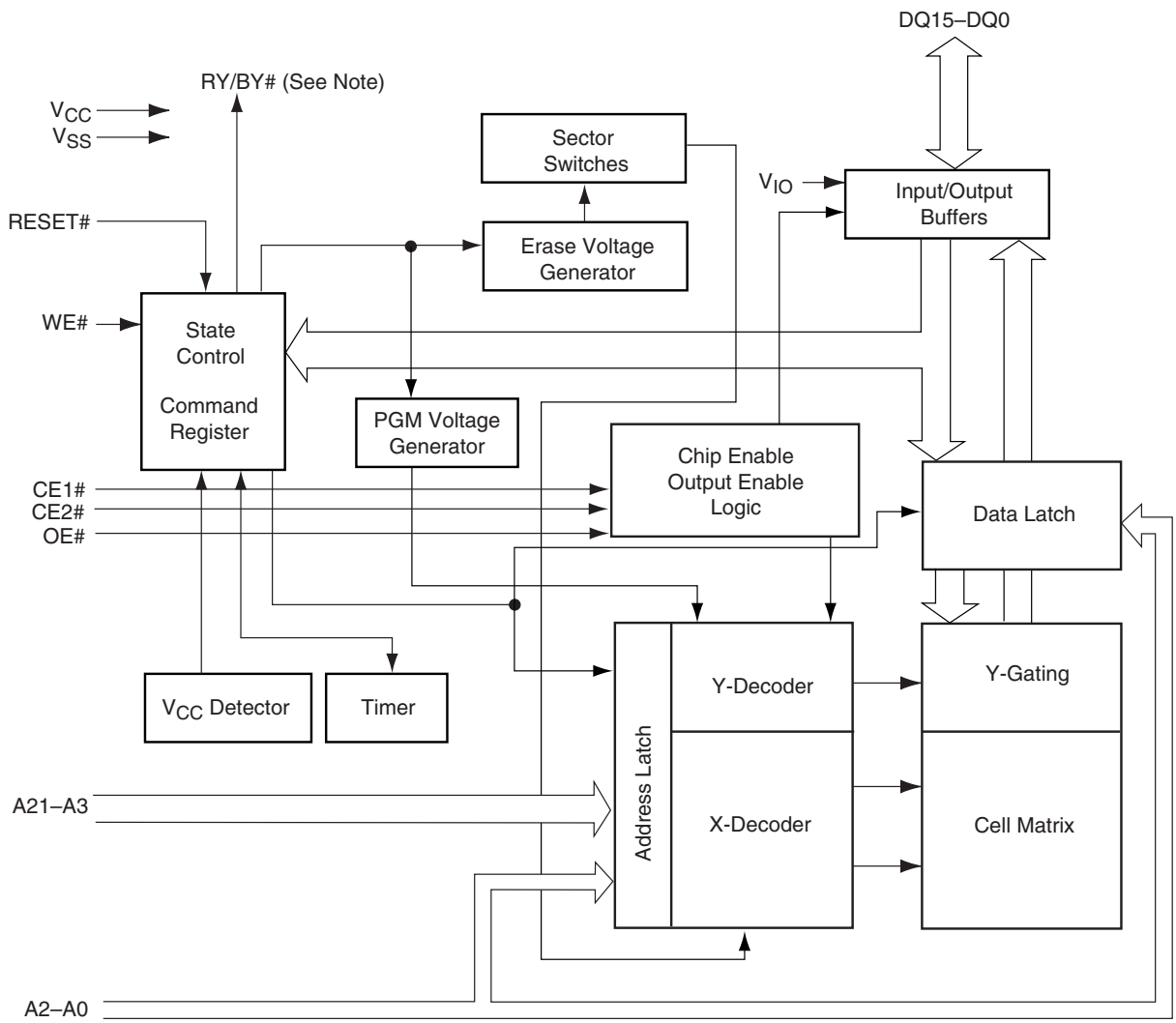
TABLE OF CONTENTS

Product Selector Guide 5
Block Diagram 5
Simultaneous Operation Block Diagram 6
Connection Diagrams 7
Pin Description 8
Logic Symbol 8
Ordering Information 9
Device Bus Operations 10
Table 1. Am29PDL129H Device Bus Operations 10
Random Read (Non-Page Read) 10
Page Mode Read 10
Table 2. Page Select 10
Simultaneous Operation 10
Table 3. Bank Select 11
Table 4. Am29PDL129H Sector Architecture 12
Table 5. Addresses 19
Table 6. Autoselect Codes (High Voltage Method) 19
Table 7. Am29PDL129H Boot Sector/Sector Block Addresses for Protection/Unprotection CE1# Control 20
Table 8. Am29PDL129H Boot Sector/Sector Block Addresses for Protection/Unprotection CE2# Control 20
Table 9. Sector Protection Schemes 21
Write Protect (WP#) 21
Persistent Protection Bit Lock 21
High Voltage Sector Protection 21
Figure 1. 21
Temporary Sector Unprotect 21
Figure 2. 21
Flash Memory Region 21
Factory-Locked Area (64 words) 21
Customer-Lockable Area (64 words) 22
Figure 3. SecSi Sector Protection Algorithm 23
SecSi Sector Protection Bits 24
Figure 4. SecSi Sector Protect Verify 24
Common Flash Memory Interface (CFI) 24
Command Definitions 27
Enter /Exit Command Sequence 27
Figure 5. 27
PPB Lock Bit Status 27
Table 14. Memory Array Command Definitions 28
Table 15. Sector Protection Command Definitions 29
Absolute Maximum Ratings 30
Figure 6. Maximum Negative Overshoot Waveform 30
Figure 7. Maximum Positive Overshoot Waveform 30
DC Characteristics 31
Test Conditions 32
Figure 8. Test Setup, VIO = 2.7 – 3.6 V 32
Figure 9. Input Waveforms and Measurement Levels 32
AC Characteristics 33
CE1#/CE2# Timing 33
Figure 10. Timing Diagram for Alternating Between CE1# and CE2# Control 33
Read-Only Operations 33
Figure 11. Read Operation Timings 34
Figure 12. Page Read Operation Timings 34
Hardware Reset (RESET#) 35
Figure 13. Reset Timings 35
Erase and Program Operations 36
Figure 14. Program Operation Timings 37
Figure 15. Accelerated Program Timing Diagram 37
Figure 16. Chip/Sector Erase Operation Timings 38
Figure 17. Back-to-back Read/Write Cycle Timings 39
Figure 18. Data# Polling Timings (During Embedded Algorithms). 39
Figure 19. Toggle Bit Timings (During Embedded Algorithms) 40
Figure 20. DQ2 vs. DQ6 40
Temporary Sector Unprotect 41
Figure 21. Temporary Sector Unprotect Timing Diagram 41
Figure 22. Sector/Sector Block Protect and Unprotect Timing Diagram 42
Alternate CE# Controlled Erase and Program Operations 43
Figure 23. Alternate CE# Controlled Write (Erase/Program) Operation Timings 44
Erase And Programming Performance 45
Latchup Characteristics 45
BGA Ball Capacitance 45
Data Retention 45
Revision Summary 46

PRODUCT SELECTOR GUIDE

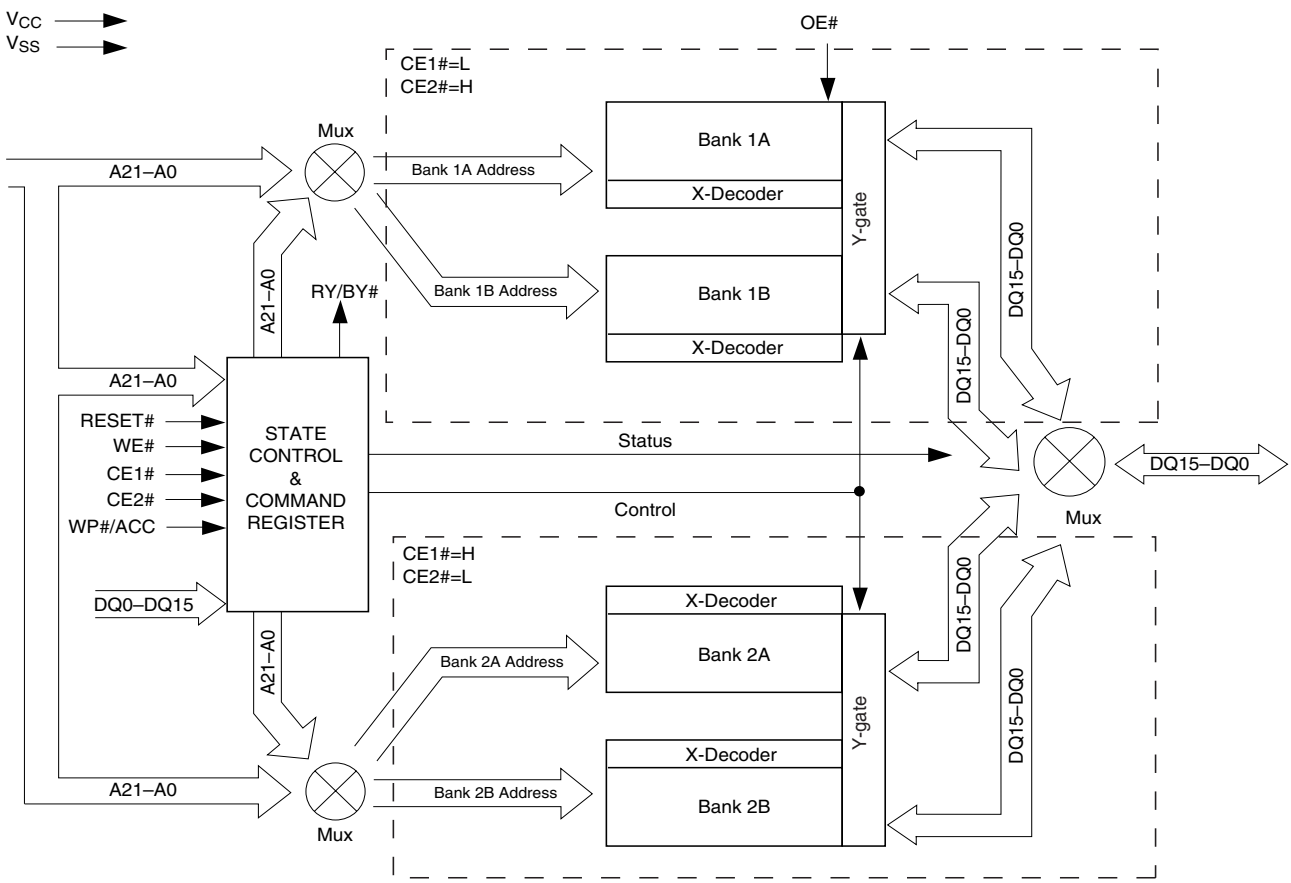
Part Number		Am29PDL129H			
Speed Option	V_{CC}, V_{IO} = 2.7–3.6 V	**53**	**63**		
	V_{CC} = 2.7–3.6 V, V_{IO} = 1.65–1.95 V			**68**	**88**
Max Access Time, ns (t_{ACC})		55	65	65	85
Max CE# Access, ns (t_{CE})		60		70	
Max Page Access, ns (t_{PACC})		20	25	30	30
Max OE# Access, ns (t_{OE})					

BLOCK DIAGRAM



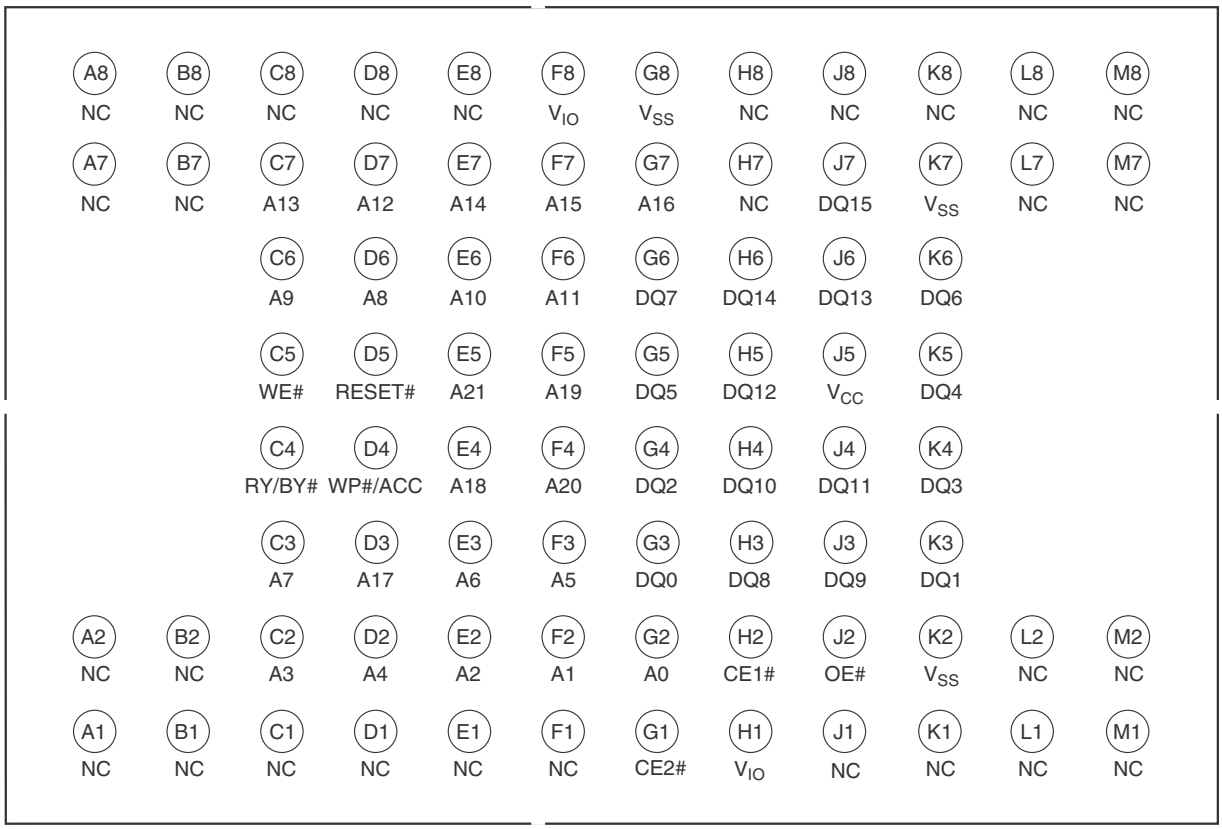
Note:*RY/BY# is an open drain output.*

SIMULTANEOUS OPERATION BLOCK DIAGRAM



CONNECTION DIAGRAMS

80-Ball Fine-pitch BGA
Top View, Balls Facing Down



Note: *On S29PL129J, G1= NC and J1= CE2#*

PIN DESCRIPTION

A21–A0 = 22-bit address bus for 2 x 64 Mb device. A9 supports 12 V autoselect inputs.

DQ15–DQ0 = 16-bit data inputs/outputs/float

CE1#, CE2# = Chip Enable Inputs. CE1# controls the 64 Mb in Banks 1A and 1B. CE2# controls the 64 Mb in Banks 2A and 2B.

OE# = Output Enable Input

WE# = Write Enable

V_{SS} = Device Ground

NC = Pin Not Connected Internally

RY/BY# = Ready/Busy output and open drain. When RY/BY#= V_{IH}, the device is ready to accept read operations and commands. When RY/BY#= V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.

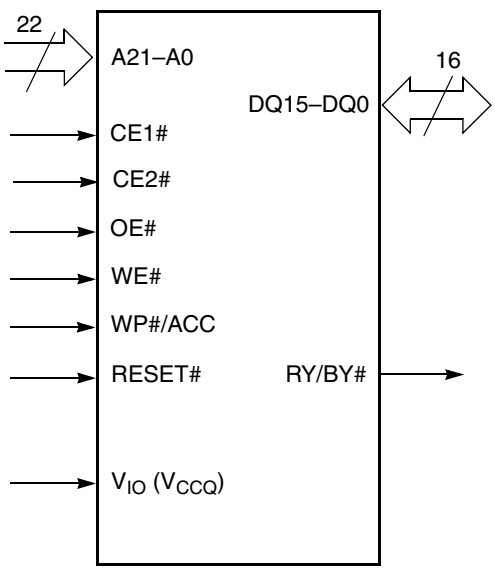
WP#/ACC = Write Protect/Acceleration Input. When WP/ACC#= V_{IL}, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP/ACC#= V_{IH}, these sector are unprotected unless the DYB or PPB is programmed. When WP/ACC#= 12V, program and erase operations are accelerated.

V_{IO} = Input/Output Buffer Power Supply (1.65 V to 1.95 V or 2.7 V to 3.6 V)

V_{CC} = Chip Power Supply (2.7 V to 3.6 V)

RESET# = Hardware Reset Pin

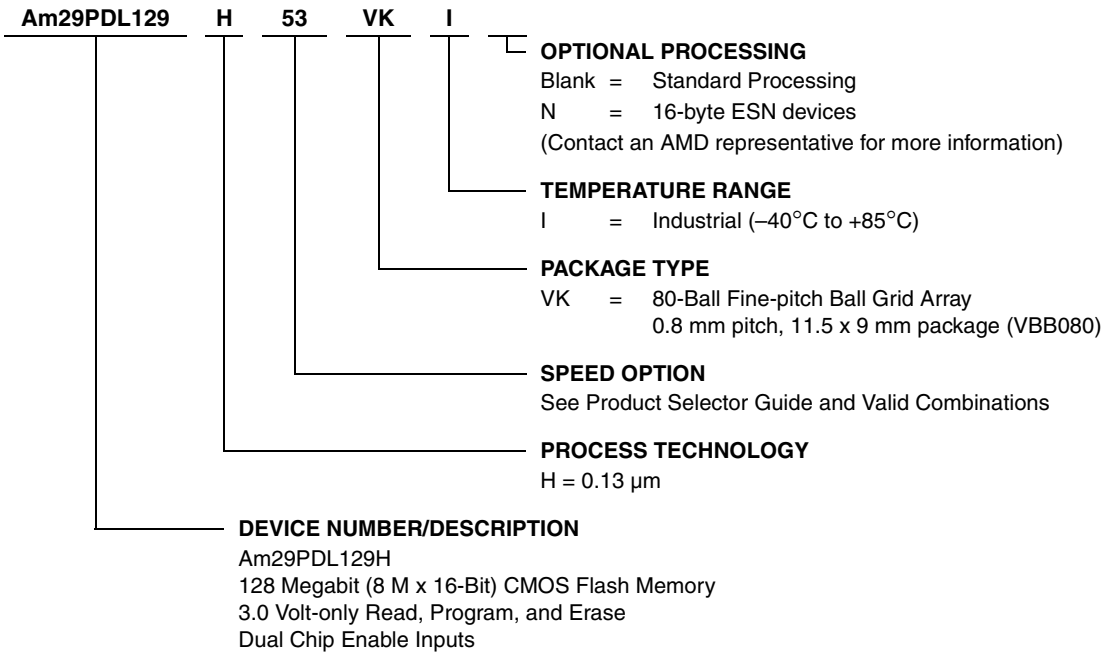
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for BGA Packages					
Order Number		Package Marking		Speed (ns)	V_{IO} Range
Am29PDL129H53	VKI	PD129H53V	I	55	2.7–3.6 V
Am29PDL129H63		PD129H63V		65	2.7–3.6 V
Am29PDL129H68		PD129H68V		65	1.65–1.95 V
Am29PDL129H88		PD129H88V		85	1.65–1.95 V

Note: *For the Am29PDL129H, the last digit of the speed grade specifies the V_{IO} range of the device. Speed grades ending in 3 (for example: 53, 63) indicate a 3 Volt V_{IO} range. Speed grades ending in 8 (for example: 68, 88) indicate a 1.8 Volt V_{IO} range. Contact AMD or Fujitsu for availability of 1.8V V_{IO} range devices.*

DEVICE BUS OPERATIONS

Table 1. Am29PDL129H Device Bus Operations

Operation	CE1#	CE2#	OE#	WE#	RESET#	WP#/ACC	Addresses (A21–A0)	DQ15–DQ0
Read	L	H	L	H	H	X	A_{IN}	D_{OUT}
	H	L						
Write	L	H	H	L	H	X (Note 2)	A_{IN}	D_{IN}
	H	L						
Standby	V_{IO}± 0.3 V	V_{IO} ± 0.3 V	X	X	V_{IO} ± 0.3 V	X	X	High-Z
Output Disable	L	L	H	H	H	X	X	High-Z
Reset	X	X	X	X	L	X	X	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	X	V_{ID}	X	A_{IN}	D_{IN}

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 8.5–9.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *The sector protect and sector unprotect functions may also be implemented via programming equipment. .*
2. *WP#/ACC must be high when writing to sectors SA1-133, SA1-134, SA2-0, or SA2-1.*

Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits A21–A3 select an 8-word page, and address bits A2–A0 select a specific work within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor fall within that page) are t_{PACC}. When CE1# and CE2# are deasserted (CE1#=CE2#=V_{IH}), the reassertion of CE1# or CE2# for subsequent access has access time of t_{ACC} or t_{CE}. Here again, CE1#/CE2# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping A21–A3 constant and changing A2 to A0 to select the specific word within that page.

Table 2. Page Select

Word	A2	A1	A0
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

Simultaneous Operation

In addition to the conventional features (read, program, erase-suspend read, and erase-suspend program), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation), The bank can be selected by bank addresses (A21–A20) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Table 3. Bank Select

Bank	CE1#	CE2#	A21–A20
Bank 1A	0	1	00, 01, 10
Bank 1B	0	1	11
Bank 2A	1	0	00
Bank 2B	1	0	01, 10, 11

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 1A	SA1-0	0	1	0000000XXX	32	000000h–007FFFh
	SA1-1	0	1	0000001XXX	32	008000h–00FFFFh
	SA1-2	0	1	0000010XXX	32	010000h–017FFFh
	SA1-3	0	1	0000011XXX	32	018000h–01FFFFh
	SA1-4	0	1	0000100XXX	32	020000h–027FFFh
	SA1-5	0	1	0000101XXX	32	028000h–02FFFFh
	SA1-6	0	1	0000110XXX	32	030000h–037FFFh
	SA1-7	0	1	0000111XXX	32	038000h–03FFFFh
	SA1-8	0	1	0001000XXX	32	040000h–047FFFh
	SA1-9	0	1	0001001XXX	32	048000h–04FFFFh
	SA1-10	0	1	0001010XXX	32	050000h–057FFFh
	SA1-11	0	1	0001011XXX	32	058000h–05FFFFh
	SA1-12	0	1	0001100XXX	32	060000h–067FFFh
	SA1-13	0	1	0001101XXX	32	068000h–06FFFFh
	SA1-14	0	1	0001110XXX	32	070000h–077FFFh
	SA1-15	0	1	0001111XXX	32	078000h–07FFFFh
	SA1-16	0	1	0010000XXX	32	080000h–087FFFh
	SA1-17	0	1	0010001XXX	32	088000h–08FFFFh
	SA1-18	0	1	0010010XXX	32	090000h–097FFFh
	SA1-19	0	1	0010011XXX	32	098000h–09FFFFh
	SA1-20	0	1	0010100XXX	32	0A0000h–0A7FFFh
	SA1-21	0	1	0010101XXX	32	0A8000h–0AFFFFh
	SA1-22	0	1	0010110XXX	32	0B0000h–0B7FFFh
	SA1-23	0	1	0010111XXX	32	0B8000h–0BFFFFh
	SA1-24	0	1	0011000XXX	32	0C0000h–0C7FFFh
	SA1-25	0	1	0011001XXX	32	0C8000h–0CFFFFh
	SA1-26	0	1	0011010XXX	32	0D0000h–0D7FFFh
	SA1-27	0	1	0011011XXX	32	0D8000h–0DFFFFh
	SA1-28	0	1	0011100XXX	32	0E0000h–0E7FFFh
	SA1-29	0	1	0011101XXX	32	0E8000h–0EFFFFh
	SA1-30	0	1	0011110XXX	32	0F0000h–0F7FFFh
	SA1-31	0	1	0011111XXX	32	0F8000h–0FFFFFh
	SA1-32	0	1	0100000XXX	32	100000h–107FFFh
	SA1-33	0	1	0100001XXX	32	108000h–10FFFFh
	SA1-34	0	1	0100010XXX	32	110000h–117FFFh
	SA1-35	0	1	0100011XXX	32	118000h–11FFFFh
	SA1-36	0	1	0100100XXX	32	120000h–127FFFh
	SA1-37	0	1	0100101XXX	32	128000h–12FFFFh

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 1A	SA1-38	0	1	0100110XXX	32	130000h–137FFFh
	SA1-39	0	1	0100111XXX	32	138000h–13FFFFh
	SA1-40	0	1	0101000XXX	32	140000h–147FFFh
	SA1-41	0	1	0101001XXX	32	148000h–14FFFFh
	SA1-42	0	1	0101010XXX	32	150000h–157FFFh
	SA1-43	0	1	0101011XXX	32	158000h–15FFFFh
	SA1-44	0	1	0101100XXX	32	160000h–167FFFh
	SA1-45	0	1	0101101XXX	32	168000h–16FFFFh
	SA1-46	0	1	0101110XXX	32	170000h–177FFFh
	SA1-47	0	1	0101111XXX	32	178000h–17FFFFh
	SA1-48	0	1	0110000XXX	32	180000h–187FFFh
	SA1-49	0	1	0110001XXX	32	188000h–18FFFFh
	SA1-50	0	1	0110010XXX	32	190000h–197FFFh
	SA1-51	0	1	0110011XXX	32	198000h–19FFFFh
	SA1-52	0	1	0110100XXX	32	1A0000h–1A7FFFh
	SA1-53	0	1	0110101XXX	32	1A8000h–1AFFFFh
	SA1-54	0	1	0110110XXX	32	1B0000h–1B7FFFh
	SA1-55	0	1	0110111XXX	32	1B8000h–1BFFFFh
	SA1-56	0	1	0111000XXX	32	1C0000h–1C7FFFh
	SA1-57	0	1	0111001XXX	32	1C8000h–1CFFFFh
	SA1-58	0	1	0111010XXX	32	1D0000h–1D7FFFh
	SA1-59	0	1	0111011XXX	32	1D8000h–1DFFFFh
	SA1-60	0	1	0111100XXX	32	1E0000h–1E7FFFh
	SA1-61	0	1	0111101XXX	32	1E8000h–1EFFFFh
	SA1-62	0	1	0111110XXX	32	1F0000h–1F7FFFh
	SA1-63	0	1	0111111XXX	32	1F8000h–1FFFFFh
	SA1-64	0	1	1000000XXX	32	200000h–207FFFh
	SA1-65	0	1	1000001XXX	32	208000h–20FFFFh
	SA1-66	0	1	1000010XXX	32	210000h–217FFFh
	SA1-67	0	1	1000011XXX	32	218000h–21FFFFh
	SA1-68	0	1	1000100XXX	32	220000h–227FFFh
	SA1-69	0	1	1000101XXX	32	228000h–22FFFFh
	SA1-70	0	1	1000110XXX	32	230000h–237FFFh
	SA1-71	0	1	1000111XXX	32	238000h–23FFFFh
	SA1-72	0	1	1001000XXX	32	240000h–247FFFh
	SA1-73	0	1	1001001XXX	32	248000h–24FFFFh
	SA1-74	0	1	1001010XXX	32	250000h–257FFFh
	SA1-75	0	1	1001011XXX	32	258000h–25FFFFh
	SA1-76	0	1	1001100XXX	32	260000h–267FFFh
	SA1-77	0	1	1001101XXX	32	268000h–26FFFFh

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 1A	SA1-78	0	1	1001110XXX	32	270000h–277FFFh
	SA1-79	0	1	1001111XXX	32	278000h–27FFFFh
	SA1-80	0	1	1010000XXX	32	280000h–287FFFh
	SA1-81	0	1	1010001XXX	32	288000h–28FFFFh
	SA1-82	0	1	1010010XXX	32	290000h–297FFFh
	SA1-83	0	1	1010011XXX	32	298000h–29FFFFh
	SA1-84	0	1	1010100XXX	32	2A0000h–2A7FFFh
	SA1-85	0	1	1010101XXX	32	2A8000h–2AFFFFh
	SA1-86	0	1	1010110XXX	32	2B0000h–2B7FFFh
	SA1-87	0	1	1010111XXX	32	2B8000h–2BFFFFh
	SA1-88	0	1	1011000XXX	32	2C0000h–2C7FFFh
	SA1-89	0	1	1011001XXX	32	2C8000h–2CFFFFh
	SA1-90	0	1	1011010XXX	32	2D0000h–2D7FFFh
	SA1-91	0	1	1011011XXX	32	2D8000h–2DFFFFh
	SA1-92	0	1	1011100XXX	32	2E0000h–2E7FFFh
	SA1-93	0	1	1011101XXX	32	2E8000h–2EFFFFh
	SA1-94	0	1	1011110XXX	32	2F0000h–2F7FFFh
	SA1-95	0	1	1011111XXX	32	2F8000h–2FFFFFh

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 1B	SA1-96	0	1	1100000XXX	32	300000h–307FFFh
	SA1-97	0	1	1100001XXX	32	308000h–30FFFFh
	SA1-98	0	1	1100010XXX	32	310000h–317FFFh
	SA1-99	0	1	1100011XXX	32	318000h–31FFFFh
	SA1-100	0	1	1100100XXX	32	320000h–327FFFh
	SA1-101	0	1	1100101XXX	32	328000h–32FFFFh
	SA1-102	0	1	1100110XXX	32	330000h–337FFFh
	SA1-103	0	1	1100111XXX	32	338000h–33FFFFh
	SA1-104	0	1	1101000XXX	32	340000h–347FFFh
	SA1-105	0	1	1101001XXX	32	348000h–34FFFFh
	SA1-106	0	1	1101010XXX	32	350000h–357FFFh
	SA1-107	0	1	1101011XXX	32	358000h–35FFFFh
	SA1-108	0	1	1101100XXX	32	360000h–367FFFh
	SA1-109	0	1	1101101XXX	32	368000h–36FFFFh
	SA1-110	0	1	1101110XXX	32	370000h–377FFFh
	SA1-111	0	1	1101111XXX	32	378000h–37FFFFh
	SA1-112	0	1	1110000XXX	32	380000h–387FFFh
	SA1-113	0	1	1110001XXX	32	388000h–38FFFFh
	SA1-114	0	1	1110010XXX	32	390000h–397FFFh
	SA1-115	0	1	1110011XXX	32	398000h–39FFFFh
	SA1-116	0	1	1110100XXX	32	3A0000h–3A7FFFh
	SA1-117	0	1	1110101XXX	32	3A8000h–3AFFFFh
	SA1-118	0	1	1110110XXX	32	3B0000h–3B7FFFh
	SA1-119	0	1	1110111XXX	32	3B8000h–3BFFFFh
	SA1-120	0	1	1111000XXX	32	3C0000h–3C7FFFh
	SA1-121	0	1	1111001XXX	32	3C8000h–3CFFFFh
	SA1-122	0	1	1111010XXX	32	3D0000h–3D7FFFh
	SA1-123	0	1	1111011XXX	32	3D8000h–3DFFFFh
	SA1-124	0	1	1111100XXX	32	3E0000h–3E7FFFh
	SA1-125	0	1	1111101XXX	32	3E8000h–3EFFFFh
	SA1-126	0	1	1111110XXX	32	3F0000h–3F7FFFh
	SA1-127	0	1	1111111000	4	3F8000h–3F8FFFh
	SA1-128	0	1	1111111001	4	3F9000h–3F9FFFh
	SA1-129	0	1	1111111010	4	3FA000h–3FAFFFh
	SA1-130	0	1	1111111011	4	3FB000h–3FBFFFh
	SA1-131	0	1	1111111100	4	3FC000h–3FCFFFh
	SA1-132	0	1	1111111101	4	3FD000h–3FDFFFh
	SA1-133	0	1	1111111110	4	3FE000h–3FEFFFh
	SA1-134	0	1	1111111111	4	3FF000h–3FFFFFh

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 2A	SA2-0	1	0	0000000000	4	000000h–000FFFh
	SA2-1	1	0	0000000001	4	001000h–001FFFh
	SA2-2	1	0	0000000010	4	002000h–002FFFh
	SA2-3	1	0	0000000011	4	003000h–003FFFh
	SA2-4	1	0	0000000100	4	004000h–004FFFh
	SA2-5	1	0	0000000101	4	005000h–005FFFh
	SA2-6	1	0	0000000110	4	006000h–006FFFh
	SA2-7	1	0	0000000111	4	007000h–007FFFh
	SA2-8	1	0	0000001XXX	32	008000h–00FFFFh
	SA2-9	1	0	0000010XXX	32	010000h–017FFFh
	SA2-10	1	0	0000011XXX	32	018000h–01FFFFh
	SA2-11	1	0	0000100XXX	32	020000h–027FFFh
	SA2-12	1	0	0000101XXX	32	028000h–02FFFFh
	SA2-13	1	0	0000110XXX	32	030000h–037FFFh
	SA2-14	1	0	0000111XXX	32	038000h–03FFFFh
	SA2-15	1	0	0001000XXX	32	040000h–047FFFh
	SA2-16	1	0	0001001XXX	32	048000h–04FFFFh
	SA2-17	1	0	0001010XXX	32	050000h–057FFFh
	SA2-18	1	0	0001011XXX	32	058000h–05FFFFh
	SA2-19	1	0	0001100XXX	32	060000h–067FFFh
	SA2-20	1	0	0001101XXX	32	068000h–06FFFFh
	SA2-21	1	0	0001110XXX	32	070000h–077FFFh
	SA2-22	1	0	0001111XXX	32	078000h–07FFFFh
	SA2-23	1	0	0010000XXX	32	080000h–087FFFh
	SA2-24	1	0	0010001XXX	32	088000h–08FFFFh
	SA2-25	1	0	0010010XXX	32	090000h–097FFFh
	SA2-26	1	0	0010011XXX	32	098000h–09FFFFh
	SA2-27	1	0	0010100XXX	32	0A0000h–0A7FFFh
	SA2-28	1	0	0010101XXX	32	0A8000h–0AFFFFh
	SA2-29	1	0	0010110XXX	32	0B0000h–0B7FFFh
	SA2-30	1	0	0010111XXX	32	0B8000h–0BFFFFh
	SA2-31	1	0	0011000XXX	32	0C0000h–0C7FFFh
	SA2-32	1	0	0011001XXX	32	0C8000h–0CFFFFh
	SA2-33	1	0	0011010XXX	32	0D0000h–0D7FFFh
	SA2-34	1	0	0011011XXX	32	0D8000h–0DFFFFh
	SA2-35	1	0	0011100XXX	32	0E0000h–0E7FFFh
	SA2-36	1	0	0011101XXX	32	0E8000h–0EFFFFh
	SA2-37	1	0	0011110XXX	32	0F0000h–0F7FFFh
	SA2-38	1	0	0011111XXX	32	0F8000h–0FFFFFh

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 2B	SA2-39	1	0	0100000XXX	32	100000h–107FFFh
	SA2-40	1	0	0100001XXX	32	108000h–10FFFFh
	SA2-41	1	0	0100010XXX	32	110000h–117FFFh
	SA2-42	1	0	0100011XXX	32	118000h–11FFFFh
	SA2-43	1	0	0100100XXX	32	120000h–127FFFh
	SA2-44	1	0	0100101XXX	32	128000h–12FFFFh
	SA2-45	1	0	0100110XXX	32	130000h–137FFFh
	SA2-46	1	0	0100111XXX	32	138000h–13FFFFh
	SA2-47	1	0	0101000XXX	32	140000h–147FFFh
	SA2-48	1	0	0101001XXX	32	148000h–14FFFFh
	SA2-49	1	0	0101010XXX	32	150000h–157FFFh
	SA2-50	1	0	0101011XXX	32	158000h–15FFFFh
	SA2-51	1	0	0101100XXX	32	160000h–167FFFh
	SA2-52	1	0	0101101XXX	32	168000h–16FFFFh
	SA2-53	1	0	0101110XXX	32	170000h–177FFFh
	SA2-54	1	0	0101111XXX	32	178000h–17FFFFh
	SA2-55	1	0	0110000XXX	32	180000h–187FFFh
	SA2-56	1	0	0110001XXX	32	188000h–18FFFFh
	SA2-57	1	0	0110010XXX	32	190000h–197FFFh
	SA2-58	1	0	0110011XXX	32	198000h–19FFFFh
	SA2-59	1	0	0110100XXX	32	1A0000h–1A7FFFh
	SA2-60	1	0	0110101XXX	32	1A8000h–1AFFFFh
	SA2-61	1	0	0110110XXX	32	1B0000h–1B7FFFh
	SA2-62	1	0	0110111XXX	32	1B8000h–1BFFFFh
	SA2-63	1	0	0111000XXX	32	1C0000h–1C7FFFh
	SA2-64	1	0	0111001XXX	32	1C8000h–1CFFFFh
	SA2-65	1	0	0111010XXX	32	1D0000h–1D7FFFh
	SA2-66	1	0	0111011XXX	32	1D8000h–1DFFFFh
	SA2-67	1	0	0111100XXX	32	1E0000h–1E7FFFh
	SA2-68	1	0	0111101XXX	32	1E8000h–1EFFFFh
	SA2-69	1	0	0111110XXX	32	1F0000h–1F7FFFh
	SA2-70	1	0	0111111XXX	32	1F8000h–1FFFFFh
	SA2-71	1	0	1000000XXX	32	200000h–207FFFh
	SA2-72	1	0	1000001XXX	32	208000h–20FFFFh
	SA2-73	1	0	1000010XXX	32	210000h–217FFFh
	SA2-74	1	0	1000011XXX	32	218000h–21FFFFh
	SA2-75	1	0	1000100XXX	32	220000h–227FFFh
	SA2-76	1	0	1000101XXX	32	228000h–22FFFFh
	SA2-77	1	0	1000110XXX	32	230000h–237FFFh
	SA2-78	1	0	1000111XXX	32	238000h–23FFFFh

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 2B	SA2-79	1	0	1001000XXX	32	240000h–247FFFh
	SA2-80	1	0	1001001XXX	32	248000h–24FFFFh
	SA2-81	1	0	1001010XXX	32	250000h–257FFFh
	SA2-82	1	0	1001011XXX	32	258000h–25FFFFh
	SA2-83	1	0	1001100XXX	32	260000h–267FFFh
	SA2-84	1	0	1001101XXX	32	268000h–26FFFFh
	SA2-85	1	0	1001110XXX	32	270000h–277FFFh
	SA2-86	1	0	1001111XXX	32	278000h–27FFFFh
	SA2-87	1	0	1010000XXX	32	280000h–287FFFh
	SA2-88	1	0	1010001XXX	32	288000h–28FFFFh
	SA2-89	1	0	1010010XXX	32	290000h–297FFFh
	SA2-90	1	0	1010011XXX	32	298000h–29FFFFh
	SA2-91	1	0	1010100XXX	32	2A0000h–2A7FFFh
	SA2-92	1	0	1010101XXX	32	2A8000h–2AFFFFh
	SA2-93	1	0	1010110XXX	32	2B0000h–2B7FFFh
	SA2-94	1	0	1010111XXX	32	2B8000h–2BFFFFh
	SA2-95	1	0	1011000XXX	32	2C0000h–2C7FFFh
	SA2-96	1	0	1011001XXX	32	2C8000h–2CFFFFh
	SA2-97	1	0	1011010XXX	32	2D0000h–2D7FFFh
	SA2-98	1	0	1011011XXX	32	2D8000h–2DFFFFh
	SA2-99	1	0	1011100XXX	32	2E0000h–2E7FFFh
	SA2-100	1	0	1011101XXX	32	2E8000h–2EFFFFh
	SA2-101	1	0	1011110XXX	32	2F0000h–2F7FFFh
	SA2-102	1	0	1011111XXX	32	2F8000h–2FFFFFh
	SA2-103	1	0	1100000XXX	32	300000h–307FFFh
	SA2-104	1	0	1100001XXX	32	308000h–30FFFFh
	SA2-105	1	0	1100010XXX	32	310000h–317FFFh
	SA2-106	1	0	1100011XXX	32	318000h–31FFFFh
	SA2-107	1	0	1100100XXX	32	320000h–327FFFh
	SA2-108	1	0	1100101XXX	32	328000h–32FFFFh
	SA2-109	1	0	1100110XXX	32	330000h–337FFFh
	SA2-110	1	0	1100111XXX	32	338000h–33FFFFh
	SA2-111	1	0	1101000XXX	32	340000h–347FFFh
	SA2-112	1	0	1101001XXX	32	348000h–34FFFFh
	SA2-113	1	0	1101010XXX	32	350000h–357FFFh
	SA2-114	1	0	1101011XXX	32	358000h–35FFFFh
	SA2-115	1	0	1101100XXX	32	360000h–367FFFh
	SA2-116	1	0	1101101XXX	32	368000h–36FFFFh
	SA2-117	1	0	1101110XXX	32	370000h–377FFFh
	SA2-118	1	0	1101111XXX	32	378000h–37FFFFh

Table 4. Am29PDL129H Sector Architecture

Bank	Sector	CE1#	CE2#	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank 2B	SA2-119	1	0	1110000XXX	32	380000h–387FFFh
	SA2-120	1	0	1110001XXX	32	388000h–38FFFFh
	SA2-121	1	0	1110010XXX	32	390000h–397FFFh
	SA2-122	1	0	1110011XXX	32	398000h–39FFFFh
	SA2-123	1	0	1110100XXX	32	3A0000h–3A7FFFh
	SA2-124	1	0	1110101XXX	32	3A8000h–3AFFFFh
	SA2-125	1	0	1110110XXX	32	3B0000h–3B7FFFh
	SA2-126	1	0	1110111XXX	32	3B8000h–3BFFFFh
	SA2-127	1	0	1111000XXX	32	3C0000h–3C7FFFh
	SA2-128	1	0	1111001XXX	32	3C8000h–3CFFFFh
	SA2-129	1	0	1111010XXX	32	3D0000h–3D7FFFh
	SA2-130	1	0	1111011XXX	32	3D8000h–3DFFFFh
	SA2-131	1	0	1111100XXX	32	3E0000h–3E7FFFh
	SA2-132	1	0	1111101XXX	32	3E8000h–3EFFFFh
	SA2-133	1	0	1111110XXX	32	3F0000h–3F7FFFh
	SA2-134	1	0	1111111XXX	32	3F8000h–3FFFFFh

Table 5. Addresses

	Sector Size	Address Range
Am29PDL129H	128 words	000000h–00007Fh
Factory-Locked Area	64 words	000000h-00003Fh
Customer-Lockable Area	64 words	000040h-00007Fh

Table 6. Autoselect Codes (High Voltage Method)

Description		CE1#	CE2#	OE#	WE#	A21 to A12	A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ0
Manufacturer ID: AMD		L	H	L	H	X	X	V_{ID}	X	L	L	X	L	L	L	L	0001h
		H	L														
Device ID	Read Cycle 1	L	H	L	H	X	X	V_{ID}	X	L	L	L	L	L	L	H	227Eh
		H	L														
	Read Cycle 2	L	H										H	H	H	L	2221h
		H	L														
	Read Cycle 3	L	H										H	H	H	H	2200h
		H	L														
Sector Protection Verification		L	H	L	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	0001h (protected), 0000h (unprotected)
		H	L														
Indicator Bit (DQ7, DQ6)		L	H	L	H	X	X	V_{ID}	X	X	L	X	L	L	H	H	00C0h (factory and customer locked), 0080h (factory locked)
		H	L														

Legend: L = Logic Low = V_{IL}, H = Logic High = V_{IH}, BA = Bank Address, SA = Sector Address, X = Don't care. Note: The autoselect codes may also be accessed in-system via command sequences

Table 7. Am29PDL129H Boot Sector/Sector Block Addresses for Protection/Unprotection

CE1# Control

Sector Group	A21-12	Sector/Sector Block Size
SA1-0–SA1-3	00000XXXXX	128 (4x32) Kwords

Sector Group	A21-12	Sector/Sector Block Size
SA1-4–SA1-7	00001XXXXX	128 (4x32) Kwords
SA1-8–SA1-11	00010XXXXX	128 (4x32) Kwords
SA1-12–SA1-15	00011XXXXX	128 (4x32) Kwords
SA1-16–SA1-19	00100XXXXX	128 (4x32) Kwords
SA1-20–SA1-23	00101XXXXX	128 (4x32) Kwords
SA1-24–SA1-27	00110XXXXX	128 (4x32) Kwords
SA1-28–SA1-31	00111XXXXX	128 (4x32) Kwords
SA1-32–SA1-35	01000XXXXX	128 (4x32) Kwords
SA1-36–SA1-39	01001XXXXX	128 (4x32) Kwords
SA1-40–SA1-43	01010XXXXX	128 (4x32) Kwords
SA1-44–SA1-47	01011XXXXX	128 (4x32) Kwords
SA1-48–SA1-51	01100XXXXX	128 (4x32) Kwords
SA1-52–SA1-55	01101XXXXX	128 (4x32) Kwords
SA1-56–SA1-59	01110XXXXX	128 (4x32) Kwords
SA1-60–SA1-63	01111XXXXX	128 (4x32) Kwords
SA1-64–SA1-67	10000XXXXX	128 (4x32) Kwords
SA1-68–SA1-71	10001XXXXX	128 (4x32) Kwords
SA1-72–SA1-75	10010XXXXX	128 (4x32) Kwords
SA1-76–SA1-79	10011XXXXX	128 (4x32) Kwords
SA1-80–SA1-83	10100XXXXX	128 (4x32) Kwords
SA1-84–SA1-87	10101XXXXX	128 (4x32) Kwords
SA1-88–SA1-91	10110XXXXX	128 (4x32) Kwords
SA1-92–SA1-95	10111XXXXX	128 (4x32) Kwords
SA1-96–SA1-99	11000XXXXX	128 (4x32) Kwords
SA1-100–SA1-103	11001XXXXX	128 (4x32) Kwords
SA1-104–SA1-107	11010XXXXX	128 (4x32) Kwords
SA1-108–SA1-111	11011XXXXX	128 (4x32) Kwords
SA1-112–SA1-115	11100XXXXX	128 (4x32) Kwords
SA1-116–SA1-119	11101XXXXX	128 (4x32) Kwords
SA1-120–SA1-123	11110XXXXX	128 (4x32) Kwords
SA1-124	1111100XXX	32 Kwords
SA1-125	1111101XXX	32 Kwords
SA1-126	1111110XXX	32 Kwords
SA1-127	1111111000	4 Kwords
SA1-128	1111111001	4 Kwords
SA1-129	1111111010	4 Kwords
SA1-130	1111111011	4 Kwords
SA1-131	1111111100	4 Kwords
SA1-132	1111111101	4 Kwords
SA1-133	1111111110	4 Kwords
SA1-134	1111111111	4 Kwords

Table 8. Am29PDL129H Boot Sector/Sector Block Addresses for Protection/Unprotection CE2# Control

Sector Group	A21-12	Sector/Sector Block Size
SA2-0	0000000000	4 Kwords
SA2-1	0000000001	4 Kwords
SA2-2	0000000010	4 Kwords
SA2-3	0000000011	4 Kwords
SA2-4	0000000100	4 Kwords
SA2-5	0000000101	4 Kwords
SA2-6	0000000110	4 Kwords
SA2-7	0000000111	4 Kwords
SA2-8	0000001XXX	32 Kwords
SA2-9	0000010XXX	32 Kwords
SA2-10	0000011XXX	32 Kwords
SA2-11 - SA2-14	00001XXXXX	128 (4x32) Kwords
SA2-15 - SA2-18	00010XXXXX	128 (4x32) Kwords
SA2-19 - SA2-22	00011XXXXX	128 (4x32) Kwords
SA2-23 - SA2-26	00100XXXXX	128 (4x32) Kwords
SA2-27 - SA2-30	00101XXXXX	128 (4x32) Kwords
SA2-31 - SA2-34	00110XXXXX	128 (4x32) Kwords
SA2-35 - SA2-38	00111XXXXX	128 (4x32) Kwords
SA2-39 - SA2-42	01000XXXXX	128 (4x32) Kwords
SA2-43 - SA2-46	01001XXXXX	128 (4x32) Kwords
SA2-47 - SA2-50	01010XXXXX	128 (4x32) Kwords
SA2-51 - SA2-54	01011XXXXX	128 (4x32) Kwords
SA2-55 - SA2-58	01100XXXXX	128 (4x32) Kwords
SA2-59 - SA2-62	01101XXXXX	128 (4x32) Kwords
SA2-63 - SA2-66	01110XXXXX	128 (4x32) Kwords
SA2-67 - SA2-70	01111XXXXX	128 (4x32) Kwords
SA2-71 - SA2-74	10000XXXXX	128 (4x32) Kwords
SA2-75 - SA2-78	10001XXXXX	128 (4x32) Kwords
SA2-79 - SA2-82	10010XXXXX	128 (4x32) Kwords
SA2-83 - SA2-86	10011XXXXX	128 (4x32) Kwords
SA2-87 - SA2-90	10100XXXXX	128 (4x32) Kwords
SA2-91 - SA2-94	10101XXXXX	128 (4x32) Kwords
SA2-95 - SA2-98	10110XXXXX	128 (4x32) Kwords
SA2-99 - SA2-102	10111XXXXX	128 (4x32) Kwords
SA2-103 - SA2-106	11000XXXXX	128 (4x32) Kwords
SA2-107 - SA2-110	11001XXXXX	128 (4x32) Kwords
SA2-111 - SA2-114	11010XXXXX	128 (4x32) Kwords
SA2-115 - SA2-118	11011XXXXX	128 (4x32) Kwords
SA2-119 - SA2-122	11100XXXXX	128 (4x32) Kwords
SA2-123 - SA2-126	11101XXXXX	128 (4x32) Kwords
SA2-127 - SA2-130	11110XXXXX	128 (4x32) Kwords
SA2-131 - SA2-134	11111XXXXX	128 (4x32) Kwords

Selecting a Sector Protection Mode

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at the factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

Table 9. Sector Protection Schemes

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting sectors without using V_{ID}. This function is provided by the WP# pin and overrides the previously discussed High Voltage Sector Protection method.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in High Voltage Sector Protection.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1" when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure 1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

Figure 1.

Temporary Sector Unprotect

Notes:

1. *All protected sectors unprotected (If WP#/ACC = V_{IL}, sectors will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure 2.

Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN) The 128-word SecSi sector is divided into 64 factory-lockable words that can be programmed and locked by the customer. The SecSi sector is located at addresses 000000h-00007Fh in both Persistent Protection mode and Password Protection mode. It uses indicator bits (DQ6, DQ7) to indicate the factory-locked and customer-locked status of the part.

The system accesses the through a command sequence (see "Enter /Exit Command Sequence"). After the system has written the Enter command sequence, it may read the by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

Factory-Locked Area (64 words)

The factory-locked area of the SecSi Sector (000000h-00003Fh) is locked when the part is shipped, whether or not the area was programmed at the factory. The SecSi Sector Factory-locked Indicator Bit (DQ7) is permanently set to a "1". AMD offers the ExpressFlash service to program the factory-locked area with a random ESN, a customer-defined code, or any combina-

tion of the two. Because only AMD can program and protect the factory-locked area, this method ensures the security of the ESN once the product is shipped to the field. Contact an AMD representative for details on using AMD's ExpressFlash service. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Customer-Lockable Area (64 words)

The customer-lockable area of the SecSi Sector (000040h-00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The SecSi Sector Customer-locked Indicator Bit (DQ6) is shipped as "0" and can be permanently locked to "1" by issuing the SecSi Protection Bit Program Command. The SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The Customer-lockable area can be protected using one of the following procedures:

Follow the SecSi Sector Protection Algorithm as shown in . This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.

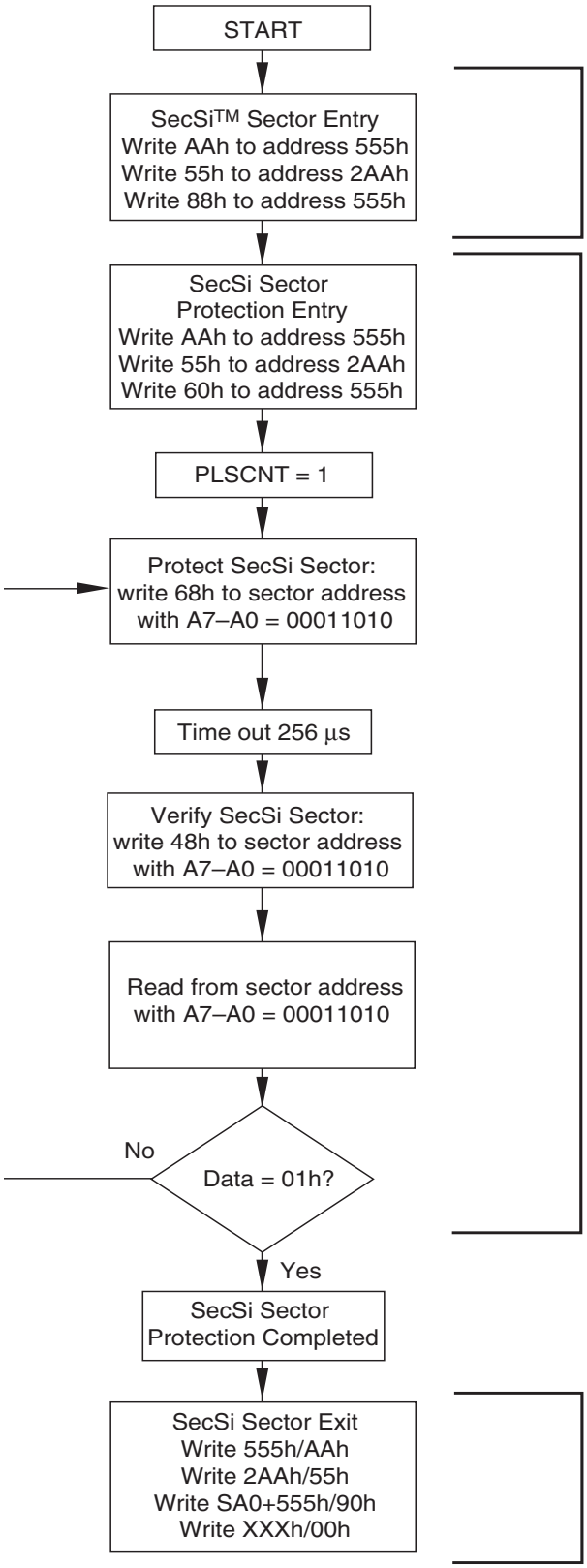


Figure 3. SecSi Sector Protection Algorithm

■ To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 4.

Once the is locked and verified, the system must write the Exit Region command sequence to return to reading and writing the remainder of the array.

The must be used with caution since, once locked, there is no procedure available for unlocking the area and none of the bits in the memory space can be modified in any way.

SecSi Sector Protection Bits

The SecSi Sector Protection Bits prevent programming of the SecSi Sector memory area. Once set, the SecSi Sector memory area contents are non-modifiable.

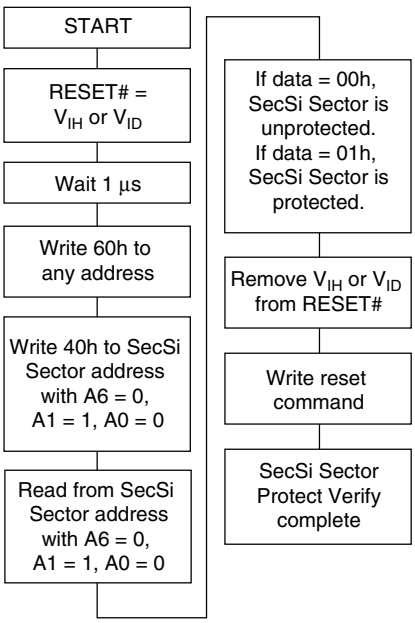


Figure 4. SecSi Sector Protect Verify

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 10–13. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 10–13. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 10. CFI Query Identification String

Addresses	Data	Description

10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 11. System Interface String

Addresses	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0004h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 12. Device Geometry Definition

Addresses	Data	Description
27h	0018h	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	00FDh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)

35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 13. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	000Ch	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h	Sector Protect/Unprotect scheme 01 =29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode
4Ah	00E7h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors excluding Bank 1
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	0001h	Program Suspend 0 = Not supported, 1 = Supported
57h	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	0027h	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	0060h	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	0060h	Bank 3 Region Information X = Number of Sectors in Bank 3
5Bh	0027h	Bank 4 Region Information X = Number of Sectors in Bank 4

COMMAND DEFINITIONS

Enter /Exit Command Sequence

The region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the region by issuing the three-cycle Enter command sequence. The device continues to access the region until the system issues the four-cycle Exit command sequence. The Exit ommand sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. shows the address and data requirements for both command sequences. See also “SecSi Sector Flash Memory Region and Enter SecSi Sector/Exit SecSi Sector Command Sequence” for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Figure 5.

If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin. If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin. μμ*After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.*

After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin.

PPB Lock Bit Status

Sector Protection Status The programming of either the PPB or DYB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DYB for a given sector group.

Command Definitions Tables

Table 14. Memory Array Command Definitions

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	(BA)X00	01				
	Device ID (10)	6	555	AA	2AA	55	555	90	(BA)X01	7E	(BA)X0E	21	(BA)X0F	00
	SecSi Sector Factory Protect (8)	4	555	AA	2AA	55	555	90	X03	(see note 8)				
	Sector Group Protect Verify (9)	4	555	AAA	2AA	55	555	90	(SA)X02	XX00/ XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (11)		1	BA	B0										
Program/Erase Resume (12)		1	BA	30										
CFI Query (13)		1	55	98										
Accelerated Program (15)		2	XX	A0	PA	PD								
Unlock Bypass Entry (15)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (15)		2	XX	A0	PA	PD								
Unlock Bypass Erase (15)		2	XX	80	XX	10								
Unlock Bypass CFI (13, 15)		1	XX	98										
Unlock Bypass Reset (15)		2	XXX	90	XXX	00								

Legend:

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by A21:A20, see Tables 4 and for more detail.

PA = Program Address (A21:A0). Addresses latch on falling edge of WE# or CE1#/CE2# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE1#/CE2# pulse, whichever happens first.

RA = Read Address (A21:A0).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (A21:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).*
7. *Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence for more information.*
8. *The data is C0h for factory or customer locked and 80h for factory locked.*
9. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Device ID must be read across cycles 4, 5, and 6.*
11. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.*
12. *Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.*
13. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
14. *must be at V_{ID} during the entire operation of command.*
15. *Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to the reading array.*

Table 15. Sector Protection Command Definitions

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)													
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0												
SecSi Sector Entry	3	555	AA	2AA	55	555	88								
SecSi Sector Exit	4	555	AA	2AA	55	555	90	XX	00						
SecSi Protection Bit Program (5, 6)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD(0)		
SecSi Protection Bit Status	5	555	AA	2AA	55	555	60	OW	48	OW	RD(0)				
Password Program (5, 7, 8)	4	555	AA	2AA	55	555	38	XX[0-3]	PD[0-3]						
Password Verify (6, 8, 9)	4	555	AA	2AA	55	555	C8	PWA[0-3]	PWD[0-3]						
Password Unlock (7, 10, 11)	7	555	AA	2AA	55	555	28	PWA[0]	PWD[0]	PWA[1]	PWD[1]	PWA[2]	PWD[2]	PWA[3]	PWD[3]
PPB Program (5, 6, 12, 17)	6	555	AA	2AA	55	555	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)		
PPB Status	5	555	AA	2AA	55	555	60	(SA)WP	48	(SA)WP	RD (0)				
All PPB Erase (5, 6, 13, 14)	6	555	AA	2AA	55	555	60	WP	60	(SA)	40	(SA)WP	RD(0)		
PPB Lock Bit Set (17)	3	555	AA	2AA	55	555	78								
PPB Lock Bit Status (15)	4	555	AA	2AA	55	555	58	SA	RD(1)						
DYB Write (7)	4	555	AA	2AA	55	555	48	SA	X1						
DYB Erase (7)	4	555	AA	2AA	55	555	48	SA	X0						
DYB Status (6, 18)	4	555	AA	2AA	55	555	58	SA	RD(0)						
PPMLB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD(0)		
PPMLB Status (5)	5	555	AA	2AA	55	555	60	PL	48	PL	RD(0)				
SPMLB Program (5, 6, 12)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD(0)		
SPMLB Status (5)	5	555	AA	2AA	55	555	60	SL	48	SL	RD(0)				

Legend:

DYB = Dynamic Protection Bit
OW = Address (A7:A0) is (00011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
PWA = Password Address. A1:A0 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A7:A0) is (00001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
SA = Sector Address where security command applies. Address bits A21:A12 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)
WP = PPB Address (A7:A0) is (00000010) (Note16)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *The reset command returns device to reading array.*
6. *Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.*
7. *Data is latched on the rising edge of WE#.*
8. *Entire command sequence must be entered for each portion of password.*
9. *Command sequence returns FFh if PPMLB is set.*
10. *The password is written over four consecutive cycles, at addresses 0-3.*
11. *A 2 µs timeout is required between any two portions of password.*
12. *A 100 µs timeout is required between cycles 4 and 5.*
13. *A 1.2 ms timeout is required between cycles 4 and 5.*
14. *Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.*
15. *DQ1 = 1 if PPB locked, 0 if unlocked.*
16. *For PDL128G and PDL640G, the WP address is 0111010. The EP address (PPB Erase Address) is 1111010.*
17. *Following the final cycle of the command sequence, the user must write the first three cycles of the Autoselect command and then write a Reset command.*
18. *If checking the DYB status of sectors in multiple banks, the user must follow Note 17 before crossing a bank boundary.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and RESET#
(Note 2). . . . . –0.5 V to +13.0 V

(Note 2) . . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See . During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 7.*
2. *Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See . Maximum DC input voltage on pin A9, OE#, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

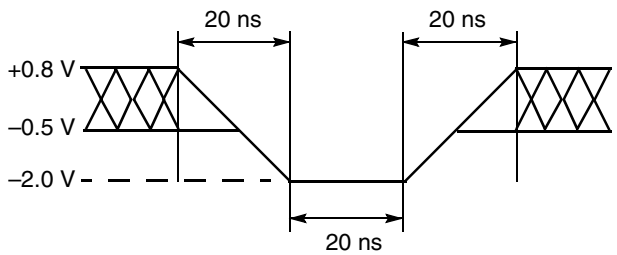


Figure 6. Maximum Negative Overshoot Waveform

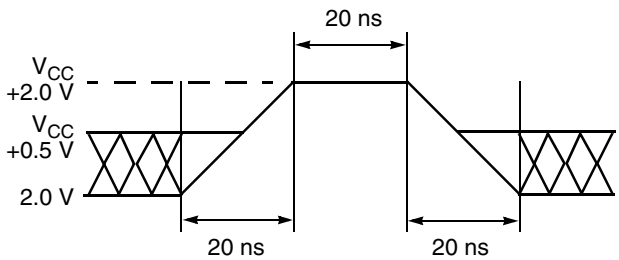


Figure 7. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Supply Voltages

V_{CC} . . . . . 2.7–3.6 V

V_{IO} (see Note) . . . . . 1.65–1.95 V or 2.7–3.6 V

For all AC and DC specifications, $V_{IO} = V_{CC}$; contact AMD for other V_{IO} options.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

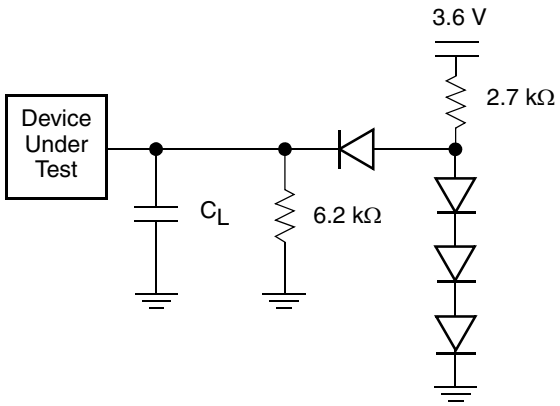
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, OE#, RESET# Input Load Current	$V_{CC} = V_{CC\ max}$; V_{ID}= 12.5 V				35	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; V_{ID}= 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, OE# = V_{IH} $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2, 3)	OE# = V_{IH}, $V_{CC} = V_{CC\ max}$ (Note 1)	5 MHz		20	30	mA
			10 MHz		45	55	
I_{CC2}	V_{CC} Active Write Current (Notes 1, 3, 4)	OE# = V_{IH}, WE# = V_{IL}			15	25	mA
I_{CC3}	V_{CC} Standby Current (Note 3)	CE1#, CE2#, RESET#, WP/ACC# = $V_{IO} \pm 0.3$ V			1	5	µA
I_{CC4}	V_{CC} Reset Current (Note 3)	RESET# = $V_{SS} \pm 0.3$ V, CE# = V_{SS}			1	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 3, 5)	$V_{IH} = V_{IO} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V, CE# = V_{SS}			1	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Notes 1, 2, 3)	OE# = V_{IH}	Word		21	45	mA
I_{CC7}	V_{CC} Active Read-While-Erase Current (Notes 1, 2, 3)	OE# = V_{IH}	Word		21	45	mA
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Notes 1, 3, 6)	OE# = V_{IH}			17	25	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.65–1.95 V		–0.4		0.4	V
		V_{IO} = 2.7–3.6 V		–0.5		0.8	V
V_{IH}	Input High Voltage	V_{IO} = 1.65–1.95 V		V_{IO}–0.4		V_{IO}+0.4	V
		V_{IO} = 2.7–3.6 V		2.0		V_{CC}+0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$, V_{IO} = 1.65–1.95 V				0.1	V
		I_{OL} = 2.0 mA, $V_{CC} = V_{CC\ min}$, V_{IO} = 2.7–3.6 V				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$, V_{IO} = 1.65–1.95 V		V_{IO}–0.1			V
		I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$, V_{IO} = 2.7–3.6 V		2.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 6)			2.3		2.5	V

Notes:

1. *Valid CE1#/CE2# conditions: (CE1#= V_{IL}, CE2#= V_{IH}) or (CE1#= V_{IH}, CE2#= V_{IL})*
2. *The I_{CC} current listed is typically less than 5 mA/MHz, with OE# at V_{IH}.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 150 ns. Typical sleep mode current is 1 µA.*
6. *Not 100% tested.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 8. Test Setup, V_{IO} = 2.7 – 3.6 V

** For V_{IO} = 1.65 – 1.95 Test Setup, the device is tested using C_L only*

Table 16. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

Note: *For 70 pF output load capacitance, 2 ns will be added to certain read-only operation parameters.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

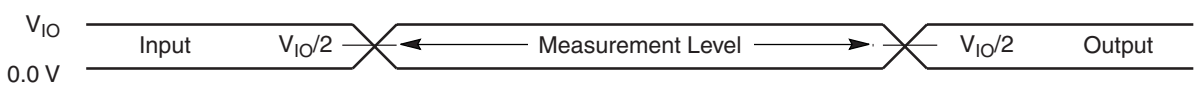


Figure 9. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

CE1#/CE2# Timing

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{CCR}	CE1#/CE2# Recover Time	Min	30	ns

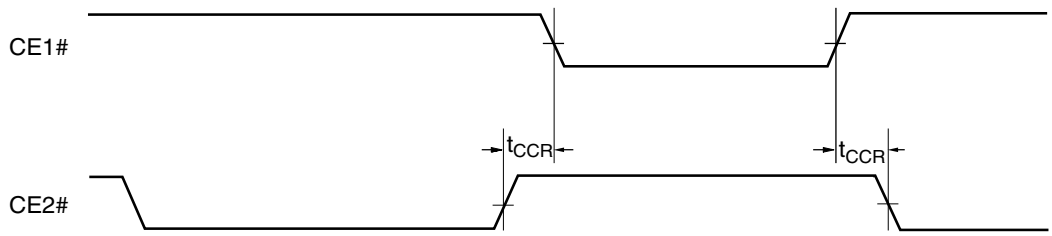


Figure 10. Timing Diagram for Alternating Between CE1# and CE2# Control

Read-Only Operations

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					53	63	68	88	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	55	65	65	85	ns
t_{AVQV}	t_{ACC}	Address to Output Delay (Note 3)		CE#, OE# = V_{IL}	Max	55	65	65	85	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (Note 4)		OE# = V_{IL}	Max	60	65	70	85	ns
	t_{PACC}	Page Access Time			Max	20	25	30		ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	20	25	30		ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 5, 6)			Max	16				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 5)			Max	16				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE#/CE2# or OE#, Whichever Occurs First (Notes 5, 6)			Min	5				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns

Notes:

1. *Not 100% tested.*
2. *See Figure 8 and Table 16 for test specifications*
3. *Valid CE1#/CE2# conditions: (CE1#= V_{IL}, CE2#= V_{IH}) or (CE1#= V_{IH}, CE2#=V_{IL}).*
4. *Valid CE1#/CE2# transitions: (CE1#= CE2#= V_{IH}) to (CE1#= V_{IL}, CE2#=V_{IH}) or (CE1#= V_{IH}, CE2#=V_{IL}).*
5. *Measurements performed by placing a 50 ohm termination on the data pin with a bias of V_{CC}/2. The time from OE# high to the data bus driven to V_{CC}/2 is taken as t_{DF}*
6. *Valid CE1#/CE2# transitions: (CE1#= V_{IL}, CE2#= V_{IH}) or (CE1#= V_{IH}, CE2#=V_{IL}) to (CE1#= CE2#= V_{IH}).*
7. *For 70 pF output load capacitance, 2 ns will be added to t_{ACC}, t_{CE}, t_{PACC}, t_{OE} values for all speed options.*

AC CHARACTERISTICS

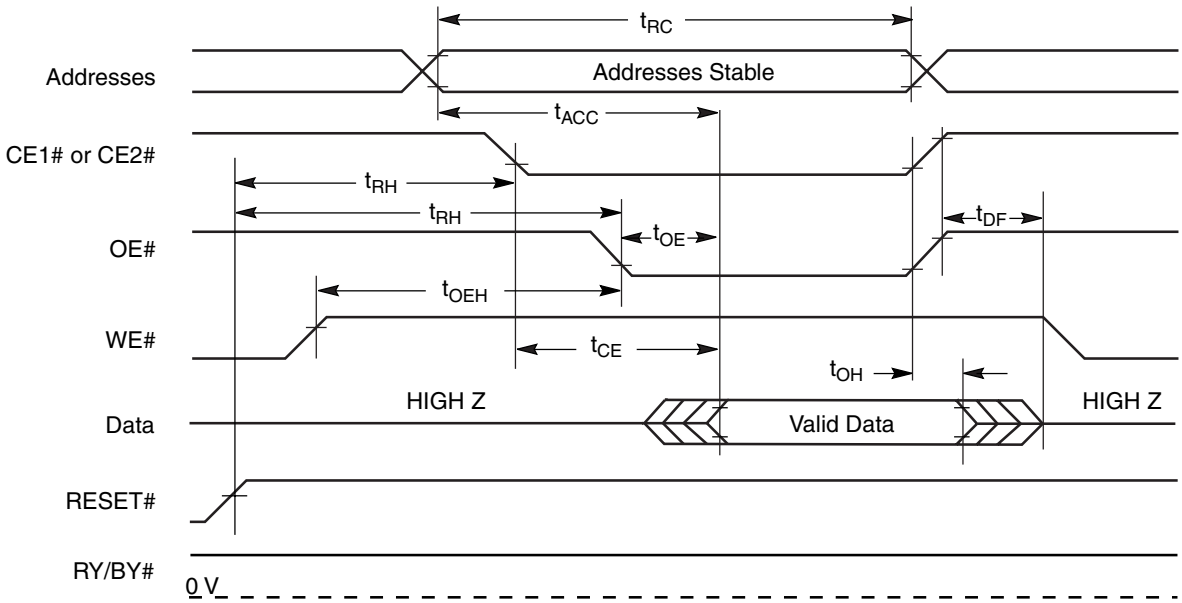


Figure 11. Read Operation Timings

Note:

1. During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}

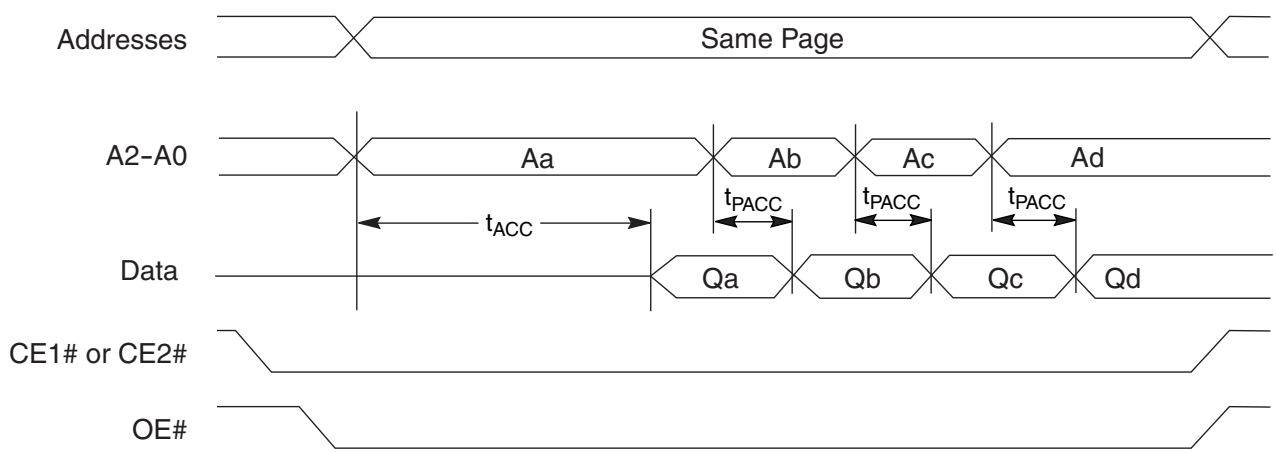


Figure 12. Page Read Operation Timings

Note:

1. During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

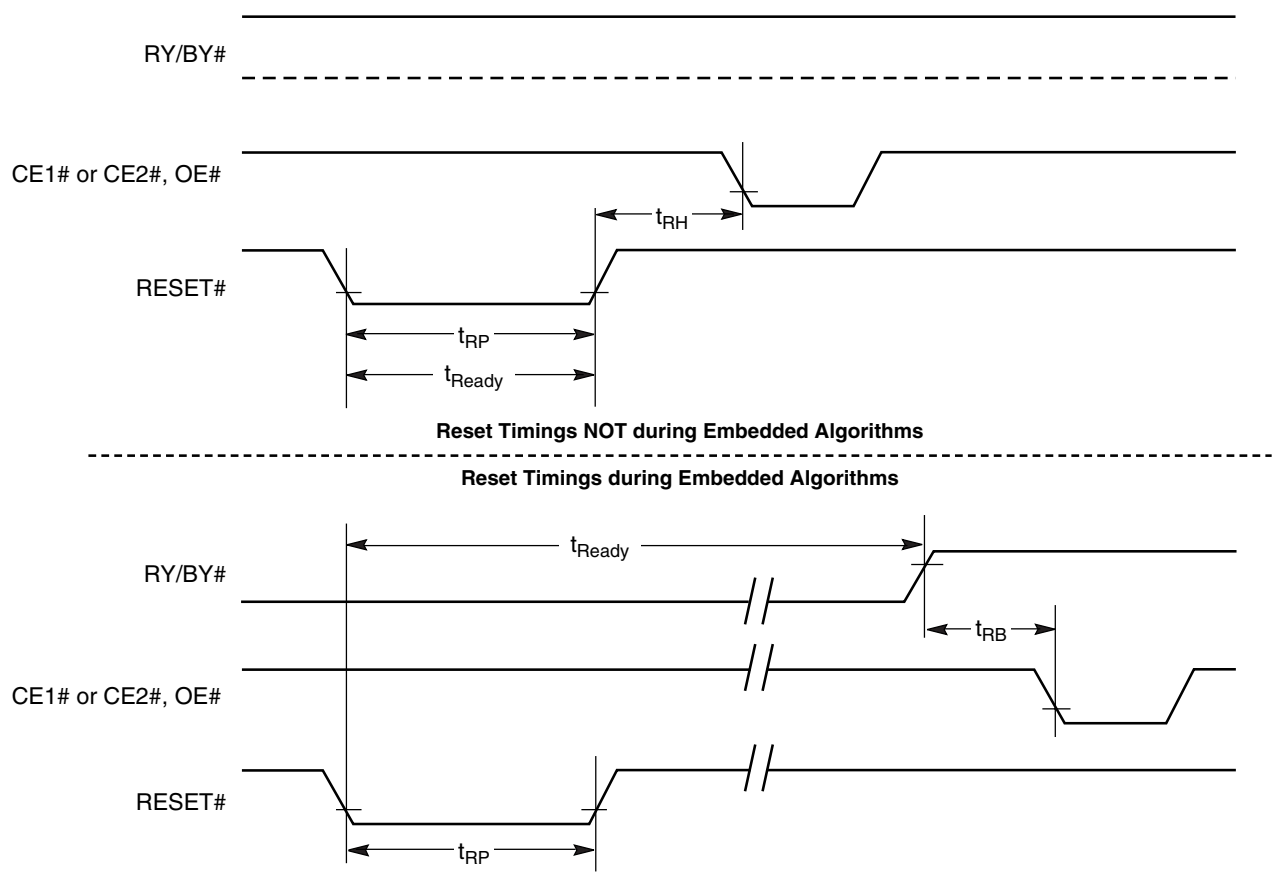


Figure 13. Reset Timings

Note:

1. *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

AC CHARACTERISTICS

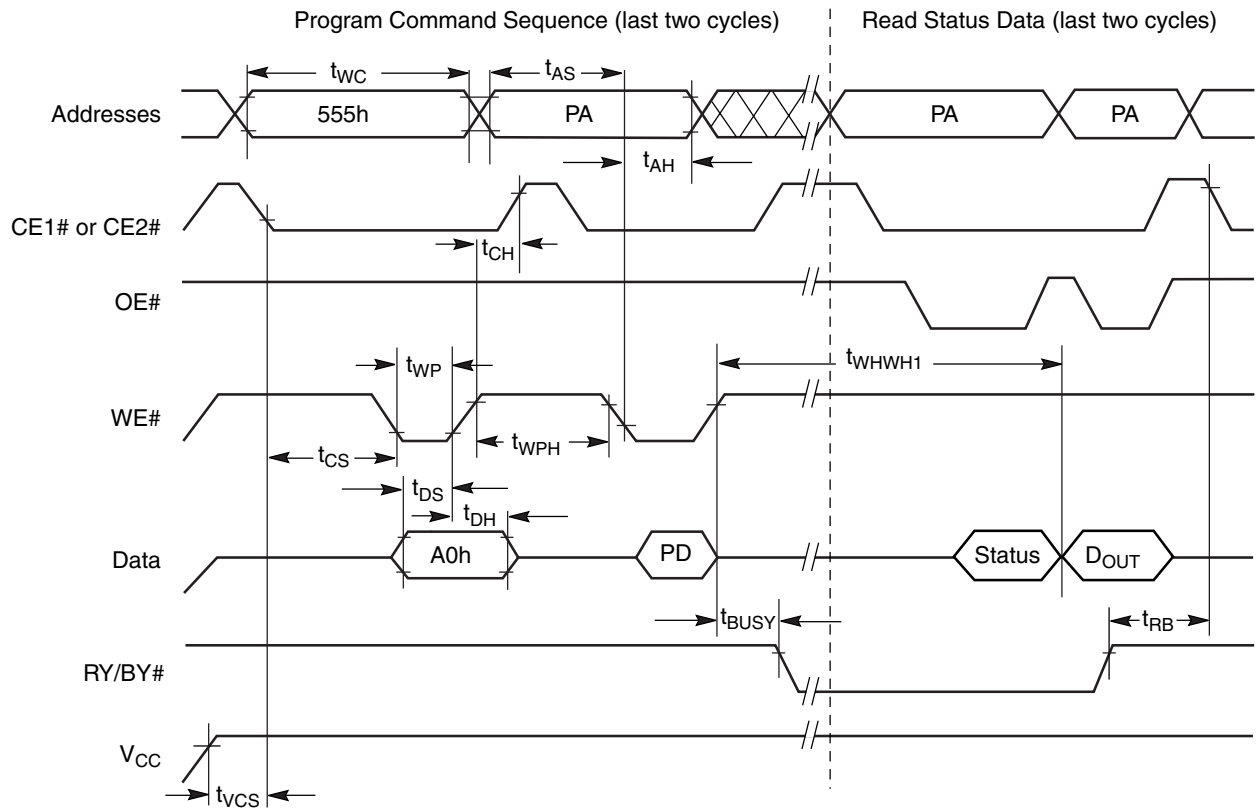
Erase and Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std.			53	63	68	88	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	65	65	85	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	30	35			ns
	t_{AHT}	Address Hold Time From CE1#, CE2#, or OE# high during toggle bit polling	Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	25	30			ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	10				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{ELWL}	t_{CS}	CE1# or CE2# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE1# or CE2# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	40			ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	20	25			ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6				µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5				sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50				µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Max	90				ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

Figure 14. Program Operation Timings

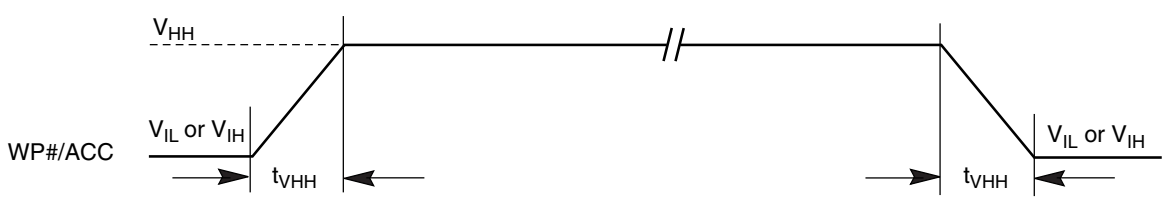
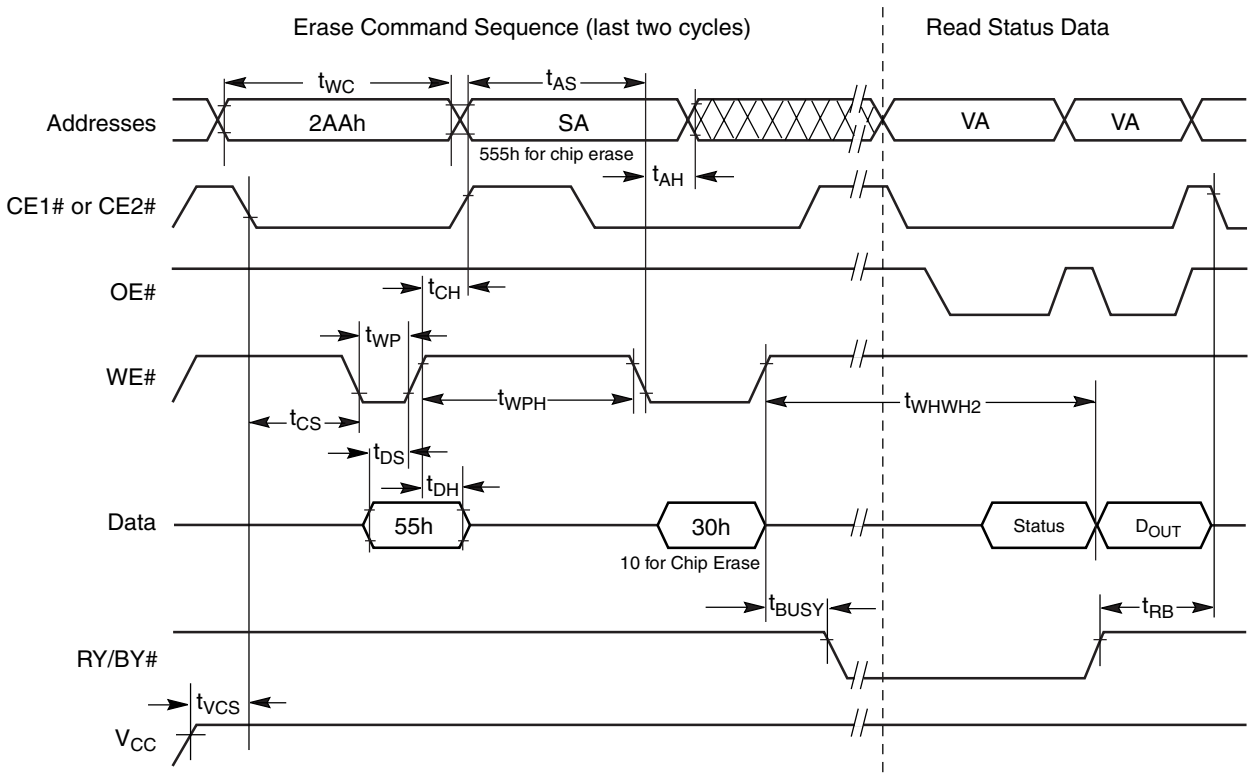


Figure 15. Accelerated Program Timing Diagram

AC CHARACTERISTICS

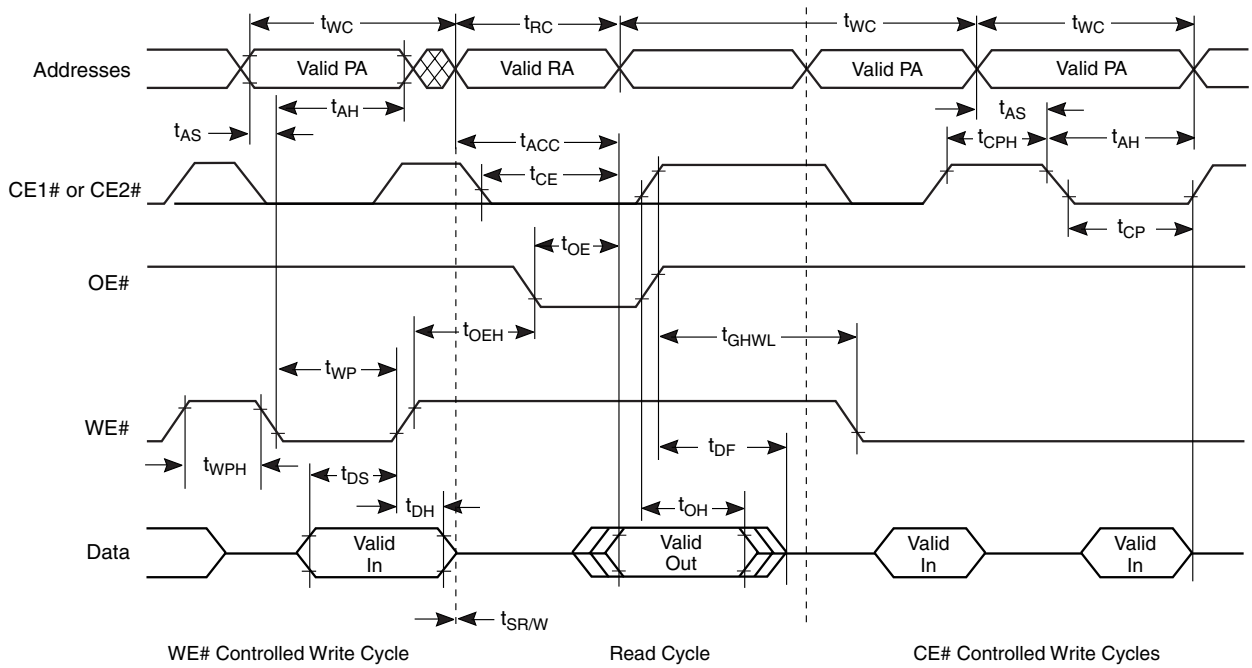


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (.)*
2. *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

Figure 16. Chip/Sector Erase Operation Timings

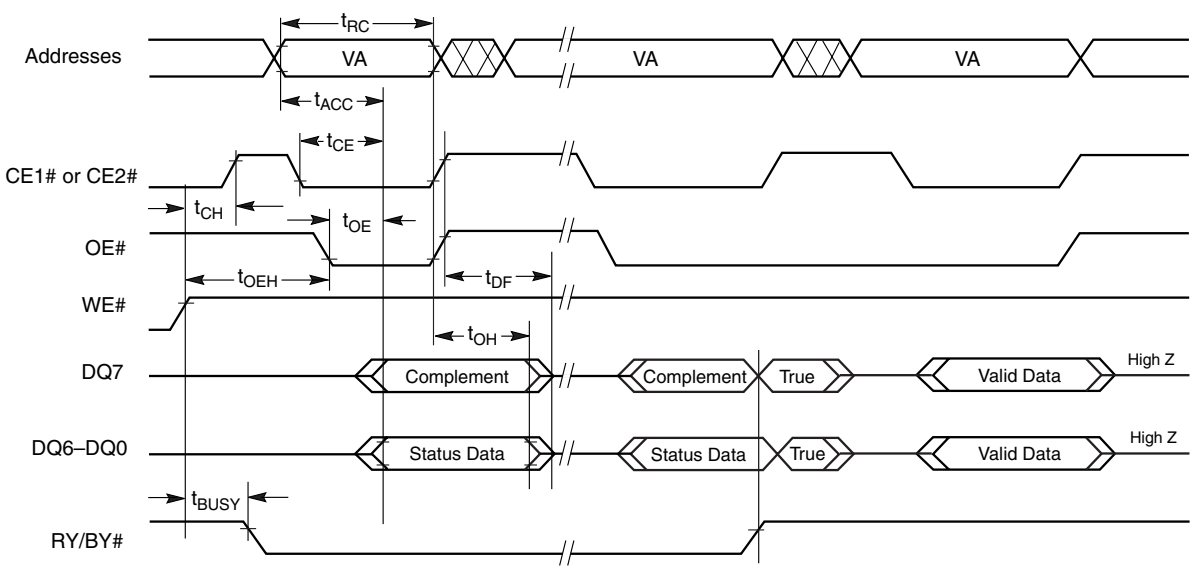
AC CHARACTERISTICS



Note:

1. *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

Figure 17. Back-to-back Read/Write Cycle Timings

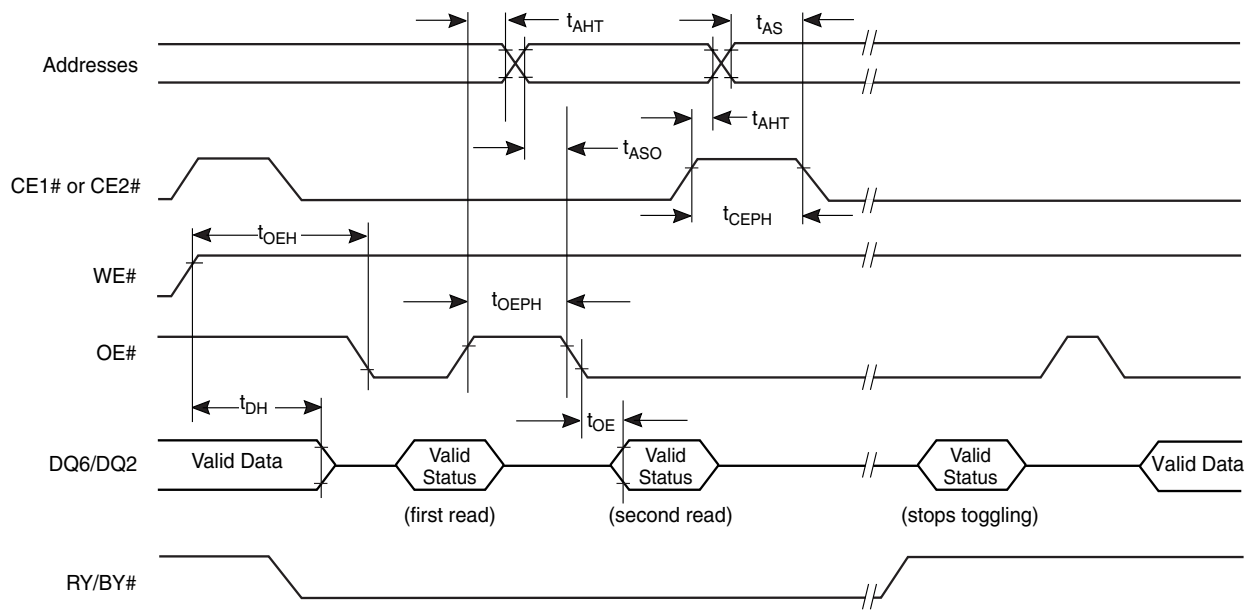


Note:

1. *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle. During CE1# transitions, CE2#= V_{IH};*
2. *During CE2# transitions, CE1#= V_{IH}*

Figure 18. Data# Polling Timings (During Embedded Algorithms)

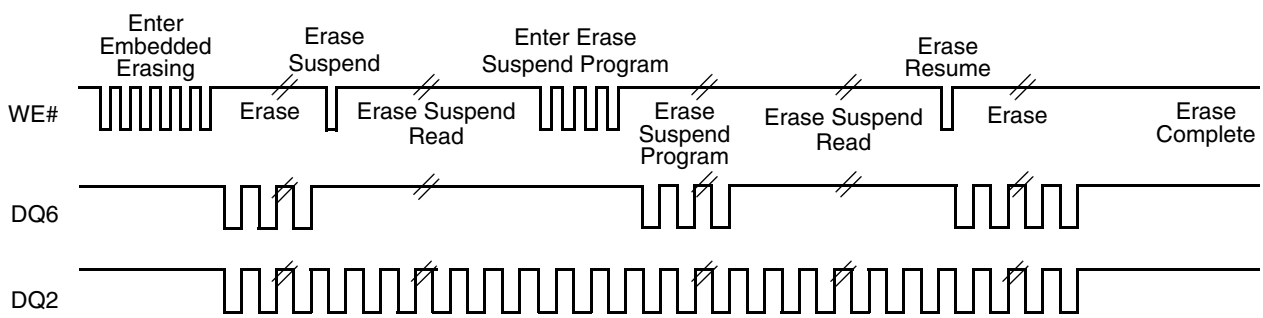
AC CHARACTERISTICS



Notes:

1. *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*
2. *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

Figure 19. Toggle Bit Timings (During Embedded Algorithms)



Note:

1. *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

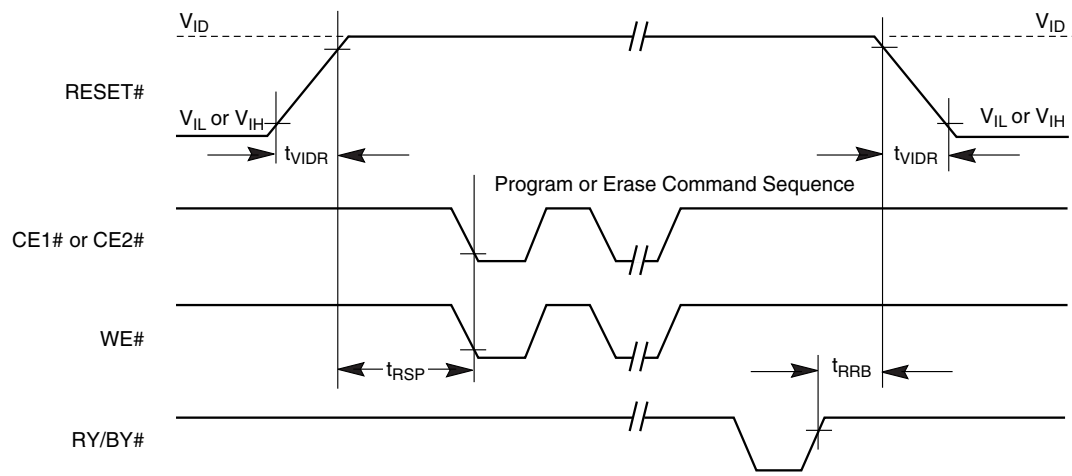
Figure 20. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

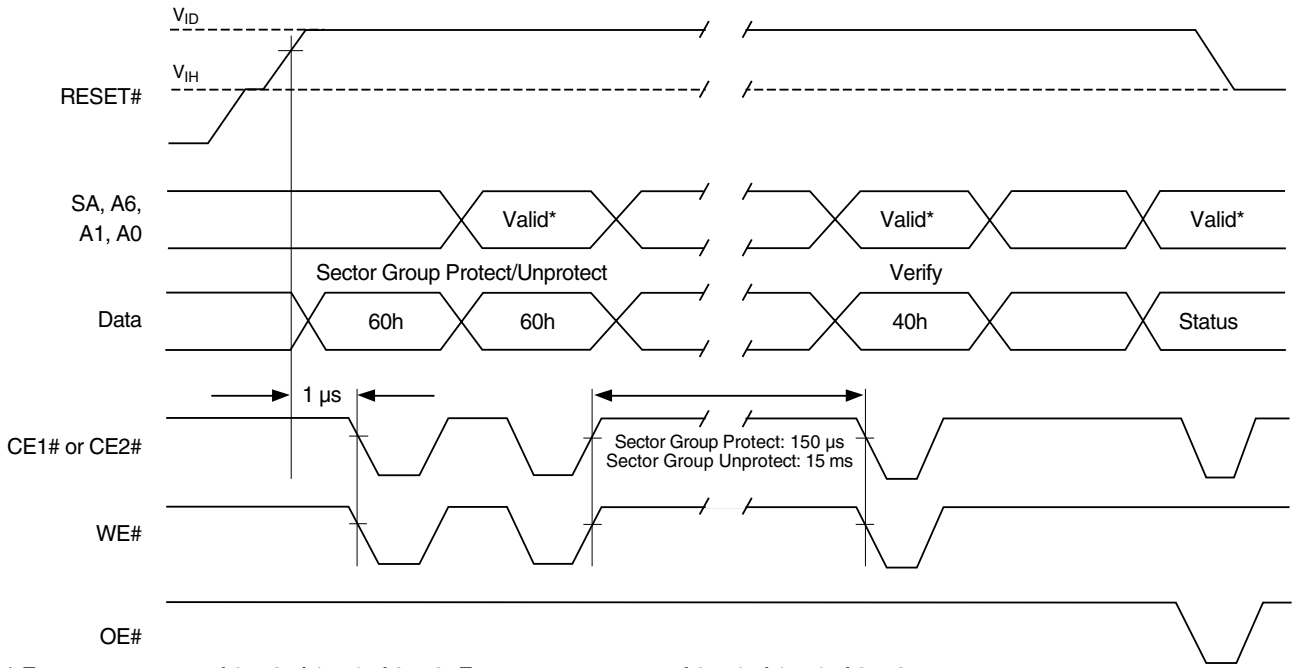
Note: *Not 100% tested.*



Note: *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

Figure 21. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



** For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Notes:

1. *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

Figure 22. Sector/Sector Block Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

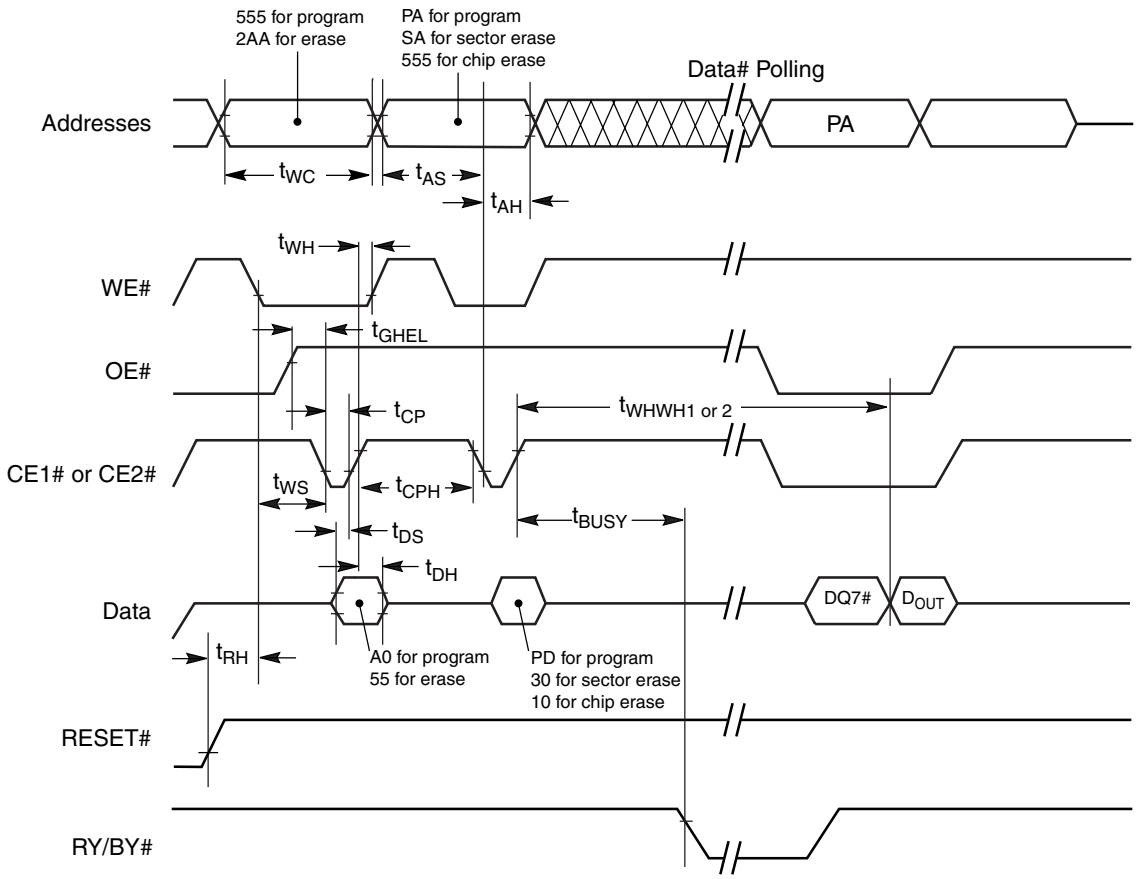
Alternate CE# Controlled Erase and Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std.			53	63	68	88	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	65	65	85	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	30	35			ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	25	30			ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE1# or CE2# Pulse Width	Min	35	40			ns
t_{EHEL}	t_{CPH}	CE1# or CE2# Pulse Width High	Min	20	25			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6				µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5				sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *During CE1# transitions, CE2#= V_{IH}; During CE2# transitions, CE1#= V_{IH}*

Figure 23. Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.4	5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	108		sec	
Word Program Time	6	210	µs	Excludes system level overhead (Note 5)
Accelerated Word Program Time	4	120	µs	
Chip Program Time (Note 3)	50	200	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern. All values are subject to change.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles. All values are subject to change.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Tables for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	13 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time, $V_{IO} = V_{CC}$*

BGA BALL CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	3.9	4.7	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

REVISION SUMMARY

Revision A (September 30, 2002)

Initial release.

Revision A+1 (October 30, 2002)

Product Selector Guide

Modified format of product selector guide table.

Ordering Information

Changed TBD to VK under the package type classification.

Added VK packages to Valid Combinations table.

Global

Changed 55 speed option to 53, changed 65 speed option to 63 and 68.

Table 1. Am29PDL127H Device Bus Operations

Added note #2.

Requirements for Reading Array Data

Reworded Page Mode Read section

Common Flash Memory Interface (CFI)

Changed wording in last sentence of third paragraph from, "...the autoselect mode." to "...reading array data."

Changed CFI website address.

Command Definitions

Changed wording in last sentence of first paragraph from, "...resets the device to reading array data." to ..."may place the device to an unknown state. A reset command is then required to return the device to reading array data."

Customer Lockable: SecSi Sector NOT Programmed or Protected at the factory.

Added second bullet, SecSi sector-protect verify text and Figure 3.

SecSi Sector Flash Memory Region and Enter SecSi Sector/Exit SecSi Sector Command Sequence

Added notes, "*Note that the ACC function and unlock bypass modes are not available when the SecSi sector is enabled.*"

Sector Erase Command Sequence and Chip Erase Command Sequence

Added ""

Table 14. "Memory Array Command Definitions

Changed the first address of the unlock bypass reset command sequence from BA to XXX.

CMOS Compatible

Added I_{LR} parameter to table.

Deleted I_{ACC} parameter from table.

Revision A+2 (January 24, 2003)

Ordering Information

Corrected the ordering part number and package markings for the 83 and 88 speed options.

Revision A+3 (February 26, 2003)

Table 16. Test Specifications

Updated output load capacitance.

Revision A + 4 (April 22, 2003)

Inserted and revised cross references.

Revision A+5 (June 20, 2003)

Distinctive Characteristics

Changed the active read current to 55 mA.

Product Selector Guide

Added row to table to expand speed options and allow for another V_{CC} range.

Physical Dimensions

Removed the LAA064 package.

Revision B (July 29, 2003)

Global

Changed most CE# references to CE1#.

Changed Bank C to Bank 1A, Bank D to Bank 1B, Bank A to Bank 2A, and Bank B to Bank 2B.

Sector Configuration Table

Corrected CE1# and CE2# bank references.

Table 4. Am29PDL129H Sector Architecture

Changed the Bank order to 1A, 1B, 2A, and 2B.

Table 7. Am29PDL129H Boot Sector/Sector Block Addresses for Protection/Unprotection

Broke table up into CE1# and CE2# versions and made modifications to table values to reflect change.

WP# Hardware Protection

Indicated that a write protect pin that can prevent program or erase operations in sectors SA1-133, SA1-134, SA2-0 and SA2-1.

Table 15. Sector Protection Command Definitions

Corrected typos in the PPB status row.

Added Note 17 to PPB Program and PPB Lock Bit Set commands.

Added Note 18 to DYB Status.

Test Conditions

Added note to Figure 10.

Table 16. Test Specifications

Added specific speed options to table.

CMOS Compatible Table

Added CE# = V_{SS} to I_{CC4} and I_{CC5}.

Figure 11. Input Waveforms and Measurement Levels

Modified values to read V_{CC}.

Revision B+1 (August 8, 2003)

Ordering Information

Corrected typo in package marking.

Revision B+2 (December 5, 2003)

Global

Deleted the 83 speed option (85 ns t_{ACC}, V_{IO} = 2.7–3.6V). Replaced the 88 speed option (85 ns t_{ACC}, V_{IO} = 1.65–1.95V) with 78 (70 ns t_{ACC}, V_{IO} = 1.65–1.95V).

Distinctive Characteristics

Performance Characteristics: Under Power Consumption bullet, changed active read current from 55 to 45 mA; changed program/erase current from 25 to 15 mA.

Connection Diagrams

Corrected signal descriptions for balls G1 and J1 on 80-ball fine-pitch BGA package (VBB080).

DC Characteristics

Changed I_{OL} test conditions for V_{OL} from 4.0 mA to 2.0 mA.

Table 16, Test Specifications

Changed C_L from 70 pF to 30 pF. Added note for 70 pF load capacitance.

AC Characteristics

Read-only Operations table: Added note for 70 pF load capacitance.

SecSi™ (Secured Silicon) Sector Flash Memory Region

Customer-Lockable Area: Added sector protection figure and changed figure reference in this section from Figure 1 to Figure 3.

Table 16. Sector Protection Command Definitions

Corrected number of cycles for SecSi Protection Bit Status, PPMLB Status, and SPMLB Status from 4 to 5 cycles. For these command sequences, inserted a cycle before the final read cycle (RD0).

Revision B+3 (November 2, 2005)

Updated migration statement on cover page and first page of data sheet.

This product has been retired and is not available for designs. For new and current designs, Am29PDL129J supersedes Am29PDL129H and is the factory-recommended migration path. Please refer to the Am29PDL129J datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

Updated trademarks.

Trademarks

Copyright © 2000–2005 Advanced Micro Devices, Inc. All rights reserved.
AMD, the AMD logo, and combinations thereof are registered trademarks of Advanced Micro Devices, Inc.
ExpressFlash is a trademark of Advanced Micro Devices, Inc.
Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.