Am29LV033C

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **22268** Revision **B** Amendment **+2** Issue Date **November 7, 2000**

Am29LV033C

32 Megabit (4 M x 8-Bit)
CMOS 3.0 Volt-only Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Zero Power Operation**
  - — Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero
- **Package options**
  - — 63-ball FBGA
  - — 40-pin TSOP
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash standard
- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Flexible sector architecture**
  - — Sixty-four 64 Kbyte sectors
- **Manufactured on 0.32 µm process technology**

PERFORMANCE CHARACTERISTICS

- **High performance**
  - — Access times as fast as 70 ns
  - — Program time: 7 µs/byte typical utilizing Accelerate function
- **Ultra low power consumption (typical values)**
  - — 2 mA active read current at 1 MHz
  - — 10 mA active read current at 5 MHz
  - — 200 nA in standby or automatic sleep mode
- **Minimum 1 million write cycles guaranteed per sector**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system

SOFTWARE FEATURES

- **Supports Common Flash Memory Interface (CFI)**
- **Erase Suspend/Erase Resume**
  - — Suspends erase operations to allow programming in same bank
- **Data# Polling and Toggle Bits**
  - — Provides a software method of detecting the status of program or erase cycles
- **Unlock Bypass Program command**
  - — Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Any combination of sectors can be erased**
- **Ready/Busy# output (RY/BY#)**
  - — Hardware method for detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - — Hardware method of resetting the internal state machine to the read mode
- **ACC input pin**
  - — Acceleration (ACC) function provides accelerated program times
- **Sector protection**
  - — Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - — Temporary Sector Unprotect allows changing data in protected sectors in-system
- **Command sequence optimized for mass storage**
  - — Specific addresses not required for unlock cycles

This Data Sheet states AMD's current technical specifications regarding the Product described herein. This Data Sheet may be revised by subsequent versions or modifications due to changes in technical specifications.

Publication# **22268** Rev: **B** Amendment/**+2**
Issue Date: **Novembe 7, 2000**

GENERAL DESCRIPTION

The Am29LV033C is a 32 Mbit, 3.0 Volt-only Flash memory organized as 4,194,304 bytes. The device is offered in 63-ball FBGA and 40-pin TSOP packages. The byte-wide (x8) data appears on DQ7–DQ0. All read, program, and erase operations are accomplished using only a single power supply. The device can also be programmed in standard EPROM programmers.

The standard device offers access times of 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

TABLE OF CONTENTS

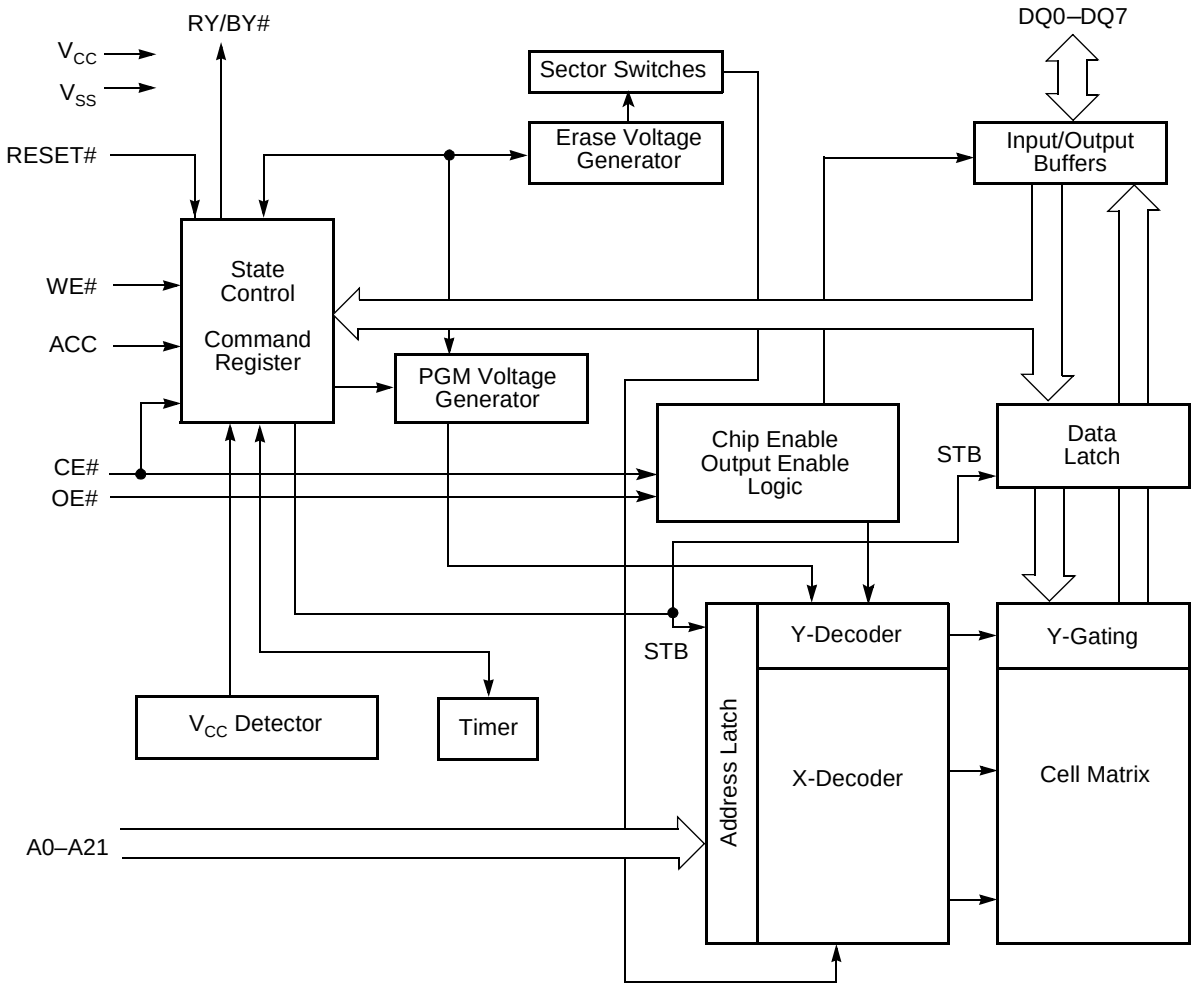
Distinctive Characteristics 1
General Description 2
Product Selector Guide 4
Block Diagram 4
Connection Diagrams 5
Pin Configuration 7
Logic Symbol 7
Ordering Information 8
Standard Products 8
Device Bus Operations 9
Table 1. Am29LV033C Device Bus Operations 9
Requirements for Reading Array Data 9
Writing Commands/Command Sequences 9
Accelerated Program Operation 10
Program and Erase Operation Status 10
Standby Mode 10
Automatic Sleep Mode 10
RESET#: Hardware Reset Pin 10
Output Disable Mode 11
Table 2. Am29LV033C Sector Address Table 11
Autoselect Mode 13
Table 3. Am29LV033C Autoselect Codes (High Voltage Method) 13
Sector/Sector Block Protection and Unprotection 13
Table 4. Sector Block Addresses for Protection/Unprotection 14
Temporary Sector/Sector Block Unprotect 14
Figure 1. Temporary Sector Unprotect Operation 14
Figure 2. In-System Sector Protect/ Unprotect Algorithms 15
Hardware Data Protection 16
Low V_{CC} Write Inhibit 16
Write Pulse “Glitch” Protection 16
Logical Inhibit 16
Power-Up Write Inhibit 16
Common Flash Memory Interface (CFI) 16
Table 5. CFI Query Identification String 16
Table 6. System Interface String 17
Table 7. Device Geometry Definition 17
Table 8. Primary Vendor-Specific Extended Query 18
Command Definitions 19
Reading Array Data 19
Reset Command 19
Autoselect Command Sequence 19
Byte Program Command Sequence 19
Unlock Bypass Command Sequence 20
Accelerated Program Operations 20
Figure 3. Program Operation 20
Chip Erase Command Sequence 20
Sector Erase Command Sequence 21
Erase Suspend/Erase Resume Commands 21
Figure 4. Erase Operation 22
Table 9. Am29LV033C Command Definitions 23
Write Operation Status 24
DQ7: Data# Polling 24
Figure 5. Data# Polling Algorithm 24
RY/BY#: Ready/Busy# 25
DQ6: Toggle Bit I 25
DQ2: Toggle Bit II 25
Reading Toggle Bits DQ6/DQ2 25
DQ5: Exceeded Timing Limits 26
DQ3: Sector Erase Timer 26
Figure 6. Toggle Bit Algorithm 26
Table 10. Write Operation Status 27
Absolute Maximum Ratings 28
Operating Ranges 28
DC Characteristics 29
CMOS Compatible 29
Zero Power Flash 30
Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents) 30
Figure 10. Typical I_{CC1} vs. Frequency 30
Test Conditions 31
Figure 11. Test Setup 31
Table 11. Test Specifications 31
Key to Switching Waveforms 31
Figure 12. Input Waveforms and Measurement Levels 31
AC Characteristics 32
Read Operations 32
Figure 13. Read Operations Timings 32
Hardware Reset (RESET#) 33
Figure 14. RESET# Timings 33
Erase/Program Operations 34
Figure 15. Program Operation Timings 35
Figure 16. Accelerated Program Timing Diagram 35
Figure 17. Chip/Sector Erase Operation Timings 36
Figure 18. Data# Polling Timings (During Embedded Algorithms) 37
Figure 19. Toggle Bit Timings (During Embedded Algorithms) 37
Figure 20. DQ2 vs. DQ6 37
Figure 21. Temporary Sector/Sector Block Unprotect Timing Diagram 38
Figure 22. Sector Protect/Unprotect Timing Diagram 39
Figure 23. Alternate CE# Controlled Write Operation Timings 41
Erase and Programming Performance 42
Latchup Characteristics 42
TSOP Pin Capacitance 42
Data Retention 42
Physical Dimensions 43
TS 040—40-Pin Standard TSOP 43
TSR040—40-Pin Reverse TSOP 44
FBD063—63-Ball Fine-Pitch Ball Grid Array (FBGA) 8 x 14 mm 45
Revision Summary 46
Revision B (January 3, 2000) 46
Revision B+1 (February 21, 2000) 46
Revision B+2 (November 7, 2000) 46

PRODUCT SELECTOR GUIDE

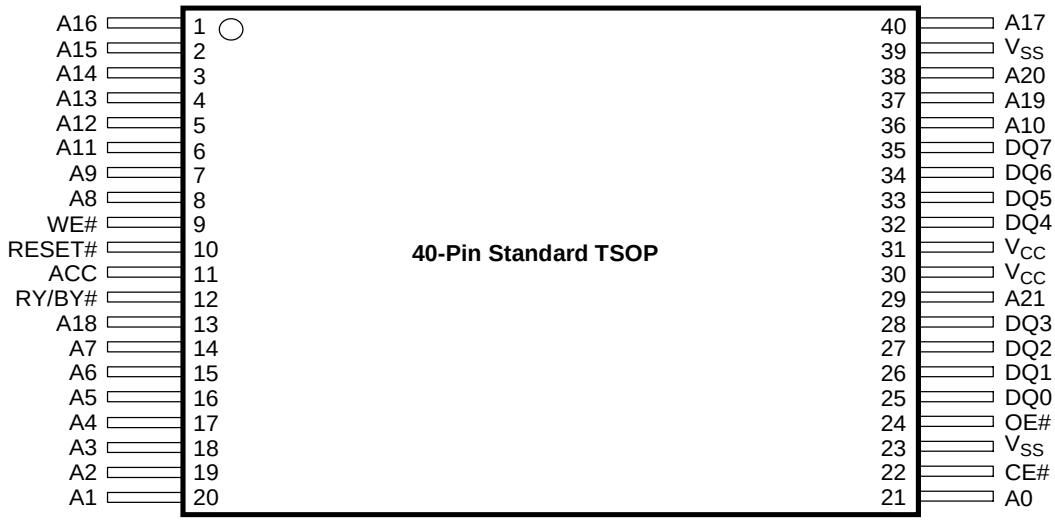
Family Part Number		Am29LV033C		
Speed Option	Full Voltage Range: V_{CC} = 2.7–3.6 V	**-70**	**-90**	**-120**
Max Access Time (ns)		70	90	120
CE# Access (ns)		70	90	120
OE# Access (ns)		30	40	50

Note: *See "AC Characteristics" for full specifications.*

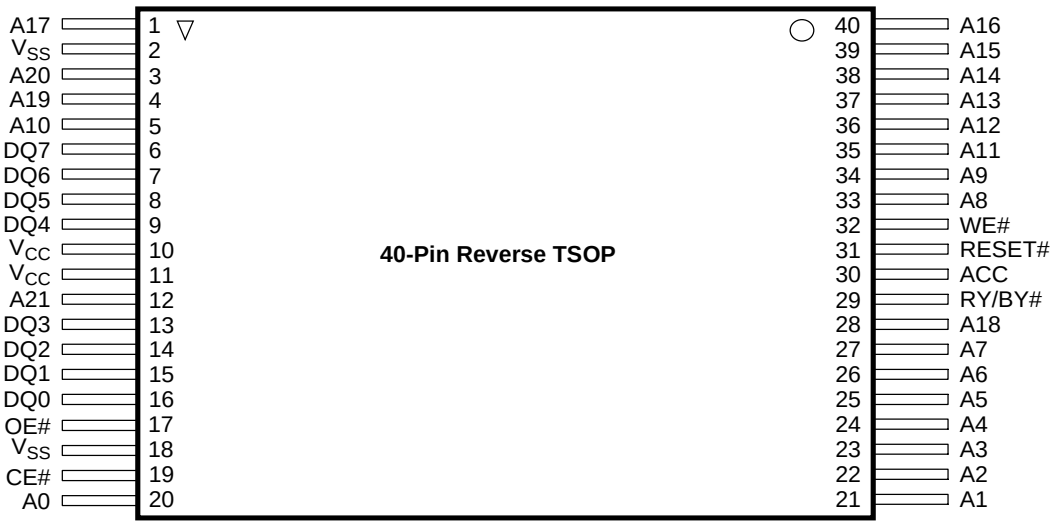
BLOCK DIAGRAM



CONNECTION DIAGRAMS



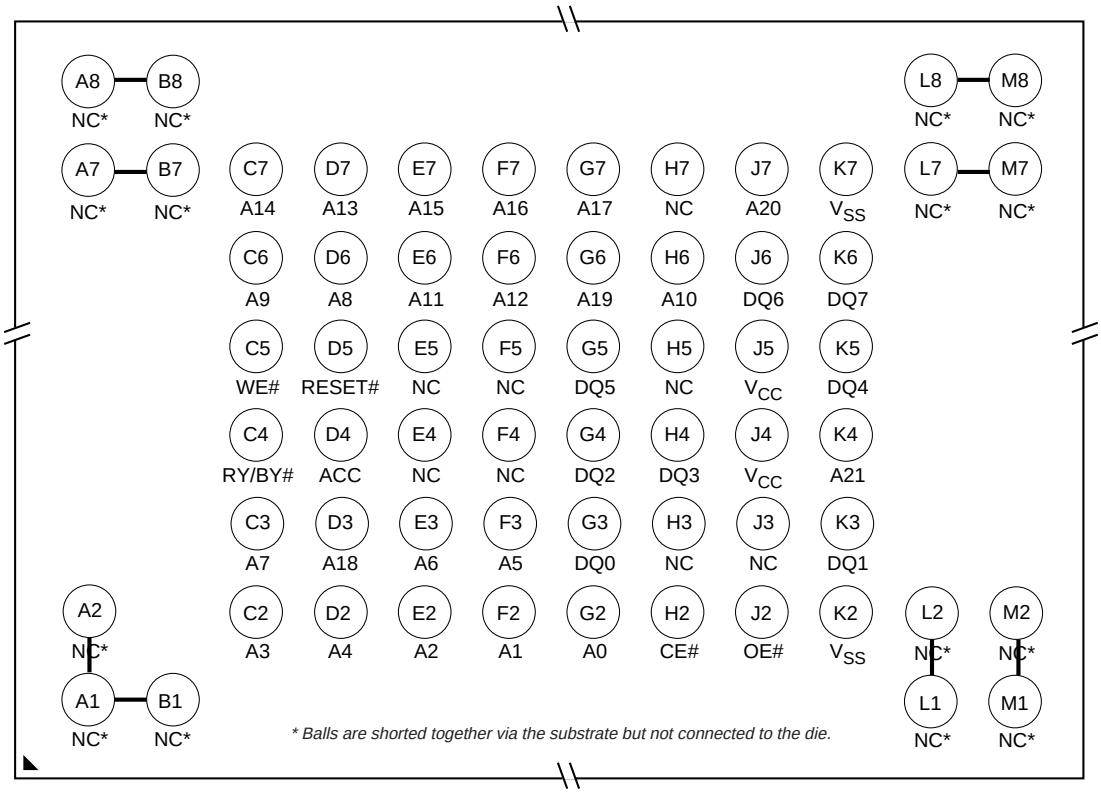
40-Pin Standard TSOP



40-Pin Reverse TSOP

CONNECTION DIAGRAMS

63-Ball FBGA (Top View, Balls Down)



Special Handling Instructions for FBGA Packages

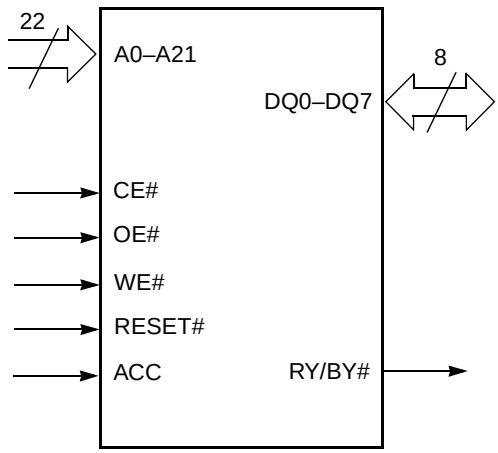
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A21	=	22 addresses
DQ0–DQ7	=	8 data inputs/outputs
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin, active low
RY/BY#	=	Ready/Busy output
ACC	=	Hardware Acceleration Pin
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am29LV033C -70 E C

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
E = 40-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 040)
F = 40-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR040)
WD = 63-ball Fine-Pitch Ball Grid Array (FBGA) 0.80 mm pitch, 8 x 14 mm package (FBD063)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29LV033C
32 Megabit (4 M x 8-Bit) CMOS Flash Memory
3.0 Volt-only Read, Program and Erase

Valid Combinations for TSOP Packages	
AM29LV033C-70	EI, FI
AM29LV033C-90	EI, EE, FI, FE
AM29LV033C-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for FBGA Packages			
Order Number		**Package Marking**	
AM29LV033C-70	WDI	L033C70V	I
AM29LV033C-90	WDI, WDE	L033C90V	I, E
AM29LV033C-120		L033C12V	

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29LV033C Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses	DQ0–DQ7
Read	L	L	H	H	A_{IN}	D_{OUT}
Write (Note 1)	L	H	L	H	A_{IN}	D_{IN}
Standby	$V_{CC} \pm$ 0.3 V	X	X	$V_{CC} \pm$ 0.3 V	X	High-Z
Output Disable	L	H	H	H	X	High-Z
Reset	X	X	X	L	X	High-Z
Sector/Sector Block Protect (Note 2)	L	H	L	V_{ID}	Sector Addresses, A6 = L, A1 = H, A0 = L	D_{IN}, D_{OUT}
Sector/Sector Block Unprotect (Note 2)	L	H	L	V_{ID}	Sector Addresses A6 = H, A1 = H, A0 = L	D_{IN}, D_{OUT}
Temporary Sector/Sector Block Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. *When the ACC pin is at V_{HH}, the device enters the accelerated program mode. See "Accelerated Program Operations" for more information.*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to Figure 13 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a byte, instead of four. The "Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address

space that each sector occupies. A “sector address” consists of the address bits required to uniquely select a sector. The “Command Definitions” section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The “AC Characteristics” section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC pin returns the device to normal operation. Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to “Write Operation Status” for more information, and to “AC Characteristics” for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

The device also enters the standby mode when the RESET# pin is driven low. Refer to the next section, “RESET#: Hardware Reset Pin”.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed

within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 14 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29LV033C Sector Address Table

Sector	A21	A20	A19	A18	A17	A16	Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	000000–00FFFF
SA1	0	0	0	0	0	1	010000–01FFFF
SA2	0	0	0	0	1	0	020000–02FFFF
SA3	0	0	0	0	1	1	030000–03FFFF
SA4	0	0	0	1	0	0	040000–04FFFF
SA5	0	0	0	1	0	1	050000–05FFFF
SA6	0	0	0	1	1	0	060000–06FFFF
SA7	0	0	0	1	1	1	070000–07FFFF
SA8	0	0	1	0	0	0	080000–08FFFF
SA9	0	0	1	0	0	1	090000–09FFFF
SA10	0	0	1	0	1	0	0A0000–0AFFFF
SA11	0	0	1	0	1	1	0B0000–0BFFFF
SA12	0	0	1	1	0	0	0C0000–0CFFFF
SA13	0	0	1	1	0	1	0D0000–0DFFFF
SA14	0	0	1	1	1	0	0E0000–0EFFFF
SA15	0	0	1	1	1	1	0F0000–0FFFFF
SA16	0	1	0	0	0	0	100000–10FFFF
SA17	0	1	0	0	0	1	110000–11FFFF
SA18	0	1	0	0	1	0	120000–12FFFF
SA19	0	1	0	0	1	1	130000–13FFFF
SA20	0	1	0	1	0	0	140000–14FFFF
SA21	0	1	0	1	0	1	150000–15FFFF
SA22	0	1	0	1	1	0	160000–16FFFF
SA23	0	1	0	1	1	1	170000–17FFFF
SA24	0	1	1	0	0	0	180000–18FFFF
SA25	0	1	1	0	0	1	190000–19FFFF
SA26	0	1	1	0	1	0	1A0000–1AFFFF
SA27	0	1	1	0	1	1	1B0000–1BFFFF
SA28	0	1	1	1	0	0	1C0000–1CFFFF
SA29	0	1	1	1	0	1	1D0000–1DFFFF
SA30	0	1	1	1	1	0	1E0000–1EFFFF
SA31	0	1	1	1	1	1	1F0000–1FFFFF

Table 2. Am29LV033C Sector Address Table (Continued)

Sector	A21	A20	A19	A18	A17	A16	Address Range (in hexadecimal)
SA32	1	0	0	0	0	0	200000–20FFFF
SA33	1	0	0	0	0	1	210000–21FFFF
SA34	1	0	0	0	1	0	220000–22FFFF
SA35	1	0	0	0	1	1	230000–23FFFF
SA36	1	0	0	1	0	0	240000–24FFFF
SA37	1	0	0	1	0	1	250000–25FFFF
SA38	1	0	0	1	1	0	260000–26FFFF
SA39	1	0	0	1	1	1	270000–27FFFF
SA40	1	0	1	0	0	0	280000–28FFFF
SA41	1	0	1	0	0	1	290000–29FFFF
SA42	1	0	1	0	1	0	2A0000–2AFFFF
SA43	1	0	1	0	1	1	2B0000–2BFFFF
SA44	1	0	1	1	0	0	2C0000–2CFFFF
SA45	1	0	1	1	0	1	2D0000–2DFFFF
SA46	1	0	1	1	1	0	2E0000–2EFFFF
SA47	1	0	1	1	1	1	2F0000–2FFFFF
SA48	1	1	0	0	0	0	300000–30FFFF
SA49	1	1	0	0	0	1	310000–31FFFF
SA50	1	1	0	0	1	0	320000–32FFFF
SA51	1	1	0	0	1	1	330000–33FFFF
SA52	1	1	0	1	0	0	340000–34FFFF
SA53	1	1	0	1	0	1	350000–35FFFF
SA54	1	1	0	1	1	0	360000–36FFFF
SA55	1	1	0	1	1	1	370000–37FFFF
SA56	1	1	1	0	0	0	380000–38FFFF
SA57	1	1	1	0	0	1	390000–39FFFF
SA58	1	1	1	0	1	0	3A0000–3AFFFF
SA59	1	1	1	0	1	1	3B0000–3BFFFF
SA60	1	1	1	1	0	0	3C0000–3CFFFF
SA61	1	1	1	1	0	1	3D0000–3DFFFF
SA62	1	1	1	1	1	0	3E0000–3EFFFF
SA63	1	1	1	1	1	1	3F0000–3FFFFF

Note: *All sectors are 64 Kbytes in size.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 3. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table). Table 3 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 9. This method does not require V_{ID}. See "Writing specific address and data commands or sequences into the command register initiates device operations. Table 9 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data." for details on using the autoselect mode.

Table 3. Am29LV033C Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A21 to A16	A15 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29LV033C	L	L	H	X	X	V_{ID}	X	L	X	L	H	A3h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected)
												00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector/Sector Block Protection and Unprotection

(Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 4).

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 22 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only AMD flash devices. Publication number 22269 contains further details; contact an AMD representative to request a copy.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

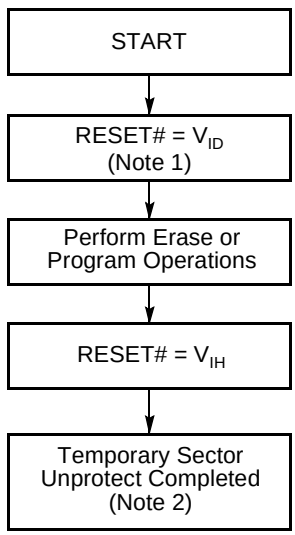
Table 4. Sector Block Addresses for Protection/Unprotection

Sector/ Sector Block	A21–A16	Sector/ Sector Block Size
SA0	000000	64 Kbytes
SA1-SA3	000001,000010, 000011	192 (3x64) Kbytes
SA4-SA7	000100, 000101, 000110, 000111	256 (4x64) Kbytes
SA8-SA11	001000, 001001, 001010, 001011	256 (4x64) Kbytes
SA12-SA15	001100, 001101, 001110, 001111	256 (4x64) Kbytes
SA16-SA19	010000, 010001, 010010, 010011	256 (4x64) Kbytes
SA20-SA23	010100, 010101, 010110, 010111	256 (4x64) Kbytes
SA24-SA27	011000, 011001, 011010, 011011	256 (4x64) Kbytes
SA28-SA31	011100, 011101, 011110, 011111	256 (4x64) Kbytes
SA32-SA35	100000, 100001, 100010, 100011	256 (4x64) Kbytes
SA36-SA39	100100, 100101, 100110, 100111	256 (4x64) Kbytes
SA40-SA43	101000, 101001, 101010, 101011	256 (4x64) Kbytes
SA44-SA47	101100, 101101, 101110, 101111	256 (4x64) Kbytes
SA48-SA51	110000, 110001, 110010, 110011	256 (4x64) Kbytes
SA52-SA55	110100, 110101, 110110, 110111	256 (4x64) Kbytes
SA56-SA59	111000, 111001, 111010, 111011	256 (4x64) Kbytes
SA60-SA62	111100, 111101, 111110	192 (4x64) Kbytes
SA63	111111	64 Kbytes

Temporary Sector/Sector Block Unprotect

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 4).

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 21 shows the timing diagrams, for this feature.



Notes:

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 1. Temporary Sector Unprotect Operation

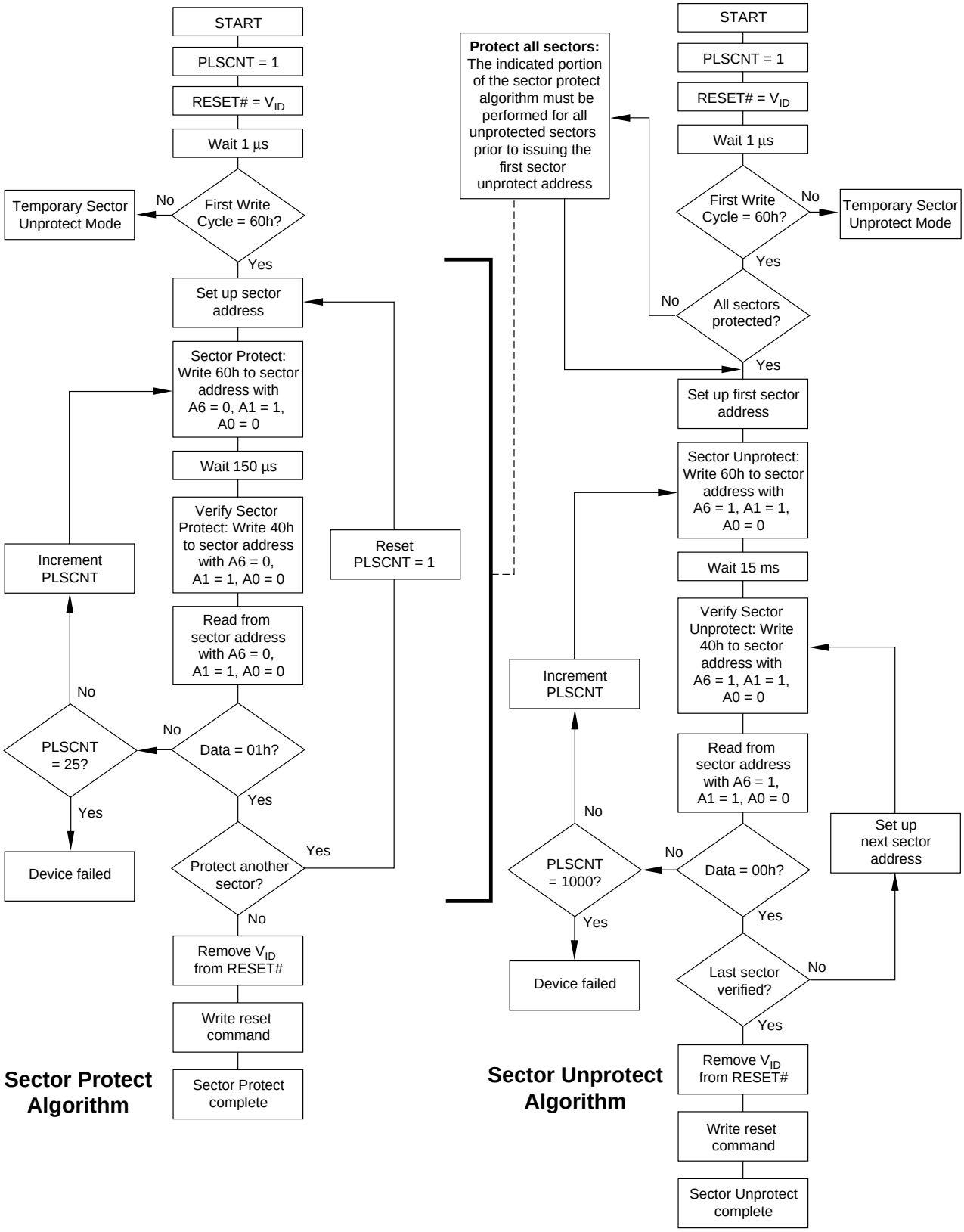


Figure 2. In-System Sector Protect/ Unprotect Algorithms

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 9 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 5–8. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 5–8. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact an AMD representative for copies of these documents.

Table 5. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	51h 52h 59h	Query Unique ASCII string “QRY”
13h 14h	02h 00h	Primary OEM Command Set
15h 16h	40h 00h	Address for Primary Extended Table
17h 18h	00h 00h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	00h 00h	Address for Alternate OEM Extended Table (00h = none exists)

Table 6. System Interface String

Addresses	Data	Description
1Bh	27h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	36h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	00h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	00h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	04h	Typical timeout per single byte/word write 2^N µs
20h	00h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0Ah	Typical timeout per individual block erase 2^N ms
22h	00h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	05h	Max. timeout for byte/word write 2^N times typical
24h	00h	Max. timeout for buffer write 2^N times typical
25h	04h	Max. timeout per individual block erase 2^N times typical
26h	00h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 7. Device Geometry Definition

Addresses	Data	Description
27h	16h	Device Size = 2^N byte
28h 29h	00h 00h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	00h 00h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	01h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	3Fh 00h 00h 01h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	00h 00h 00h 00h	Erase Block Region 2 Information
35h 36h 37h 38h	00h 00h 00h 00h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	00h 00h 00h 00h	Erase Block Region 4 Information

Table 8. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	50h 52h 49h	Query-unique ASCII string “PRI”
43h	31h	Major version number, ASCII
44h	30h	Minor version number, ASCII
45h	01h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	02h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	01h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	04h	Sector Temporary Unprotect: 04 = Supported
49h	04h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	20h	Simultaneous Operation: 20 = Not Supported
4Bh	00h	Burst Mode Type: 00 = Not Supported, 01 = Supported
4Ch	00h	Page Mode Type: 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 9 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 9 shows the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Program Command Sequence

The device programs one byte of data for each program operation. The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 9 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command se-

quence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set DQ5 to "1," or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Unlock Bypass Command Sequence

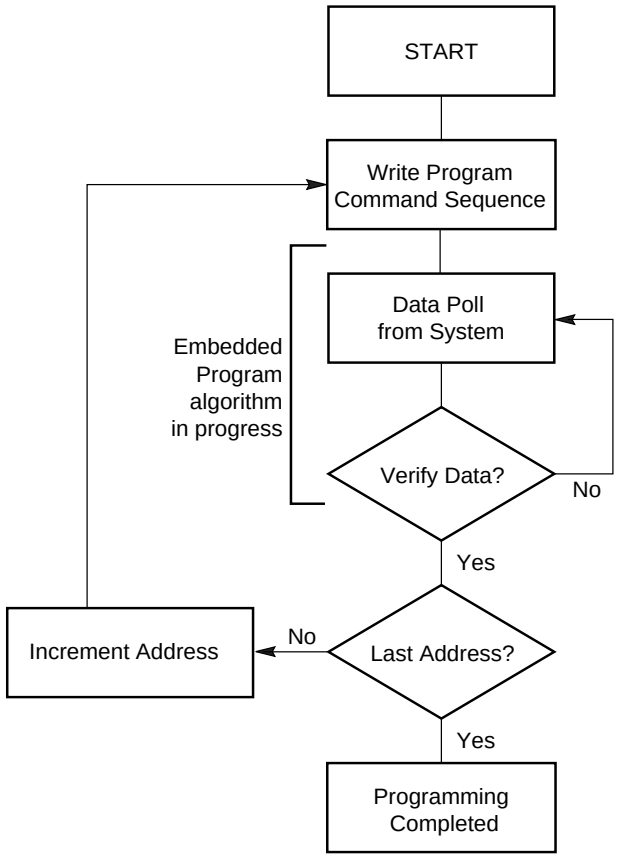
The unlock bypass feature allows the system to program bytes to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 9 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't cares for both cycles. The device then returns to reading array data.

Accelerated Program Operations

The device offers accelerated program operations through the ACC pin. When the system asserts V_{HH} on the ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence, eliminating two cycles from the command sequence. In addition, the device uses the higher voltage on the ACC pin to accelerate the operation. *Note that the ACC pin must not be at V_{HH} during read or erase operations, or device damage may result.* If ACC is to be permanently set, it is recommended that it be tied to V_{CC} to minimize current consumption.

Figure 3 illustrates the algorithm for the program operation. See the Erase/Program Operations table in "AC Characteristics" for parameters, and to Figure 15 for timing diagrams.



Note: *See Table 9 for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 9 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the de-

vice has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 17 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 9 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to "Write Operation Status" for information on these status bits.)

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to Figure 17 for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the time-out period 50 µs during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

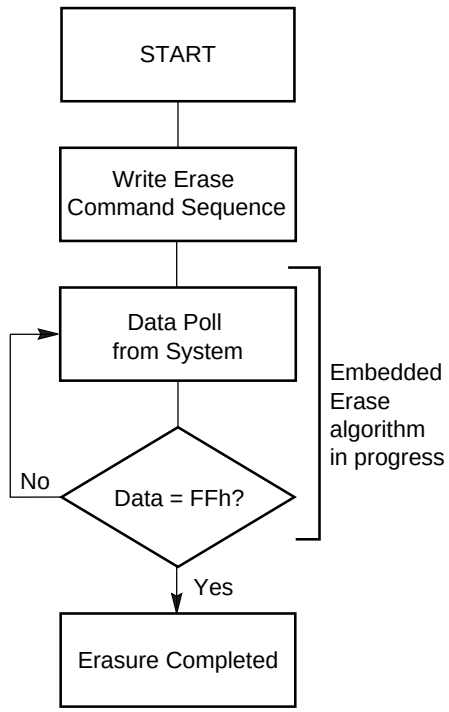
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard pro-

gram operation. See “Write Operation Status” for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Notes:

1. *See Table 9 for erase command sequence.*
2. *See “DQ3: Sector Erase Timer” for more information.*

Figure 4. Erase Operation

Table 9. Am29LV033C Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID (Note 8)	4	XXX	AA	XXX	55	0XXXXX	90	0XXX00	01				
	Device ID (Note 8)	4	XXX	AA	XXX	55	0XXXXX	90	0XXX01	A3				
	Sector Protect Verify (Note 9)	4	XXX	AA	XXX	55	0XXXXX or 2XXXXX	90	SA X02	00				
			XXX		XXX					01				
Byte Program		4	XXX	AA	XXX	55	XXX	A0	PA	PD				
Unlock Bypass		3	XXX	AA	XXX	55	XXX	20						
Unlock Bypass Program (Note 10)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)		2	XXX	90	XXX	00								
Chip Erase		6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	XXX	10
Sector Erase		6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	SA	30
Erase Suspend (Note 12)		1	XXX	B0										
Erase Resume (Note 13)		1	XXX	30										
CFI Query (Note 14)		1	XXX	98										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse.

PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse.

SA = Address of the sector to be erased or verified. Address bits A21–A16 uniquely select any sector.

Notes:

1. *See Table 1 for descriptions of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Address bits are don't care for unlock and command cycles, except when PA or SA is required.*
5. *No unlock or command cycles required when device is in read mode.*
6. *The Reset command is required to return to the read mode when the device is in the autoselect mode or if DQ5 goes high.*
7. *The fourth cycle of the autoselect command sequence is a read cycle.*
8. *In the third and fourth cycles of the command sequence, set A21 to 0.*
9. *In the third cycle of the command sequence, address bit A21 must be set to 0 if verifying sectors 0–31, or to 1 if verifying sectors 32–64. The data in the fourth cycle is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the Unlock Bypass mode.*
12. *The system may read and program functions in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
13. *The Erase Resume command is valid only during the Erase Suspend mode.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 10 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

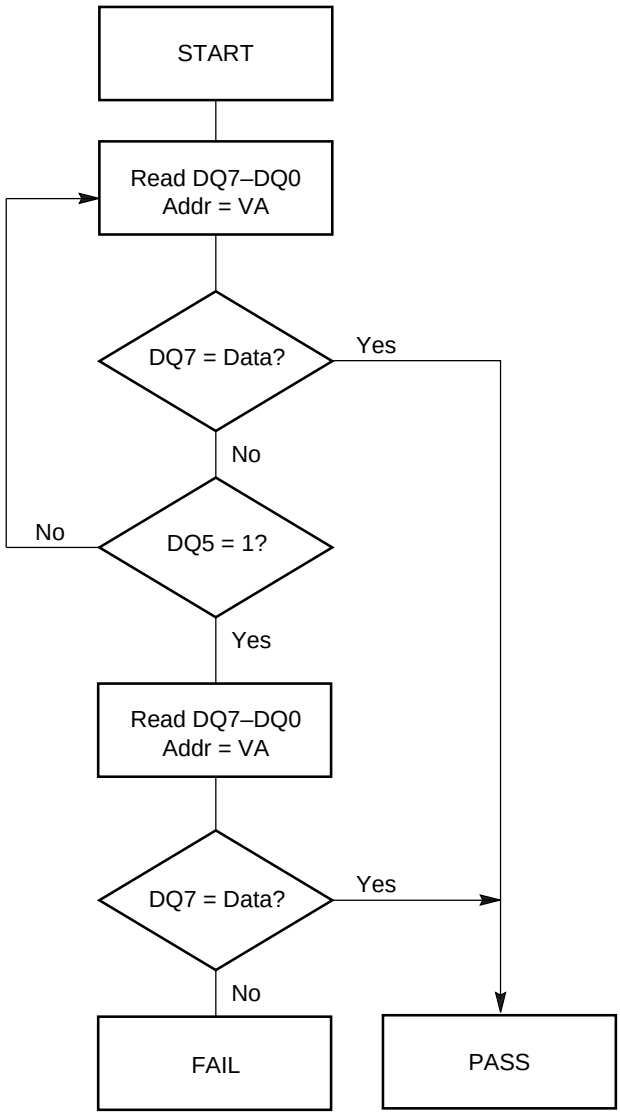
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 18, Data# Polling Timings (During Embedded Algorithms), in the “AC Characteristics” section illustrates this.

Table 10 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 10 shows the outputs for RY/BY#. Figures 14, 15 and 17 shows RY/BY# for reset, program, and erase operations, respectively.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle (The system may use either OE# or CE# to control the read cycles). When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 10 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm in flowchart form, and the section “Reading Toggle Bits DQ6/DQ2” explains the algorithm. Figure 19 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 20 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 10 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section “Reading Toggle Bits DQ6/DQ2” explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 19 shows the toggle bit timing diagram. Figure 20 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer

toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

Table 10 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 19 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 20 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

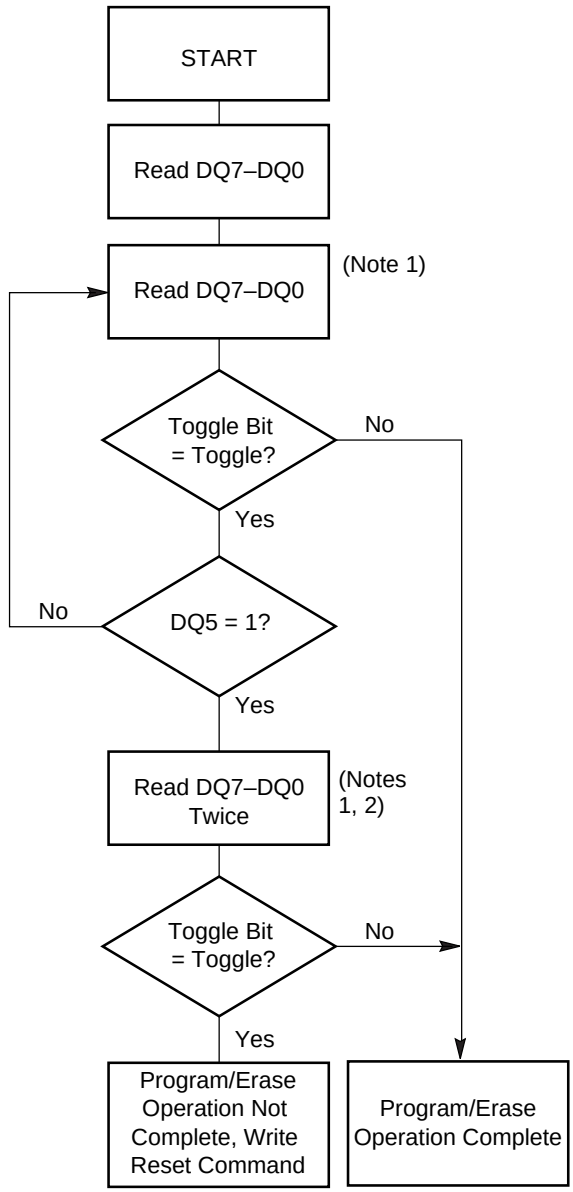
The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.”

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the “Sector Erase Command Sequence” section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to “1”. See text.*

Figure 6. Toggle Bit Algorithm

DQ3 is “1”, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 10 shows the outputs for DQ3.

Table 10. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and
RESET# (Note 2) . . . . . –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A). . . . . .0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . .–40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). . . . . .–55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for full voltage range. . . . . +2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

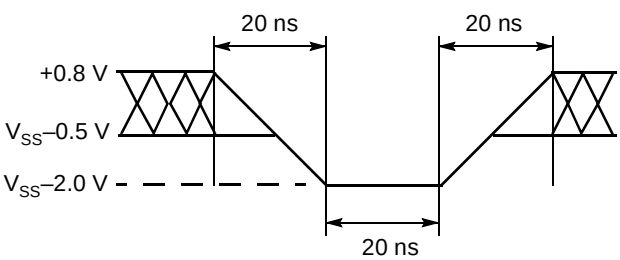


Figure 7. Maximum Negative Overshoot Waveform

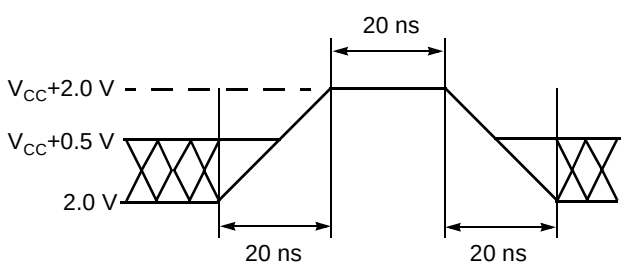


Figure 8. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS

CMOS Compatible

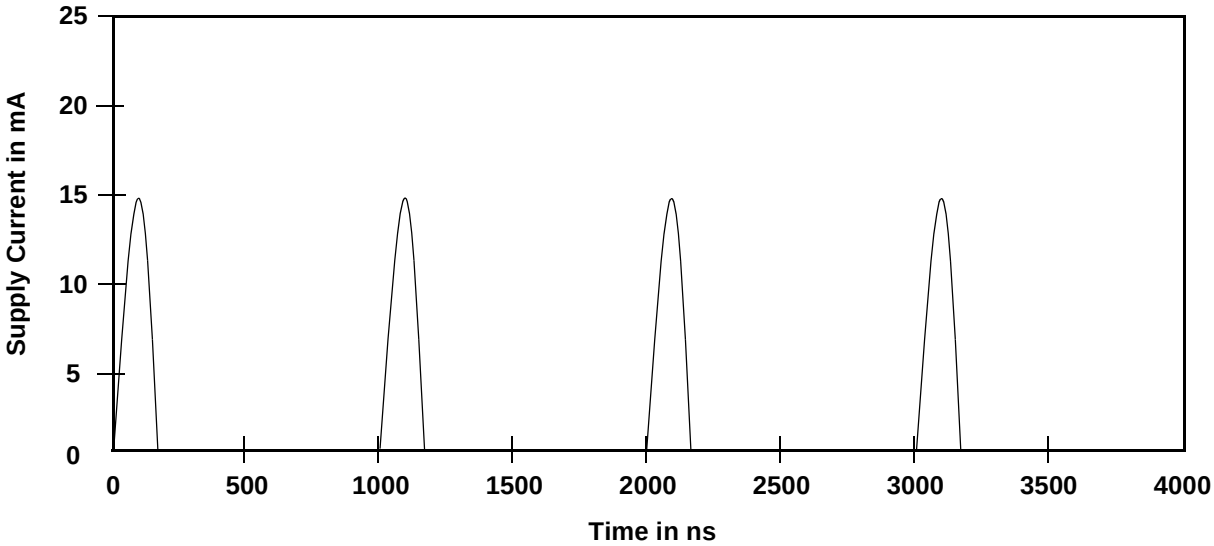
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (Note 1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		10	16	mA
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 4, 6)	CE# = V_{IL}, OE# = V_{IH}			15	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET#, ACC = V_{CC}±0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V, ACC = V_{CC} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 5)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V, ACC = V_{CC} ± 0.3 V			0.2	5	µA
I_{ACC}	ACC Accelerated Program Current, Word or Byte	CE# = V_{IL}, OE# = V_{IH}	ACC pin		5	10	mA
			V_{CC} pin		15	30	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Voltage for ACC Sector Protect/Unprotect and Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 6)			2.3		2.5	V

Notes:

1. *On the ACC pin only, the maximum input load current when ACC = V_{IL} is ±5.0 µA.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *The I_{CC} current listed is typically is less than 2 mA/MHz, with OE# at V_{IH}. Typical specifications are for V_{CC} = 3.0 V.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
6. *Not 100% tested.*

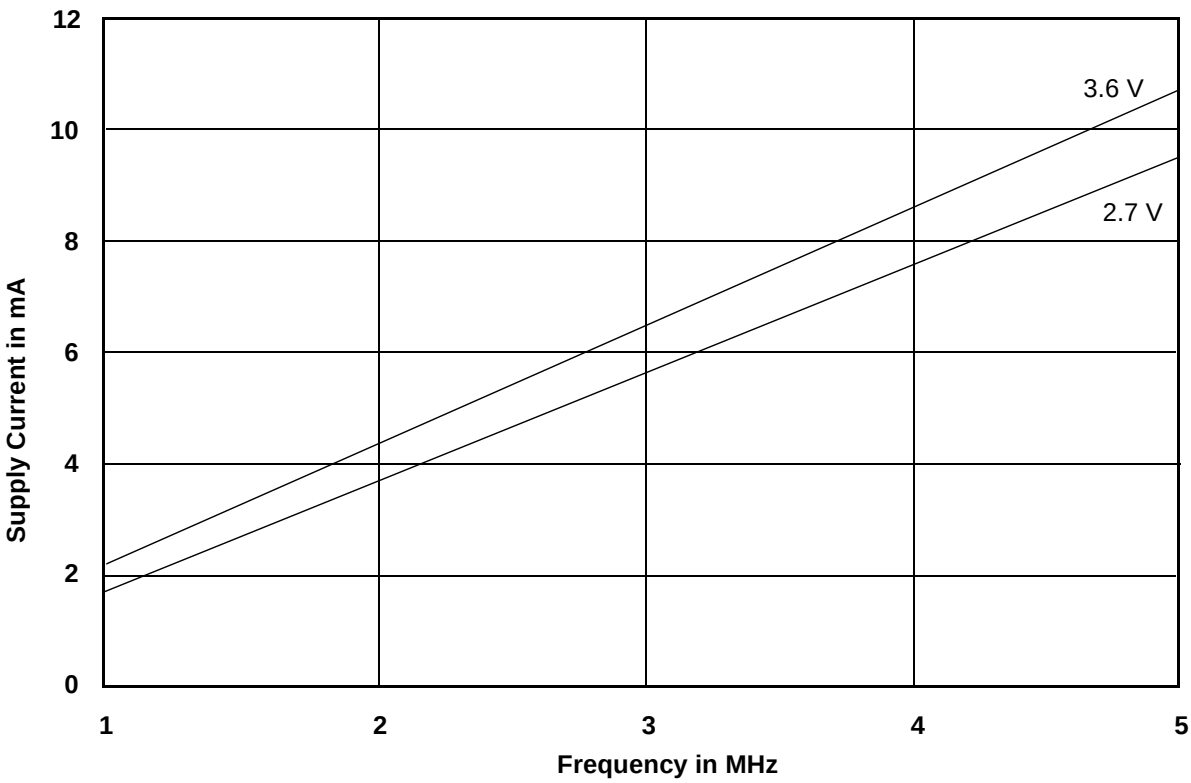
DC CHARACTERISTICS (Continued)

Zero Power Flash



Note: *Addresses are switching at 1 MHz*

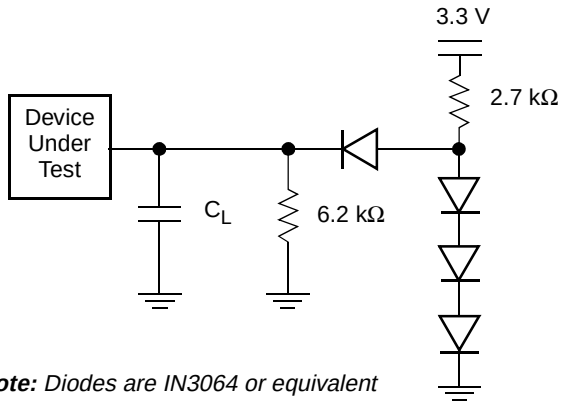
Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 10. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



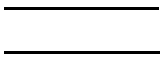
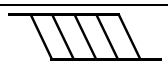
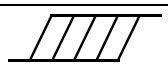
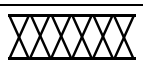
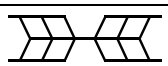
Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 11. Test Specifications

Test Condition	-70	-90, -120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

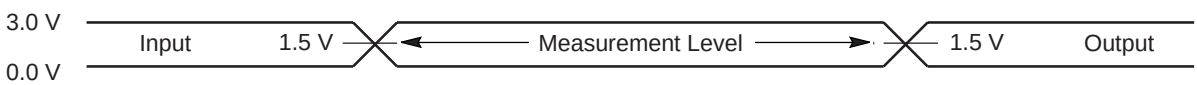


Figure 12. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Option			Unit
JEDEC	Std					-70	-90	-120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	40	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	25	30	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0			ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 11 for test specifications.*

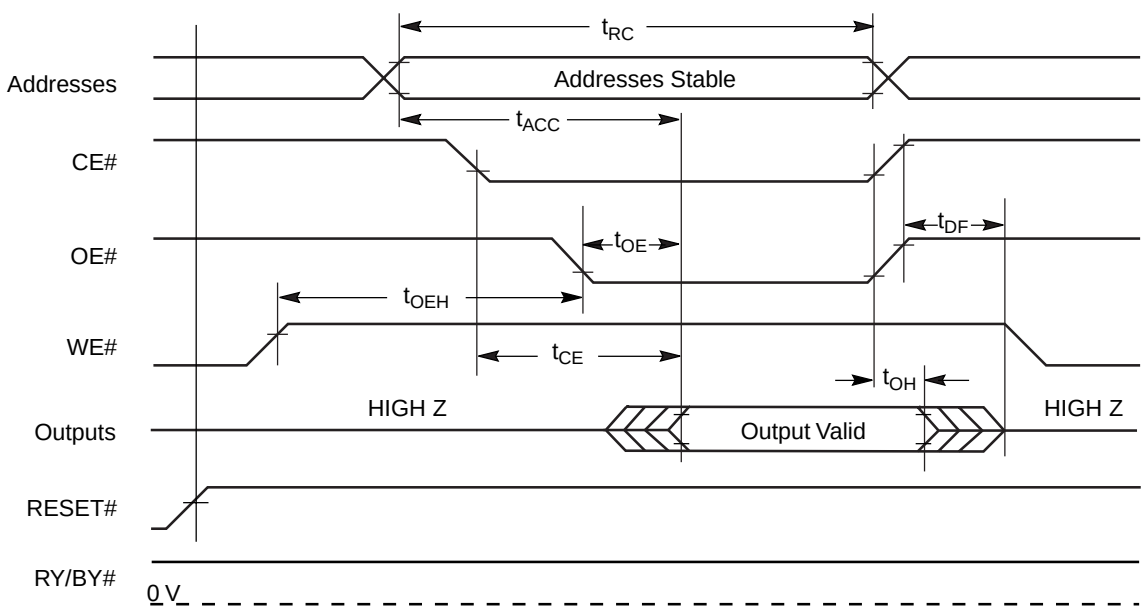


Figure 13. Read Operations Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: *Not 100% tested.*

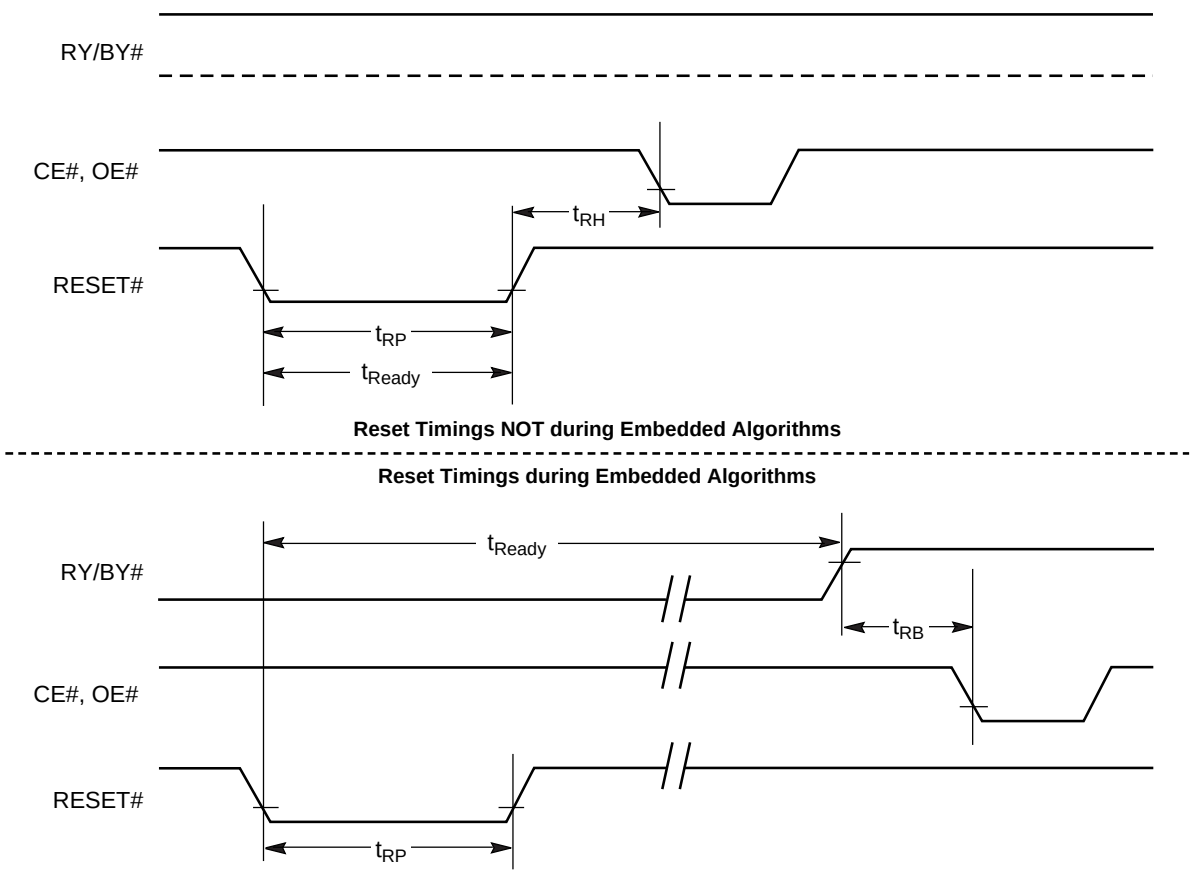


Figure 14. RESET# Timings

AC CHARACTERISTICS

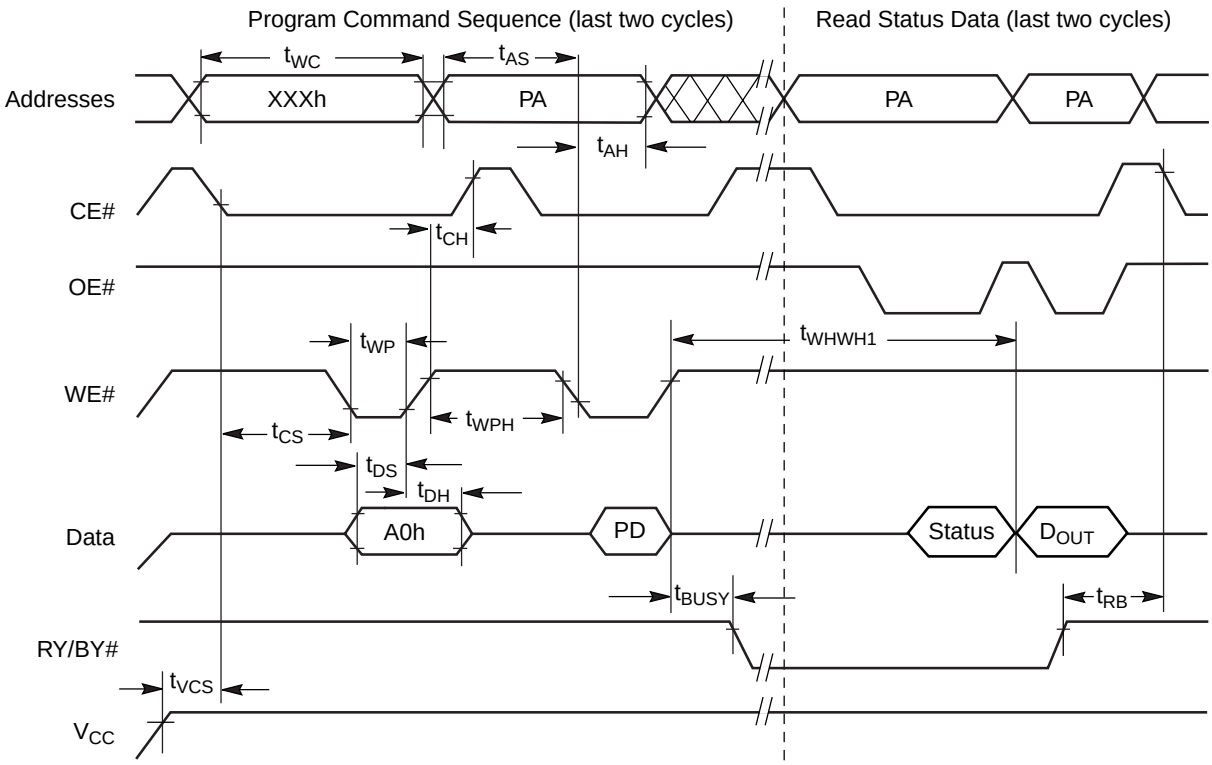
Erase/Program Operations

Parameter		Description		Speed Option			Unit
JEDEC	Std			-70	-90	-120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0			ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0			ns
	t_{OES}	Output Enable Setup Time (Note 1)	Min	0			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	30	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9			µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	7			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.7			sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50			µs
	t_{RB}	Recovery Time from RY/BY#	Min	0			ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Min	90			ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC CHARACTERISTICS



Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

Figure 15. Program Operation Timings

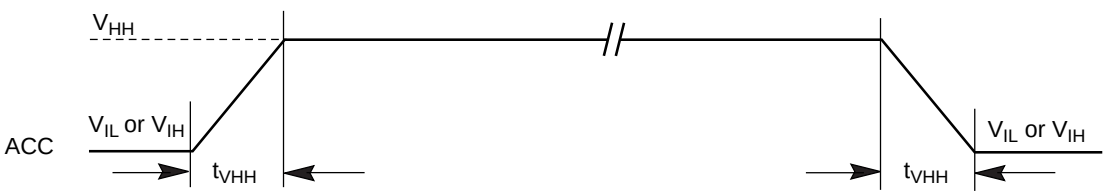
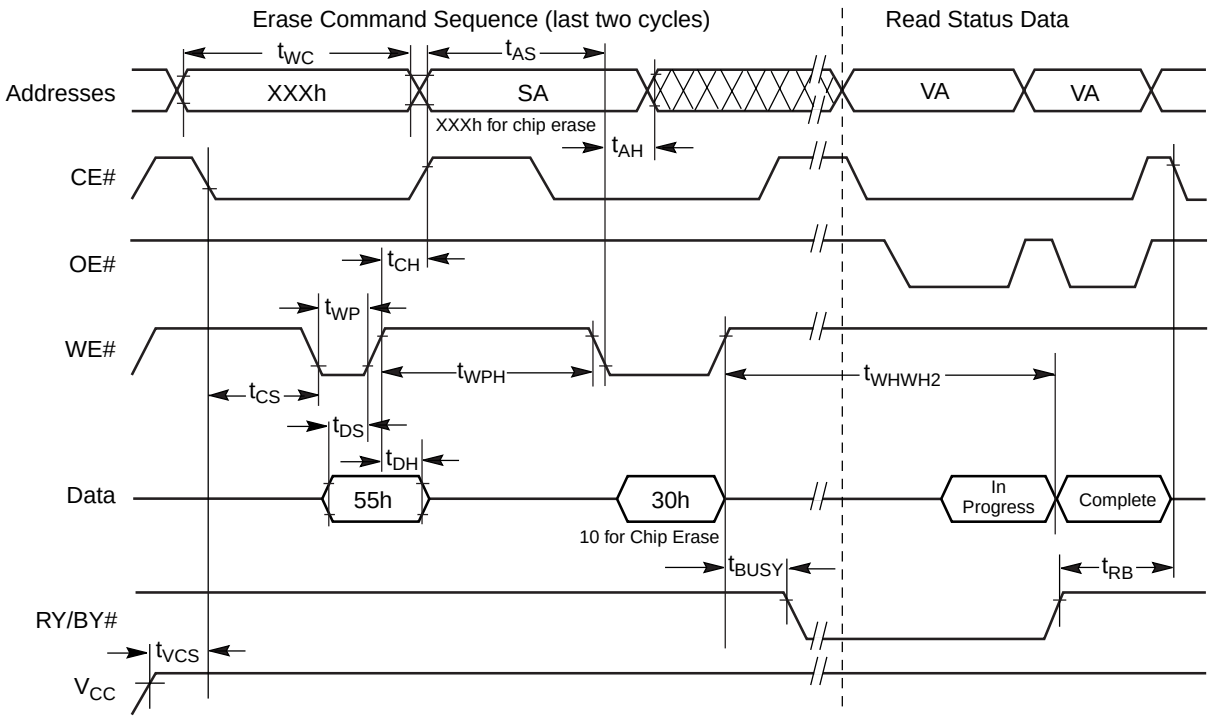


Figure 16. Accelerated Program Timing Diagram

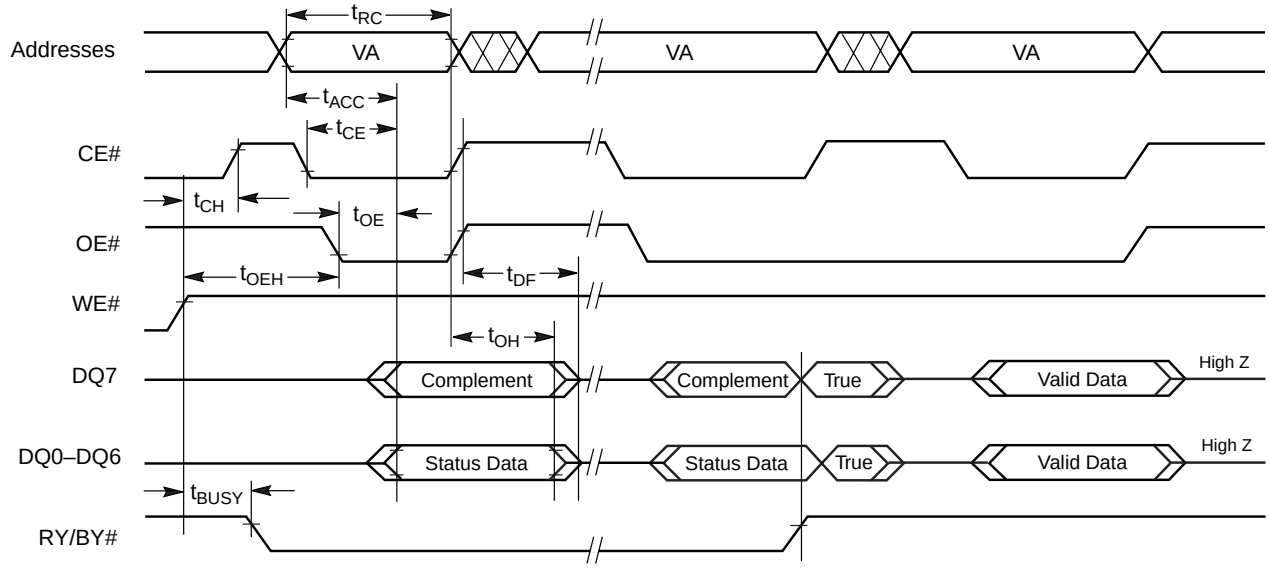
AC CHARACTERISTICS



Note: *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*

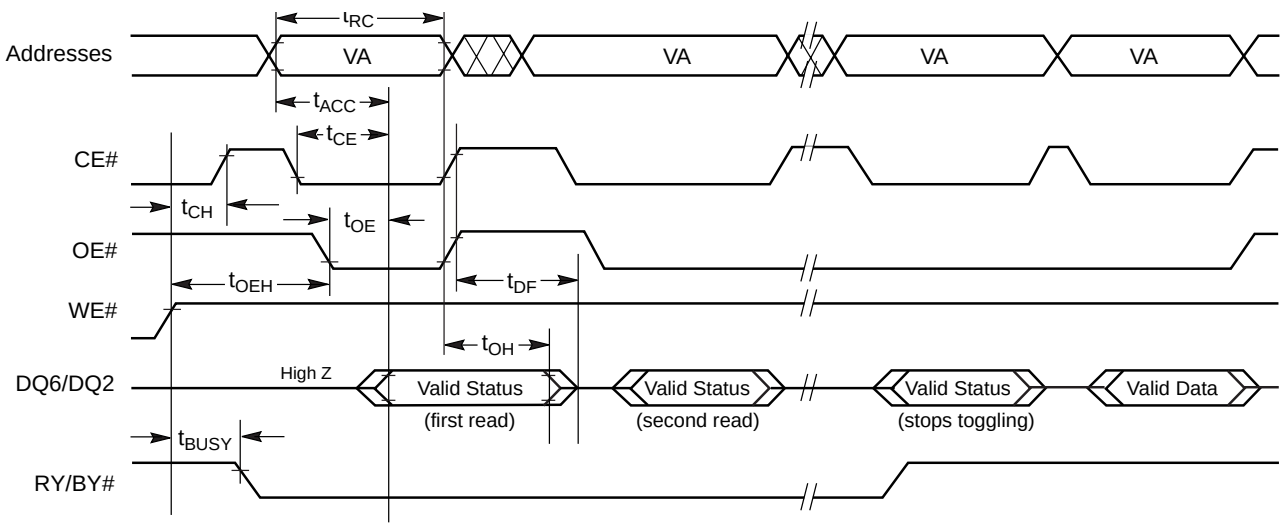
Figure 17. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS



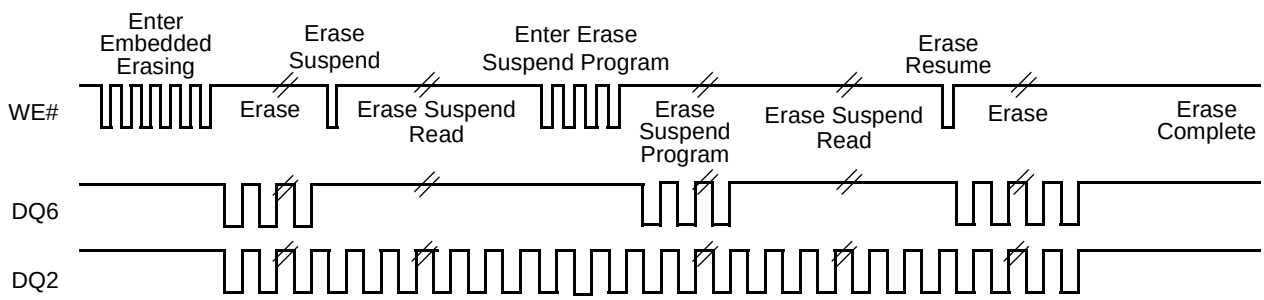
Note: *VA = Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 18. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 19. Toggle Bit Timings (During Embedded Algorithms)



Note: *The system can use OE# or CE# to toggle DQ2/DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 20. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector/Sector Block Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector/Sector Block Unprotect	Min	4	µs

Note: *Not 100% tested.*

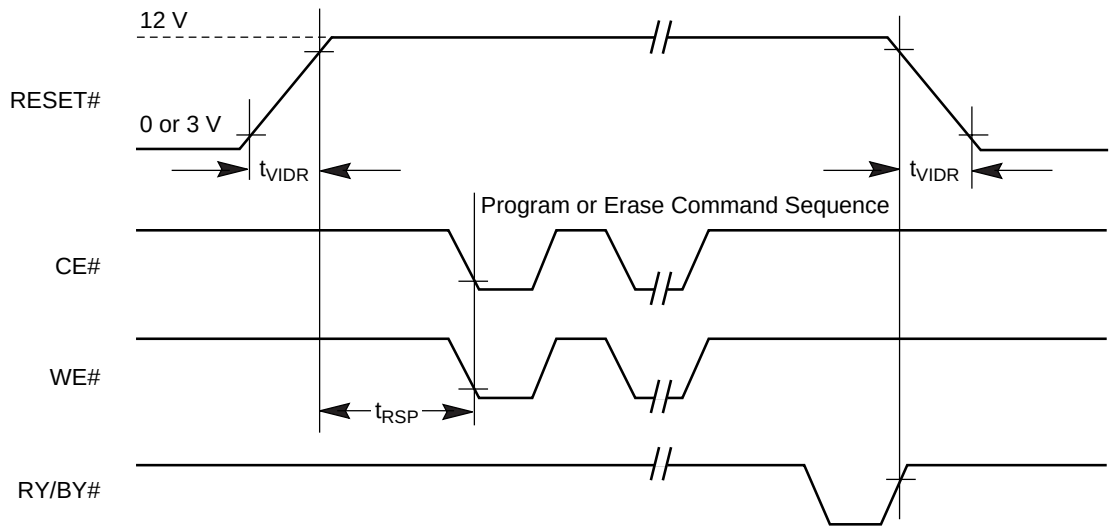
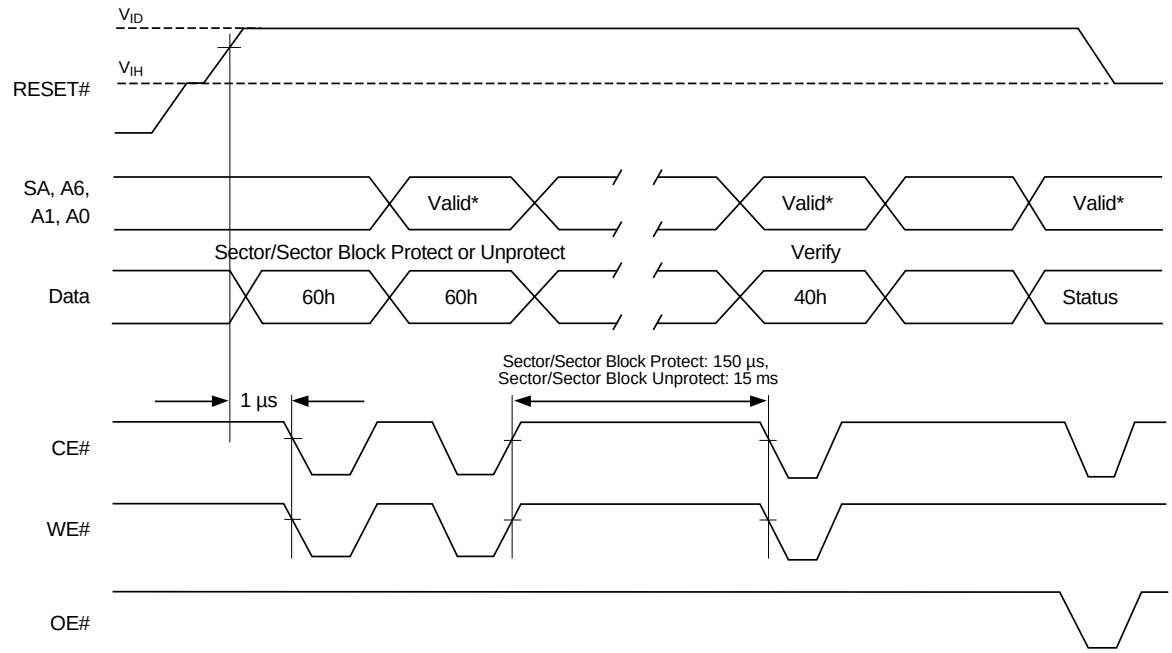


Figure 21. Temporary Sector/Sector Block Unprotect Timing Diagram



Note: *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 22. Sector Protect/Unprotect Timing Diagram

AC CHARACTERISTICS

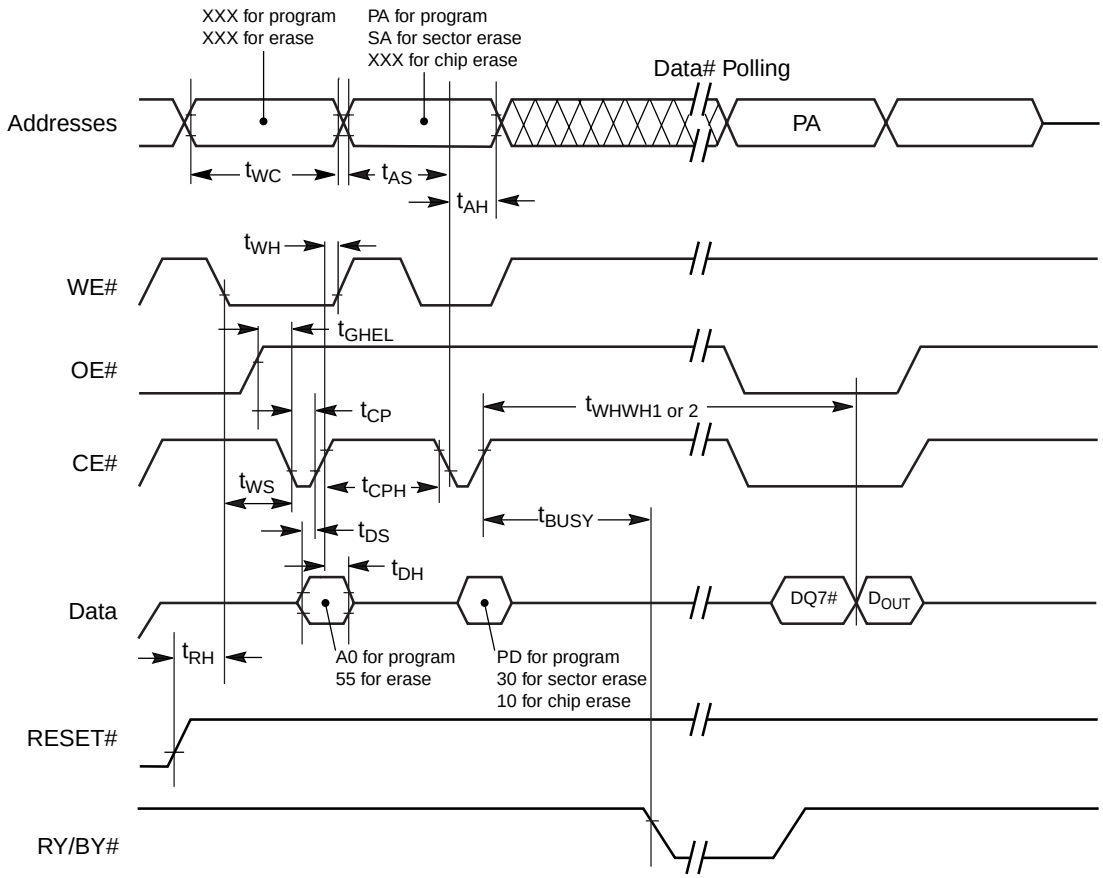
Alternate CE# Controlled Erase/Program Operations

Parameter				Speed Option			
JEDEC	Std	Description		-70	-90	-120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0			ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0			ns
	t_{OES}	Output Enable Setup Time	Min	0			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	30	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.7			sec

Notes:

1. *Not 100% tested.*
2. *See the “Erase and Programming Performance” section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = Program Address, PD = Program Data, D_{OUT} = Data Out, DQ7# = complement of data written to device.*
2. *Figure indicates the last two bus cycles of the command sequence.*

Figure 23. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.7	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	45		s	
Byte Programming Time	9	300	µs	Excludes system level overhead (Note 5)
Accelerated Byte Program Time	7	210	µs	
Chip Programming Time (Note 3)	36	108	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V $V_{CC,}$ 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four- or two-bus-cycle sequence for the program command. See Table 9 for further information on command definitions.*
6. *The device has a guaranteed minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

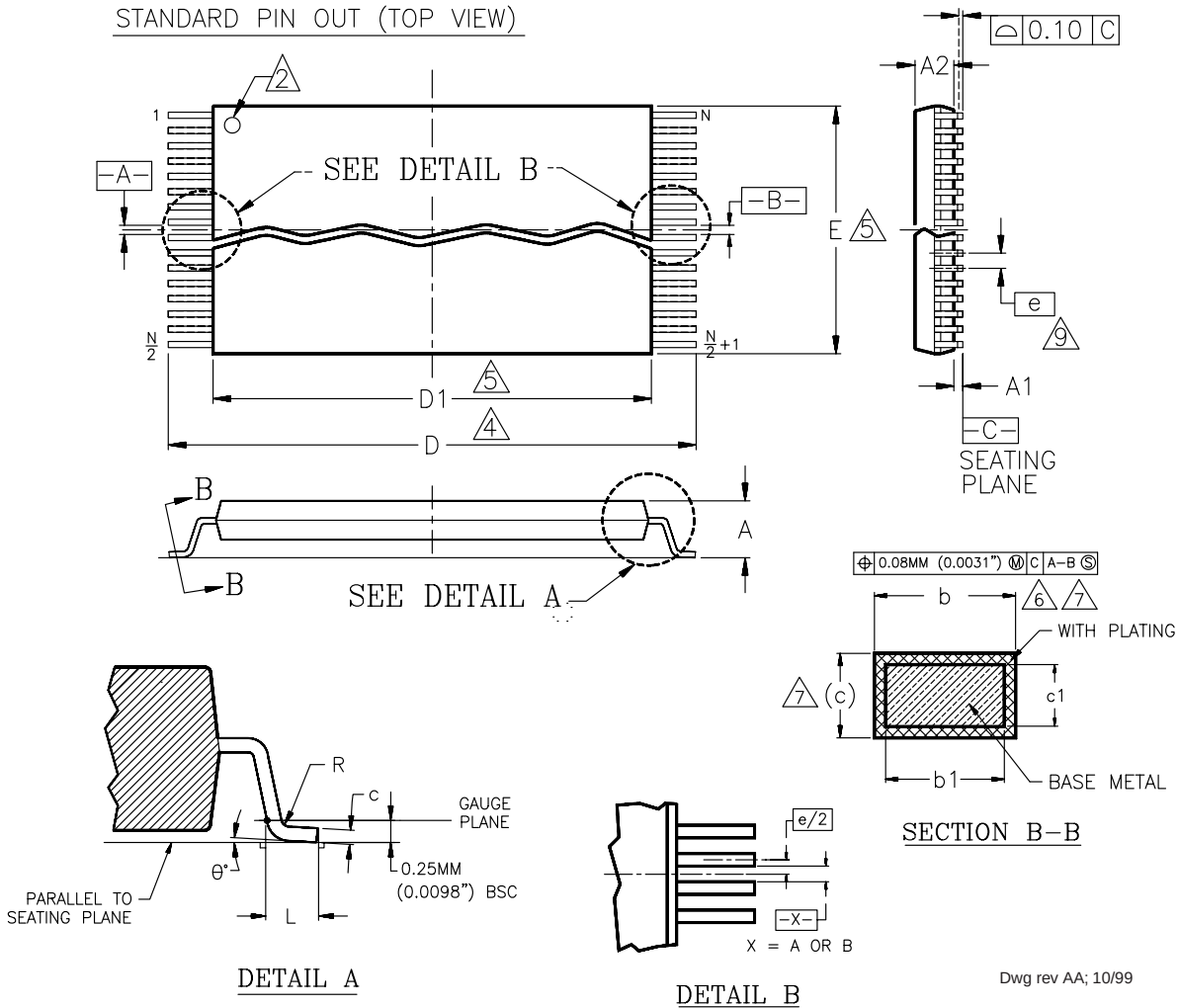
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS*

TS 040—40-Pin Standard TSOP



Package	TS 40		
Jedec	MO-142 (B) CD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

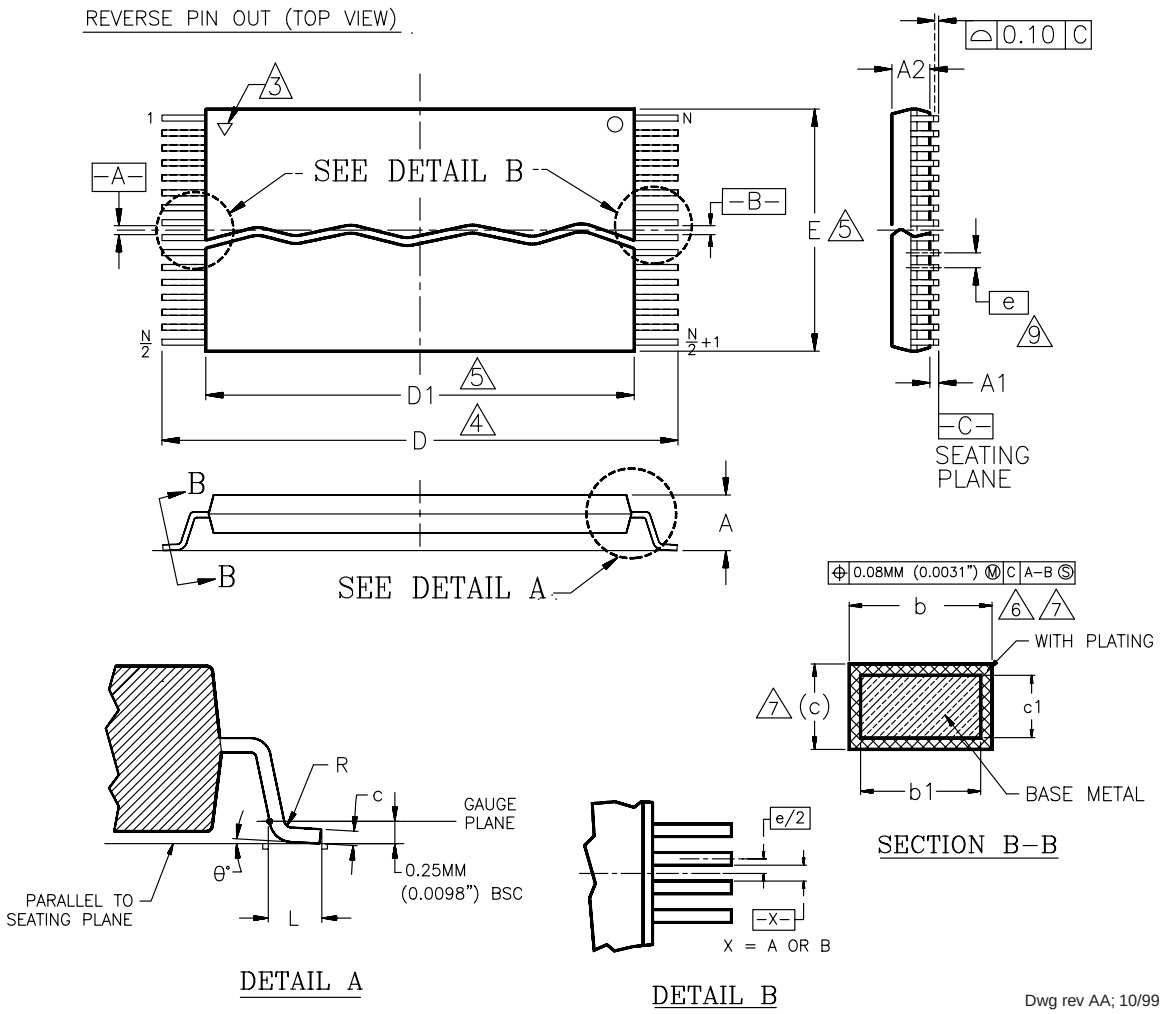
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS

TSR040—40-Pin Reverse TSOP



Dwg rev AA; 10/99

Package	TSR 40		
Jedec	MO-142 (B) CD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

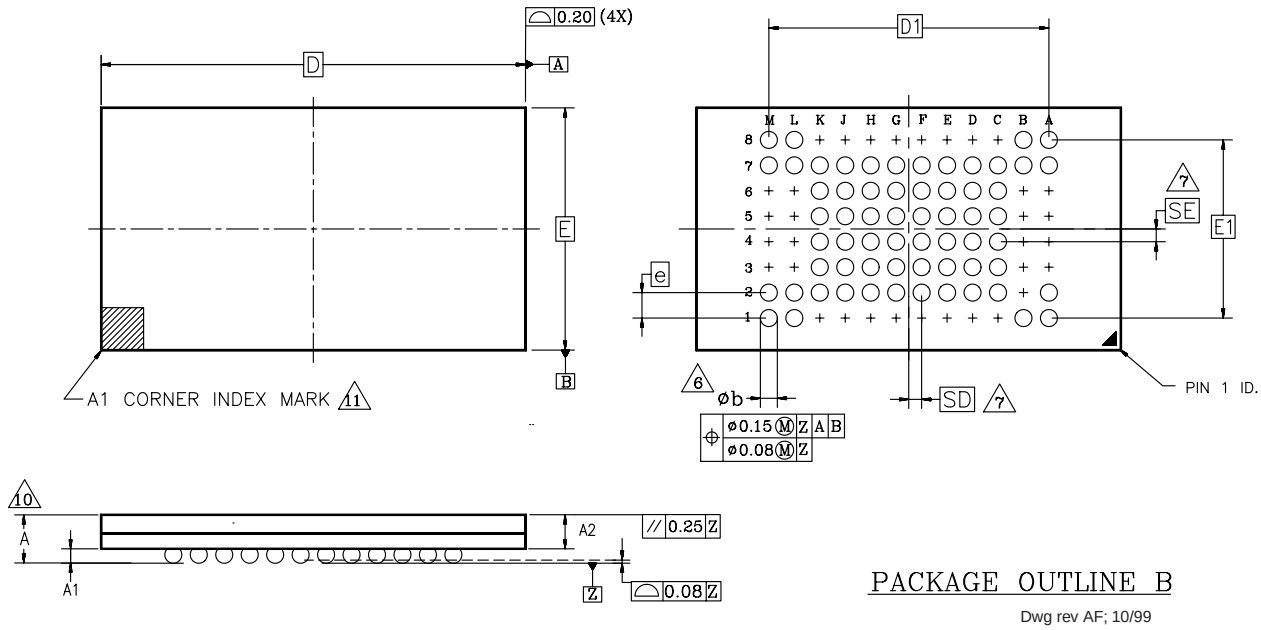
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS

FBD063—63-Ball Fine-Pitch Ball Grid Array (FBGA) 8 x 14 mm



PACKAGE OUTLINE B

Dwg rev AF; 10/99

PACKAGE	xFBD 063			
JEDEC	N/A			
	8.00mmx14.00mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	OVERALL THICKNESS
A1	0.20	—	—	BALL HEIGHT
A2	0.84	—	0.94	BODY THICKNESS
D	14.00 BSC			BODY SIZE
E	8.00 BSC			BODY SIZE
D1	8.80 BSC			BALL FOOTPRINT
E1	5.60 BSC			BALL FOOTPRINT
MD	12			ROW MATRIX SIZE D DIRECTION
ME	8			ROW MATRIX SIZE E DIRECTION
N	63			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC			SOLDER BALL PLACEMENT
	A3–A6,B2–B6, L3–L6,M3–M6, C1–K1,C8–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.

10 FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.

11 A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

REVISION SUMMARY

Revision A+1 (January 1999)

Device Bus Operations

Sector/Sector Block Addresses for Protection/Unprotection Table: Corrected the address bits and values in the middle column of the table.

Autoselect Codes (High Voltage Method Table: Changed the device ID to A3h.

Revision A+2 (January 1999)

Command Definitions

Command Definition Table: Changed the device ID to A3h.

Revision A+3 (March 17, 1999)

Connection Diagrams

Modified FBGA drawing to show how outrigger balls are shorted.

Revision A+4 (May 17, 1999)

Global

Deleted references to WP#. The device does not offer this function.

Table 4. Sector Block Addresses for Protection/Unprotection

Deleted “Top Boot Sector/” from table title.

Revision A+5 (June 7, 1999)

Global

The 70 ns speed option now operates over the full 2.7–3.6 V V_{CC} range.

Common Flash Memory Interface

Corrected data for the following addresses: 27h, 2Dh, 37h, 48h, and 49h. Modified the description for 48h and 49h.

Revision A+6 (June 25, 1999)

Command Definitions Table

Indicated that address bit A21 must be specified in the third cycle when entering the autoselect mode.

Revision A+7 (August 2, 1999)

Block Diagram

Added ACC signal to drawing.

Accelerated Program Operations

Clarified how to permanently set ACC.

Accelerated Program Timing Diagram

Deleted WP# designation from ACC signal.

Revision A+8 (August 18, 1999)

Ordering Information, Physical Dimensions

Corrected FBGA package dimensions to 8 x 14 mm.

Revision A+9 (August 31, 1999)

Ordering Information

Speed Option: Changed 70R to 70.

Revision B (January 3, 2000)

AC Characteristics—Figure 15. Program Operations Timing and Figure 17. Chip/Sector Erase Operations

Deleted t_{GHWL} and changed OE# waveform to start at high.

Physical Dimensions

Replaced figures with more detailed illustrations.

Revision B+1 (February 21, 2000)

Global

Changed data sheet status to “Preliminary” from “Advance Information. Added dash to speed options.

Ordering Information

Added dash to OPN.

Revision B+2 (November 7, 2000)

Global

Added Table of Contents. Deleted burn-in option. Deleted Preliminary status from data sheet.

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