Am29F004B

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **Am29F004B** Revision **E** Amendment **2** Issue Date **July 29, 2005**

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Am29F004B

4 Megabit (512 K x 8-Bit) CMOS 5.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 Volt single power supply operation**
  - — Minimizes system-level power requirements
- **High performance**
  - — Access times as fast as 70 ns
- **Manufactured on 0.32 µm process technology**
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 20 mA typical active read current
  - — 30 mA typical program/erase current
  - — 1 µA typical standby mode current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Minimum 1,000,000 write cycle guarantee per sector**
- **Package option**
  - — 32-pin PLCC
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **20-year data retention at 125°C**

This document contains information on a product under development at Advanced Micro Devices. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice. 8/5/05This document contains information on a product under development at Advanced Micro Devices. The information is intended to help you evaluate this product. AMD reserves the right to change or

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GENERAL DESCRIPTION

The Am29F004B is a 4 Mbit, 5.0 volt-only Flash memory device organized as 524,288 bytes. The data appears on DQ0–DQ7. The device is offered in a 32-pin PLCC package. This device is designed to be programmed in-system with the standard system 5.0 volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29F004B is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm-an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm–an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle is completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector** protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The device offers a **standby mode** as a power-saving feature. Once the system places the device into the standby mode power consumption is greatly reduced.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

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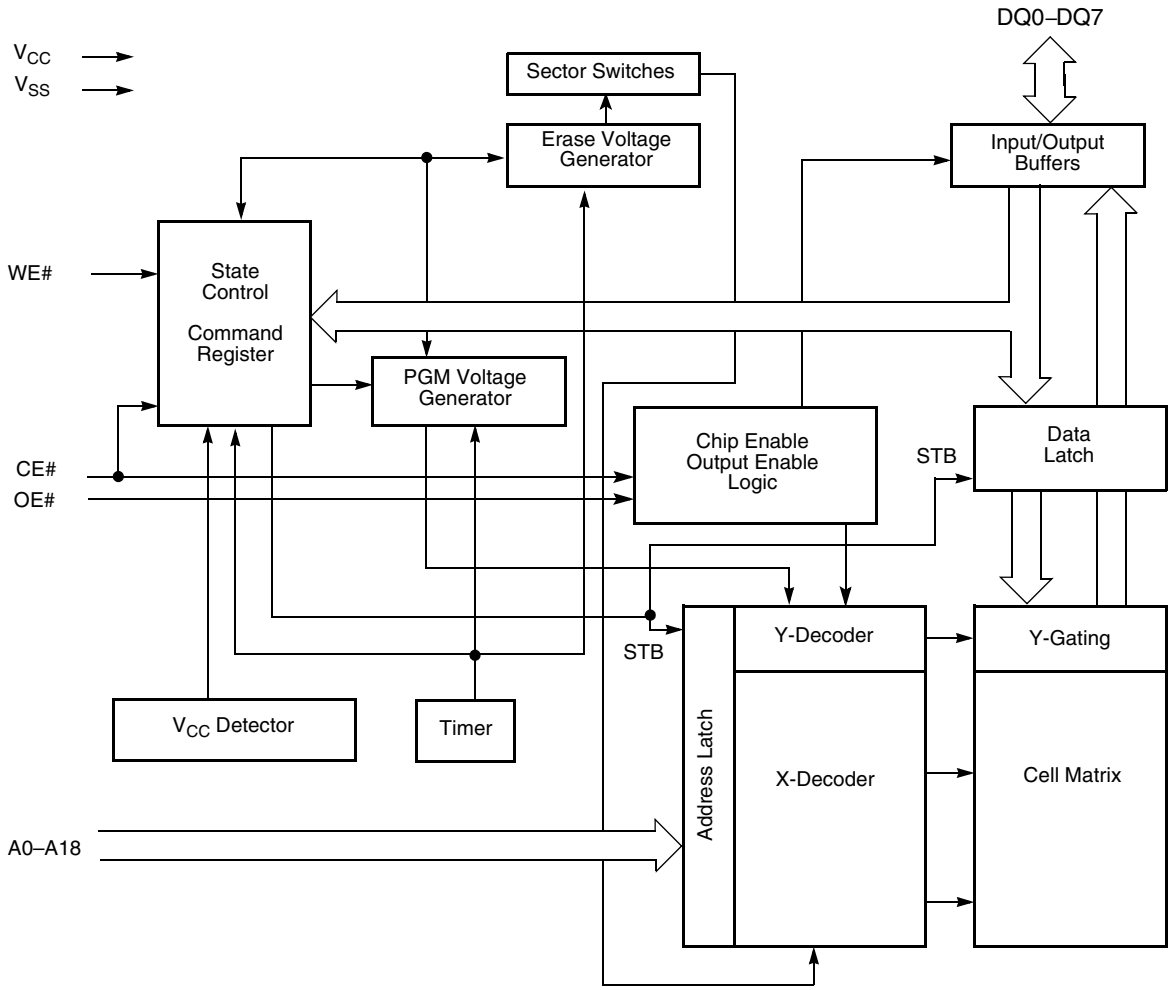
PRODUCT SELECTOR GUIDE

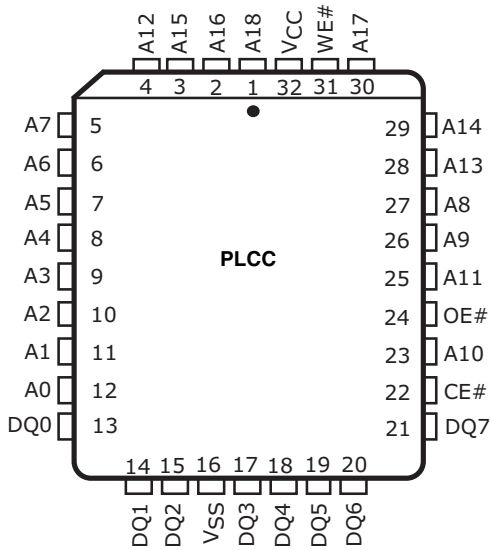
Family Part Number		Am29F004B		
Speed Option	V_{CC} = 5.0 V ± 10%	**-70**	**-90**	**-120**
Max access time, ns (t_{ACC})		70	90	120
Max CE# access time, ns (t_{CE})		70	90	120
Max OE# access time, ns (t_{OE})		30	35	45

Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



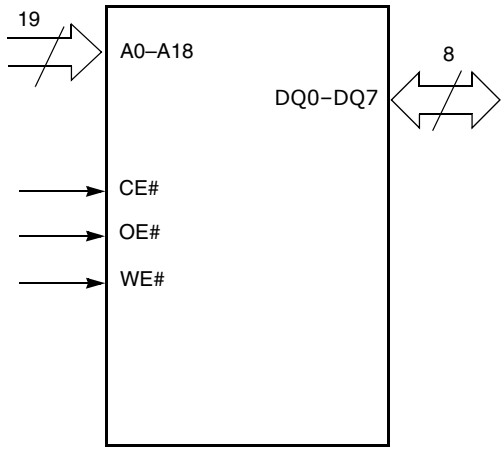
CONNECTION DIAGRAMS



PIN CONFIGURATION

A0–A18	=	19 addresses
DQ0–DQ7	=	8 data inputs/outputs
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
V_{CC}	=	+5.0 V single power supply (see Product Selector Guide for device speed ratings and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Product

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am29F004B T -70 J I

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)
F = Industrial (–40°C to +85°C) for Pb-free package
E = Extended (–55°C to +125°C)
K = Extended (–55°C to +125°C) for Pb-free package

PACKAGE TYPE
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
Am29F004B
4 Megabit (512 K x 8-Bit) CMOS Flash Memory
5.0 Volt-only Program and Erase

Valid Combinations		V_{CC} Voltage
AM29F004BT-70 AM29F004BB-70	JI, JF	5.0 V ± 10%
AM29F004BT-90 AM29F004BB-90	JI, JE, JF, JK	
AM29F004BT-120 AM29F004BB-120		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F004B Device Bus Operations

Operation	CE#	OE#	WE#	A0–A18	DQ0–DQ7
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
CMOS Standby	$V_{CC} \pm 0.5$ V	X	X	X	High-Z
TTL Standby	H	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z
Temporary Sector Unprotect (See Note)	X	X	X	X	X

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In

Note: *See the sections on Sector Protection and Temporary Sector Unprotect for more information.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See *Reading Array Data on page 13* for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the *Command Definitions on page 13* section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the *Autoselect Mode on page 10* and Autoselect Command Sequence sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The *AC Characteristics on page 24* section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to *Write Operation Status on page 17* for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when CE# pin is held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# pin is held at V_{IH}. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics tables, I_{CC3} represents the standby current specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29F004B Top Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	Sector Size (Kbytes)	Address Range (in hexadecimal)
SA0	0	0	0	X	X	X	64	00000h–0FFFFh
SA1	0	0	1	X	X	X	64	10000h–1FFFFh
SA2	0	1	0	X	X	X	64	20000h–2FFFFh
SA3	0	1	1	X	X	X	64	30000h–3FFFFh
SA4	1	0	0	X	X	X	64	40000h–4FFFFh
SA5	1	0	1	X	X	X	64	50000h–5FFFFh
SA6	1	1	0	X	X	X	64	60000h–6FFFFh
SA7	1	1	1	0	X	X	32	70000h–77FFFh
SA8	1	1	1	1	0	0	8	78000h–79FFFh
SA9	1	1	1	1	0	1	8	7A000h–7BFFFh
SA10	1	1	1	1	1	X	16	7C000h–7FFFFh

Table 3. Am29F004B Bottom Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	Sector Size (Kbytes)	Address Range (in hexadecimal)
SA0	0	0	0	0	0	X	16	00000h–03FFFh
SA1	0	0	0	0	1	0	8	04000h–05FFFh
SA2	0	0	0	0	1	1	8	06000h–07FFFh
SA3	0	0	0	1	X	X	32	08000h–0FFFFh
SA4	0	0	1	X	X	X	64	10000h–1FFFFh
SA5	0	1	0	X	X	X	64	20000h–2FFFFh
SA6	0	1	1	X	X	X	64	30000h–3FFFFh
SA7	1	0	0	X	X	X	64	40000h–4FFFFh
SA8	1	0	1	X	X	0	64	50000h–5FFFFh
SA9	1	1	0	X	X	1	64	60000h–6FFFFh
SA10	1	1	1	X	X	X	64	70000h–7FFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See *Command Definitions on page 13* for details on using the autoselect mode.

Table 4. Am29F004B Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A18 to A13	A12 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29F004B (Top Boot Block)	L	L	H	X	X	V_{ID}	X	L	X	L	H	77h
	L	L	H									
Device ID: Am29F004B (Bottom Boot Block)	L	L	H	X	X	V_{ID}	X	L	X	L	H	7Bh
	L	L	H									
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected)
												00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The primary method requires V_{ID} on the OE# pin only, and can be implemented either in-system or via programming equipment. Figure 1, on page 11 and 2 show the algorithms and Figure 16, on page 28, Figure 17, on page 28, and Figure 18, on page 29 show the timing diagrams. This method uses standard microprocessor bus cycle timing in addition to the sector unlock and sector relock sequences. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment required V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 5.0 volt-only AMD Flash devices. Publication number 22289 contains further details; contact an AMD representative to request a copy.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's Express-Flash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode on page 10* for details.

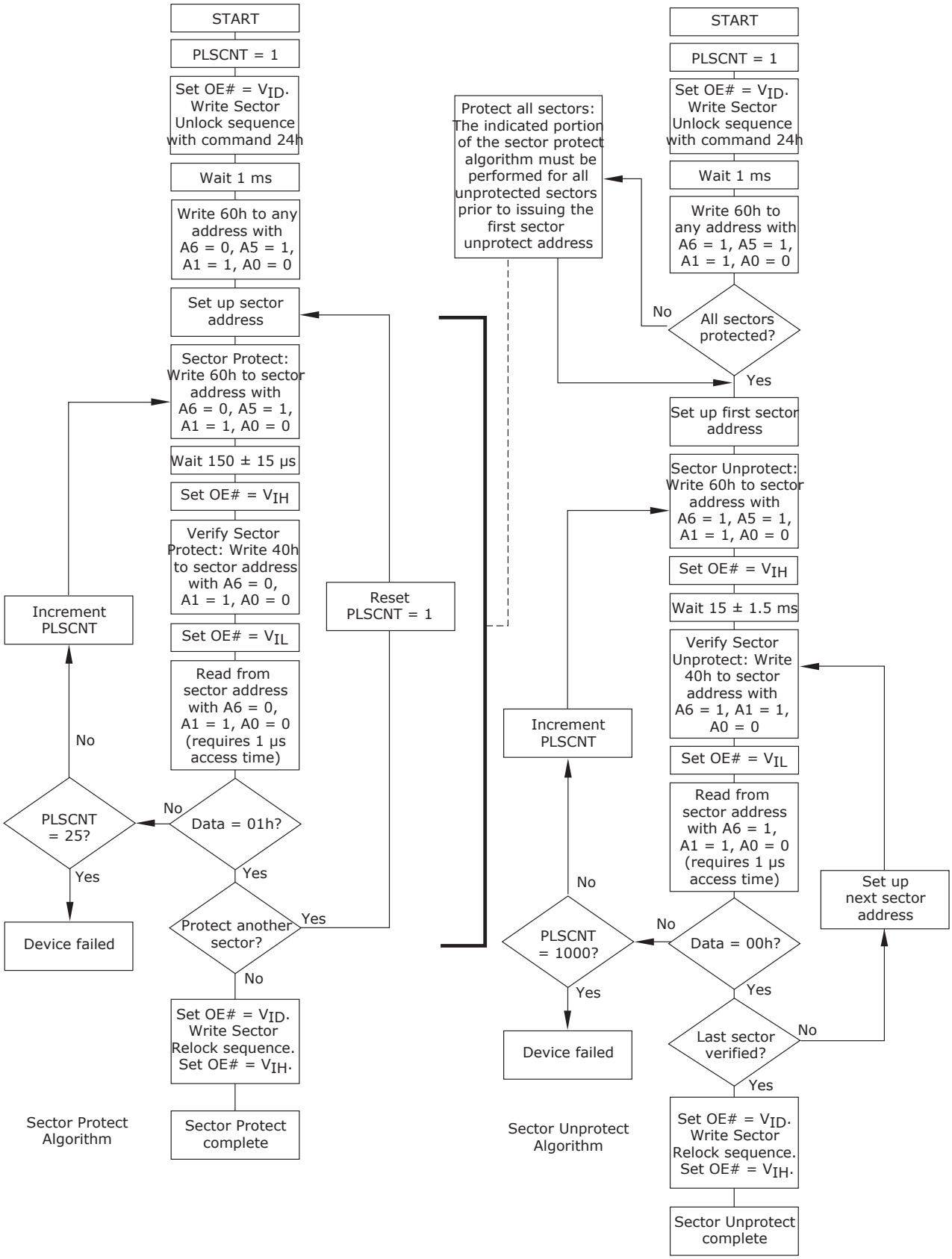


Figure 1. In-System Sector Protect/Sector Unprotect Algorithms

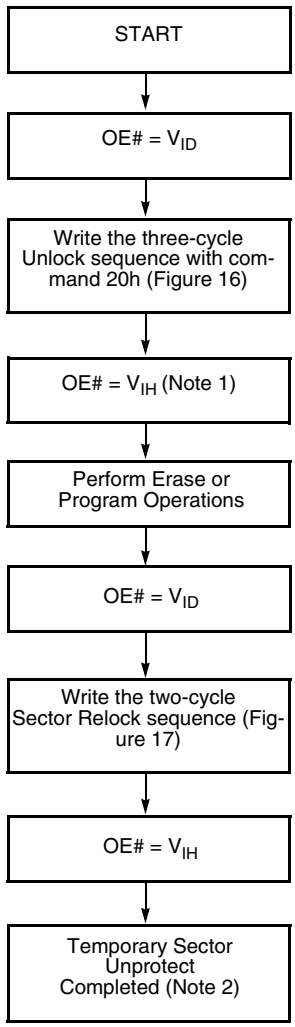
Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the OE# pin to 12.0 Volts (V_{ID}). Figure 2 shows the algorithm, and Figure 16, on page 28 and Figure 17, on page 28 show the timing diagrams, for this feature. While OE# is at V_{ID}, the sector unlock sequence is written to the device. After the sector unlock sequence is written, the OE# pin is taken back to V_{IH}. The device is now in the temporary sector unprotect mode.

While in this mode, formerly protected sectors can be programmed or erased by selecting the appropriate sector address during programming or erase operations. Either sector erase or chip erase operations can be performed in this mode. Byte program operations require only two cycles, while sector and chip erase operations only require four cycles. Refer to the Command Definitions table.

Exiting the temporary sector unprotect mode is accomplished by either removing V_{CC} from the device or by taking OE# back to V_{ID} and writing the sector relock sequence.

After writing the sector relock sequence, the OE# pin is taken back to V_{IH} and all previously protected sectors are protected again.



Notes:

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 2. Temporary Sector Unprotect Operation

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse *Glitch* Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions table defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in *AC Characteristics on page 24*.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Reset Command* for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the *Reset Command* section, next.

See also “Requirements for Reading Array Data” in the *Device Bus Operations on page 8* section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don’t care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This method is an alternative to that shown in the Autoselect Codes (High Voltage Method) table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h or retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in returns 01h if that sector is protected, or 00h if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Program Command Sequence

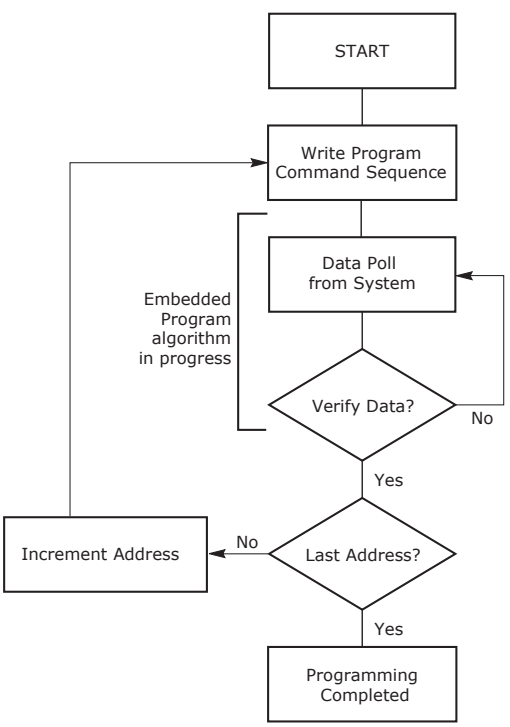
Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write

cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. (Note that if the device is in the temporary sector unprotect mode, the byte program command sequence only requires two cycles.) The Command Definitions table shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See *Write Operation Status on page 17* for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. The Sector Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to *1*, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read shows that the data is still *0*. Only erase operations can convert a *0* to a *1*".



Note: *See the appropriate Command Definitions table for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. (Note that if the device is in the temporary sector unprotect mode, the chip erase command sequence only requires four cycles.) The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The Sector Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See *Write Operation Status on page 17* for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 4, on page 15 illustrates the algorithm for the erase operation. See the *Erase/Program Operations on page 25* for parameters, and to Figure 12, on page 26 for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six-bus-cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. (Note that if the device is in the temporary sector unprotect mode, the sector erase command sequence only requires four cycles.) The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command

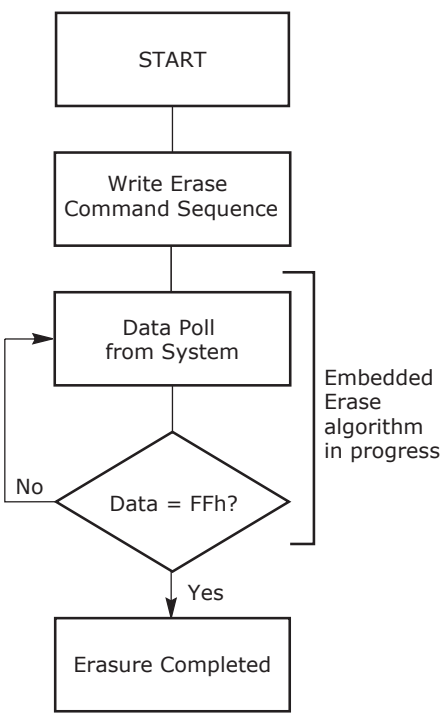
sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer timed out. (See *DQ3: Sector Erase Timer on page 18*.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. The Sector Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to *Write Operation Status on page 17* for information on these status bits.

Figure 4 illustrates the algorithm for the erase operation. Refer to the *Erase/Program Operations on page 25* for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.



Note:

1. *See the appropriate Command Definitions table for erase command sequence.*
2. *See DQ3: Sector Erase Timer on page 18 for more information.*

Figure 4. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are *don't-cares* when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation is suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See *Write Operation Status on page 17* for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See *Write Operation Status on page 17* for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See *Autoselect Command Sequence on page 13* for more information.

The system must write the Erase Resume command (address bits are *don't care*) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device resumes erasing.

Table 5. Am29F004B Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID, Top Boot Block	4	555	AA	2AA	55	555	90	X01	77				
	Device ID, Bottom Boot Block	4	555	AA	2AA	55	555	90	X01	7B				
	Sector Protect Verify (Note 8)	4	555	AA	2AA	55	555	90	(SA) X02	00				
										01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 11)		1	XXX	B0										
Erase Resume (Note 12)		1	XXX	30										
Temporary Sector Unprotect Mode (Note 9)	Enter TSU Mode	3	555	AA	2AA	55	555	20						
	Program	2	XXX	A0	PA	PD								
	Sector Erase	4	XXX	80	XXX	AA	XXX	55	SA	30				
	Chip Erase	4	XXX	80	XXX	AA	XXX	55	555	10				
Sector Unlock (Note 9)		3	555	AA	2AA	55	555	24	SA+	60	SA+	60	SA+	40
Sector Relock (Notes 9, 10)		2	XXX	90	XXX	00								

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18–A13 uniquely select any sector.

SA+ = The sector address must be asserted in combination with A0 = 0, A1 = 1, A5 = 1, and A6 = 0 (for protect) or 1 (for unprotect).

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Address bits A18–A11 are don't cares for unlock and command cycles, except when PA or SA is required.*
5. *No unlock or command cycles required when reading array data.*
6. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
7. *The fourth cycle of the autoselect command sequence is a read cycle.*
8. *The data is 00h for an unprotected sector and 01h for a protected sector. See Autoselect Command Sequence on page 13 for more information.*
9. *To activate the sequence, OE# must be at V_{ID}.*
10. *The sector relock command in the second cycle may be written as either 00h or F0h.*
11. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
12. *The Erase Resume command is valid only during the Erase Suspend mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 6 on page 19 and the following subsections describe the functions of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

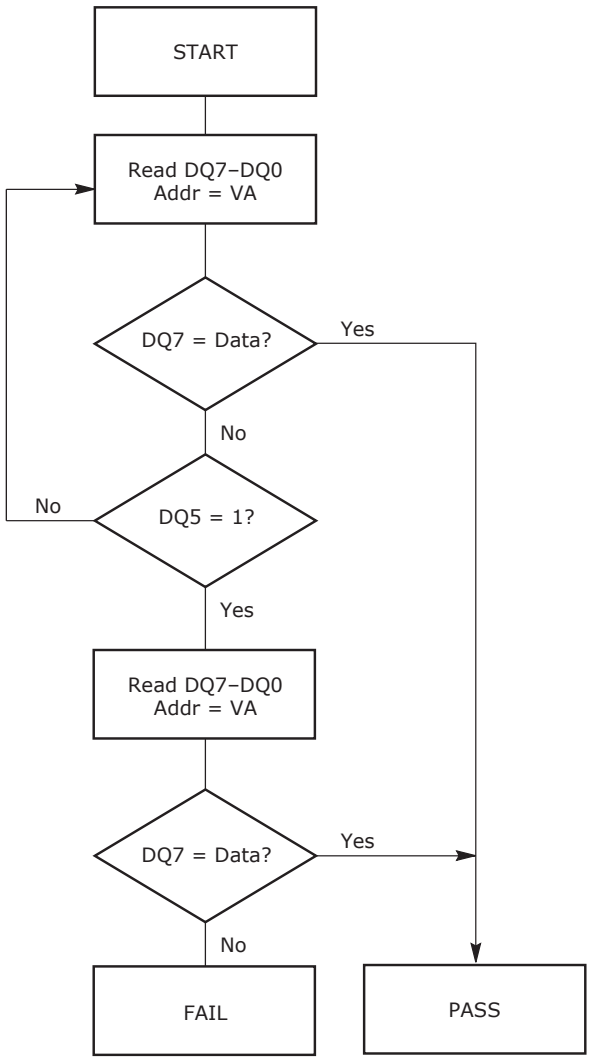
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 2 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 changes from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. The Data# Polling Timings (During Embedded Algorithms) figure in the *AC Characteristics on page 24* section illustrates this.

Table 6 on page 19 shows the outputs for Data# Polling on DQ7. Figure 5, on page 17 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

The Write Operation Status table shows the outputs for Toggle Bit I on DQ6. Refer to Figure 6 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The *Toggle Bit II* on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that were selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 on page 19 to compare outputs for DQ2 and DQ6.

Figure 6, on page 19 shows the toggle bit algorithm in flowchart form, and the section *DQ2: Toggle Bit II on page 18* explains the algorithm. See also the *DQ6: Toggle Bit I on page 18* subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6, on page 19 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6, on page 19).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a *1* to a location that is previously programmed to *0*. **Only an erase operation can change a "0" back to a *1*.** Under this condition, the device halts the operation, and when the operation exceeds the timing limits, DQ5 produces a *1*.

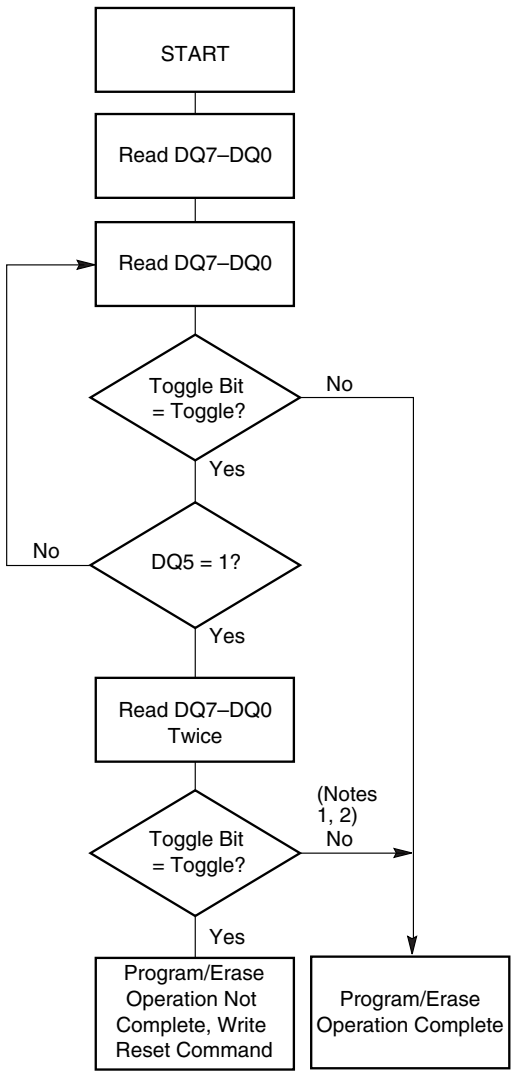
Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation started. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from *0* to *1*. The system may ignore DQ3 if the system can guarantee that the time between additional sector

erase commands is always less than 50 µs. See also the *Sector Erase Command Sequence on page 14* section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device accepts the command sequence, and then read DQ3. If DQ3 is *1*, the internally controlled erase cycle started; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device accepts additional sector erase commands. To ensure the command was accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 6 on page 19 shows the outputs for DQ3.



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to* 1*. See text.*

Figure 6. Toggle Bit Algorithm

Table 6. Write Operation Status

Operation		DQ7 (Note 1)	DQ6	DQ5 (Note 2)	DQ3	DQ2 (Note 1)
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A

Notes:

1. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
2. *DQ5 switches to* 1 *when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits on page 18 for more information.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –2.0 V to +7.0 V

A9, OE# (Note 2) . . . . . –2.0 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to +7.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7, on page 20. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8, on page 20.*
2. *Minimum DC input voltage on pins A9 and OE# is –0.5 V. During voltage transitions, A9 and OE# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7, on page 20. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to +13.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under Absolute Maximum Ratings *may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

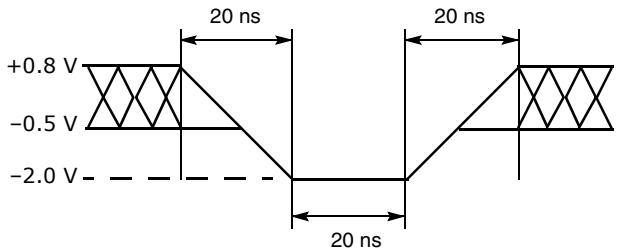


Figure 7. Maximum Negative Overshoot Waveform

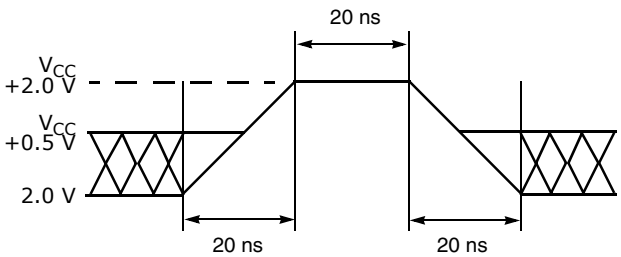


Figure 8. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for ± 5% devices. . . . . .+4.75 V to +5.25 V

V_{CC} for ± 10% devices. . . . . .+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{LIT}	A9, OE# Input Load Current (Note 4)	$V_{CC} = V_{CC\ max}$; A9, OE# = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}		20	30	mA
I_{CC2}	V_{CC} Active Write Current (Notes 1, 3, 4)	CE# = V_{IL}, OE# = V_{IH}		30	40	mA
I_{CC3}	V_{CC} Standby Current (Note 1)	CE#, OE# = V_{IH}		0.4	1	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 5.0 V	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC\ min}$			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC\ min}$	2.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2		4.2	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Not 100% tested.*

DC CHARACTERISTICS

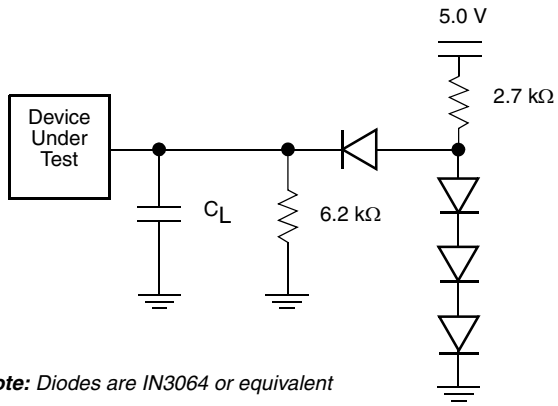
CMOS Compatible

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{LIT}	A9, OE#, Input Load Current (Note 4)	$V_{CC} = V_{CC\ max}$; A9, OE# = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}		20	30	mA
I_{CC2}	V_{CC} Active Write Current (Notes 1, 3, 4)	CE# = V_{IL}, OE# = V_{IH}		30	40	mA
I_{CC3}	V_{CC} Standby Current (Notes 1, 5)	CE# = V_{CC} ± 0.5 V		0.3	5	µA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 5.0 V	11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC\ min}$			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC\ min}$	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$	V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2		4.2	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Not 100% tested.*
5. *I_{CC3} = 20 µA max at extended temperature (>+85° C).*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 9. Test Setup

Table 7. Test Specifications

Test Condition	70, 90, 120	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	100	pF
Input Rise and Fall Times	20	ns
Input Pulse Levels	0.45–2.4	V
Input timing measurement reference levels	0.8, 2.0	V
Output timing measurement reference levels	0.8, 2.0	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Options			Unit
JEDEC	Std					-70	-90	-120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	45	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20	20	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0			ns

Notes:

1. *Not 100% tested.*
2. *See Table 7 and Figure 9, on page 23 for test specifications.*

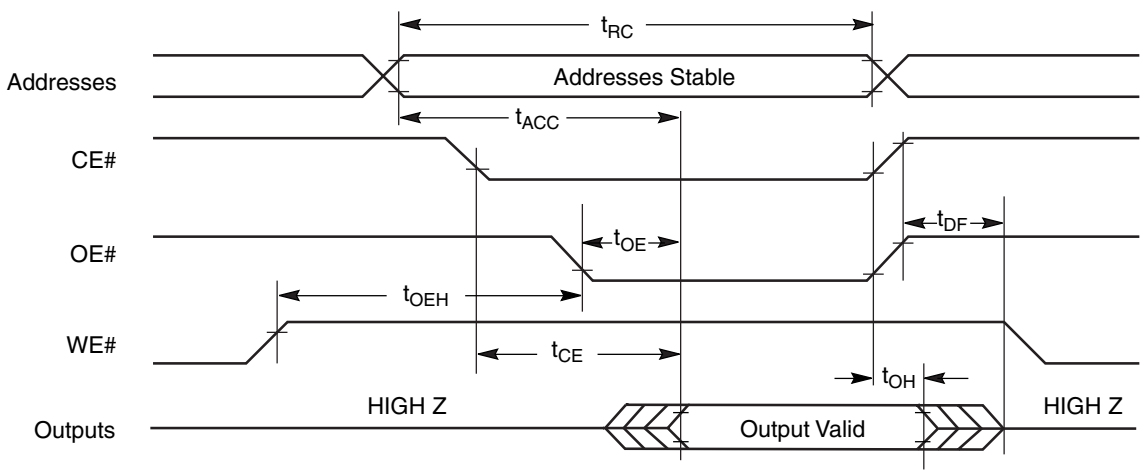


Figure 10. Read Operations Timings

AC CHARACTERISTICS

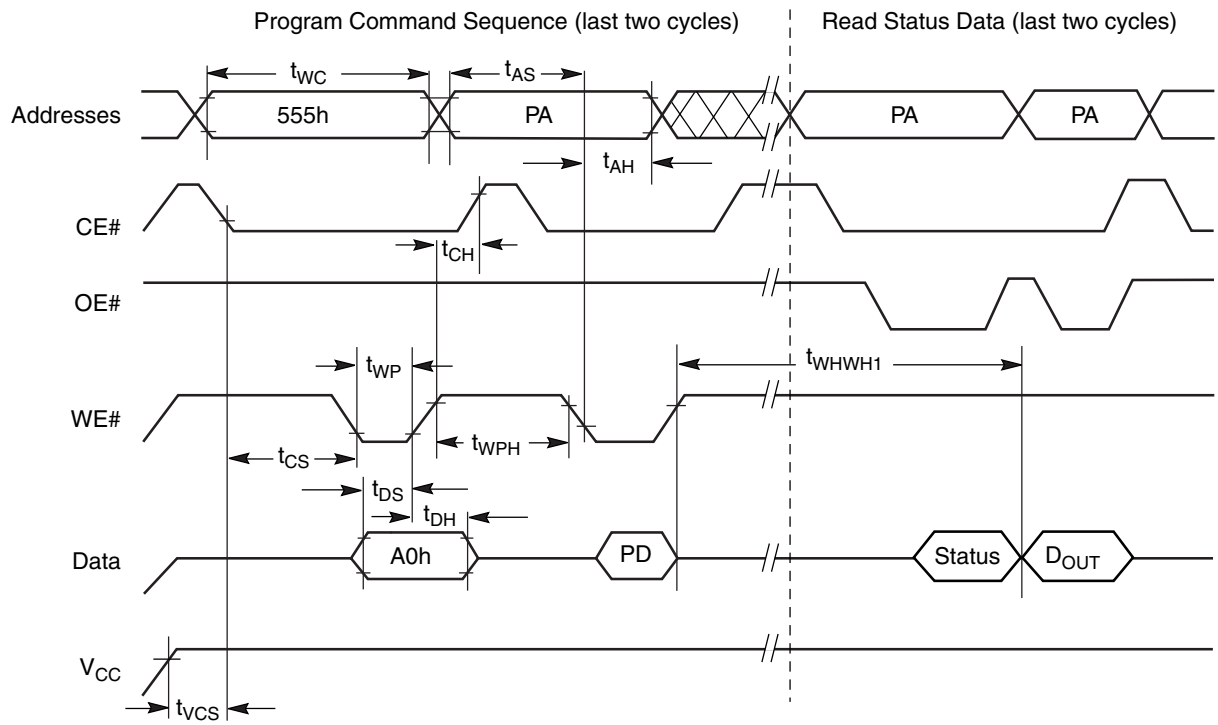
Erase/Program Operations

Parameter				Speed Options			
JEDEC	Std	Description		-70	-90	-120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0			ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0			ns
	t_{OES}	Output Enable Setup Time	Min	0			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	7			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1			sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50			µs

Notes:

1. *Not 100% tested.*
2. *See Erase and Programming Performance on page 32 for more information.*

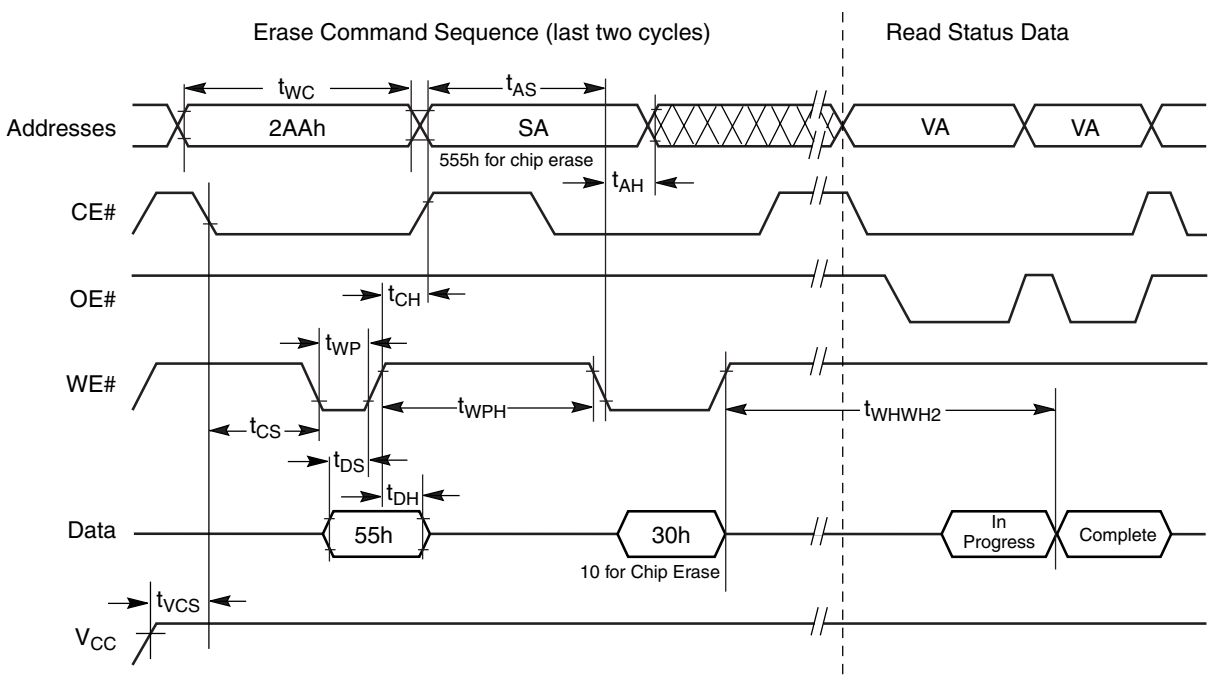
AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

Figure 11. Program Operation Timings

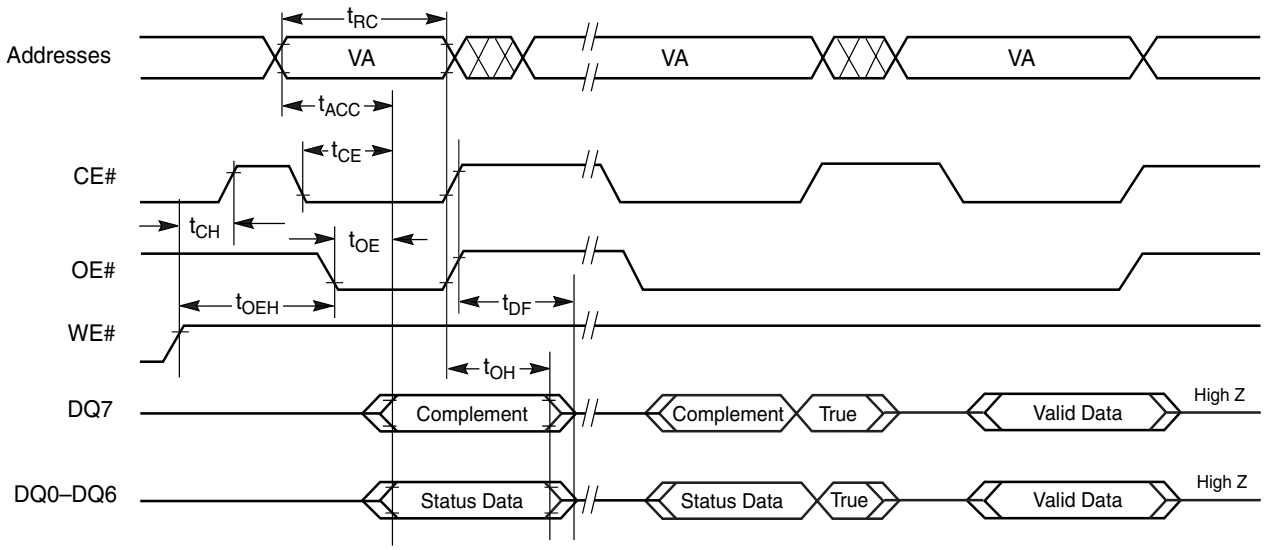


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data ("see Write Operation Status on page 17).*

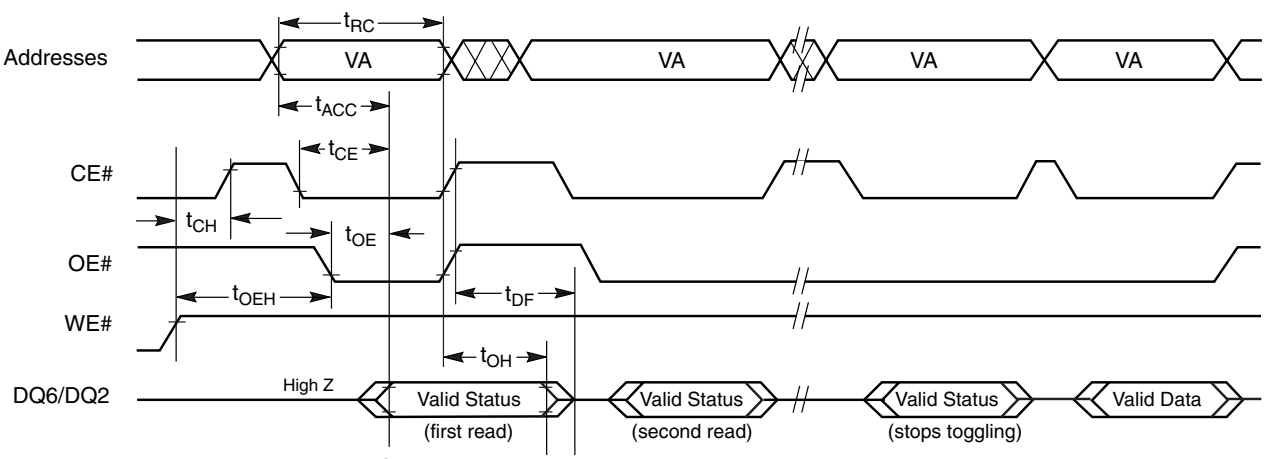
Figure 12. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS



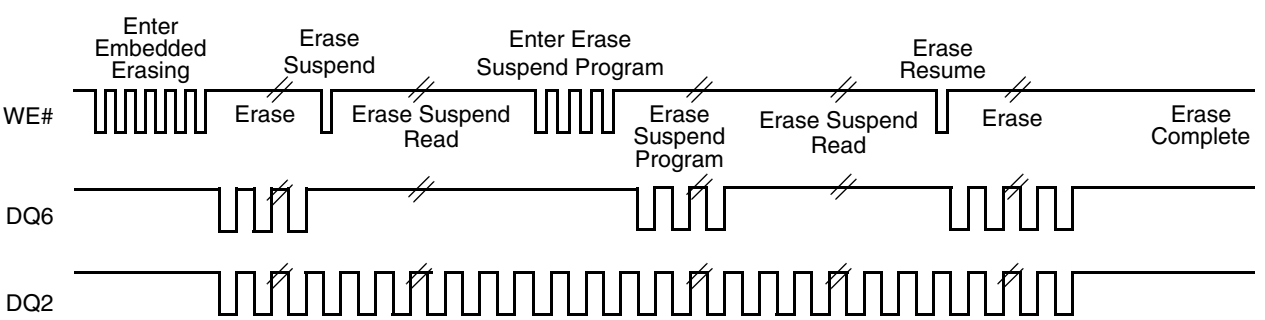
Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 13. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 14. Toggle Bit Timings (During Embedded Algorithms)



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 15. DQ2 vs. DQ6

AC CHARACTERISTICS

Parameter					
JEDEC	Std.	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (Not 100% tested)	Min	500	ns

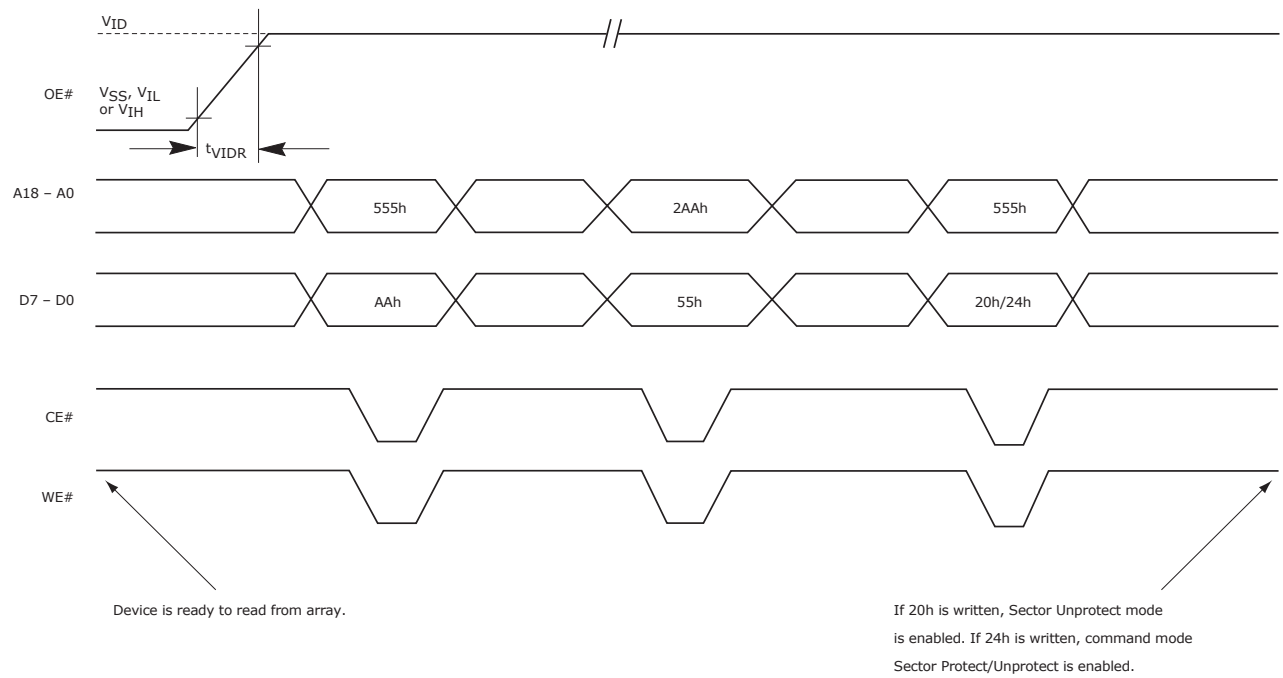


Figure 16. Sector Unlock Sequence Timing Diagram

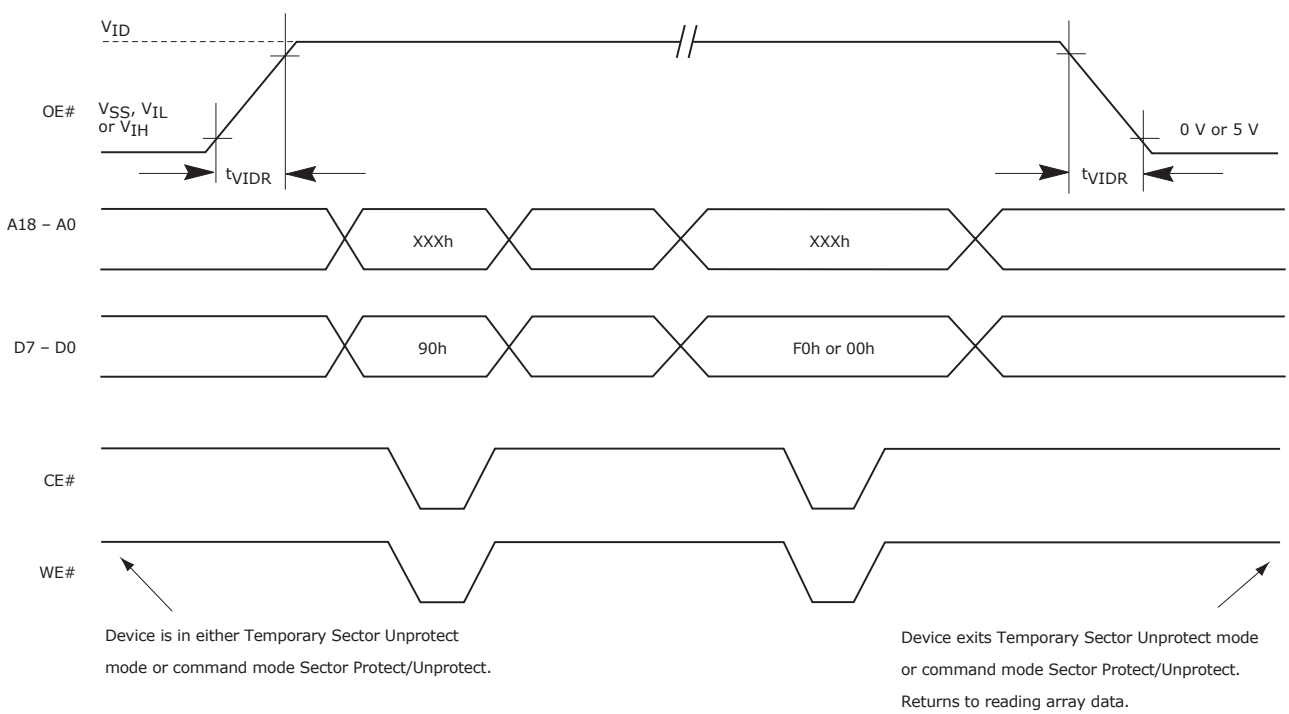
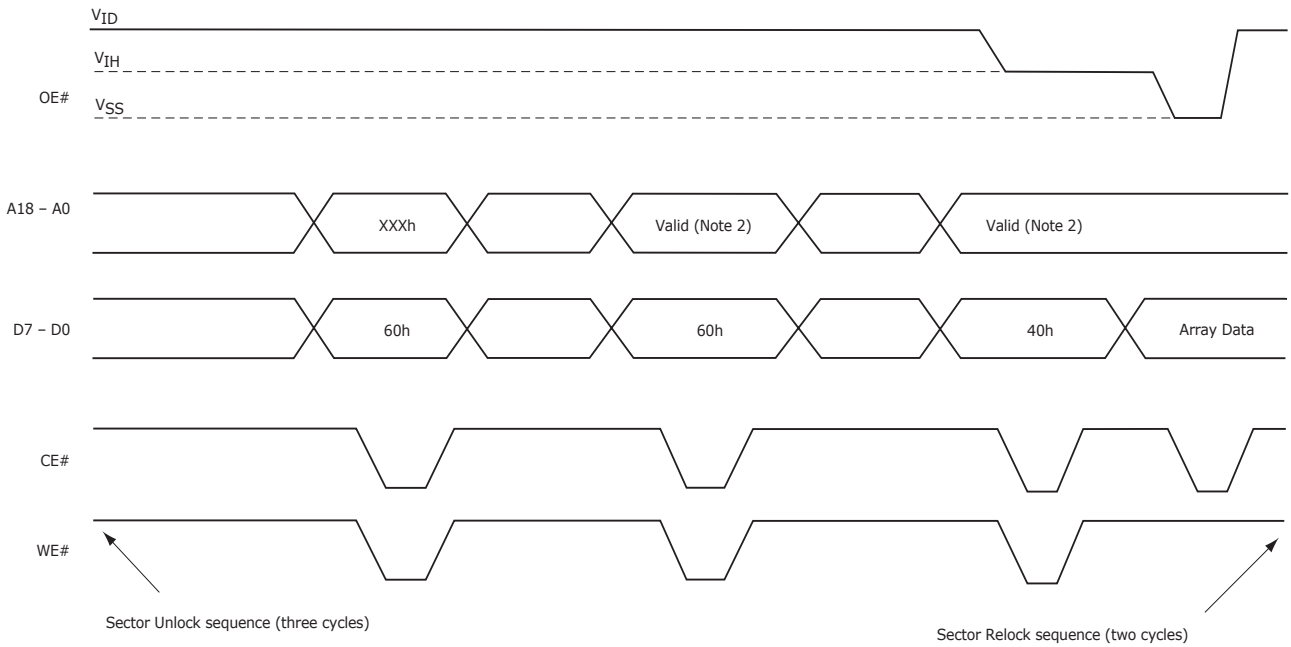


Figure 17. Sector Relock Timing Diagram

AC CHARACTERISTICS



Notes:

1. *To enable the command mode sector protection/unprotection algorithm, the system must issue the command 24h in the sector unlock sequence.*
2. *For sector protection, a valid address consists of the sector address with A6 = 0, A5 = 1, A1 = 1, A0 = 0. For sector unprotection, a valid address consists of the sector address with A6 = 1, A5 = 1, A1 = 1, A0 = 0.*

Figure 18. Sector Protect/Unprotect Timing Diagram

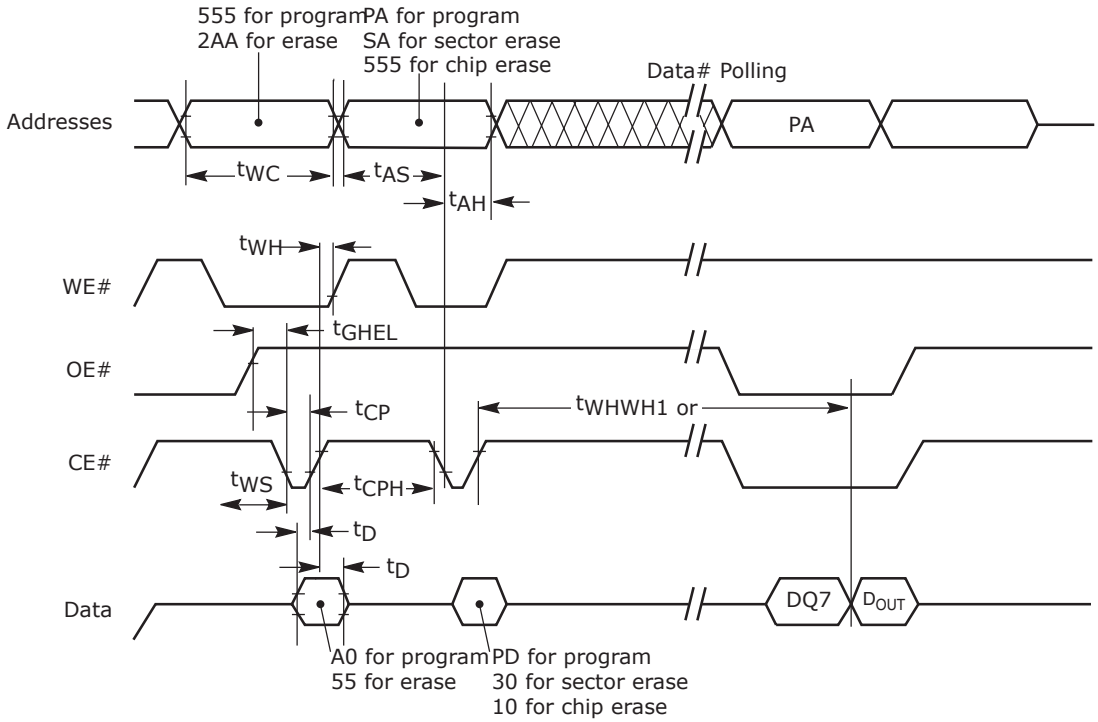
AC CHARACTERISTICS

Alternate CE# Controlled Erase/Program Operations

Parameter				Speed Options			
JEDEC	Std.	Description		-70	-90	-120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0			ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0			ns
	t_{OES}	Output Enable Setup Time	Min	0			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	20			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	7			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1			sec

1. *Not 100% tested.*
2. *See Erase and Programming Performance on page 32 for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = Program Address, PD = Program Data, DQ7# = complement of data written to device, D_{OUT} = data written to device.*
2. *Figure indicates the last two bus cycles of the command sequence.*

Figure 19. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	1	8	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	8		s	
Byte Programming Time	7	300	µs	Excludes system level overhead (Note 5)
Chip Programming Time (Note 3)	3.6	10.8	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 5.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 4.5 V (4.75 V for ±5% devices), 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four-bus-cycle sequence for the program command. See Table for further information on command definitions.*
6. *The device has a minimum guaranteed erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9 and OE#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.*

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:

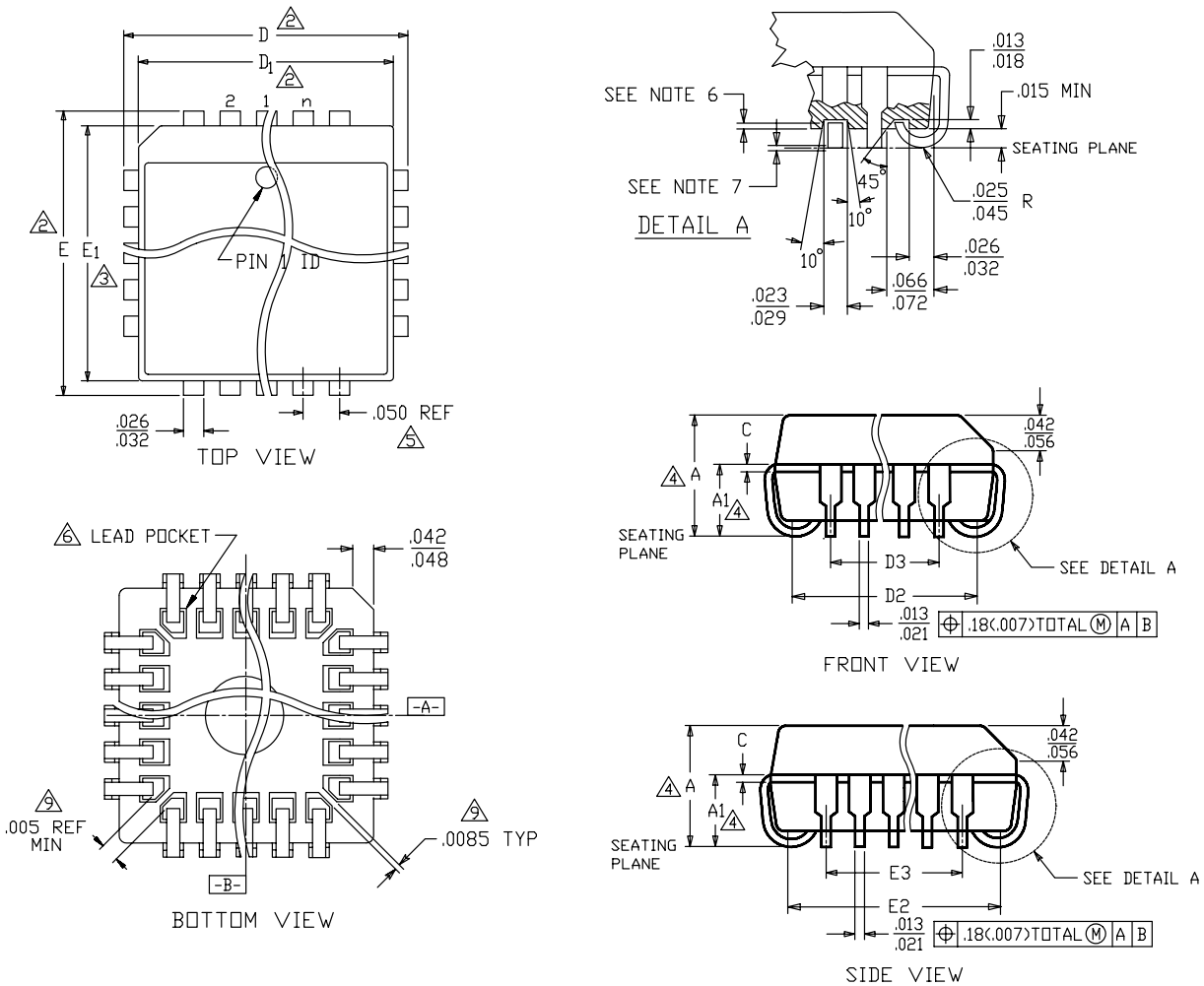
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

PL 032—32-Pin Plastic Leaded Chip Carrier



PACKAGE	PL32	
JEDEC	MO-052(A)AE	
SYMBOL	MIN	MAX
A	.125	.140
A1	.080	.095
D	.485	.495
D1	.447	.453
D2	.390	.430
D3	.300	REF
E	.585	.595
E1	.547	.553
E2	.490	.530
E3	.400	REF
C	.009	.015

NOTES:

Dwg rev AH; 10/99

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010"
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005".
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004" AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045" ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

REVISION SUMMARY

Revision A (January 1999)

Initial release.

Revision B (March 10, 1999)

Global

Revised document into full data sheet.

Revision B+1 (March 18, 1999)

In-System Sector Protect/Sector Unprotect Algorithms figure

Added requirements for asserting address A5 and setting OE# to V_{IH} during both algorithms.

Command Definitions table

Added A5 requirement to definition for SA+ in the legend. In the fourth cycle of the Sector Relock sequence, changed address from XXX to SA+.

Sector Protect/Unprotect Timing Diagram

Modified drawing to indicate that OE# should be dropped to V_{IH} during the third cycle.

Revision B+2 (May 14, 1999)

Ordering Information

Changed the temperature range in the example to I.

Device Bus Operation table

Corrected the highest bit in the address range column header to A18.

Command Definitions table

In Note 4, changed the address range for bits that are don't care to A18–A12.

DC Characteristics table

In Note 5, deleted reference to I_{CC4}.

Read Operations Timings and Alternate CE# Controlled Write Operations figures

Deleted RESET# waveform.

Revision B+3 (July 12, 1999)

Global

Deleted all references to the PDIP package. Changed data sheet status to Preliminary.

In-System Sector Protect/Unprotect Algorithms figure

Added tolerance specifications to the 150 µs and 15 ms waits. Clarified that reading from the sector address during either sector protect or unprotect algorithm requires an access time of 1 µs.

Revision C (November 12, 1999)

AC Characteristics—Figure 11, Program Operations Timing and Figure 12, Chip/Sector Erase Operations

Deleted t_{GHWL} and changed OE# waveform to start at high.

Physical Dimensions

Replaced figures with more detailed illustrations.

Revision D (February 22, 2000)

Global

The "preliminary" designation was removed from the document. Parameters are now stable, and only speed, package, and temperature range combinations are expected to change in future data sheet revisions.

Revision E (November 29, 2000)

Added table of contents.

Ordering Information

Deleted burn-in option.

Table , Command Definitions

In Note 4, corrected lower address bit of don't care range to A11.

Revision E+1 (March 28, 2005)

Global

Added Colophon

Updated Trademark

Ordering Information

Added Pb-free temperature ranges for Industrial and Extended packaging

Added Valid Combination Codes

Revision E+2 (July 26, 2005)

Global

Removed all 55 ns information from the Datasheet.

Colophon

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