PRELIMINARY

AMD

Am29BDS323D

32 Megabit (2 M x 16-Bit)
CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single 1.8 volt read, program and erase (1.7 to 1.9 volt)**
- **Multiplexed Data and Address for reduced I/O count**
  - A0–A15 multiplexed as D0–D15
  - Addresses are latched with AVD# control inputs while CE# low
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Read access times at 40 MHz**
  - Burst access times of 20 ns @ 30 pF at industrial temperature range
  - Asynchronous random access times of 110 ns @ 30 pF
  - Synchronous random access times of 120 ns @ 30 pF
- **Burst length**
  - Continuous linear burst
- **Power dissipation (typical values, 8 bits switching, C_L = 30 pF)**
  - Burst Mode Read: 25 mA
  - Simultaneous Operation: 40 mA
  - Program/Erase: 15 mA
  - Standby mode: 0.2 µA
- **Sector Architecture**
  - Eight 4 Kword sectors and sixty-three sectors of 32 Kwords each
  - Bank A contains the eight 4 Kword sectors and fifteen 32 Kword sectors
  - Bank B contains forty-eight 32 Kword sectors
- **Sector Protection**
  - Software command sector locking
  - WP# protects the last two boot sectors
  - All sectors locked when $V_{PP} = V_{IL}$
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29F and Am29LV families
- **Minimum 1 million erase cycle guarantee per sector**
- **20-year data retention at 125°C**
  - Reliable operation for the life of the system
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset input (RESET#)**
  - Hardware method to reset the device for reading array data
- **CMOS compatible inputs, CMOS compatible outputs**
- **Low V_{CC} write inhibit**
- **Package Option**
  - 47-ball FBGA

This Data Sheet states AMD's current technical specifications regarding the Product described herein. This Data Sheet may be revised by subsequent versions or modifications due to changes in technical specifications.

Publication# **23476** Rev: **B** Amendment/**+4**
Issue Date: **September 4, 2001**

GENERAL DESCRIPTION

The Am29BDS323 is a 32 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory device, organized as 2,097,152 words of 16 bits each. This device uses a single V_{CC} of 1.7 to 1.9 V to read, program, and erase the memory array. A 12.0-volt V_{PP} may be used for faster program performance if desired. The device can also be programmed in standard EPROM programmers.

The Am29BDS323 provides a burst access of 20 ns at 30 pF with initial access times of 120 ns at 30 pF. The device operates within the industrial temperature range of –40°C to +85°C. The device is offered in the 47-ball FBGA package.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into two banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is divided as shown in the following table:

Bank A Sectors		Bank B Sectors	
Quantity	**Size**	**Quantity**	**Size**
8	4 Kwords	48	32 Kwords
15	32 Kwords		
8 Mbits total		24 Mbits total	

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Power Saving (PS), Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The device offers complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bit** DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers three types of data protection at the sector level. The **sector lock/unlock command sequence** disables or re-enables both program and erase operations in any sector. When at V_{IL}, **WP#** locks the two outermost sectors. Finally, when $\mathbf{V_{PP}}$ is at V_{IL}, all sectors are locked.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

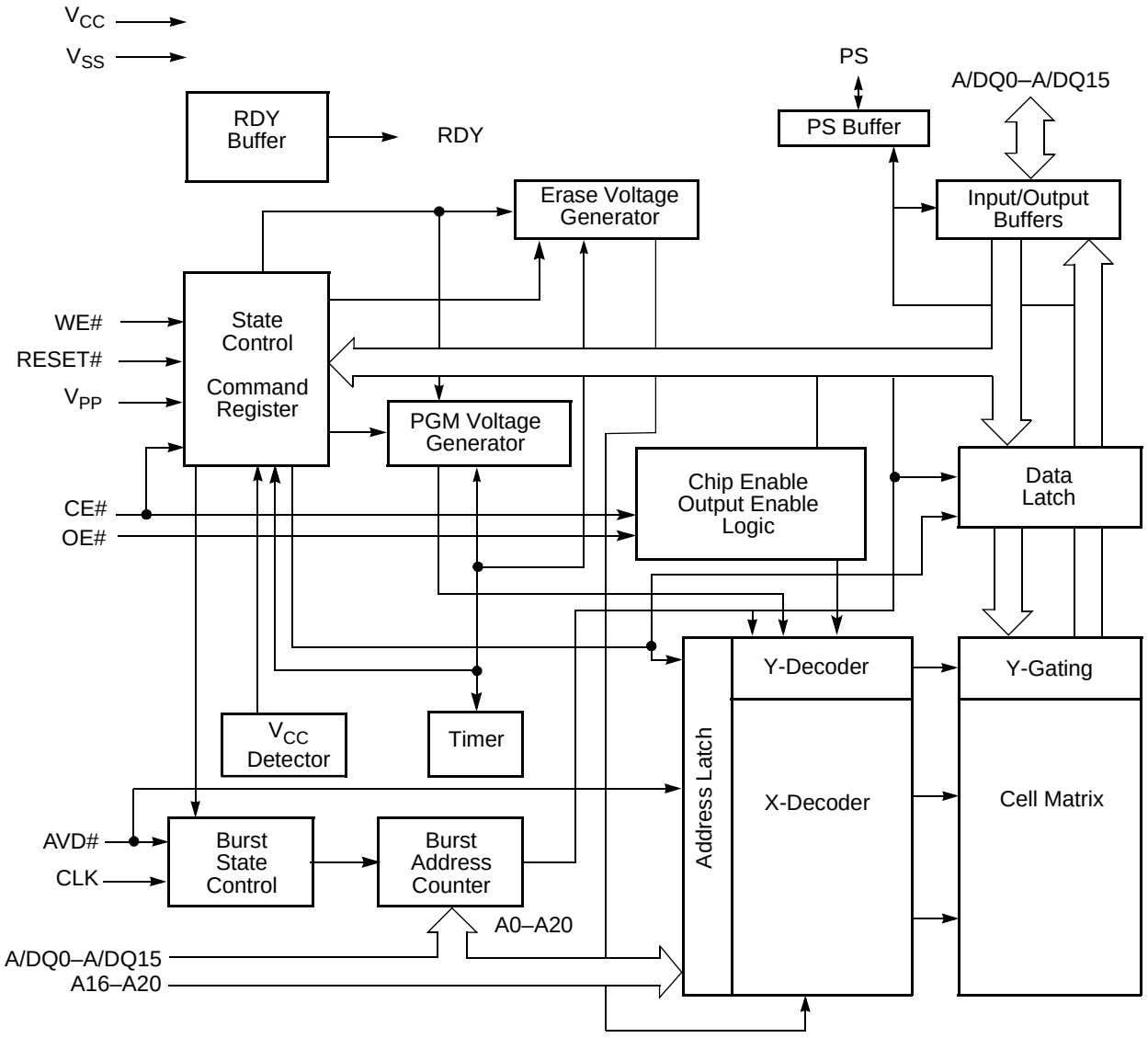
TABLE OF CONTENTS

Product Selector Guide 4
Block Diagram 4
Simultaneous Operation Circuit Block Diagram . 5
Connection Diagram 6
Special Handling Instructions for FBGA Package 6
Input/Output Descriptions 7
Logic Symbol 7
Ordering Information 8
Device Bus Operations 9
Table 1. Device Bus Operations 9
Requirements for Asynchronous Read Operation (Non-Burst) 9
Requirements for Synchronous (Burst) Read Operation 9
Programmable Wait State 10
Power Saving Function 10
Simultaneous Read/Write Operations with Zero Latency 10
Writing Commands/Command Sequences 10
Accelerated Program Operation 11
Autoselect Functions 11
Automatic Sleep Mode 11
RESET#: Hardware Reset Input 11
Output Disable Mode 11
Hardware Data Protection 11
Low VCC Write Inhibit 12
Write Pulse “Glitch” Protection 12
Logical Inhibit 12
Table 2. Sector Address Table 13
Command Definitions 15
Reading Array Data 15
Set Wait State Command Sequence 15
Table 3. Third Cycle Address/Data 15
Enable PS (Power Saving) Mode Command Sequence 15
Sector Lock/Unlock Command Sequence 15
Reset Command 15
Autoselect Command Sequence 16
Program Command Sequence 16
Unlock Bypass Command Sequence 16
Figure 1. Program Operation 17
Chip Erase Command Sequence 17
Sector Erase Command Sequence 17
Erase Suspend/Erase Resume Commands 18
Figure 2. Erase Operation 19
Command Definitions 20
Table 4. Command Definitions 20
Write Operation Status 21
DQ7: Data# Polling 21
Figure 3. Data# Polling Algorithm 21
DQ6: Toggle Bit I 22
Figure 4. Toggle Bit Algorithm 22
DQ2: Toggle Bit II 23
Table 5. DQ6 and DQ2 Indications 23
Reading Toggle Bits DQ6/DQ2 23
DQ5: Exceeded Timing Limits 23
DQ3: Sector Erase Timer 24
Table 6. Write Operation Status 24
Absolute Maximum Ratings 25
Figure 5. Maximum Negative Overshoot Waveform 25
Figure 6. Maximum Positive Overshoot Waveform 25
Operating Ranges 25
DC Characteristics 26
Test Conditions 27
Figure 7. Test Setup 27
Table 7. Test Specifications 27
Figure 8. Input Waveforms and Measurement Levels 27
AC Characteristics 28
Synchronous/Burst Read 28
Figure 9. Burst Mode Read 28
Asynchronous Read 29
Figure 10. Asynchronous Mode Read 29
Figure 11. Reset Timings 30
Erase/Program Operations 31
Figure 12. Program Operation Timings 32
Figure 13. Chip/Sector Erase Operations 33
Figure 14. Accelerated Unlock Bypass Programming Timing 34
Figure 15. Data# Polling Timings (During Embedded Algorithm) . . 35
Figure 16. Toggle Bit Timings (During Embedded Algorithm) 35
Figure 17. Latency with Boundary Crossing 36
Figure 18. Initial Access with Power Saving (PS) Function and Address Boundary Latency 37
Figure 19. Initial Access with Address Boundary Latency 37
Figure 20. Example of Five Wait States Insertion 38
Figure 21. Back-to-Back Read/Write Cycle Timings 39
Erase and Programming Performance 40
Data Retention. 40
Physical Dimensions* 41
FDD047—47-Pin Fine-Pitch Ball Grid Array (FBGA) 7 x 10 mm package 41
Revision Summary 43
Revision A (February 15, 2000) 43
Revision B (June 20, 2000) 43
Revision B+1 (November 27, 2000) 43
Revision B+2 (November 30, 2000) 43
Revision B+3 (December 21, 2000) 43
Revision B+4 (September 4, 2001) 43

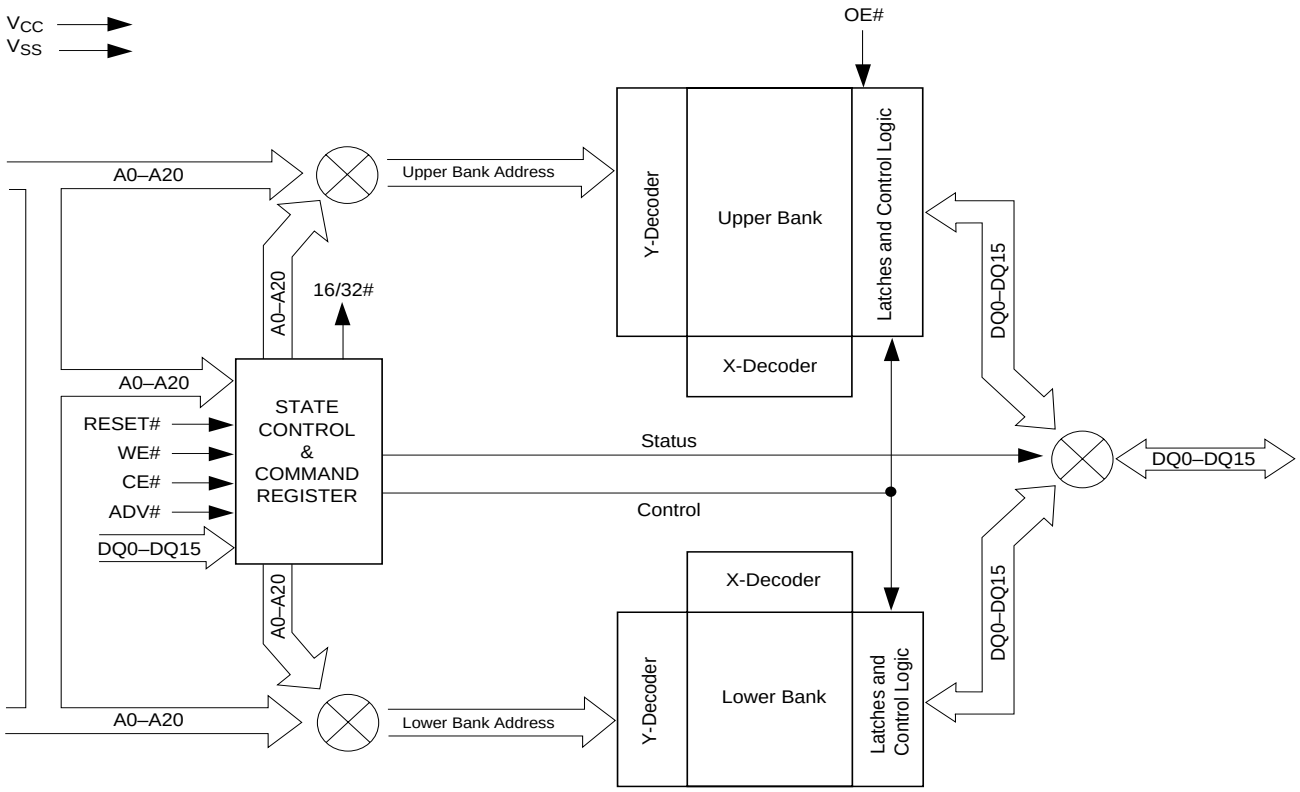
PRODUCT SELECTOR GUIDE

Part Number	Am29BDS323D			
	Synchronous/Burst		Asynchronous	
	Speed Option	11A (40 MHz)	Speed Option	11A
V_{CC} = 1.7 – 1.9 V	Max Initial Access Time, ns (t_{IACC})	120	Max Access Time, ns (t_{ACC})	110
	Max Burst Access Time, ns (t_{BACC})	20	Max CE# Access, ns (t_{CE})	110
	Max OE# Access, ns (t_{OE})	20	Max OE# Access, ns (t_{OE})	35

BLOCK DIAGRAM



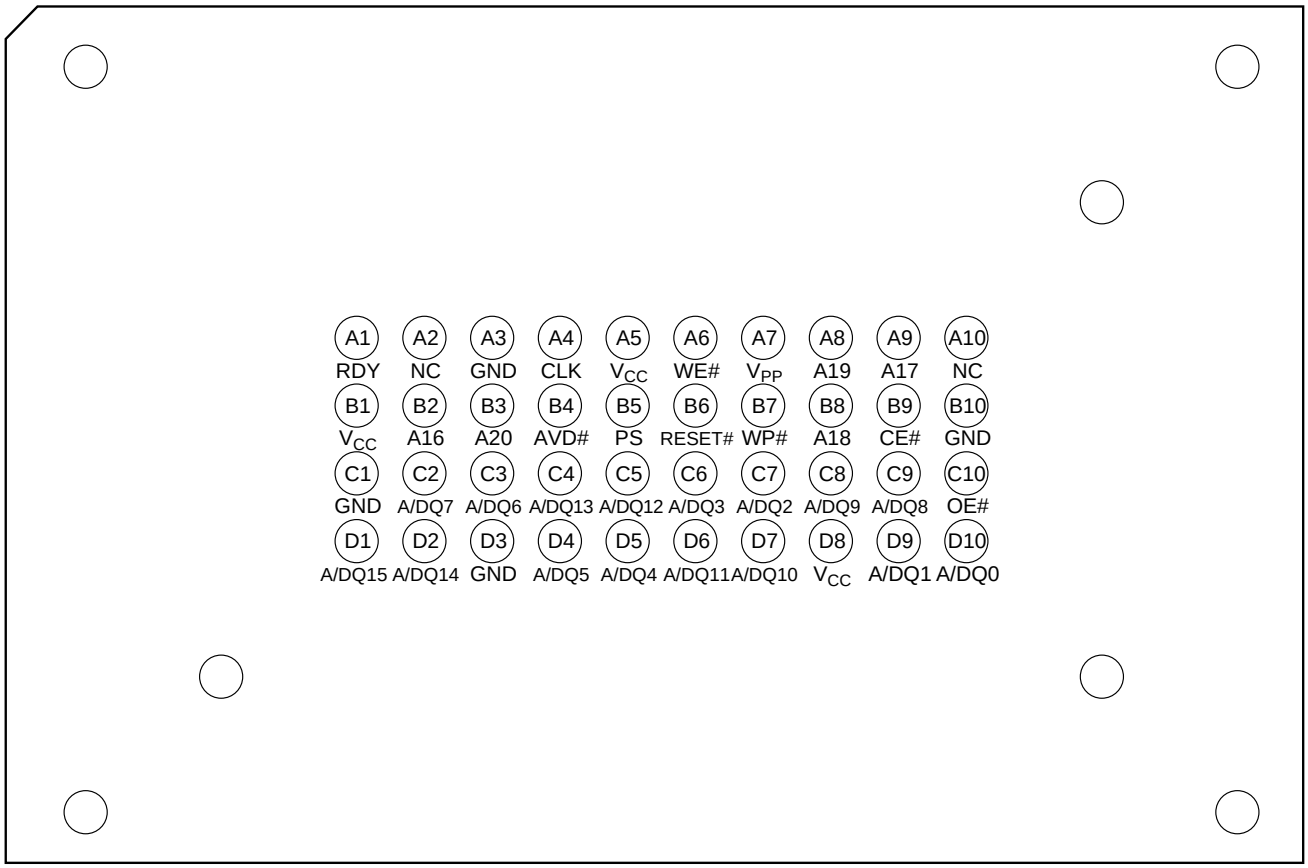
SIMULTANEOUS OPERATION CIRCUIT BLOCK DIAGRAM



Note: *A0–A15 are multiplexed with DQ0–DQ15.*

CONNECTION DIAGRAM

47-Ball FBGA
Top View, Balls Facing Down



Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

INPUT/OUTPUT DESCRIPTIONS

A16–A20 = Address Inputs

A/DQ0–A/DQ15 = Multiplexed Address/Data input/output

CE# = Chip Enable Input. Asynchronous relative to CLK for the Burst mode.

OE# = Output Enable Input. Asynchronous relative to CLK for the Burst mode.

WE# = Write Enable Input.

V_{CC} = Device Power Supply (1.7 V–1.9 V).

V_{SS} = Ground

NC = No Connect; not connected internally

RDY = Ready output; indicates the status of the Burst read. Low = data not valid at expected time. High = data valid.

CLK = The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.

AVD# = Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A0–A15 are multiplexed, address bits A16–A20 are address only).

Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK.
High = device ignores address inputs

PS = Power Saving input/output

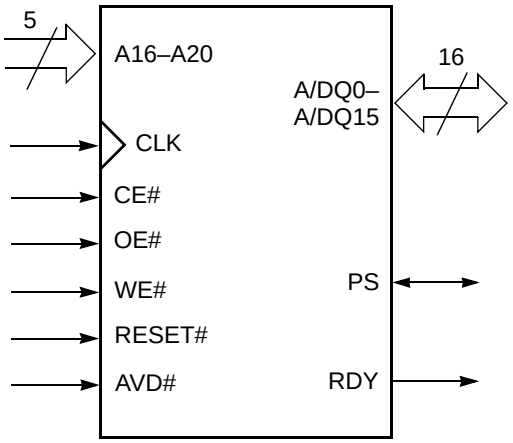
During a read operation, PS indicates whether or not the data on the outputs are inverted. Low = data not inverted; High = data inverted

RESET# = Hardware reset input. Low = device resets and returns to reading array data. RESET# must be low during device power up.

WP# = Hardware write protect input. Low = disables writes to SA70 and SA71

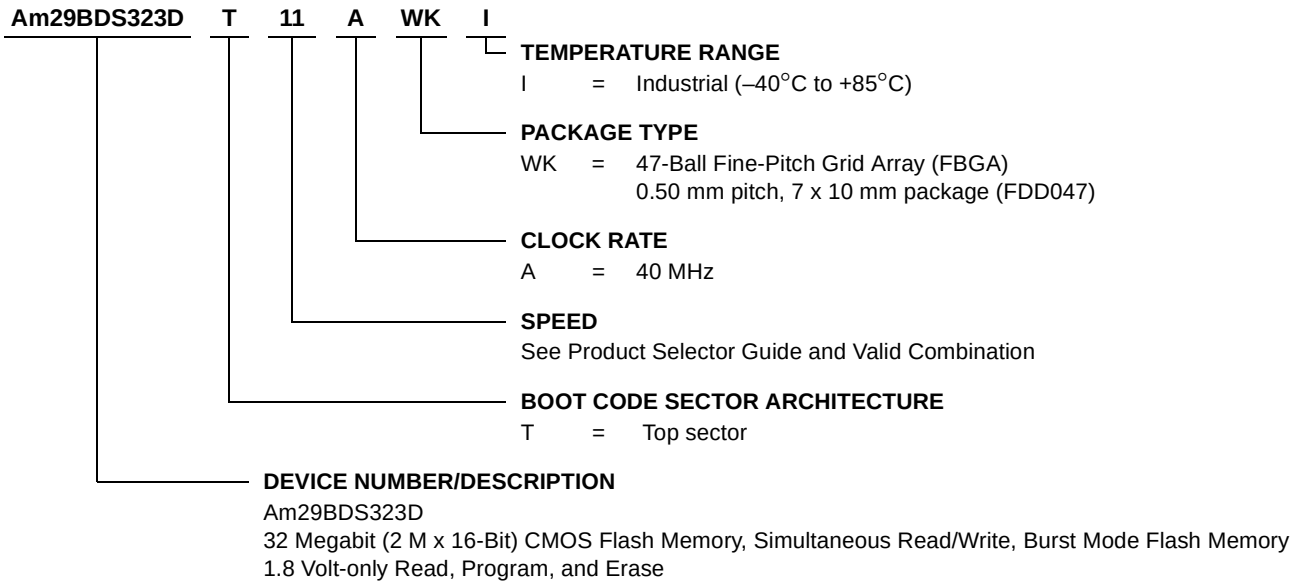
V_{PP} = At 12 V, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions.

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:



Valid Combinations

Valid Combination configuration planned to be supported for this device.

Valid Combinations	
Order Number	**Package Marking**
Am29BDS323DT11AWKI	N323DT1AVI

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	A16–20	A/DQ0–15	RESET#	CLK	AVD#
Asynchronous Read	L	L	H	Addr In	I/O	H	L	
Write	L	H	L	Addr In	I/O	H	L	
Standby (CE#)	H	X	X	HIGH Z	HIGH Z	H	X	X
Hardware Reset	X	X	X	HIGH Z	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	H	H	Addr In	I/O	H		
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	HIGH Z	Burst Data Out	H		H
Terminate current Burst read cycle	H	X	H	HIGH Z	HIGH Z	H		X
Terminate current Burst read cycle via RESET#	X	X	H	HIGH Z	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	H	H	HIGH Z	I/O	H		

Legend: *L = Logic 0, H = Logic 1, X = Don't Care.*

Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must first assert a valid address on A/DQ0–A/DQ15 and A16–A20, while driving AVD# and CE# to V_{IL}. WE# should remain at V_{IH}. Note that CLK must remain low for asynchronous read operations. The rising edge of AVD# latches the address, after which the system can drive OE# to V_{IL}. The data will appear on A/DQ0–A/DQ15. Since the memory array is divided into two banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Requirements for Synchronous (Burst) Read Operation

The device is capable of continuous, sequential (linear) burst operation. However, when the device first powers up, it is enabled for asynchronous read operation. The device will automatically be enabled for burst mode on the first rising edge on the CLK input, while AVD# is held low for one clock cycle. Prior to activating the clock signal, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst session. The system would then write the Set Wait Count command sequence (see "Programmable Wait State"). The system may optionally activate the PS mode (see "Power Saving Function") by writing the Enable PS Mode command sequence at this time, but note that the PS mode can only be disabled by a hardware reset. (See "Command Definitions" for further details).

The initial word is output t_{IACC} after the rising edge of the first CLK cycle. Subsequent words are output t_{BACC}

after the rising edge of each successive clock cycle, which automatically increments the internal address counter. **Note that the device has a fixed internal address boundary that occurs every 64 words, starting at address 00000h**. During the time the device is outputting the 64th word (address 0003Fh, 0007Fh, 000BFh, etc.), a one cycle latency occurs before data appears for the next address (address 00040h, 00080h, 000C0h, etc.). The RDY output indicates this condition to the system by pulsing low. See Figure 17.

The device will continue to output sequential burst data, wrapping around to address 00000h after it reaches the highest addressable memory location, until the system asserts CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 1. The reset command does *not* terminate the burst read operation.

If the host system crosses the bank boundary while reading in burst mode, and the device is not programming or erasing, a one cycle latency will occur as described above. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide asynchronous read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after AVD# is driven active before data will be available. Upon power up, the device defaults to the maximum of seven total cycles. The total number of wait states is programmable from four to seven cycles. See Figure 20.

Power Saving Function

The Power Save function reduces the amount of switching on the data output bus by changing the minimum number of bits possible, thereby reducing power consumption. This function is active only during burst mode operations.

The device compares the word previously output to the system with the new word to be output. If the number of bits to be switched is 0–8 (less than half the bus width), the device simply outputs the new word on the data bus. If, however, the number of bits that must be switched is 9 or higher, the data is *inverted* before being output on the data bus. This effectively limits the maximum number of bits that are switched for any given read cycle to eight. The device indicates to the system whether or not the data is inverted via the PS (power saving) output. If the word on the data bus is *not* inverted, PS = V_{OL}; if the word on the data bus is inverted, PS = V_{OH}.

During initial power up the PS function is disabled. To enable the PS function, the system must write the Enable PS command sequence to the flash device (see the Command Definitions table).

When the PS function is enabled, one additional clock cycle is inserted during the initial and second access of a burst sequence. See Figure 18. The RDY output indicates this condition to the system.

The device is also capable of receiving inverted data during program operations. The host system must indicate to the device via the PS input whether or not the program data are inverted. PS must be driven to V_{IH} for inverted data, or to V_{IL} for non-inverted data.

To disable the PS function, the system must hardware reset the device (drive the RESET# input low).

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 21 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

Writing Commands/Command Sequences

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive CLK, AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive CLK, WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies. The device address space is divided into two banks: Bank A contains the boot/parameter sectors, and Bank B contains the larger, code sectors of uniform size. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” is the address bits required to uniquely select a sector.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through V_{PP}. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{ID} on this input, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the input to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{ID} from the V_{PP} input returns the device to normal operation. Note that sectors must be unlocked using the Sector Lock/Unlock command sequence prior to raising V_{PP} to V_{ID}.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Functions and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at $V_{CC} \pm 0.2$ V. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 60 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.2$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.2$ V, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory. Note that RESET# must be asserted low during device power-up for proper operation.

If RESET# is asserted during a program or erase operation, the device requires a time of t_{READY} (during Embedded Algorithms) before the device is ready to read data again. If RESET# is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 11 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 4 for command definitions).

The device offers three types of data protection at the sector level:

- The sector lock/unlock command sequence disables or re-enables both program and erase operations in any sector.

- When WP# is at V_{IL}, the two outermost sectors are locked.
- When V_{PP} is at V_{IL}, all sectors are locked.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Table 2. Sector Address Table

	Sector	Sector Size	(x16) Address Range
Bank B	SA0	32 Kwords	00000h—07FFFh
	SA1	32 Kwords	08000h—0FFFFh
	SA2	32 Kwords	10000h—17FFFh
	SA3	32 Kwords	18000h—1FFFFh
	SA4	32 Kwords	20000h—27FFFh
	SA5	32 Kwords	28000h—2FFFFh
	SA6	32 Kwords	30000h—37FFFh
	SA7	32 Kwords	38000h—3FFFFh
	SA8	32 Kwords	40000h—47FFFh
	SA9	32 Kwords	48000h—4FFFFh
	SA10	32 Kwords	50000h—57FFFh
	SA11	32 Kwords	58000h—5FFFFh
	SA12	32 Kwords	60000h—67FFFh
	SA13	32 Kwords	68000h—6FFFFh
	SA14	32 Kwords	70000h—77FFFh
	SA15	32 Kwords	78000h—7FFFFh
	SA16	32 Kwords	80000h—87FFFh
	SA17	32 Kwords	88000h—8FFFFh
	SA18	32 Kwords	90000h—97FFFh
	SA19	32 Kwords	98000h—9FFFFh
	SA20	32 Kwords	A0000h—A7FFFh
	SA21	32 Kwords	A8000h—AFFFFh
	SA22	32 Kwords	B0000h—B7FFFh
	SA23	32 Kwords	B8000h—BFFFFh
	SA24	32 Kwords	C0000h—C7FFFh
	SA25	32 Kwords	C8000h—CFFFFh
	SA26	32 Kwords	D0000h—D7FFFh
	SA27	32 Kwords	D8000h—DFFFFh
	SA28	32 Kwords	E0000h—E7FFFh
	SA29	32 Kwords	E8000h—EFFFFh
	SA30	32 Kwords	F0000h—F7FFFh
	SA31	32 Kwords	F8000h—FFFFFh
	SA32	32 Kwords	100000h—107FFFh
	SA33	32 Kwords	108000h—10FFFFh
	SA34	32 Kwords	110000h—117FFFh
	SA35	32 Kwords	118000h—11FFFFh
	SA36	32 Kwords	120000h—127FFFh
	SA37	32 Kwords	128000h—12FFFFh

Table 2. Sector Address Table (Continued)

	Sector	Sector Size	(x16) Address Range
Bank B	SA38	32 Kwords	130000h—137FFFh
	SA39	32 Kwords	138000h—13FFFFh
	SA40	32 Kwords	140000h—147FFFh
	SA41	32 Kwords	148000h—14FFFFh
	SA42	32 Kwords	150000h—157FFFh
	SA43	32 Kwords	158000h—15FFFFh
	SA44	32 Kwords	160000h—167FFFh
	SA45	32 Kwords	168000h—16FFFFh
	SA46	32 Kwords	170000h—177FFFh
	SA47	32 Kwords	178000h—17FFFFh
Bank A	SA48	32 Kwords	180000h—187FFFh
	SA49	32 Kwords	188000h—18FFFFh
	SA50	32 Kwords	190000h—197FFFh
	SA51	32 Kwords	198000h—19FFFFh
	SA52	32 Kwords	1A0000h—1A7FFFh
	SA53	32 Kwords	1A8000h—1AFFFFh
	SA54	32 Kwords	1B0000h—1B7FFFh
	SA55	32 Kwords	1B8000h—1BFFFFh
	SA56	32 Kwords	1C0000h—1C7FFFh
	SA57	32 Kwords	1C8000h—1CFFFFh
	SA58	32 Kwords	1D0000h—1D7FFFh
	SA59	32 Kwords	1D8000h—1DFFFFh
	SA60	32 Kwords	1E0000h—1E7FFFh
	SA61	32 Kwords	1E8000h—1EFFFFh
	SA62	32 Kwords	1F0000h—1F7FFFh
	SA64	4 Kwords	1F8000h—1F8FFFh
	SA65	4 Kwords	1F9000h—1F9FFFh
	SA66	4 Kwords	1FA000h—1FAFFFh
	SA67	4 Kwords	1FB000h—1FBFFFh
	SA68	4 Kwords	1FC000h—1FCFFFh
	SA69	4 Kwords	1FD000h—1FDFFFh
	SA70	4 Kwords	1FE000h—1FEFFFh
	SA71	4 Kwords	1FF000h—1FFFFFh

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 4 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the rising edge of AVD#. All data is latched on the rising edge of WE#. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Asynchronous Read Operation (Non-Burst) and Requirements for Synchronous (Burst) Read Operation in the Device Bus Operations section for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figures 9 and 10 show the timings.

Set Wait State Command Sequence

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency. The first two cycles of the command sequence are for unlock purposes. On the third cycle, the system should write C0h to the address associated with the intended wait state setting (see Table 3). Address bits A12 and A13 determine the setting.

Table 3. Third Cycle Address/Data

Address	Total Wait State Cycles	Data
000555h	4	C0h
001555h	5	
002555h	6	
003555h	7	

Upon power up, the device defaults to the maximum seven cycle wait state setting (see Figure 20). It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

Enable PS (Power Saving) Mode Command Sequence

The Enable PS (Power Saving) Mode command sequence is required to set the device to the PS mode. On power up, the Power Saving mode is disabled. The command sequence consists of two unlock cycles followed by a command cycle in which the address and data should 555h/70h, respectively. The PS mode remains enabled until the device is hardware reset (either device is powered down or RESET# is asserted low).

Sector Lock/Unlock Command Sequence

The sector lock/unlock command sequence allows the system to determine which sectors are protected from accidental writes. When the device is first powered up, all sectors are locked. To unlock a sector, the system must write the sector lock/unlock command sequence. Two cycles are first written: addresses are don't care and data is 60h. During the third cycle, the sector address (SLA) and unlock command (60h) is written, while specifying with address A6 whether that sector should be locked (A6 = V_{IL}) or unlocked (A6 = V_{IH}). After the third cycle, the system can continue to lock or unlock additional cycles, or exit the sequence by writing F0h (reset command).

Note that the last two outermost boot sectors can be locked by taking the WP# signal to V_{IL}. Also, if V_{PP} is at V_{IL} all sectors are locked; if the V_{PP} input is at V_{PP}, all sectors are unlocked.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which

the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 4 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence:

- A read cycle at address (BA)XX00h (where BA is the bank address) returns the manufacturer code.
- A read cycle at address (BA)XX01h returns the device code.
- A read cycle to an address containing a sector address (SA) within the same bank, and the address 0002h on A15–A0 returns 0001h if the sector is locked, or 0000h if it is unlocked. (Refer to Table 2 for valid sector addresses).

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 4 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from “0” back to a “1.”** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bit to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

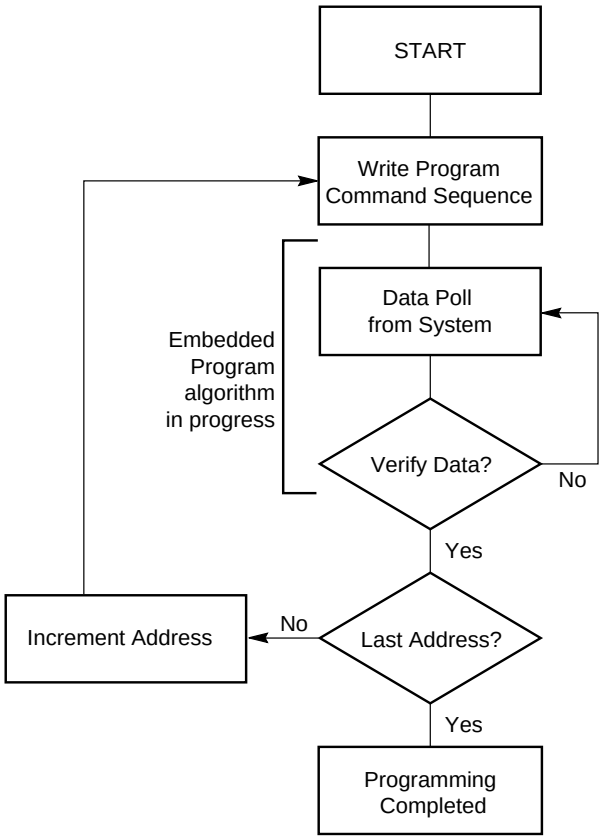
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. The host system may also initiate the chip erase and sector erase sequences in the unlock bypass mode. The erase command sequences are four cycles in length instead of six cycles. Table 4 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

The device offers accelerated program operations through V_{PP}. When the system asserts V_{ID} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the V_{PP} input to accelerate the operation. Note that sectors must be unlocked using the Sector Lock/Unlock command sequence prior to raising V_{PP} to V_{ID}.

Figure 1 illustrates the algorithm for the program operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 12 for timing diagrams.



Note: *See Table 4 for program command sequence.*

Figure 1. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The host system may also initiate the chip erase command sequence while the device is in the unlock bypass mode. The command sequence is two cycles cycles in length instead of six cycles. Table 4 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 13 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 4 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector

erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank.

The system can determine the status of the erase operation by reading DQ7 or DQ6/ DQ2 in the erasing bank. Note that the host system must wait 200 µs after the last sector erase command to obtain status information if the first status read is in a different bank than the last sector selected for erasure. For example, if sector 0, which is in bank B, was the last sector selected for erasure, and the host system requests its first status read from sector 71, which is in bank A, then the device requires 200 µs before status information will be available. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the sector erase command sequence while the device is in the unlock bypass mode. The command sequence is four cycles cycles in length instead of six cycles.

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 13 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

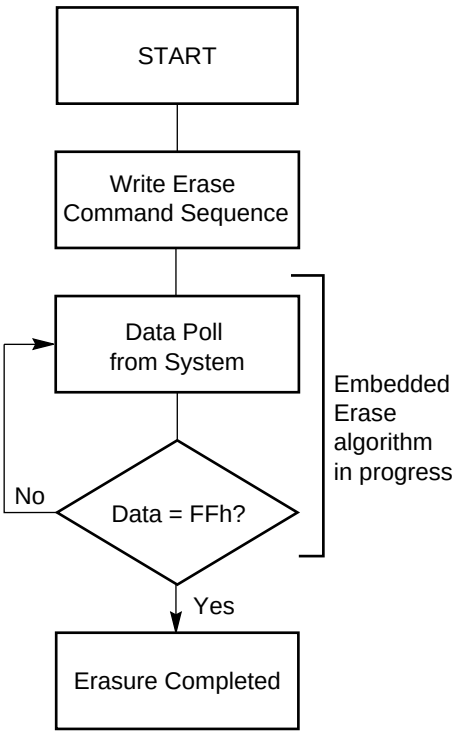
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Functions and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 4 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 2. Erase Operation

Command Definitions

Table 4. Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	(BA)555	90	(BA)X00	0001				
	Device ID (Note 9)	4	555	AA	2AA	55	(BA)555	90	(BA)X01	22D1	(BA)X03	20/00		
	Sector Lock Verify (Note 10)	4	555	AA	2AA	55	(SA)555	90	(SA)X02	00/01				
Program		4	555	AA	2AA	55	555	A0	PA	Data				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 11)		2	XXX	A0	PA	PD								
Unlock Bypass Sector Erase (Note 11)		2	XXX	80	SA	30								
Unlock Bypass Chip Erase (Note 11)		2	XXX	80	XXX	10								
Unlock Bypass Reset (Note 12)		2	BA	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 13)		1	BA	B0										
Erase Resume (Note 14)		1	BA	30										
Sector Lock/Unlock		3	XXX	60	XXX	60	SLA	60						
Set Wait Count (Note 15)		3	555	AA	2AA	55	(WS)555	C0						
Enable PS Mode		3	555	AA	2AA	55	555	70						

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20–A12 uniquely select any sector.

BA = Address of the bank (A20, A19) that is being switched to autoselect mode, is in bypass mode, or is being erased.

SLA = Address of the sector to be locked. Set sector address (SA) and either A6 = 1 for unlocked or A6 = 0 for locked.

WS = Number of wait states defined by A12, A13.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A20–A11 are don't cares.*
6. *No unlock or command cycles required when bank is reading array data.*
7. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
9. *The fifth cycle of the device ID autoselect command sequence is an extended device ID code. The data is 00h for devices that do not require additional latency when burst address begins at an address boundary, and 20h for devices that require additional latency when burst address begins at an address boundary.*
10. *The data is 0000h for an unlocked sector and 0001h for a locked sector. All sectors are again locked upon hardware reset.*
11. *The Unlock Bypass command is required prior to this command sequence.*
12. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*
13. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
14. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
15. *The addresses in the third cycle must contain, on A12 and A13, the additional wait counts to be set. See "Set Wait State Command Sequence".*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 6 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

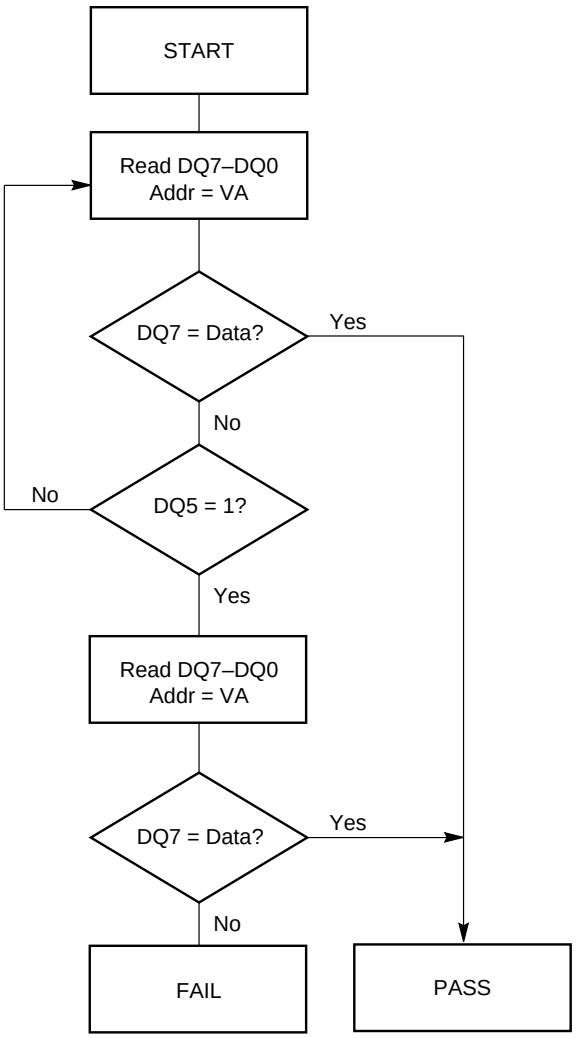
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7. Note that the host system must wait 200 µs after the last sector erase command to obtain status information if the first status read is in a different bank than the last sector selected for erasure. For example, if sector 0, which is in bank B, was the last sector selected for erasure, and the host system requests its first status read from sector 71, which is in bank A, then the device requires 200 µs before status information will be available.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 6 shows the outputs for Data# Polling on DQ7. Figure 3 shows the Data# Polling algorithm. Figure 15 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 3. Data# Polling Algorithm

RDY: Ready

The RDY is a dedicated output that indicates (when at logic low) the system should wait 1 clock cycle before expecting the next word of data.

RDY functions only while reading data in burst mode. Three conditions may cause the RDY output to be low: during the initial access (in burst mode) when PS is enabled; after the boundary that occurs every 64 words beginning at address 00000h; and when the clock frequency is less than 6 MHz (in which case RDY is low every third clock).

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. Note that OE# must be low during toggle bit status reads. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

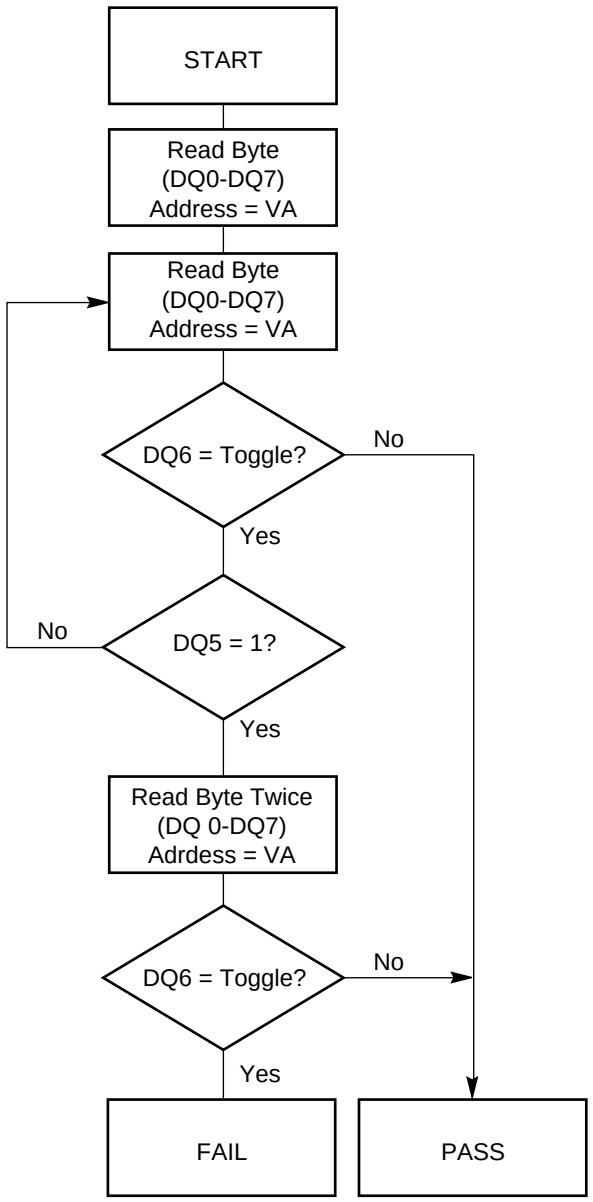
Note that the host system must wait 200 µs after the last sector erase command to obtain status information if the first status read is in a different bank than the last sector selected for erasure. For example, if sector 0, which is in bank B, was the last sector selected for erasure, and the host system requests its first status read from sector 71, which is in bank A, then the device requires 200 µs before status information will be available.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: Figure 4 (toggle bit flowchart), DQ6: Toggle Bit I (description), Figure 16 (toggle bit timing diagram), and Table 5 (compares DQ2 and DQ6).



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 4. Toggle Bit Algorithm

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. Note that OE# must be low during toggle bit status reads. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for DQ2 and DQ6.

See the following for additional information: Figure 4 (toggle bit flowchart), DQ6: Toggle Bit I (description), Figure 16 (toggle bit timing diagram), and Table 5 (compares DQ2 and DQ6).

Table 5. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 4 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 4).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the

device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 6 shows the status of DQ3 relative to the other status bits.

Table 6. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
Erase Suspend Mode	Erase-Suspend-Read (Note 4)	Erase Suspended Sector	1	No toggle	0	N/A	Toggle
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A

Notes:

1. *DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*
4. *The system may read either asynchronously or synchronously (burst) while in erase suspend. RDY will function exactly as in non-erase-suspended mode.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground,
All I/Os except V_{PP} (Note 1). . . –0.5 V to V_{CC} + 0.5 V

V_{CC} (Note 1) . . . . . –0.5 V to +2.5 V

V_{PP} (Note 2) . . . . . –0.5 V to +12.5 V

Output Short Circuit Current (Note 3) . . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, input at I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns during voltage transitions inputs might overshooot to V_{CC} +0.5 V for periods up to 20 ns. See Figure 5. Maximum DC voltage on output and I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 6.*
2. *Minimum DC input voltage on V_{PP} is –0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 5. Maximum DC input voltage on V_{PP} is +12.5 V which may overshoot to +13.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

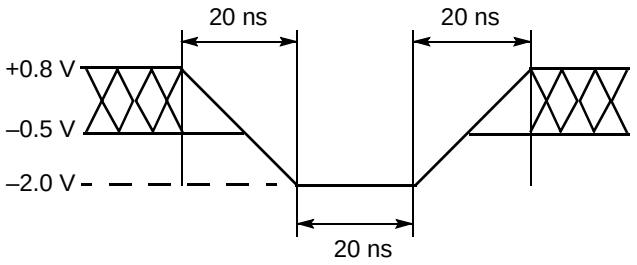


Figure 5. Maximum Negative Overshoot Waveform

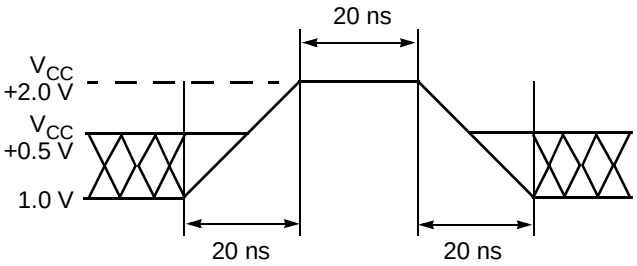


Figure 6. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

V_{CC} Supply Voltages

V_{CC} Supply Voltages . . . . . +1.7 V to +1.9 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

Parameter	Description	Test Conditions (Note 1)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{CCB1}	V_{CC} Active Burst Read Current	CE# = V_{IL}, OE# = V_{IL}			25	30	mA
I_{CCB2}		CE# = V_{IL}, OE# = V_{IH} (Note 2)			0.5	1	mA
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		10	16	mA
			1 MHz		2	4	mA
I_{CC2}	V_{CC} Active Write Current (Note 4)	CE# = V_{IL}, OE# = V_{IH}, $V_{PP} = V_{IH}$			15	40	mA
I_{CC3}	V_{CC} Standby Current (Note 5)	CE# = V_{IH}, RESET# = V_{IH}			0.2	10	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			0.2	10	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IL}			40	60	mA
I_{PP}	Accelerated Program Current (Note 6)	CE# = V_{IL}, OE# = V_{IH}, V_{PP} = 12.0 ± 0.5 V	V_{PP}		7	15	mA
			V_{CC}		5	10	mA
V_{IL}	Input Low Voltage			–0.5		0.2	V
V_{IH}	Input High Voltage			V_{CC} – 0.2		V_{CC} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC} – 0.1			V
V_{ID}	Voltage for Accelerated Program			11.5		12.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Note:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *When OE# = V_{IH}, burst mode is deactivated. If OE# = V_{IL} is reasserted, the last data prior to OE# = V_{IH} will remain available from the device. A new burst read sequence is initiated when new address is asserted, AVD# = V_{IL} and OE# = V_{IH} .*
3. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 60 ns. Typical sleep mode current is equal to I_{CC3}.*
6. *Total current during accelerated programming is the sum of V_{PP} and V_{CC} currents.*

TEST CONDITIONS

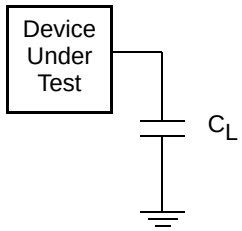
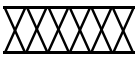
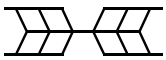


Figure 7. Test Setup

Table 7. Test Specifications

Test Condition	11A	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	V_{CC}/2	V
Output timing measurement reference levels	V_{CC}/2	V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

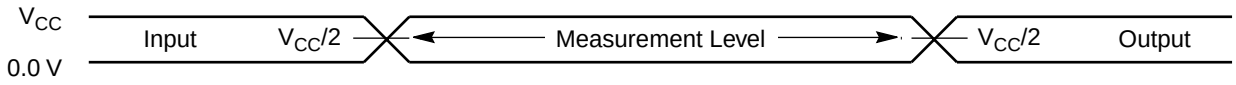
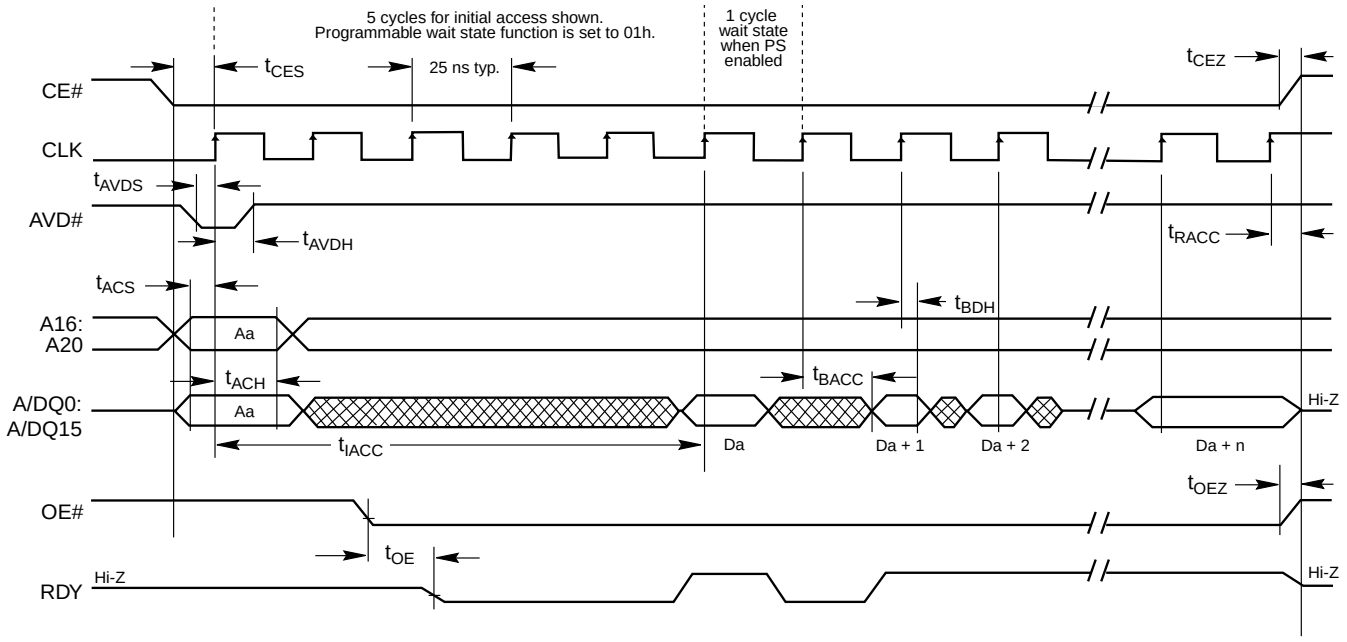


Figure 8. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Synchronous/Burst Read

Parameter		Description		11A (40 MHz)	Unit
JEDEC	Standard				
	t_{IACC}	Initial Access Time	Max	120	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	20	ns
	t_{AVDS}	AVD# Setup Time to CLK	Min	5	ns
	t_{AVDH}	AVD# Hold Time from CLK	Min	7	ns
	t_{AVDO}	AVD# High to OE# Low	Min	0	ns
	t_{ACS}	Address Setup Time to CLK	Min	5	ns
	t_{ACH}	Address Hold Time from CLK	Min	7	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Max	4	ns
	t_{OE}	Output Enable to Output Valid	Max	20	ns
	t_{CEZ}	Chip Enable to High Z	Max	10	ns
	t_{OEZ}	Output Enable to High Z	Max	10	ns
	t_{CES}	CE# Setup Time to CLK	Min	5	ns
	t_{CEH}	CE# Hold Time from CLK	Min	7	ns
	t_{RDYS}	RDY Setup Time to CLK	Min	5	ns
	t_{RACC}	Ready access time from CLK	Max	20	ns



Notes:

1. *Figure shows total number of wait states set to five cycles. The total number of wait states can be programmed from four cycles to seven cycles.*
2. *Figure shows that PS (power saving mode) has been enabled; one additional wait state occurs during initial data Da. Latency is not present if PS is not enabled.*
3. *If any burst address occurs at a 64-word boundary, one additional clock cycle is inserted, and is indicated by RDY.*

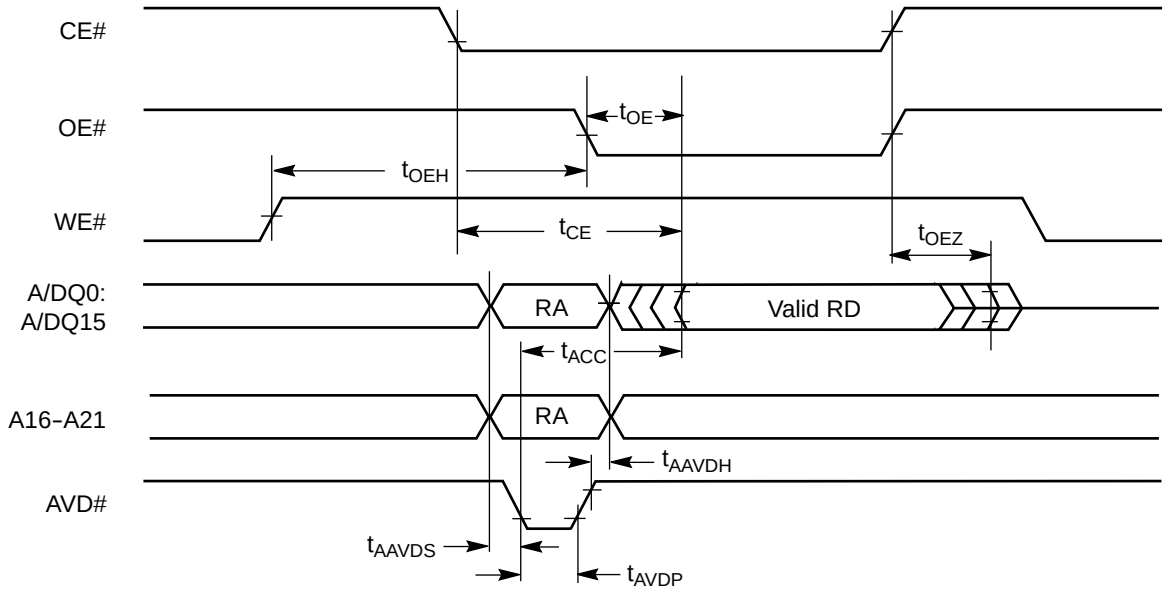
Figure 9. Burst Mode Read

AC CHARACTERISTICS

Asynchronous Read

Parameter		Description			11A	Unit
JEDEC	Standard					
	t_{CE}	Access Time from CE# Low		Max	110	ns
	t_{ACC}	Asynchronous Access Time		Max	110	ns
	t_{AVDP}	AVD# Low Time		Min	12	ns
	t_{AAVDS}	Address Setup Time to Falling Edge of AVD		Min	5	ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	7	ns
	t_{OE}	Output Enable to Output Valid		Max	35	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0	ns
			Toggle and Data# Polling	Min	10	ns
	t_{OEZ}	Output Enable to High Z (See Note)		Max	20	ns

Note: *Not 100% tested.*



Note: *RA = Read Address, RD = Read Data.*

Figure 10. Asynchronous Mode Read

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

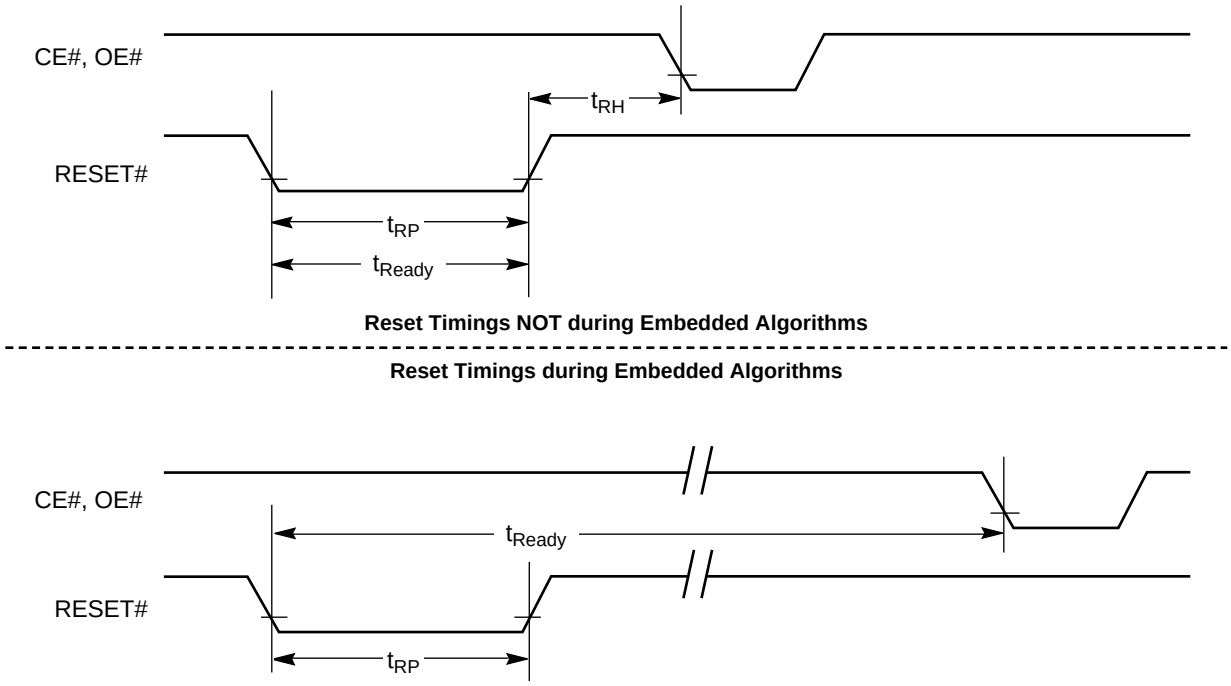


Figure 11. Reset Timings

AC CHARACTERISTICS

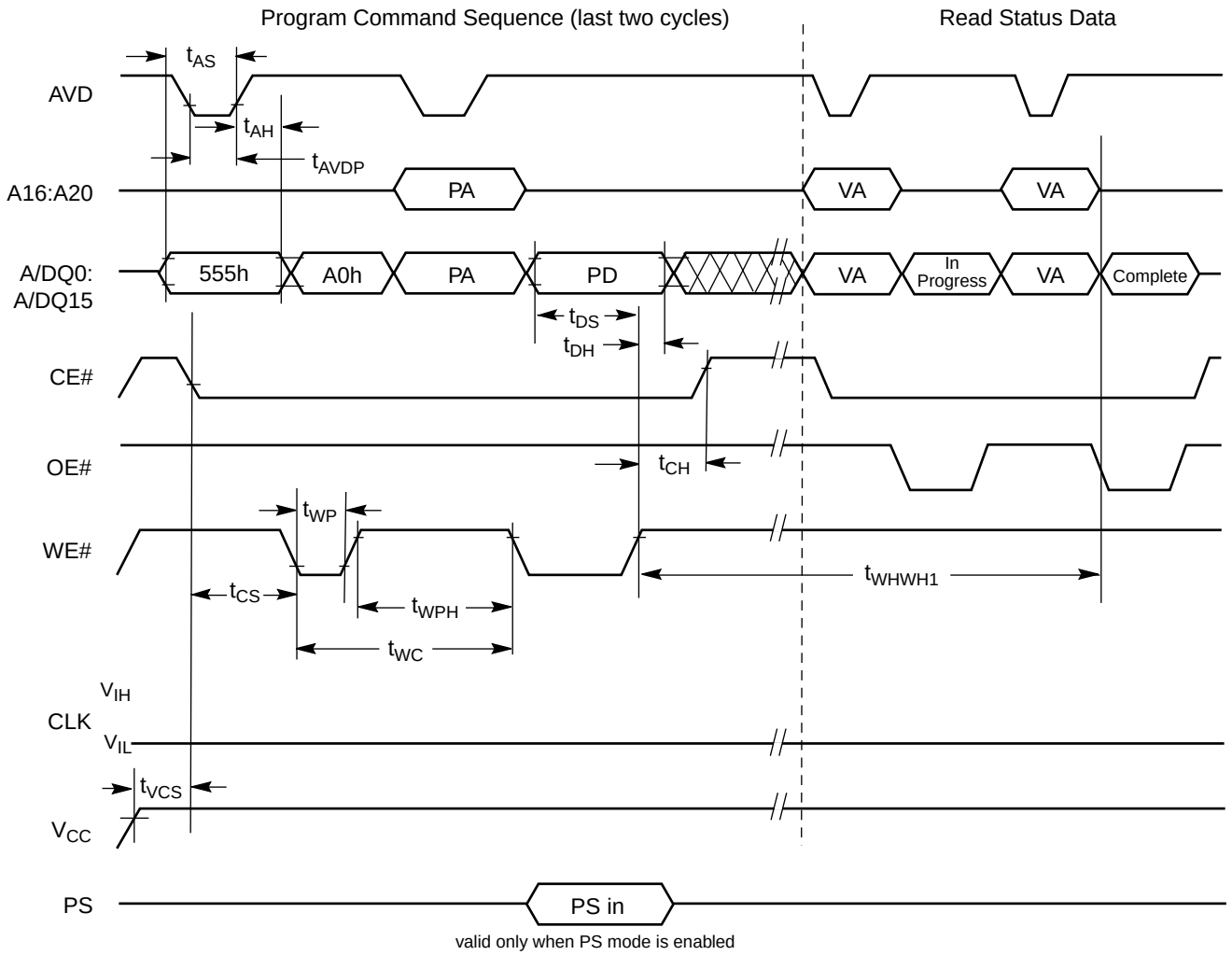
Erase/Program Operations

Parameter		Description		11A	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	100	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	5	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	7	ns
	t_{AVDP}	AVD# Low Time	Min	12	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Typ	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Typ	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Typ	0	ns
t_{WLWH}	t_{WP}/t_{WRL}	Write Pulse Width	Typ	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Typ	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	11.5	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 2, 3)	Typ	1.5	sec
	t_{VPP}	V_{PP} Rise and Fall Time	Min	500	ns
	t_{VPS}	V_{PP} Setup Time (During Accelerated Programming)	Min	1	µs
	t_{VCS}	V_{CC} Setup Time	Min	50	µs

Notes:

1. *Not 100% tested.*
2. *See the “Erase and Programming Performance” section for more information.*
3. *Does not include the preprogramming time.*

AC CHARACTERISTICS

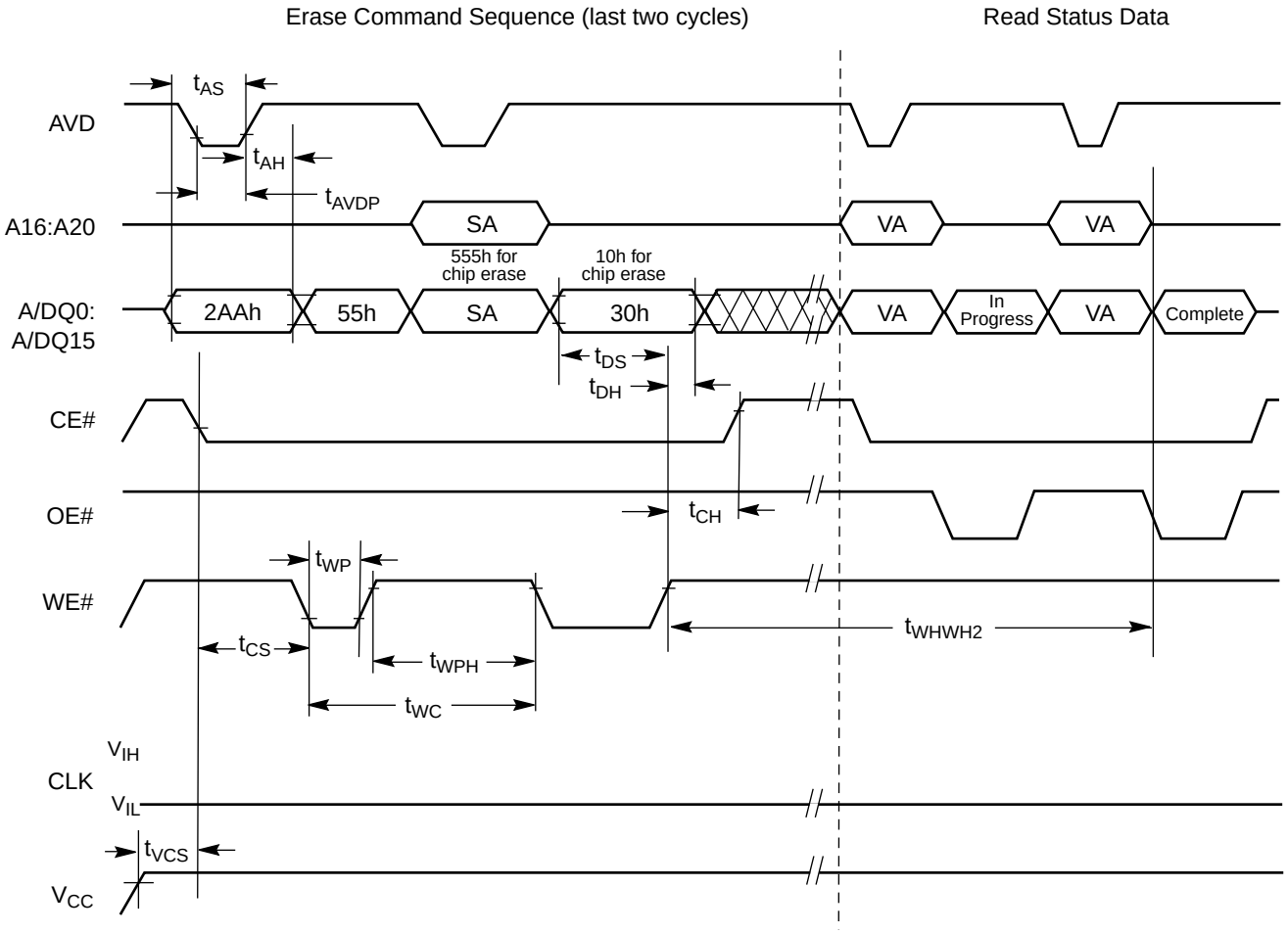


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A16–A20 are don't care during command sequence unlock cycles.*

Figure 12. Program Operation Timings

AC CHARACTERISTICS

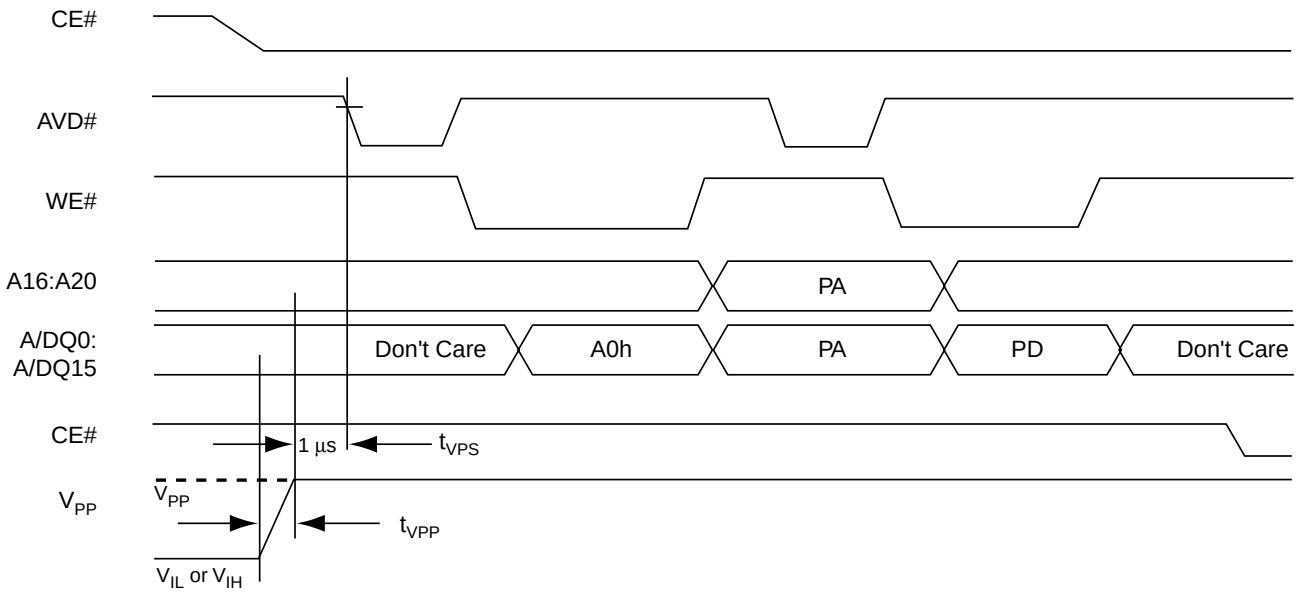


Notes:

1. *SA is the sector address for Sector Erase.*
2. *Address bits A16–A20 are don't cares during unlock cycles in the command sequence.*

Figure 13. Chip/Sector Erase Operations

AC CHARACTERISTICS

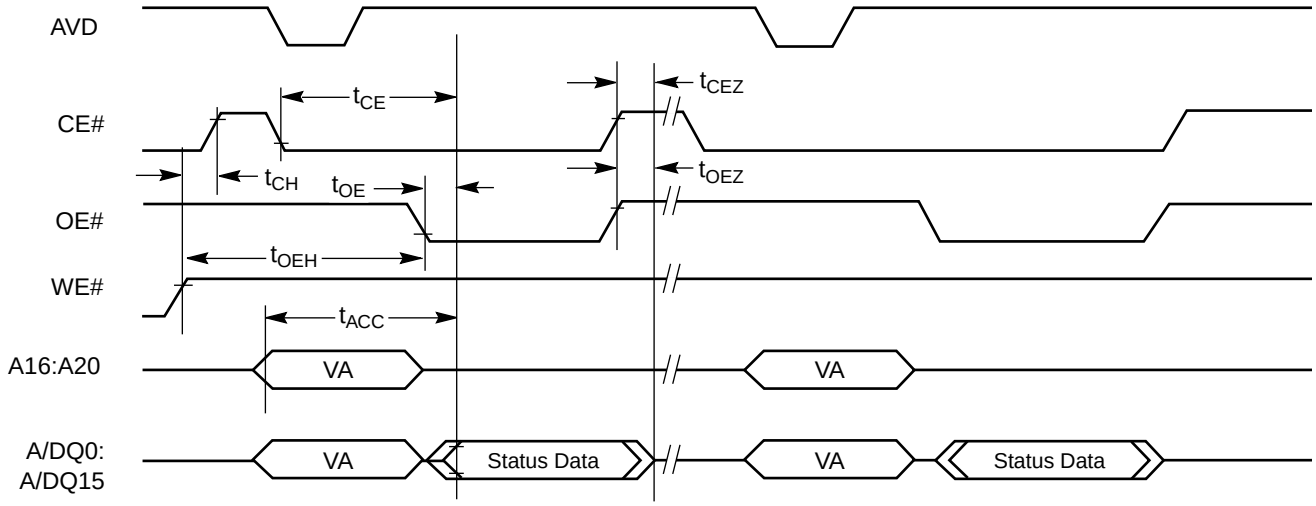


Notes:

1. *V_{PP} can be left high for subsequent programming pulses.*
2. *Use setup and hold times from conventional program operation.*
3. *Sectors must be unlocked using the Sector Lock/Unlock command sequence prior to raising V_{PP} to V_{ID}.*

Figure 14. Accelerated Unlock Bypass Programming Timing

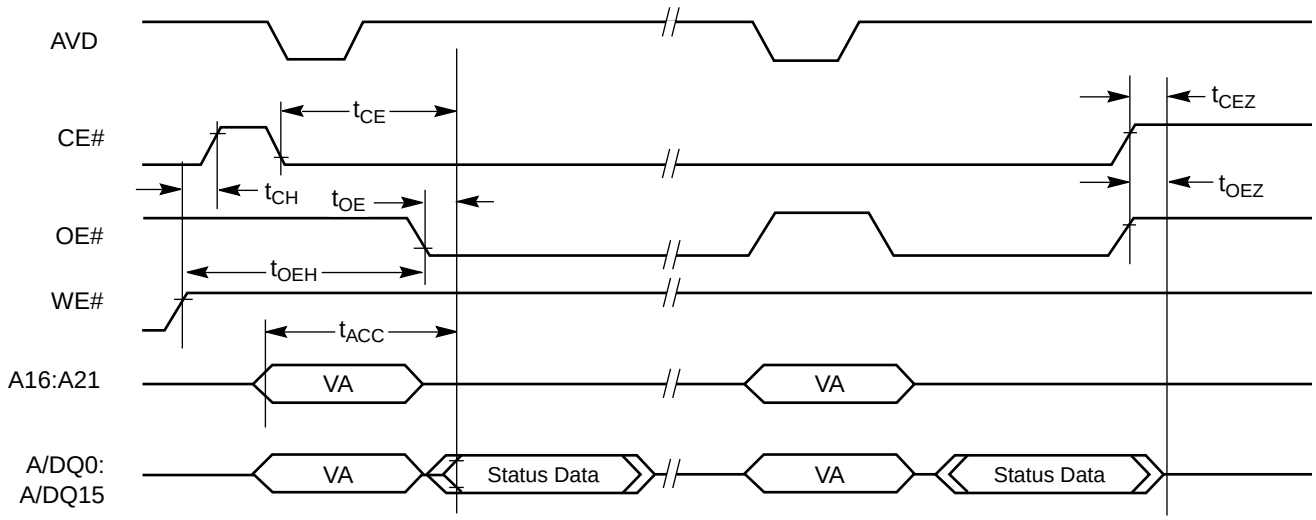
AC CHARACTERISTICS



Notes:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*

Figure 15. Data# Polling Timings (During Embedded Algorithm)

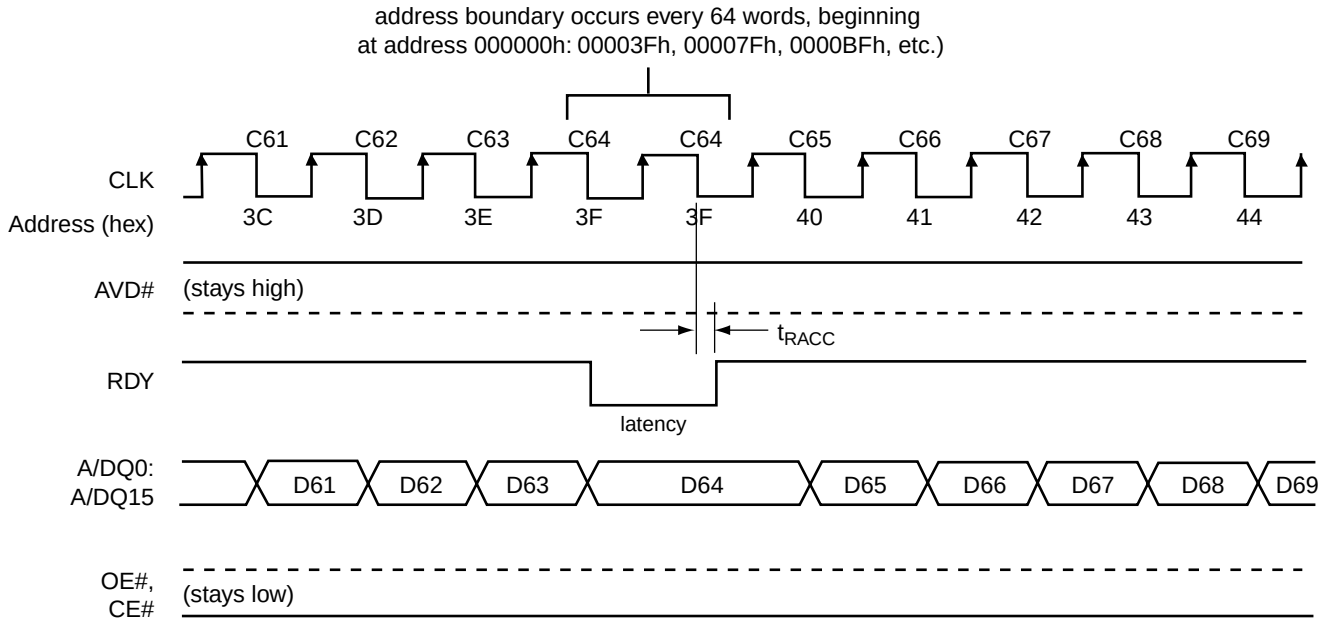


Notes:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*

Figure 16. Toggle Bit Timings (During Embedded Algorithm)

AC CHARACTERISTICS



Notes:

1. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C61 triggers D61.*
2. *If PS is enabled, RDY will be low for an additional cycle prior to the boundary crossing latency.*

Figure 17. Latency with Boundary Crossing

AC CHARACTERISTICS

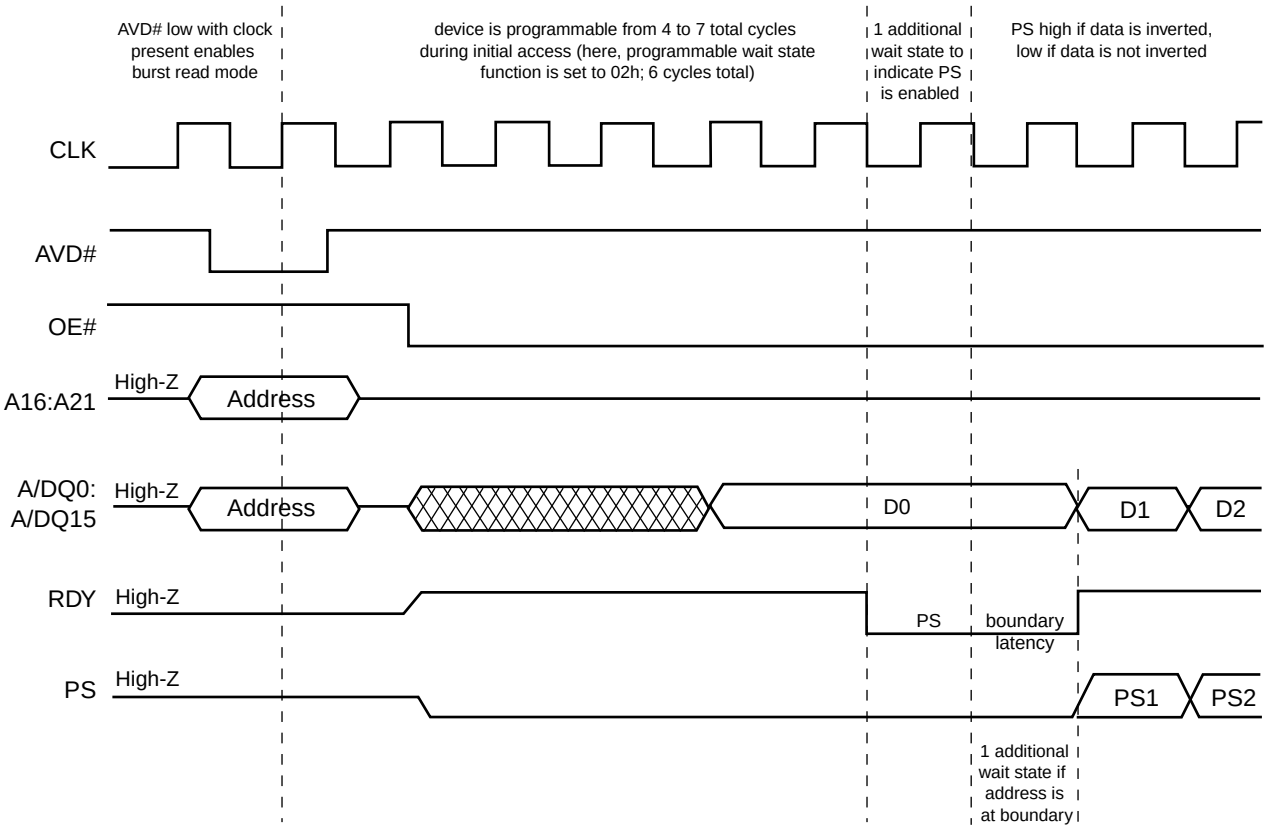


Figure 18. Initial Access with Power Saving (PS) Function and Address Boundary Latency

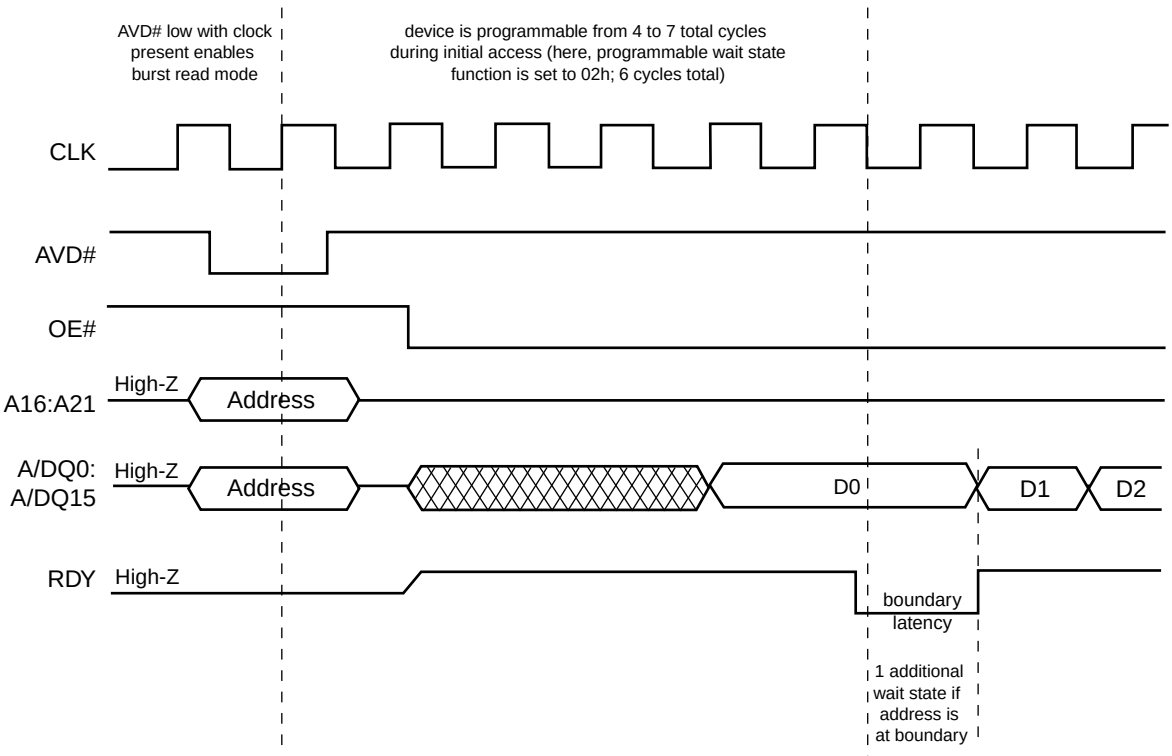
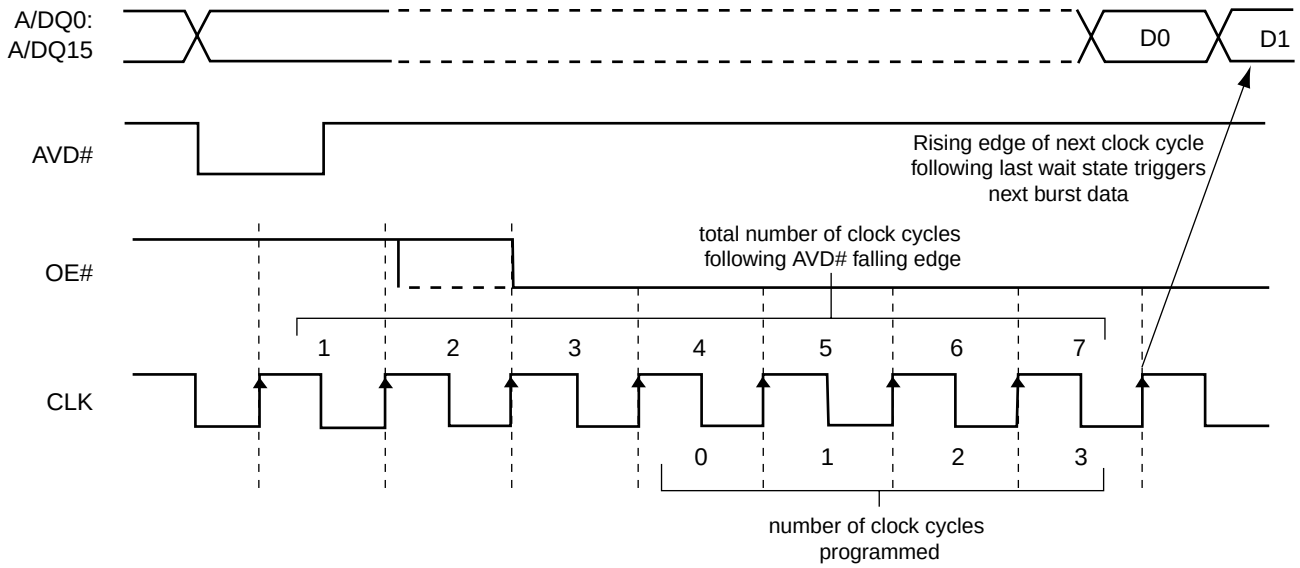


Figure 19. Initial Access with Address Boundary Latency

AC CHARACTERISTICS

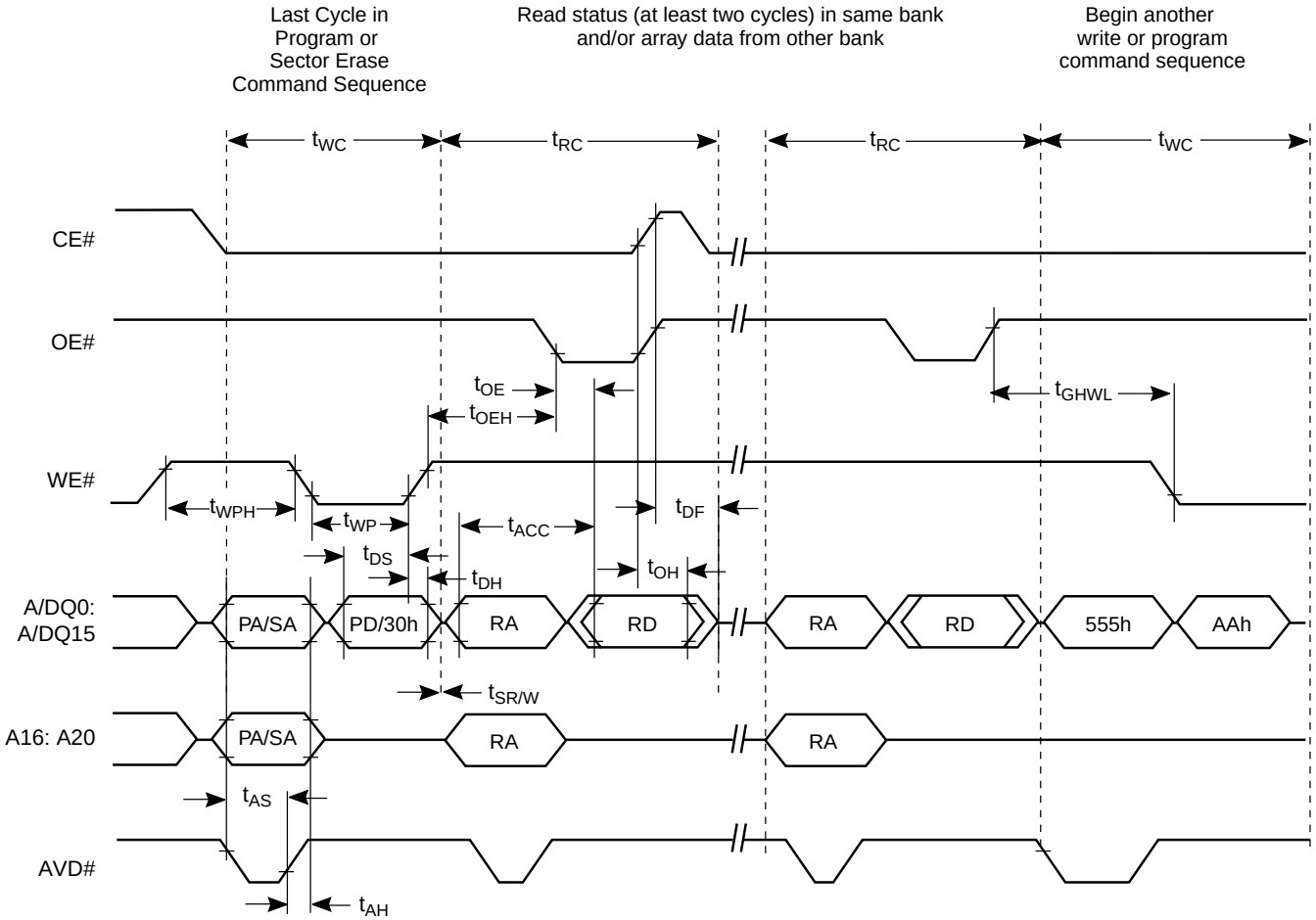


Wait State Decoding Addresses:
A13, A12 = "11" ⇒ 3 programmed, 7 total
A13, A12 = "10" ⇒ 2 programmed, 6 total
A13, A12 = "01" ⇒ 1 programmed, 5 total
A13, A12 = "00" ⇒ 0 programmed, 4 total

Note: *Figure assumes that PS is not enabled, and address D0 is not at an address boundary.*

Figure 20. Example of Five Wait States Insertion

AC CHARACTERISTICS



Note: *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

Figure 21. Back-to-Back Read/Write Cycle Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	32 Kword	1.5	15	s	Excludes 00h programming prior to erasure (Note 4)
	4 Kword	0.3	5		
Chip Erase Time		97		s	
Word Programming Time		11.5	360	µs	Excludes system level overhead (Note 5)
Accelerated Word Programming Time		4	210	µs	
Chip Programming Time (Note 3)		24	72	s	Excludes system level overhead (Note 5)
Accelerated Chip Programming Time		8	24	s	

Notes:

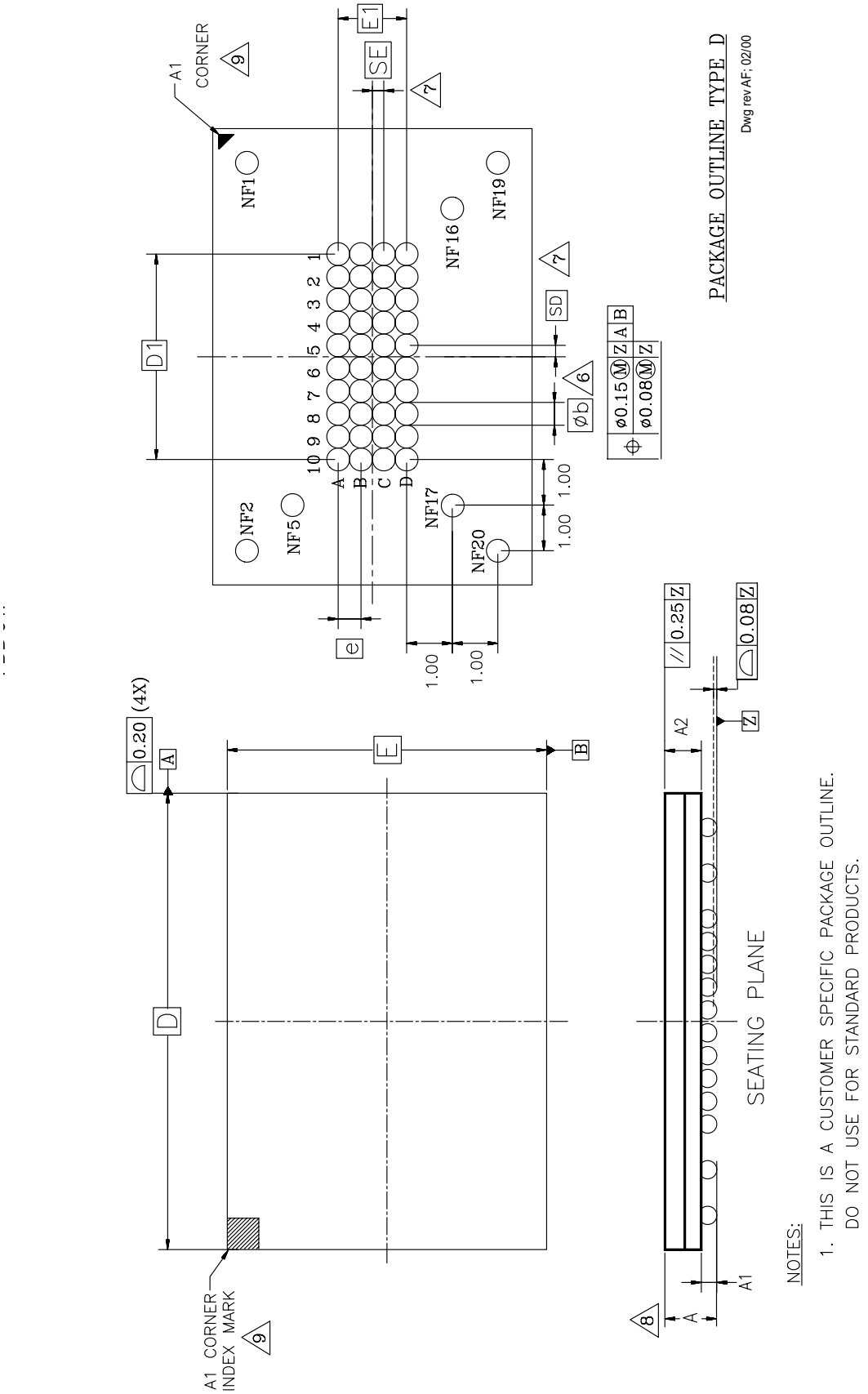
1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 1 million cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.8 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 4 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1 million cycles.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS*

FDD047—47-Pin Fine-Pitch Ball Grid Array (FBGA) 7 x 10 mm package



** For reference only. BSC is an ANSI standard for Basic Space Centering*

PHYSICAL DIMENSIONS

FDD047—47-Pin Fine-Pitch Ball Grid Array (FBGA) 7 x 10 mm (continued)

PACKAGE	FDD 047			
JEDEC	N/A			
	7.00mmx10.00mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	OVERALL THICKNESS
A1	0.20	—	—	BALL HEIGHT
A2	0.84	—	0.94	BODY THICKNESS
D	10.00 BSC			BODY SIZE
E	7.00 BSC			BODY SIZE
D1	4.50 BSC			BALL FOOTPRINT
E1	1.50 BSC			BALL FOOTPRINT
MD	10			ROW MATRIX SIZE D DIRECTION
ME	4			ROW MATRIX SIZE E DIRECTION
N	47			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.50 BSC			BALL PITCH
SD/SE	0.25 BSC			SOLDER BALL PLACEMENT
	NF			DENOTES NON FUNCTIONAL SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8 FOR PACKAGE THICKNESS A IS THE CONTROLLING DIMENSION.

9 A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

REVISION SUMMARY

Revision A (February 15, 2000)

Limited, non-public release.

Revision B (June 20, 2000)

Public release, with the following changes:

Block Diagram

Corrected address range to A0–A20.

Ordering Information

Deleted reference to 54 MHz speed option.

Device Bus Operations table

Split address range column into two columns.

AC Characteristics

Asynchronous Read: In table, changed “falling” to “rising” in description of t_{AAVDS}. In diagram, modified t_{AAVDS} and t_{AAVDH} waveforms to reference from the rising edge of AVD#.

Synchronous/Burst Read table: Added t_{RDYS}, t_{CEH} specifications.

Erase/Program Operations table, Program Operations Timings figure, Chip/Sector Erase Operations Timings figure: Added t_{AVDP}. Added PS waveforms to program operations timings figure.

Initial Access with Power Savings (PS) and Address Boundary Latency figure

Modified D0 data to extended to D1.

Erase and Programming Performance

Added typical and maximum accelerated chip programming time.

Revision B+1 (November 27, 2000)

Accelerated Program Operation, Program Command Sequence

Added text indicating that setors must be unlocked prior to raising V_{PP} to V_{ID}.

Chip Erase Command Sequence

Corrected the command sequence length during unlock bypass mode from four cycles to two.

DC Characteristics table

Added specification for active burst mode current with OE# high, I_{CCB2}. Original I_{CCB} specification is now named I_{CCB1}.

AC Characteristics

Figure 9, Burst Mode Read: Corrected RDY waveform to indicate behavior when PS is enabled and when RDY is in the high impedance state.

Figure 14, Accelerated Unlock Bypass Programming Timing: Modified Note 3 to indicate that sectors must be unlocked prior to raising V_{PP} to V_{ID}.

Revision B+2 (November 30, 2000)

Figure 10, Asynchronous Mode Read

Corrected endpoint for t_{AAVDS} specification.

Figure 16, Toggle Bit Timings (During Embedded Algorithm)

Corrected OE# waveform during second VA (valid address) period.

Revision B+3 (December 21, 2000)

Figure 9, Burst Mode Read

Corrected RDY waveform.

Revision B+4 (September 4, 2001)

Global

The 90 ns asynchronous access time has been changed to 110 ns. Note that the device now has a new ordering part number and a new package marking.

Sector Erase Command Sequence, DQ7: Data# Polling, and DQ6: Toggle Bit I

Added explanatory text to indicate 200 µs wait for first status read occurring in a different bank than the last sector selected for erasure in a multiple bank sector erase command sequence.

Table 4, Command Definitions

Added extended autoselect device ID to table (fifth cycle). Added Note 9.

Figure 18, Initial Access with Power Saving (PS) Function and Address Boundary Latency

Modified the pulse time RDY is low and in High-Z. Added note to indicate that RDY exhibits the same behavior when the burst address begins on an address boundary without PS enabled.

Figure 19, Initial Access with Address Boundary Latency

Added figure.

Copyright © 2001 Advanced Micro Devices, Inc. All rights reserved.

AMD, the AMD logo, and combinations thereof are registered trademarks of Advanced Micro Devices, Inc.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.